Errata

Title & Document Type: 54111D Digitizing Oscilloscope Service Manual

Manual Part Number: 54111-90912

Revision Date: June 1988

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

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Agilent no longer sells or supports this product. You will find any other available product information on the Agilent Test & Measurement website:

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Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

Agilent Technologies

HEWLETT PACKARD

SERVICE MANUAL

HP 54111D

DIGITIZING OSCILLOSCOPE

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed:

2808A

With changes described within, this manual also applies to instruments with serial prefixes:

2640A
2710A
2726A
2733A

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

Manual Part No. 54111-90912
Microfiche Part No. 54111-90812

PRINTED: June 1988

GEWERBEAUFSICHTSAMT STUTTGART

- Zentrale Stelle für Sicherheitstechnik und Vorschriftenwesen in Baden-Württemberg -

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Hewlett-Packard GmbH
Herrenberger Straße 110

7030 Boblingen

Stuttgart, den 02.06.1986
Fernsprecher
(0711) 205 01 (Behördenzentrum)
Durchwahl 2050 - 4798
Aktenzeichen: Z 5108/Hewlett-
(Bitte bei Antwort angeben)
Packard/Ws Vg

Betr.: Durchfuhrung der Rontgenverordnung (RoV)
hier: Bauartzulassung gem. § 7 Abs. 2 RoV

Bezug: Ihr Antrag vom 22.05.1986; PSD US-ab

Nachtrag 1

zum Zulassungsschein Nr. BW/218/86/Ro

Aufgrund des § 7 Abs. 2 der Rontgenverordnung vom 1.3.1973 (BGBl. I S. 173) wird die der Firma Hewlett-Packard GmbH, Herrenberger Straße 110, 7030 Boblingen, erteilte Zulassung Nr. BW 218/86/Ro vom 16.01.1986 wie folgt erweitert:

Gegenstand:	Digital-Oszilloskop
Firmenbezeichnung:	HP Typ 54 111 D HP Typ 54 112 D HP Typ 54 120 A
Bauartunterlagen:	Service Manuals Nr. 54 111 - 90 902 vom 21.94.86 Nr. 54 112 - 90 902 vom 24.04.86 Nr. 54 120 - 90 902 vom 26.04.86

Die fur den Strahlenschutz wesentlichen Merkmale entsprechen der bereits zugelassenen Ausfuhrung.

Typenbezeichnung der Bildrohre, Auflagen, Hinweise und Befristung ergeben sich aus dem Zulassungsschein Nr. BW 218/86/Ro vom 16.01.1986.

Dieser Nachtrag gilt nur im Zusammenhang mit dem vollständigen Text des o.g. Zulassungsscheins.

Reutter

GEWERBEAUFSICHTSAMT STUTTGART

Dieses Gerät wurde nach den Auflagen der Zulassungsbehörde einer Stuckprüfung unterzogen und entspricht in den für den Strahlenschutz wesentlichen Merkmalen der Bauartzulassung. Die Beschleunigungsspannung beträgt maximal 22,3 kV.

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1900 Garden of the Gods Road
Colorado Springs
Colorado 80907, USA

GEWERBEAUFSICHTSAMT STUTTGART

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Stuttgart, den 16.01.1986

Fernsprecher
(0711) 20501 (Behördenzentrum)
Durchwahl 2050 4798

Aktenzeichen: Z 5108/HP/Ws/Eh
(Bitte bei Antwort angeben)

Firma
Hewlett Packard GmbH
Herrenberger Str. 110/130

7030 Böblingen

Zulassungsschein Nr. BW/218/86/Rö

Gemäß § 9 der Röntgenverordnung vom 01.03.1973 (BGBl. I S. 173) wird die Zulassung der Bauart durch den Bauartzulassungsbescheid vom 16.01.1986 mit Aktenzeichen Z 5108/HP/Ws/Eh für den nachfolgend aufgeführten Störstrahler bescheinigt:

Gegenstand	:	Digital-Oszilloskop
Firmenbezeichnung	:	HP Typ 54110D
Bildröhre	:	Sony Typ M23 JHU 15X
Hersteller	:	Hewlett-Packard 1900 Garden of the Gods Road Colorado Springs Colorado 80907, USA
Betriebsbedingungen	:	Hochspannung: max. 22,3 kV Strahlstrom: max. 0,4 mA
Zulassungskennzeichen	:	BW/218/86/Rö

Die Bauartzulassung ist befristet bis 16.01.1996.

Für den Strahlenschutz wesentliche Merkmale

1. Die Art und Qualität der Bildröhre,
2. die der Hochspannungserzeugung und -stabilisierung dienenden Bauelemente.

Auflagen:

1. Die Geräte sind bezüglich der für den Strahlenschutz wesentlichen Merkmale entsprechend den vorgestellten und geprüften Mustern und Antragsunterlagen herzustellen.

2. Die Geräte sind einer Stückprüfung daraufhin zu unterziehen, ob sie bezüglich der für den Strahlenschutz wesentlichen Merkmale der Bauartzulassung entsprechen.

   Die Prüfung muß umfassen:

   a) Kontrolle der Hochspannung an jedem einzelnen Gerät,

   b) Messung und Dosisleistung nach Festlegung im Bauartzulassungsbescheid.

3. Die Herstellung und die Stückprüfung sind durch den von der Zulassungsbehörde bestimmten Sachverständigen überwachen zu lassen.

4. Die Geräte sind deutlich sichtbar und dauerhaft mit dem Kennzeichen

   BW/218/86/R5

   zu versehen sowie mit einem Hinweis folgenden Mindestinhalts:

   "Die in diesem Gerät entstehende Röntgenstrahlung ist ausreichend abgeschirmt. Beschleunigungsspannung maximal 22,3 kV."

Hinweis für den Benutzer des Geräts:

Unsachgemäße Eingriffe, insbesondere Verändern der Hochspannung oder Auswechseln der Bildröhre können dazu führen, daß Röntgenstrahlung in erheblicher Stärke auftritt. Ein so verändertes Gerät entspricht nicht mehr dieser Zulassung und darf infolgedessen nicht mehr betrieben werden.

Reutter

GEWERBEAUFSICHTSAMT STUTTGART

Dieses Gerät wurde nach den Auflagen der Zulassungsbehörde einer Stückprüfung unterzogen und entspricht in den für den Strahlenschutz wesentlichen Merkmalen der Bauartzulassung. Die Beschleunigungsspannung beträgt maximal 22,3 kV.

Hewlett-Packard
1900 Garden of the Gods Road
Colorado Springs
Colorado 80907, USA

SAFETY CONSIDERATIONS

GENERAL - This is a Safety Class I instrument (provided with terminal for protective earthing).

OPERATION - BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNING

- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates hazardous voltages.

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

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SECTION 1
GENERAL INFORMATION

1-1. INTRODUCTION

This Service Manual contains information necessary to test, adjust, and service the Hewlett-Packard 54111D Digitizing Oscilloscope. This manual is divided into nine sections as follows:

1 - General Information

2 - Installation

3 - Performance Tests

4 - Adjustments

5 - Replaceable Parts

6A - Instrument Disassembly

6B - Theory of Operation

6C - Service Menus/Keys

6D - Self-Tests/Troubleshooting

Information for operating, programming, and interfacing the HP 54111D is contained in the HP 54111D Operating and Programming Manual supplied with each instrument.

The General Information Section includes a description of the HP 54111D Digitizing Oscilloscope, its specifications, characteristics, options, and available accessories.

Listed on the title page of this manual is a Microfiche part number. This number can be used to order 4 X 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement as well as pertinent Service Notes.

1-2. DESCRIPTION

The HP 54111D is a fully programmable, real-time digitizing oscilloscope. It uses a sample rate of 1 GS/second which gives a repetitive bandwidth of 500MHz and a real-time bandwidth of 250 MHz.

The inputs include two vertical signal channels and two trigger channels. The inputs can be set up for 50 Ohm impedance with dc coupling or 1 MOhm at 6.5 pf with ac or dc coupling. The signals from the vertical and trigger channels can be used to provide a qualified trigger for the instrument that can be a pattern of levels and/or edges (see table 1-2).

The color display of the HP 54111D provides 16 colors which are mapped to provide specific colors for specific functions. For example, channel 1 is displayed in yellow, channel 2 is displayed in green and error messages are displayed in red.

To ensure proper operation, extensive self-tests have been designed into the instrument. These self-tests are in addition to internal diagnostics which aid in efficient fault locating and repair should a failure occur.

1-3. SPECIFICATIONS

Instrument specifications are listed in table 1-1. These specifications are the performance standards against which the oscilloscope is tested.

1-4. OPERATING CHARACTERISTICS

Table 1-2 is a listing of the instruments operating characteristics. The operating characteristics are not specifications, but are typical operating characteristics included as additional information for the user.

1-5. GENERAL CHARACTERISTICS

Table 1-3 gives environmental limits, input power requirements, and mechanical dimensions.

1-6. SAFETY CONSIDERATIONS

This product is a Safety Class 1 instrument (provided with a protective earth terminal). Review the instrument and manual for safety markings and instructions before operating. A page, Safety Considerations, covering general safety concerns, is in the front of this manual. Specific warnings, cautions, and instructions are placed wherever applicable throughout the manual. These precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this instrument. Hewlett-Packard assumes no liability for the customer's failure to comply with these requirements.

1-7. INSTRUMENTS COVERED BY MANUAL

The instrument serial number is located on the rear panel. Hewlett-Packard uses a two-part serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter **(0000A00000).** The prefix is the same for all identical instruments and changes only when a modification is made that affects parts compatibility. The suffix is assigned and is different for each instrument. This manual applies directly to instruments with the serial prefixes shown on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-8. OPTIONS

In addition to power cord options, the following options are available for the HP 54111D:

- W30: Additional two years "return to HP"service support commencing at the end of the standard warranty.
- 090: Deletion of the two 10:1 divider probes.
- 908: Rack mounting kit.
- 910: Extra set of manuals consisting of Operating and Programming manuals and one Service manual.

1-9. ACCESSORIES SUPPLIED.

The following accessories are supplied with the HP 54111D:

- Two 10:1 divider probes, HP Model No. 10431A.
- One power cord.
- One set of operating and programming manuals.
- One service manual.

1-10. RECOMMENDED TEST EQUIPMENT

Equipment recommended to maintain the HP 54111D is listed in table 1-4. The function for which a piece of equipment is needed (Performance Tests, Adjustments, or Troubleshooting) is also given in the table.

Table 1-1. Specifications

VERTICAL (VOLTAGE) [1]

Channels	2	
Bandwidth (−3 dB)[2]	**Real-time**	**Repetitive**
dc-coupled	dc to 250MHz	dc to 500 MHz[3]
ac-coupled	10 Hz to 250 MHz	10 Hz to 500 MHz[3]
Transition Time (10% to 90%)	See "Operating Characteristics"	700 ps
Deflection Factor (full-scale=8 div)	1 mV/div to 5 V/div continuous	
Resolution (% of full scale)	8 bits to 25 MHz, (0.4%) 7 bits to 100 MHz, (0.8%) 6 bits to 250 MHz, (1.6%)	6 bits, (1.6%) 8 bits with averaging to 500 MHz, (0.4%)
DC Gain Accuracy	±2% of full-scale [4]	
DC Offset Accuracy	±1.5% of setting ±0.2 div [5]	
DC Measurement Accuracy **single data point**	±Gain Acc. ±Offset Acc. ±Resolution	
between data points on same waveform	±Gain Acc. ±2 × Resolution	
DC Offset Range	±200 mV (1 mV/div to 4 mV/div) ±1 V (5 mV/div to 49 mV/div) ±10 V (50 mV/div to 499 mV/div) ±40 V (500 mV/div to 5 V/div)	
Input Coupling	ac/dc/dc-50 Ω/gnd	
Maximum Safe Input Voltage	±40 Volts @ 1 MΩ (dc + peak ac), 5 Vrms @ 50 Ω	

NOTE *All voltages in table correspond to a 1:1 attenuation setting. If a 10:1 probe is attached, multiply all voltages by 10. The HP 10033A has a maximum voltage of ±200 V*

1 Applies for temperature ranges ±5° C from point of last self-calibration.

2 Upper bandwidth limit for settings 1 mV/div to 4 mV/div is reduced to 150 MHz

3 Repetitive bandwidth at sweep speeds 10 us/div and slower is not specified

4 When calibrated to probe tip using the front panel calibration source. Applies to major ranges (5 mV/div, 10 mV/div, 20 mV/div, 50 mV/div, 100 mV/div, 200 mV/div, 500 mV/div, 1 V/div, 2 V/div). All settings other than these ranges are ±3% of full-scale. All settings from 1 mV/div to 4 mV/div are ±4% of full-scale

5 Increases to ± 4 divisions at 5 mV/div to 9 mV/div, and ±1 division below 5 mV/div.

Table 1-1. Specifications (cont.)

HORIZONTAL (TIME) [1]	Real-time	Repetitive
Digitizing Rate	1 gigasample/s to 50 sample/s	
Deflection Factor	500 ps/div to 1 s/div	
Memory Depth per Channel	8K	501
Pre-trigger Delay Range	−8 μs at timebase settings 50 ns/div and faster, increasing to −160 s at 1 s/div.	
Post-trigger Delay Range	160 ms at timebase settings 500 ns/div and faster, increasing to 10,000 s at 1 s/div.	
Time Interval Measurement Accuracy		
single channel	±300 ps [2] ±0.03% of reading	±100 ps [2] ±0.03% of reading
dual channel	±600 ps [3] ±0.03% of reading	±200 ps [3] ±0.03% of reading

TRIGGERING

Sources	Internal Channels 1,2	External Triggers 3,4
Sensitivity	0.1 of full-scale, dc to 200 MHz [4]	15 mV (high sensitivity) [5] dc to 200 MHz
	0.2 of full-scale, 200 MHz to 500 MHz [4]	45 mV (high sensitivity) [5] 200 MHz to 500 MHz
Trigger Level Range	±3 x full-scale [6]	±1 V (high sensitivity) [5]
Maximum Safe Voltage	NA	±10 volts @ 1MΩ (dc + peak ac), 5 Vrms @ 50 Ω
Input Operating Range	NA	±1 V (high sensitivity) [5] dc + peak ac

1 Applies for temperature ranges ±5° C from point of last self-calibration

2 Decreased to [±0.2% of time range(time/div x 10) ±0.03% of reading] for time ranges 200 ns and slower

3 Decreased to [±0.4% of time range(time/div x 10) ±0.03% of reading] for time ranges 200 ns and slower

4 Applies to settings 5 mV/div to 5 V/div only.

5 For low sensitivity, multiply voltage values by 10

6 The trigger level range is centered on the offset level. Trigger level range is limited at ±600 mV from 25 to 49 mV/div inclusive, ±6.0 V from 250 to 499 mV/div inclusive, and by the maximum safe input voltages at 2 V/div and above.

Table 1-2. Operating Characteristics

VERTICAL

Real-time Mode Transition Time (10% to 90%): 1.4 ns.
Calculated by measuring a 1.4 ns risetime source. In the 6-bit filter mode, a 1.4 ns input risetime is measured as; 2.0 ns = $\sqrt{(1.4)^2 + (1.4)^2}$.
Input Impedance: 1 MΩ @ <6.5 pF or 50 Ω (dc)
Input Protection: 50 ohm input resistance is protected where input rating is exceeded.
Dynamic Performance (typical):

	Effective Bits of Resolution				
Input Frequency	1 MHz	20MHz	90MHz	250MHz	500MHz
6-bit Mode	5.5	5.5	5.2	5.0 *	N/A
7-bit Mode	6.2	6.2	6.0	N/A	N/A
8-bit Mode	7.2	7.0	N/A	N/A	N/A

* Unfiltered data transfered over HP-IB

Channel-to-channel Isolaton: 60dB at 500MHz.

HORIZONTAL

Delay Between Channels: difference in delay between channels can be front panel calibrated to compensate for differences in input cables or probe length.
Reference Location: the reference point can be located at the left edge, center, or right edge of the display. The reference point is the trigger plus the delay time.

TRIGGER

Holdoff

Holdoff-by-events: range of events counter is from 2 to 67 million events. Maximum counting rate is 80 MHz. An event is defined as anything that satisfies the triggering conditions selected.
Holdoff-by-time: adjustable from 70 ns to 670 ms.

Trigger Modes

Edge trigger: on any source.
Pattern trigger: a pattern can be specified for all sources. Each source can be specified as high, low, or don't care. Trigger can occur on the last edge to enter the specified pattern or the first edge to exit the specified pattern

Time qualified pattern trigger: Trigger occurs on the first edge to exit the specified pattern, only if the pattern was present for less than [greater than] the specified time. Filter time is adjustable from 10 ns to 5 seconds. Recovery time is ≤ 8 ns. In the "Pattern present < [time]" mode, the pattern must be present ≥ 1 ns for the trigger to respond.
State trigger: a pattern can be specified for any of the sources. Trigger can be set to occur on an edge of either polarity on the source specified as the clock (not one of the pattern sources) when the pattern is present or not present. Setup time for the pattern to be present prior to the clock edge is < 4 ns; hold time is zero. Maximum clock repetition rate is 80 MHz.

Delayed Trigger

Events-delayed mode: the trigger can be armed by an edge on any source, then triggered by the nth edge on any other source. The number of events, n, can be set from 1 to 10^8 - 1. Maximum event counting rate is 150 MHz.
Time-delayed mode: the trigger can be armed by an edge on any source, then triggered by the first edge on any other source after a specified time has elapsed.

Table 1-2 Operating Characteristics (cont.)

DISPLAY

Data Display Resolution: 501 points horizontally by 256 points vertically.

Data Display Formats

Split screen: channel displays are two or four divisions high, corresponding to quad or dual display mode.

Full screen: channels are overlaid and are eight divisions high.

Display Modes

Variable persistence: the time that each data point is retained on the display can be varied from 200 ms to 10 seconds, or it can be displayed in the infinite persistence mode.

Averaging: the number of averages can be varied from 1 to 64. On each acquisition, 1/n times the new data is added to (n-1)/n of the previous value at each time coordinate. Averaging operates continously; the average does not converge to a final value after n acquisitions, except over HP-IB.

Graticules: Full grid, axes with tic marks, frame with tic marks, or graticule off.

Data Reconstruction: on sweep speeds when less than 500 points are acquired across the screen, a built-in digital filter will automatically reconstruct the data in the real-time acquisition modes (single-shot acquisition). The filter "off" position in the display mode will display raw data.

Display Colors: A default color selection is set up. Different colors are used for display background, channels, functions, background text, highlighted text, advisories, markers, overlapping waveforms, and memories. If desired, colors may be changed either from the front panel or over HP-IB.

HP-IB

Data Transfer Rate: 80k bytes/s

MEASUREMENT AIDS

Markers: dual voltage markers and dual time markers are available. Voltage markers can be assigned to channels, memories, or functions.

Automatic Edge Finders: the time markers can be assigned automatically to any displayed edge of either polarity on any channel. The voltage markers establish the threshold reference for the time markers in this mode.

Automatic Pulse Parameter Measurements: the following pulse parameter measurements are performed automatically (as defined by IEEE standard 194-1977, "IEEE Standard Pulse Terms and Definitions").

Frequency	Overshoot
Period	Peak-to-peak voltage
Duty Cycle	Average voltage
Pos Pulse Width	RMS voltage
Neg Pulse Width	Top voltage *
Rise time	Base voltage *
Fall time	Maximum voltage
Preshoot	Minimum voltage

* only available over the HP-IB.

Waveform Math: two independent functions are provided for waveform math. The operations provided are +, −, and invert. The vertical channels or any of the waveform memories can be used as operands for the waveform math.

SETUP AIDS

Presets: vertical deflection factor, offset, and trigger level can be preset independently on each channel for ECL and TTL levels.

Auto-Scale: pressing the Auto-Scale button causes the vertical and horizontal deflection factors and the trigger source to be set for a display appropriate to the signals applied to the inputs. Requires a duty cyle greater than 0.1% and frequency greater than 50 Hz. Operative only for relatively stable input signals.

Save/Recall: ten front panel setups may be saved in non-volatile memory. If Auto-Scale is inadvertently pressed, pressing Recall followed by Auto-Scale, restores the instrument to the state prior to the first Auto-Scale.

Table 1-3. General Characteristics

ENVIRONMENTAL CONDITIONS

Temperature

Operating: 0°C to +55°C (+32°F to +131°F)

Non-operating: -40°C to +75°C (-40°F to +167°F)

Humidity

Operating: up to 95% relative humidity (non-condensing) at +40°C (+104°F)

Non-operating: up to 90% relative humidity at +65°C (+149°F).

Altitude

Operating: up to 4600 meters (15,000 ft)

Non-operating: up to 15,300 meters (50,000 ft).

Vibration: vibrated in three orthogonal axes for 15 minutes each axis; 0.38 mm (0.015 in) peak-to-peak excursion; 5 to 55 Hz; 1 minute/octave sweep.

POWER REQUIREMENTS

Voltage: 115/230 V ac, -25% to + 15%, 48-66 Hz.

Power: 350 watts maximum, 700 VA maximum.

WEIGHT

Net: approximately 27 kg (59 lb).

Shipping: approximately 32 kg (70 lb).

DIMENSIONS

Refer to the outline drawings.

NOTES:

1. *Dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP field engineer*
2. *Dimensions are in millimetres and (inches).*

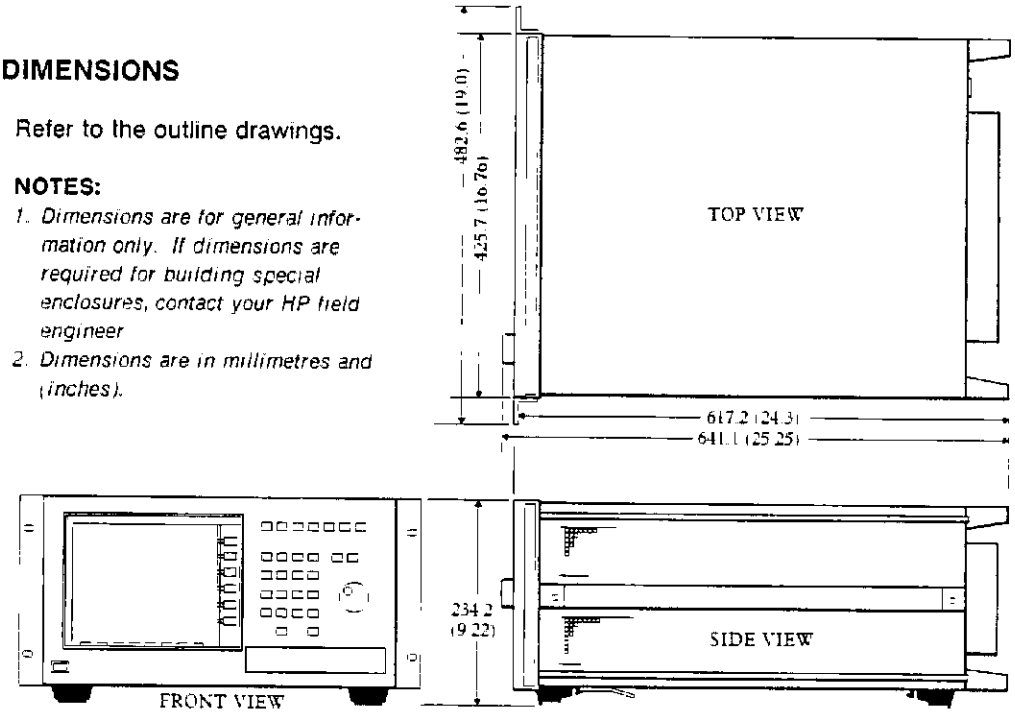


Table 1-4. Recommended Test Equipment

Equipment Required	Critical Specifications	Recommended Model	Use*
Signal Generator	100 KHz to 500 MHz, <-34 dBm to >+12 dBm, timebase within ±0.003%	HP 8656B check time-base to ±0.003%	P
Power Meter/Sensor	100 KHz to 1 GHz, <-22 dBm to >+8 dBm	HP 436A/8482A	P,A
Pulse Generator	≈70 ps transition time	TEK Type 284	P
Digital Multimeter	Better than ±0.05% accuracy	HP 3468A	P,A,T
DC Supply	±30 mV to ±70 V, 0.1 mV resolution	HP 6115A	P,A
Pulse Generator	≤1% perturbation after 10 ns, 0 to -300 mV output pulse	Tektronix PG 506	A
Pulse Generator	20 ns pulse width at 300 ns period, square wave at >2 μs period, ≤2 ns risetime and falltime	HP 8082A	A
Frequency Counter	51 MHz with 50 mV sensitivity and 6 digit resolution	HP 5384A	A
Oscilloscope	General purpose 300 MHz BW	HP 54201A	T
Divider Probe	10:1, 1 MΩ	HP 10431A/033A/017A	P,A,T
Power Splitter	Outputs within 0.15 dB to 500 MHz	HP 11667B	P
Attenuator	10 ±0.6 dB from 200-500 MHz	HP 8491B	P
Low-pass Filter	>35 dB attenuation at 2 GHz, -3 dB point above 1.250 GHz	RLC F30-1500-N	A
Adjustment tool	Non-metallic (for display)	HP 8710-1355	A
Adjustment tool	(for attenuator adjustment)	HP 8710-1515	A
Product Support Kit	No substitute	HP 54100-69006	T

* P = Performance Tests, A = Adjustment Procedures, T = Troubleshooting

SECTION 2
INSTALLATION

2-1. INTRODUCTION

This section contains the initial operation information for the HP 54111D digitizing oscilloscope. Included are power and grounding requirements, operating environment requirements, cleaning methods and storage and shipment requirements.

2-2. PREPARATION FOR USE

POWER REQUIREMENTS. The instrument requires a power source of either 115 or 230 VAC, -25% to +15%; single phase, 48 to 66 Hz; 350 watts, 700 VA maximum.

CAUTION

The instrument may be damaged if the Line Voltage Select Switch is not properly set to match the input line voltage.

LINE VOLTAGE SELECTION. Before turning ON the instrument verify that the Line Voltage Select Switch on the rear panel matches the input line voltage.

POWER CABLE. This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See table 2-1 for option numbers of power cables and plug configurations available. Part numbers for each cable option are also listed in the parts list in Section VI.

2-3. OPERATING ENVIRONMENT

The operating environment is noted in table 1-3. Note should be made of the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Protection should be provided against internal condensation.

2-4. CLEANING REQUIREMENTS

When cleaning the instrument, CAUTION must be exercised on which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE damaged.

CAUTION

BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuitry if it seeps under the keys

2-5. STORAGE AND SHIPMENT

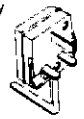
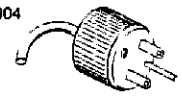
2-6. Environment

The instrument may be stored or shipped in environments within the following limits:

Temperature: -40 to +75° C (-40 to +167° F)
Humidity: Up to 90% at 65° C (+149° F)
Altitude: Up to 15 300 metres (50 000 feet)

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause malfunction if the instrument is operated under these conditions.

Table 2-1. Power Cord Configurations

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 250V 900 	8120-1351* 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom Cyprus, Nigeria, Zimbabwe, Singapore
OPT 250V 901 	8120-1369 8120-0696	Straight *NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray	Australia, New Zealand
OPT 250V 902 	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So Africa, India (Unpolarized in many nations)
OPT** 125V 903 	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical) UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Mexico, Philippines, Taiwan,
OPT** 250V 904 	8120-0698	Straight *NEMA6-15P	90/228	Black	United States, Canada
OPT 250V 905 	8120-1396 8120-1625	CEE22-V1 (System Cabinet Use) 250V	30/76 96/244	Jade Gray	For interconnecting system components and peripherals United States and Canada only
OPT 250V 906 	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 220V 912 	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark
OPT 250V 917 	8120-4211 8120-4600	Straight SABS164 90°	79/200 79/200	Jade Gray	Republic of South Africa India
OPT 100V 918 	8120-4753 8120-4754	Straight Mitl 90°	90/230 90/230	Dark Gray	Japan

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug.
**These cords are included in the CSA certification approval of the equipment
E = Earth Ground
L = Line
N = Neutral

AC CABLES3

2-7. Packaging

TAGGING FOR SERVICE. If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

ORIGINAL PACKAGING. If the original packing material is not available or is unserviceable, material identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for servicing, attach a tag showing owner (with address), model number, complete instrument serial number, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials.

a. Wrap instrument in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

NOTES

SECTION 3
PERFORMANCE TESTS

3-1. INTRODUCTION

The procedures in this section test the instrument's electrical performance using specifications in Section I as performance standards. The specification is also listed at the test for reference.

3-2. CALIBRATION CYCLE

This instrument requires periodic verification of performance. The instrument should be checked using the following performance tests yearly or every 2000 hours of operation. Amount of use, environmental conditions, and the users experience concerning need for calibration will contribute to performance verification requirements.

3-3. CALIBRATION REQUIREMENTS

To perform calibration of the HP 54111D, follow these steps:

1. Perform CLOCK and GAP adjustments in section 4.

2. Set up and look at the flatness using the GAIN and FLAT Adjustments procedure in section 4. Do not adjust unless necessary. If necessary, follow the procedure to adjust.

3. Ensure that the front panel CAL signal is 800 ±2 mV. Follow the Calibrator Amplitude Adjustment procedure in section 4 but do not adjust unless it is outside the above tolerance.

4. Perform the vertical self-calibration, ADC Reference Cal, Vertical Cal, and Probe Tip Cal per section 4.

5. Check the DC Gain Adjustment as in section 4. Do not adjust unless needed.

6. Perform Trigger Cal per section 4.

7. Perform Channel Skew per section 4.

8. Perform the Trigger Qualifier Adjustment procedures, checking first and adjusting only if necessary.

9. Perform all Performance Test procedures and record the results.

Use the following table to take the appropriate action in the event of a failed specification.

FAILED PERF. TEST	ADJUSTMENT(S) OR ACTION
Measurement Accuracy	-Vertical self-cals DC GAIN
Time Interval Accuracy	-Timebase Frequency Cal
Bandwidth	-Call HP Cust. Service
Transition Time	-Call HP Cust. Service
Trigger Sensitivity	-Call HP Cust. Service

To perform a MIL STD calibration, do all Performance Tests first and record results in the performance record. Then perform the calibration as above.

3-4. TEST EQUIPMENT REQUIRED

Equipment recommended for performance tests is listed in table 1-4. Individual tests list the equipment necessary for that test. Any equipment that satisfies critical specifications given in the tables may be substituted.

3-5. TEST RECORD

Results of performance tests may be entered in the Performance Test Record (table 3-2) at the end of the procedures. The Test Record lists the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and when testing after repairs or adjustments.

3-6. ABBREVIATED TEST PROCEDURES

To save time and the need for some test equipment, some tests can be dropped from the complete procedure. Following are two tests which may be dropped and reasons why.

TRANSITION TIME. Transition time has a close relationship with bandwidth. If bandwidth passes, the Transition Time test is not likely to fail. Dropping this test saves time and avoids the need for the fast transition pulse generator that is only used for this test (see Recommended Test Equipment table).

TIME INTERVAL ACCURACY. This test can be dropped if the Channel Skew and Timebase Frequency Cal are accurate. If such is the case, the Time Interval Accuracy test is not likely to fail. Dropping this test saves time.

3-7. TESTS AFTER REPLACEMENTS

Some performance tests may be necessary after replacement of an assembly, though it may not be necessary to test the entire instrument. Table 3-A (below) gives the minimum performance testing required after replacement of major assemblies.

Table 3-1. Performance Tests Required After Assembly Replacement.

PERF. TEST / ASSEMBLY	Calibrator Amplitude	Measurement Accuracy	Offset Accuracy	Band-width	Rise-time	Time Interval Accuracy	Trigger Sens.
Timebase	#	X				X	
ADC Control		RCO	RCO				RCO
ADC		RCO	RCO	RCO	RCO		
Trigger							Trig 3,4
Channel Atten.		RCO	RCO	RCO	RCO		RCO
Trigger Atten.							RCO

NOTE: No performance tests are required after replacing either the **Microprocessor, Input/output, Trigger Qualifier** or **Color Display** assemblies, the **Color CRT Module**, or the **Power Supplies**.

KEY:
- # Timebase assembly replacement requires Calibrator Amplitude adjustment. Adjustment sets calibrator amplitude with greater accuracy than the performance test requires so the performance test is unnecessary
- X This test must be performed
- RCO Replaced Channel Only. Perform the test only on the channel in which the assembly was replaced.

3-8. PROBES USED DURING TESTS

The HP 54111D uses a ring around the input BNC to sense a grounded contact pin on certain 10:1 probes, such as the HP 10431A, or 10033A. The HP 54111D scales the input properly when those 10:1 probes are being used.

Some parameters of the HP 54111D are specified with the instrument calibrated through a probe to the front panel CAL signal or a 10 V supply. Therefore, some of the performance tests require the use of a 10:1 divider probe and using the Probe Tip Cal to calibrate the instrument with that probe.

In the event that the probes shipped with the HP 54111D are not available for performance tests, any probe with comparable specifications, it must be a 1 MΩ probe designed for 1 MΩ inputs, may be used whether it has the grounded contact pin or not. Probe Tip Cal assumes that a 10:1 probe is being used so the calibration is properly done. The performance test procedures are written to allow use of unsensed probes, such as the HP 10017A.

Calibration with the probe is a user function. The HP 54111D can be calibrated to other probes once it is returned to the user.

3-9. PERFORMANCE TEST PROCEDURES

Performance test procedures start with the next paragraph. Any one, or all procedures may be done in any order.

NOTE

Allow instrument to warm up for at least 30 minutes prior to beginning performance tests.

3-10. ONE-KEY POWER UP

A one-key power up is a procedure where any one key is held depressed when the power is turned on. The key is held depressed until the power up cycle completes; "Powerup Self Test Passed!" (or Failed) is displayed. This is done to preset or reset the instrument to default conditions and prevent previous setups from interfering with the next test. It also simplifies the instrument setup procedure.

The one-key powerup is a part of many procedures and should be performed like any other procedural step.

3-11. CALIBRATOR AMPLITUDE

Description:

This procedure checks the amplitude of the front panel calibrator. This signal is used to run calibration routines in the instrument.

When being adjusted, this signal has a tighter specification than that required for passing this test. This is done to maintain the performance specification to the end of the calibration cycle (see Calibration Requirements).

Specification:

+0.8 ±0.008 Vdc

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Voltmeter	Better than 0.25% accuracy	HP 3468A

Procedure A:

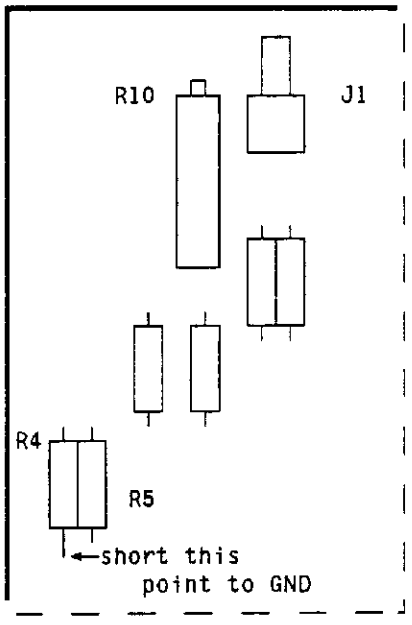
1. Connect the voltmeter input to the front panel calibrator signal. Connect the voltmeter ground to the CHAN 1 input BNC ground.
2. With the softkeys, press ***more, Utility, Cal Menu, Timebase Cal***, and ***Timebase Freq Cal***.
3. If the voltmeter reads about +0.8 Vdc continue to step 4. If the measurement is about +0.4 Vdc, this instrument's hardware requires manual intervention to perform this test. Press ***Exit*** and continue with Procedure B on the next page.
4. The CAL signal should be +0.8 ±0.008 Vdc. Record the value and press ***Exit***.

Procedure B:

The calibrator output must be forced high manually.

1. Remove the top rear feet and the top cover.
2. Connect the voltmeter to the front panel CAL signal.
3. The drawing shows the top front corner of the Timebase assembly A1. The Timebase assembly is the left-most assembly in the card cage. Note the position of R4, specifically the bottom end of this resistor.
4. Connect one end of a jumper wire to the body of J1 on the Timebase. Connect a long grabber to the other end of the jumper.
5. Connect the grabber to the bottom end of R4.
6. The CAL signal should be +0.8 ±0.008 V. Record the value.

Top-front corner of Timebase assy. (A1)



3-12. MEASUREMENT ACCURACY

Description:

This test verifies the measurement accuracy of the instrument with a 10:1 probe at the input. Measurement accuracy consists of gain accuracy and resolution. The test uses positive and negative DC levels so that any OFFSET errors are nulled.

Specification:

Repetitive 6-bit with averaging and with a 10:1 probe at the input.

10 mV to 40 mV/div = ±4.8% of full scale * [4% gain +2 x resolution(0.4%)]
50 mV/div and above ** = ±2.8% of full scale * [2% gain +2 x resolution(0.4%)]
* Full scale = 8 div x V/div ** Major ranges only

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Supply	±30 mv to ±100 Vdc 0.1 mV resolution	HP 6115A
DC Voltmeter	Better than 0.1% accuracy	HP 3468A
Oscilloscope Probe	10:1 1 MΩ	HP 10431A/033A/017A

Procedure:

In this procedure, a positive then negative voltage is applied at each V/div range. Each voltage is measured and the difference is used to check gain on that range. With a supply like the HP 6115A, polarity is changed by floating the supply and reversing the connection of the probe to get the negative value. If you are using a supply with a polarity switch (or a voltage standard with negative voltage capability), reversing the probe connection is not necessary.

1. Perform a one-key powerup* to set instrument to default conditions, then set the following additional parameters.
   *Power to STBY Press and hold one key Power to ON Release key when "Powerup Self Test Passed!" is displayed

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1,2	Display VOLTS/DIV	Chan 1 ON/Chan 2 OFF as required
Timebase	TIME/DIV	2 us/div
Display	NUMBER OF AVERAGES Screen	64 Single
Delta V	V Markers	ON

2. Connect the 10:1 divider probe to the CHAN 1 input of the HP 54111D and the front panel CAL signal and press *more*.

3. If you are using an HP 10431A or 10033A probe, skip this step. Press ***Utility***, ***Probe Menu***, and ***CHAN 1 PROBE ATTN***, then in the ENTRY keys, 10 and ENTER.

4. Calibrate the HP 54111D to the 10:1 probe being used for the test. Press ***Utility***, ***Cal Menu***, ***Probe Tip Cal***, ***Calibrate Probe Tip CHAN 1***, and ***Continue***. When calibration is done press ***Exit***, ***more***, ***Chan 1***, and ***VOLTS/DIV***.

5. Set the power supply to 0.0 V and remove any connection between the output and ground.

6. Use the following table for steps 7 through 17. For the first three V/div settings it is necessary to set the supply within ±0.1 mV with the voltmeter.

WARNING

This test uses voltages of ±70 Vdc. Excercise caution to avoid shock hazard.

SCOPE V/div	INPUT VOLTAGE SETTINGS#	Δ	MEASURED Δ VOLTAGE LIMITS TOLERANCE	MIN		MAX
10 mv	±35 mV*	70 mV	±4 mV	66.0 mV	_____	74.0 mV
20 mv	±70 mV*	140 mV	±8 mV	132 mV	_____	148 mV
50 mV	±175 mV*	350 mV	±12 mV	338 mV	_____	362 mV
100 mv	±350 mV	700 mV	±24 mV	676 mV	_____	724 mV
200 mv	±700 mV	1.40 V	±50 mV	1.35 V	_____	1.45 V
500 mV	±1.75 V	3.50 V	±120 mV	3.38 V	_____	3.62 V
1 V	±3.5 V	7.00 V	±240 mV	6.76 V	_____	7.24 V
2 V	±7.0 V	14.0 V	±500 mV	13.5 V	_____	14.5 V
5 V	±17.5 V	35.0 V	±1.2 V	33.8 V	_____	36.2 V
10 V	±35.0 V	70.0 V	±2.4 V	67.6 V	_____	72.4 V
20 V	±70.0 V	140 V	±5 V	135 V	_____	145 V

#For a supply without a polarity switch (like the HP 6115A) polarity is changed by switching the probe tip and ground of the 10:1 probe.

*Confirm these settings with the Voltmeter.

7. Connect the probe to the output of the supply (probe tip to +, ground clip to −).

8. Press ***Chan 1*** and ENTER the SCOPE V/div range with the ENTRY keypad.

9. Set the supply to the positive value of the voltage in the INPUT VOLTAGE - SETTINGS column of the table and press CLEAR DISPLAY to restart averaging.

10. Press ***Delta V*** and ***MARKER 2 POSITION***. When ***#Avgs = 64***, use the knob and cursors to set the marker over the trace. With the marker at best overlap the most overlap color will show.

11. Set the supply to the negative value of the voltage in the INPUT VOLTAGE - SETTINGS column of the table (or reverse the probe connections, probe tip to − and ground clip to +) and press CLEAR DISPLAY.

12. Press ***MARKER 1 POSITION*** and when ***#Avgs = 64***, overlap the trace with the marker.

13. Read and record the $\Delta V=$ in the lower right corner of the screen. It should fall within the specified limits in the table above.

14. If you are using a supply with no polarity switch reverse the probe connection (probe tip to +, ground to −).

15. Repeat steps 7 through 14 with the rest of the V/div ranges in the table.

16. Press ***Chan 1***, ***Display (OFF)***, ***Chan 2***, and ***Display (ON)***.

17. Repeat steps 2 through 15 substituting ***Chan 2*** for ***Chan 1***.

18. Set the dc power supply to 0.0V.

19. If you are doing the Offset Accuracy tests next, skip this step. If probe attenuation factors (step 3) were entered, set them back to 1.000 to avoid improper results in further tests. Press ***more***, ***Utility***, ***Probe Menu***; then, for both channels, ***CHAN X PROBE ATTN*** and in the ENTRY keys, 1 and ENTER.

3-13. OFFSET ACCURACY

Description:

This test verifies Offset accuracy. Resolution is a part of the specification for this test.

Specification:

Repetitive 6-bit with averaging and with a 10:1 probe at the input.

±1.5% of setting ± 0.2 div* ±Resolution[0.4% of full scale (8 div.)]

* ±0.4 div from 50-90 mV/div and ±1 div below 50 mV/div

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Supply *	±300 mV and ±9.5 V 1.0 mV resolution	HP 6115A
DC Voltmeter	Better than ±0.1% accuracy	HP 3468A
Oscilloscope Probe	10:1 1MΩ	HP 10431A/033A/017A

* The voltage source used for these tests could be any stable supply with the parameters shown above. You may use the offset of a signal generator or a dc calibration standard that meets the specifications. The HP 6115A is recommended because it is used in another test.

Procedure:

1. Perform a one-key powerup* to set instrument to default conditions, then set the following additional parameters.

*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1,2	Display	Chan 1 ON/Chan 2 OFF
Timebase	TIME/DIV	2 us/div
Display	NUMBER OF AVERAGES Screen Graticule	64 Single Grid

2. Connect the 10:1 probe to CHAN 1 of the HP 54111D.

3. If you are using an HP 10431A or 10033A probe skip this step. Press ***more***, ***Utility***, ***Probe Menu***, and ***CHAN 1 PROBE ATTN***, then ENTER 10.

4. If you just did the Vertical Accuracy tests skip this step. Calibrate the HP 54111D to the 10:1 probe being used for the test. Press ***Utility***, ***Cal Menu***, ***Probe Tip Cal***, ***Calibrate Probe Tip CHAN 1***, and ***Continue***. When calibration is done, press ***Exit***, ***more***, ***Chan 1***, and ***VOLTS/DIV***.

5. Use the following table for steps 6 through 13.

SUPPLY VOLTAGE	MEASUREMENT LIMITS TOLERANCE	MAX		MIN
0.00 V	±24 mV	-24 mV	_____	24 mV
300 mV	±28 mV	272 mV	_____	328 mV
-300 mV	±28 mV	-272 mV	_____	-328 mV
-9.50 V	±170 mV	-9.33 V	_____	-9.67 V
9.50 V	±170 mV	9.33 V	_____	9.67 V

6. Connect the probe ground clip to the probe tip.

7. Press ***VOLTS/DIV*** and ENTER 100 mV.

8. Press ***OFFSET*** and use the arrow keys to set the trace exactly to center screen when ***#Avgs = 64***. The ***Offset*** reading should be within the specification for 0.00 V in the table. Record the reading.

9. Set the supply to 0.00 V then connect the voltmeter and probe to the output of the supply (probe tip to + and ground clip to –).

10. Set the supply voltage and scope offset to the next value in the table. It is easiest to enter the offset value directly, using the key pad.

11. Adjust the offset using the knob and arrow keys until the trace is at center screen when ***#Avgs = 64***.

12. The ***Offset*** = value should be within the limits given in the table. Record the reading.

13. Repeat steps 10 through 12 with the other values in the above table. If using a supply with no polarity switch, for negative voltages reverse the probe tip and ground at the supply.

14. Remove the probe from the power supply and connect the probe ground to the probe tip.

15. Use the following table for steps 16 through 23. Follow steps 17 through 21 for a pass/fail test, or steps 17a through 20a for a precise test. The pass/fail test is faster. If a range is close to the specification for a pass/fail test, make a precise test of that range.

V/div	PASS/FAIL LIMITS(div)	PRECISE LIMITS		
10 mV	±1.0	-10.4 mV	_____	+10.4 mV
20 mV	±1.0	-20.6 mV	_____	+20.6 mV
50 mV	±0.4	-22 mV	_____	+22 mV
100 mV	tested in step 4			
200 mV	±0.2	-46 mV	_____	+46 mV
500 mV	±0.2	-120 mV	_____	+120 mV
1 V	±0.2	-230 mV	_____	+230 mV
2 V	±0.2	-460 mV	_____	+460 mV
5 V	±0.2	-1.2 V	_____	+1.2 V
10 V	±0.2	-2.3 V	_____	+2.3 V
20 V	±0.2	-4.6 V	_____	+4.6 V

NOTE

Note that the minor division marks on the display are at 0.25 division increments and the specifications in the PASS/FAIL column of the table are 1.0, 0.4, and 0.2 divisions

16 Press ***VOLTS/DIV*** and ENTER 10 mV.

PASS/FAIL TEST

17. Press ***OFFSET*** and ENTER 0 V.

18. Check the distance of the trace from the center horizontal axis. It should be within the DIVISIONS limits shown in the table above when ***#Avgs = 64***.

19. If trace is within limits in step 18, record the range as passing. If it appears to be outside the limits, make a precise test of this range (steps 17a and 18a at right), then continue with step 20.

20. Repeat steps 18 and 19 for each V/div range in the table.

21. After checking all ranges go to step 22.

PRECISE TEST

17a. Press ***OFFSET*** and use the cursor keys to set the trace to exactly center screen when ***#Avgs = 64***.

18a. Check that the Offset reading is within the specification in the LIMITS - VOLTAGE column. Record the reading and set offset to 0.0 V.

19a. Repeat steps 17a and 18a for each V/div range in the table. If if your doing a precise test of all ranges it is not necessary to set the offset to 0.00 V (step 18a) after each range check.

20a. After checking all ranges go to step 22.

22. Press ***Chan 1***, ***Display (Off)***, ***Chan 2***, and ***Display (On)***.

23. Repeat steps 2 through 21 (or 20a) for channel 2, substituting Chan 2 for Chan 1.

24. If probe attenuation factors (step 3) were entered, set them back to 1.000 to avoid improper results in further tests. Press ***more***, ***Utility***, ***Probe Menu***; then for both channels ***CHAN X PROBE ATTN*** and in the ENTRY keys, 1 and ENTER.

3-14. BANDWIDTH

Description:

This test checks the repetitive and real-time bandwidths of the HP 54111D.

Specification:*

	Real-time	Repetitive*
DC Coupled	0 to 250 MHz	0 to 500 MHz
AC Coupled ***	10 Hz to 250 MHz	10 Hz to 500 MHz

* Upper bandwidth limit at input sensitivities below 5 mV/div is 150 MHz

** Repetitive bandwidth at sweep speeds 10 us/div and slower not specified.

*** Not tested.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Signal Generator	100 kHz to 500 MHz -22 to +12 dBm	HP 8656B
Power Meter/Sensor	100 kHz to 500 MHz -28 dBm to +8 dBm	HP 436A/8482A
Power splitter Attenuator Type (N)	Outputs differ by <0.15dB 10 dB 100 kHz to 150 MHz	HP 11667A HP 8491B
Cable Adapter	Type N(m) 24 inch N(m) to BNC(m)	HP 11500B HP 1250-0082

Procedure:

1. Zero and calibrate the power meter using the Power Reference on the meter and the REF Cal Factor on the power sensor.

2. Connect the equipment as shown in the following diagram.

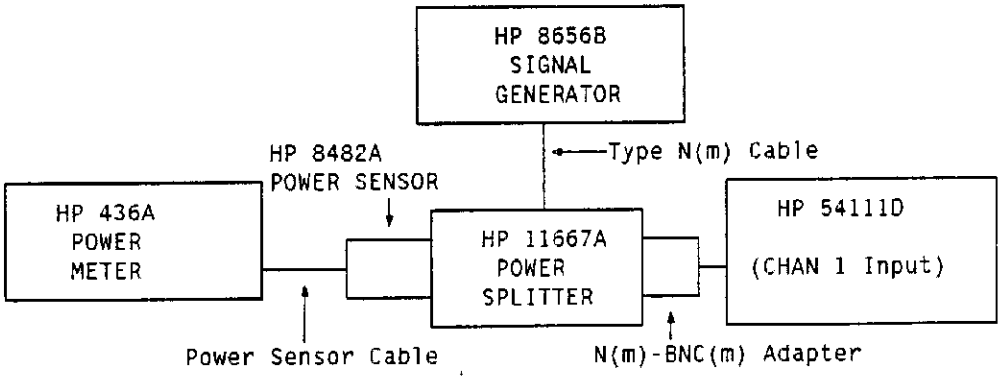


Figure 3-1. Bandwidth Test Connections.

3. Perform a one-key powerup* to set instrument to default conditions, then set the following additional parameters in the order given.

*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed

MENU SELECT	FUNCTION SELECT	SETTING
Display	Disp Mode	Real Time
	Resol'n	6 bits
	Screen	Single
Chan 1,2	Display	Chan 1 ON/Chan 2 OFF
	VOLTS/DIV	200 mvolts/div
	Input Impedance	50Ω
Timebase	TIME/DIV	2 us/div
	Auto/Trgd Sweep	Trgd
Delta V	V Markers	ON
	Preset Levels	0-100%

REAL-TIME BANDWIDTH

4. Set up the 8656B signal generator with a 100 kHz signal at +12 dBm. The HP 54111D should display two cycles of a sinewave signal.

5. Set power meter Cal Factor % to 100 kHz value from the cal chart on the probe, press dB[REF] to set a 0 dB reference.

6. Press ***Delta V*** and ***Auto Level Set***. The V Markers will mark the top and bottom of the signal. Note the ΔV= value at the bottom of the screen.

7. Change the frequency of the signal generator to 250 MHz.

8. Change the power meter Cal Factor to the 250 MHz % value from cal chart.

9. Press ***Timebase*** and ***TIME/DIV*** and ENTER 2 ns.

10. Press ***Delta V***. Increment the signal generator output amplitude while occasionally pressing ***Auto Level Set*** on the HP 54111D.

11. When the ΔV= value (bottom of screen) is the same as noted in step 6, read and record the level on the power meter. It should be less than ±2.85 dB from the zero reference.

REPETITIVE BANDWIDTH

12. Set signal generator frequency to 100 kHz and amplitude to +12 dBm.

13. Set power meter Cal Factor % to 100 kHz value from the cal chart on the probe, press dB[REF] to set a 0 dB reference.

14. Press ***Timebase*** and ***TIME/DIV*** and ENTER 2 μsec.

15. Press ***Display*** then ***Disp Mode*** to obtain Repetitive mode Confirm ***Averaging On*** and press ***Number of Averages***, and ENTER 8.

16. Press ***Delta V*** and ***Auto Level Set***. The V Markers will mark the top and bottom of the signal. Note the ΔV= value shown at the bottom-right of the display.

17. Press ***Timebase*** and ***TIME/DIV*** and ENTER 1 nsec.

18. Change the signal generator frequency to 500 MHz and set the power meter Cal Factor % to the 500 MHz value on the probe cal chart.

19. Press ***Delta V***. Do not press ***Auto Level Set*** yet.

20. Slowly adjust the signal generator output amplitude while occasionally pressing CLEAR DISPLAY. When the signal seems to be averaging so the peaks are near the markers, press CLEAR DISPLAY, allow ***#Avgs*** = to reach 8, then press ***Auto Level Set***.

21. When you can press CLEAR DISPLAY, wait for ***Avgs=8***, then press ***Auto Level Set***, and get the same ΔV= value as noted in step 16, read and record the level on the power meter. It should be less than ±2.85 dB from the zero reference.

22. Connect the signal to the CHAN 2 input and change the following menus on the HP 54111D.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1	Display	OFF
Chan 2	Display	ON
Timebase	TIME/DIV	2.00 us/div
Trigger	Trig Src	Chan 2
Display	Disp Mode	Real Time

23. Repeat steps 4 through 21 for channel 2.

BANDWIDTH BELOW 5 MV/DIV (repetitive)

24. Insert the 10 dB attenuator between the power splitter and the channel input of the instrument being tested.

25. Set signal generator frequency to 100 kHz at -12 dBm.

26. Set power meter Cal Factor % to 100 kHz value from the cal chart on the probe, press dB[REF] to set a 0 dB reference.

27. Press ***Timebase*** and ***TIME/DIV*** and ENTER 2 μsec.

28. On the HP 54111D, press ***Chan 2*** and ***VOLTS/DIV*** and ENTER 4 mV. The display should show two cycles of signal.

29. Press ***Delta V*** and ***Auto Level Set***. The V Markers will mark the top and bottom of the signal Note the ΔV= value shown at the bottom-right of the display.

30. Press ***Timebase*** and ***TIME/DIV*** and ENTER 5 ns.

31. Change the signal generator frequency to 150 MHz and set the power meter Cal Factor % to the 150 MHz value on the probe cal chart.

32. Press ***Delta V***. Do not press ***Auto Level Set*** yet.

33. Slowly adjust the signal generator output amplitude while occasionally pressing CLEAR DISPLAY. When the signal seems to be averaging so the peaks are near the markers, press CLEAR DISPLAY, allow ***#Avgs*** = to reach 8, then press ***Auto Level Set***.

34. When you can press CLEAR DISPLAY, wait for ***Avgs=8***, then press ***Auto Level Set***, and get the same ΔV= value as noted in step 28, read and record the level on the power meter. It should be less than ±2.85 dB from the zero reference. Record the reading.

35. Press ***Chan 2, Display (Off)***, then ***Chan 1, Display (On)***.

36. Connect the signal to the CHAN 1 input and repeat steps 25 to 34 for channel 1, substituting Chan 1 for Chan 2.

3-15. TRANSITION TIME

Description:

Transition Time (Risetime) is tested by applying a fast risetime pulse to the HP 54111D and making an automatic risetime measurement.

This test could be dropped for an abbreviated performance test (see paragraph 3-5).

Specification:

The repetitive transition time is ≤700 ps.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse Generator	≈70 ps risetime	Tektronix TYPE 284
Cable	BNC(m)	HP 10503A
Adapter	GR-to-BNC(f)	HP 1250-0850

Procedure:

1. Connect the pulse generator PULSE OUTPUT to the CHAN 1 input.
2. Press ***Chan 1*** and confirm or set ***Input Impedance*** to 50Ω. Press AUTOSCALE to establish the display, then continue setup of the 54111D as follows:

MENU SELECT	FUNCTION SELECT	SETTING
Timebase	TIME/DIV	500 ps/div
Display	Disp Mode	Repetitive
	Averaging	ON
	NUMBER OF AVERAGES	8

3. Set the ***V/div*** and ***OFFSET*** to provide the maximum waveform without clipping the signal. You can set ***VOLTS/DIV*** and ***OFFSET*** with the ENTRY keys with 1 mV resolution.
4. Press ***more*** in the menu keys, then ***Measure*** and ***more*** in the function keys.
5. When ***#Avgs*** = is greater than 1, press ***Rise Time***. If you need a more accurate measurement wait for the number of averages to reach 8 then press ***Rise Time*** again.
6. Risetime should read ≤700 ps. Record the reading.
7. Repeat steps 1 through 6 for channel 2, substituting Chan 2 for Chan 1.

3-16. TIME INTERVAL ACCURACY

Description:

Time interval accuracy is checked by correlating delay settings with a frequency-stable signal.

Usually performance tests are done before any adjustments. The HP 54111D however has self-calibration that may have been done by the user. Two of these self-cals, Timebase Cal and Channel Skew, will affect the time interval accuracy of the instrument.

- Though Timebase Cal is not usually a user calibration, particularly when traceability is being maintained, it can be easily done by the user. If the user has done Timebase Cal, the time interval measurement traceability is affected and the instrument may fail the Time Interval Accuracy tests.

- The Channel Skew self-cal is a user calibration. The user calibrates the time reference between channels to suit his measurements. If the Channel-to-Channel Accuracy part of the Time Interval Accuracy tests is done without adjusting Channel Skew, the test will be done with the users calibration and the instrument may fail.

If it is necessary to return the instrument to traceable calibration by doing Timebase Cal and Channel Skew before the Time Interval Accuracy tests, see the appropriate sections in the adjustment procedures, section 4 of this service manual. Timebase Cal and Channel Skew can be done without affecting any other performance tests or adjustments.

Specification:

Accuracy of the time interval measurements is to be within the following limits:

	Repetitive	Real-time
Single Channel	±100 ps ±0.03% of reading	±300 ps ±0.03% of reading
Dual Channel	±200 ps ±0.03% of reading	±600 ps ±0.03% of reading

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Signal Generator	1.0 MHz and 500 MHz time base ±0.003%	HP 8656B-check time base to be within ±0.003%
Power splitter	1.0 to 500 MHz frequency range	HP 11667A
Cable	Type N(m) 24 inch	HP 11500B
Adapter (2)	N(m) to BNC(f)	HP 1250-0780
Cables (2)	BNC(m) 9 inch(equal length)	HP 10502A

Procedure:

1. Read and record the Timebase Freq Cal figure. Press ***more***, ***Utility***, ***Cal Menu***, ***Timebase Cal***, and ***Timebase Freq Cal***.

2. Record the ***Current value*** in the Performance Test Record; on the first page where it can be easily found, and at the Time Interval Accuracy section where the results of these tests are recorded. Continue with the rest of the tests.

3. Set the signal generator frequency to 500 MHz and amplitude to 120 mV.

4. Connect the signal generator to the input of the power splitter with the type N cable. With the N-to-BNC adapters and the BNC-to-BNC cables, connect the outputs of the power splitter to the channel inputs.

5. Perform a one-key powerup* to set instrument to default conditions.
   *Power to STBY. Press and hold one key. Power to ON. Release key when 'Powerup Self Test Passed!' is displayed

6. Press ***Chan 1*** and ***Chan 2*** menu keys in turn and set the ***Input Impedance*** on both to 50Ω.

7. Press AUTOSCALE to establish the display, then set or confirm the following parameters in the order given.

MENU SELECT	FUNCTION SELECT	SETTING
Display	NUMBER OF AVERAGES Screen	4 Single
Chan 1,2	Display VOLTS/DIV OFFSET	Chan 1 ON/Chan 2 OFF 20 mvolts/div 0.00 V
Timebase	TIME/DIV	500 ps/div
Trigger Chan 1,2	Trig Src TRIGGER LEVEL Slope	Chan 1 0.00 V (both channels) Pos (both channels)

SHORT DELAY - TIMEBASE ACCURACY

8. Press ***Timebase*** and ***DELAY***. Adjust the delay so the positive edge of the signal crosses the horizontal graticule exactly at center screen. Note the Delay reading on the display.

9. Add the delay reading from step 8 to each of the Set Delay values in the following table and use the entry keys to ENTER each sum as a Delay value. For each entry, check that the positive edge of the signal crosses the horizontal graticule within the "Divisions" specification from center screen. Record a pass or fail for each delay setting.

If you want to measure the error, for each Set Delay value ENTER the delay sum as above, then use the cursors or knob to make the positive edge cross the horizontal graticule exactly at center screen. Record the difference between the instrument reading and the delay sum Each should be within the "Time" specification.

Set Delay	Specification Divisions	Time	Record
2 ns	±0.2	±102 ps	_____
4 ns	±0.2	±102 ps	_____
6 ns	±0.2	±102 ps	_____
8 ns	±0.2	±104 ps	_____
10 ns	±0.2	±104 ps	_____
100 ns	±0.26	±130 ps	_____
334 ns	±0.4	±200 ps	_____

NOTE. 0.2 div = one minor graticule division

CHANNEL TO CHANNEL ACCURACY

10. Further set up the HP 54111D with the following parameters.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 2	Display	ON
Timebase	Delay	0.00 s
Delta V	V Markers	ON
	MARKER 1 POSITION	Chan 1 0.00 V
	MARKER 2 POSITION	Chan 2 0.00 V
	Preset Levels	50-50%
Delta t	T Markers	ON
	START ON XXX	POS
	EDGE X	1
	STOP ON XXX	POS
	EDGE X	1

11. At ***Delta t*** press ***Edge Find***. The Δt= reading, in the lower-right corner of the display, should be 0.00 ±200 ps. Record the reading.

LONG DELAY - TIMEBASE ACCURACY

12. Change the frequency of the signal generator to 1 MHz.

13. Press AUTOSCALE to establish the signal.

14. Change the HP 54111D with the following parameters.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 2	Display	OFF
Timebase	TIME/DIV	200 ns/div
Display	Screen	Single
Delta V	V Markers	OFF
Delta t	T Markers	OFF

15. Press ***Trigger*** and ***Trigger Level***. Adjust the trigger so that the positive edge of the signal crosses exactly at center screen.

16. Press ***Timebase*** and ***Delay***. Enter 1 ms. The positive edge of the signal should cross within 1.5 divisions of center screen. Use the knob or cursors to set the positive slope at center screen. The delay should read 1.0 ms ±300 ns. Record the reading.

3-17. TRIGGER SENSITIVITY

Description:

Channel and external trigger paths are checked for sensitivity vs. frequency. The displayed signal must remain triggered for various frequency and input amplitude combinations.

Specification:

	Channels 1 and 2	Triggers 3 and 4
dc to 200 MHz	0.1 of full scale *	15 mV p-p
200MHz to 500 MHz	0.2 of full scale *	45 mV p-p

* 5 mV/div to 5 V/div

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Signal Generator	200 MHZ and 500 MHz <-33 dBm to >-13 dBm	HP 8656B
Power Meter/Sensor	200 - 500 MHz measure approximately -22 dBm	HP 436A/8482A
Power splitter	200 to 500 Mhz frequency range	HP 11667A
Attenuator	10 ±0.6 dB 200-500 MHz	HP 8491B
Cable	Type N(m) 24 inch	HP 11500B
Adapter	N(f) to BNC(m)	HP 1250-0077
Adapters (2)	N(m) to BNC(f)	HP 1250-0780
Cables (2)	BNC(m) 9 inch	HP 10502A

Procedure:

CHAN 1, 2 TRIGGER TEST

1. With the Type N cable and N(f)-to-BNC(m) adapter, connect the signal generator to the CHAN 1 input.

2. Perform a one-key powerup* to set instrument to default conditions.
   *Power to STBY Press and hold one key Power to ON Release key when "Powerup Self Test Passed!" is displayed

3. Set the signal generator frequency for 200 MHz and amplitude to 9 mV rms.

4. Press ***Chan 1*** then ***Input Impedance*** to set 50Ω. Press AUTOSCALE to establish the display, then set or confirm the following parameters on the 54111D.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1	VOLTS/DIV	20 mvolts/div
Display	NUMBER OF AVERAGES	8
Delta V	V Markers Preset Levels	ON 0-100%

5. Press ***Trigger*** and ***Trigger Level***.

6. Reduce the output of the signal generator until ***Auto Triggering*** appears (top of display). Adjust ***Trigger Level*** as necessary to maintain triggering as long as possible. Increase output until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

7. Press CLEAR DISPLAY. When ***#Avgs*** = becomes greater than 1, press ***Delta V*** and ***Auto Level Set***. Read and record ***ΔV***=. It should be less than 16 mV (0.1 of full scale or 0.8 div.). Waiting for the number of averages to become 8 will give a more accurate reading but 1 average will usually give an indication the test has passed.

8. Change the frequency of the signal generator to 500 MHz.

9. Press ***Trigger*** and ***Trigger Level***.

10. While optimizing triggering with the Trigger Level, increase the output of the signal generator until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

11. Press CLEAR DISPLAY. When ***#Avgs*** = becomes greater than 1, press ***Delta V*** and ***Auto Level Set***. Read and record ***ΔV***=. It should be less than 32 mV (0.2 of full scale or 1.6 div.).

12. Connect the signal generator to the CHAN 2 input.

13. Repeat steps 3 through 11 for channel 2, substituting Chan 2 for Chan 1.

TRIG 3, 4 TRIGGER TEST

14. Connect the equipment as shown in the following diagram.

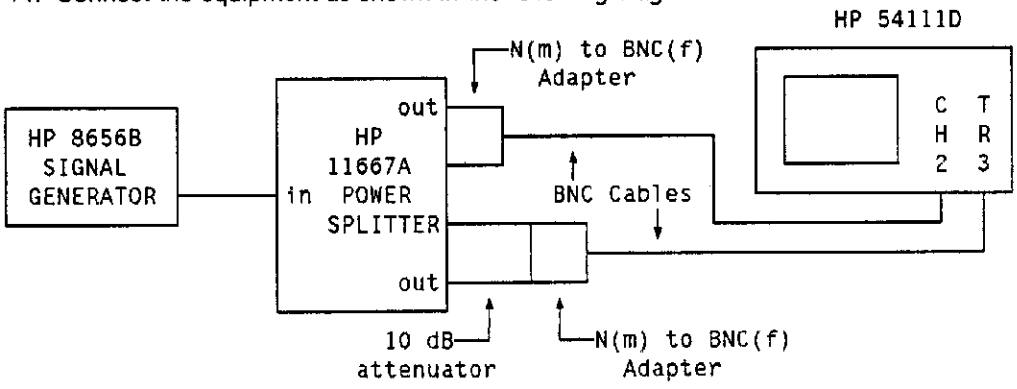


Figure 3-2. Trigger Sensitivity Test Connections.

15. Press ***Delta V*** and ***V Markers*** to shut them off and press ***Chan*** 2 and ***VOLTS/DIV*** and ENTER 10 mV.

16. Zero and calibrate the power meter using the Power Reference on the meter and the REF Cal Factor on the power sensor.

17. Set the signal generator frequency to 200 MHz and output level to 50 mV rms.

18. Set the power meter Cal Factor % to the 200 MHz value from the chart on the probe.

19. Press ***Trigger*** and ***Trigger Src*** to select TRIG 3 and press the left arrow key to select ***HI SENS***.

20. Press ***INPUT Coupling*** and the left arrow key to select 50Ω.

21. Reduce the output of the signal generator until ***Auto Triggering*** appears in the display. Adjust ***Trigger Level*** as necessary to maintain triggering as long as possible. Increase output until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

22. Disconnect the 10 dB attenuator at the power splitter and connect the power meter to this port of the splitter.

23. Read and record the power reading. It should be less than 5.62μW (15 mV p-p + 10 dB).

24. Set the signal generator to 500 MHz and set the power meter Cal Factor % to the 500 MHz value from the chart on the probe.

25. Disconnect the power meter and connect the TRIG 3 input to this port of the splitter with just the N to BNC adapter and BNC cable (no 10 dB attenuator).

26. Adjust ***Trigger Level*** to obtain ***Running*** in the display.

27. Reduce the output of the signal generator until ***Auto Triggering*** appears in the display. Adjust ***Trigger Level*** to maintain triggering as long as possible. Increase the output of the signal generator until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

28. Disconnect the TRIG 3 input at the power splitter and connect the power meter.

29. Read and record the power reading. It should be less than 5.06 μW (45 mV p-p).

30. Disconnect the power meter and connect this splitter port through the 10 dB attenuator, N to BNC adapter, and BNC cable to the TRIG 4 input.

31. Repeat steps 17 through 29, substituting Trig 4 for Trig 3.

NOTES

Table 3-2. Performance Test Record

HEWLETT PACKARD

HP 54111D
DIGITIZING OSCILLOSCOPE

Tested by _____

Serial No. _____ Work Order No. _____

Recommended Calibration Interval - 1 Year/2000 hours Date _____

Recommended Next Calibration _____ Temperature _____

Timebase Freq. Cal - current value _____ Humidity _____

TEST	LIMITS		RESULTS	
3-9 Calibrator Amplitude		0.792 to 0.808 V		
	RANGE		CHAN 1	CHAN 2
3-10 Measurement Accuracy	10 mV	66.0 mV to 74.0 mV		
	20 mV	135 mV to 145 mV		
	50 mV	338 mV to 362 mV		
	100 mV	676 mV to 724 mV		
	200 mV	1.35 V to 1.45 V		
	500 mV	3.38 V to 3.62 V		
	1 V	6.76 V to 7.24 V		
	2 V	13.5 V to 14.5 V		
	5 V	33.8 V to 36.2 V		
	10 V	67.6 V to 72.4 V		
	20 V	135 V to 145 V		
	RANGE		CHAN 1	CHAN 2
3-11 Offset Accuracy	100 mV	-24 mV to 24 mV		
		272 mV to 328 mV		
		-272 mV to -328 mV		
		-9.33 V to -9.67 V		
		9.33 V to 9.67 V		
	10 mV	±1 div or ±10.4 mV		
	20 mV	±1 div or ±20.6 mV		
	50 mV	±0.4 div or ±22 mV		

Table 3-2. Performance Test Record (con't.)

TEST	LIMITS			RESULTS	
3-11 Vertical Offset Accuracy (con't.)	RANGE			CHAN 1	CHAN 2
	200 mV	±0.2 div or	±46 mV	_____	_____
	500 mV	±0.2 div or	±120 mV	_____	_____
	1 V	±0.2 div or	±230 mV	_____	_____
	2 V	±0.2 div or	±460 mV	_____	_____
	5 V	±0.2 div or	±1.2 V	_____	_____
	10 V	±0.2 div or	±2.3 V	_____	_____
	20 V	±0.2 div or	±4.6 V	_____	_____
3-12 Bandwidth			Down from reference	CHAN 1	CHAN 2
	Real Time	250 MHz	<3 dB	_____	_____
	Repetitive	500 MHz	<3 dB	_____	_____
	@ 4 mV/div	150 MHz	<3 dB	_____	_____
3-13 Transition Time			≤700 ps	CHAN 1 _____	CHAN 2 _____
3-14 Time Interval Accuracy	Timebase Freq Cal current value			_____	
	Short Delay - Timebase Acc.				
	2 ns	±0.2 div or	±102 ps	_____	
	4 ns	±0.2 div or	±102 ps	_____	
	6 ns	±0.2 div or	±102 ps	_____	
	8 ns	±0.2 div or	±104 ps	_____	
	10 ns	±0.2 div or	±104 ps	_____	
	100 ns	±0.26 div or	±130 ps	_____	
	334 ns	±0.4 div or	±200 ps	_____	
	Channel-to-Channel Accuracy				
	Δt = 0.00		±200 ps	_____	
	Long Delay - Timebase Acc.				
	1.0 ms		±300 ns	_____	
3-15 Trigger Sensitivity		Better than: full scale	or mV	CHAN 1	CHAN 2
	dc to 200 MHz	0.1 div	16	_____	_____
	200 to 500 MHz	0.2 div	32	_____	_____
		Better than: mV p-p	or μW	TRIG 3	TRIG 4
	dc to 200 MHz	15	5.62	_____	_____
	200 to 500 MHz	45	5.06	_____	_____

SECTION 4
ADJUSTMENTS

4-1. INTRODUCTION

This section describes the adjustments required to make the instrument meet published specifications. Included are adjustments to the power supplies, acquisition system and color display.

4-2. ADJUSTMENT REQUIREMENTS

Adjustments should be performed as warranted by the Calibration Procedure (see section 3), by requirements after repair, or requirements due to failure of a performance test (see section 3). Adjustments should not be performed only on the basis of an elapsed period of time.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures. The apparatus should be disconnected from all voltage sources before it is opened for any adjustment, replacement, maintenance, or repair.

4-3. TEST EQUIPMENT REQUIRED

Required test equipment is listed in Table 4-1 Recommended Test Equipment.

4-4. ACCESS TO ADJUSTMENTS

Most adjustments can be accessed by removing the instrument top cover. Remove the top-rear feet and then the top cover.

Power supply adjustments (not done during routine calibration) require the additional removal of the power supply cover (under the top cover).

Adjustment of the attenuators requires partial removal of the front panel and attenuators. For this reason, and because misadjustment is unlikely, attenuator adjustment is not recommended during routine calibration.

One adjustment in the Trigger Qualifier Adjustment section is near the center of the assembly and is hard to reach from the top. It may be necessary to remove the handle, bottom-right rear foot, and right side cover in addition to the top cover.

Most adjustments of the Color CRT Module are under the clear plastic covers and are accessable from the sides or bottom of the instrument. However, several are at the rear of the module and require removal of the module from the instrument and operation of the module while outside the instrument. They also require a special tool as noted in the procedure.

4-5. ONE-KEY POWER UP

A one-key power up is a procedure where any one key is held depressed when the power is turned on. The key is held depressed until the power up cycle completes; "Powerup Self Test Passed!" (or Failed) is displayed. This is done to preset or reset the instrument to default conditions and prevent previous setups from interfering with the next test. It also simplifies the instrument setup procedure.

The one-key powerup is a part of many procedures and should be performed like any other procedural step.

4-6. ADJUSTMENTS REQUIRED AFTER REPLACEMENTS

Some adjustments may be necessary after replacement of an assembly, though it may not be necessary to make all adjustments. The table below gives the adjustments necessary after replacement of a major assembly.

Table 4-1. Adjustments Required After Assembly Replacement.

ADJUSTMENT / ASSEMBLY	Power Supplies	Clk & Gap	Gain & Flat	Calibrator Amplitude	Atten-uator	Complete* Self-Cal	DC Gain	Trigger Qualifier
Timebase		X		X		X		
Microprocessor						X		
Input/Output						X		
ADC Control						X	RCO	
ADC		RCO	RCO			Skip Probe Tip and Trigger cals		
Trigger						Skew only		
Trigger Qual.						Skew only		X
Channel Atten.					Adj. at factory	X	RCO	
Trigger Atten.						X		
Power Supplies	Adjust supply replaced							

NOTE: No adjustments are required after replacing the **Color Display** assembly and **Color CRT Module**.

KEY: RCO Replaced Channel Only. Perform this adjustment only on the channel in which the assembly was replaced

X This adjustment must be performed

* Self-calibration includes: ADC Reference Cal, Vertical Cal, Probe Tip Cal, Trigger Cal, and Timebase Cal (Timebase Frequency Cal and Channel Skew). See the appropriate procedures in this section

4-7. POWER SUPPLY ADJUSTMENTS

Description:

This procedure is provided to adjust the power supply voltages in cases where either of the power supplies has been inadvertently mis-adjusted or repairs have been made.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Voltmeter	Better than 0.3% accuracy	HP 3468A

Analog Power Supply Procedure:

NOTE

First, check for the presence of A12R61. It is located at the top front corner of the Analog Supply assembly. If there is no potentiometer there, the instrument is a later version and no adjustment is required; continue with the Digital Supply procedure.

This procedure adjusts the supply voltage to the fans.

The locations of the test points are marked on the power supply cover as well as the PC board. A12R61 is the only adjustment on the analog power supply.

NOTE

*The instrument **MUST** be stabilized at ambient temperature with power off (front panel power switch to STBY) before this adjustment is made. This voltage will rise as internal temperature increases.*

1. Connect positive voltmeter lead to the FAN test point.
2. Connect negative voltmeter lead to the -18 V test point.
3. Turn on instrument power (from STBY to ON).
4. Before instrument warms up, adjust A12R61 (the only pot on the board) for a voltmeter reading of 9.5 Vdc ±0.1 V.

Digital Power Supply Procedure:

The locations of test points are marked on the power supply cover as well as the assemblies. A13R56 is the only adjustment on the digital power supply. First, the voltage is measured to be sure that it requires adjustment.

1. Allow the instrument to stabilize (power on) for one to two minutes.
2. Connect positive voltmeter lead to the +5 V test point (actual voltage = +5.1 V).
3. Connect negative voltmeter lead to the −5 V test point (actual voltage = −5.3 V).
4. The voltmeter should read 10.4 Vdc ±0.01 V. If the measurement is within specifications stop here, if not then continue.
5. Disconnect power cord and remove voltmeter leads.

WARNING

Hazardous voltages capable of causing injury or death are present on the Primary Power Supply board (A11) when power is applied and for a period of time after power is removed from the instrument. To avoid this hazard, DO NOT remove the top power supply shield until the LED on the Primary Power Supply board (A11) is extinguished. This LED is visible through an inspection hole in the cover labeled "+300 V WHEN LAMP IS ON".

6. When the +300 V LED is extinguished, remove the top power supply cover.
7. Reconnect voltmeter leads per steps 2 and 3 above.
8. Reconnect power cord and allow instrument to stabilize for 1 to 2 minutes.
9. Adjust A13R56 for a voltmeter reading of 10.4 Vdc ± 0.01 V.
10. Disconnect power cord and wait for the +300 V LED to extinguish before re-installing power supply shield.

4-8. CLOCK AND GAP ADJUSTMENTS

Description:

These adjustments provide a clean clock to the sampling circuitry. There are two procedures: adjustment and testing. Testing is only necessary in certain cases per the adjustment procedure.

If this adjustment is a result of an assembly replacement (table 4-A), after doing all required adjustments, refer to table 3-A for required performance tests. Otherwise, perform Measurement Accuracy, Offset Accuracy, Bandwidth, and Risetime tests (section 3) on channel adjusted.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Power Meter/Sensor	1 GHz bandwidth	HP 436A with 8482A
Lowpass Filter	>35 dB attenuation at 2 GHz -3 dB point above 1.25 GHz	RLC F30-1500-N
Digital Voltmeter	±0.5%	HP 3468A
Adapter * Adapter * Cable *	BNC (f) to N (f) SMB (f) to BNC (f) BNC (m)	HP 1250-1474 HP 1250-1236 HP 10503A

* It is necessary to adapt the SMB (m) connector at J6 to the filter and power meter. Use whatever you have that can properly handle the 1 GHz signal. You can use cables and adapters that are part of the HP 54100 Family Support Kit.

Adjustment Procedure:

1. Zero the power meter. It isn't necessary to calibrate it since all measurements are relative.

NOTE

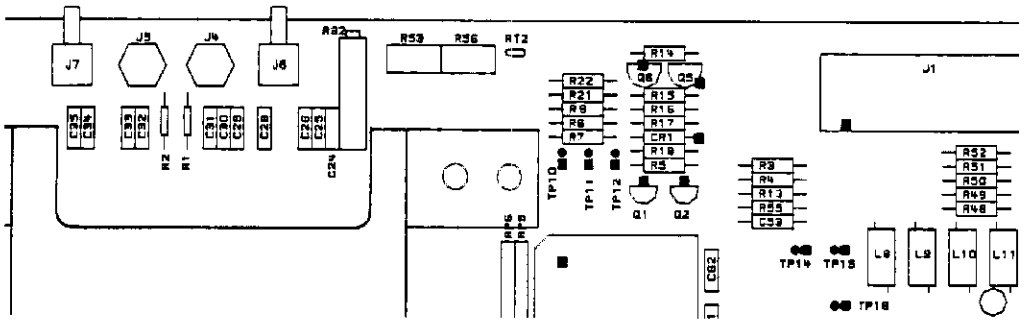
The instrument must be warm during the following adjustments. Be sure that it is turned off only for short periods when installing or removing jumpers.

CAUTION

The instrument power must not be on while installing or removing jumpers. Improper shorting can cause hardware failure resulting in expensive repair.

2. With POWER at STBY, use a jumper wire to short across R22 on the channel 1 ADC assembly (A5). See drawing below If you have two jumpers, save time and short the resistor on channel 2 ADC (A7) also. Set POWER to ON.

   View of center section of ADC assembly (A5, A7).



3. Press ***more, Utility, Cal Menu, Timebase Cal***, and ***Timebase Frequency Cal.***

4. Locate the two FFCLK cables connecting J4 and J5 of the channel 1 ADC assembly (A5) and the Timebase assembly (A1). Disconnect them at the Timebase assembly.

5. Set the GAP (R56) adjustment on the channel 1 ADC assembly (A5) to mechanical center.

6. Connect the DVM to the J6 (T1) SMB connector on the channel 1 ADC assembly (A5).

7. Turn the CLK (R53) adjustment on the channel 1 ADC (A5) fully **counter-clockwise** and note the reading on the DVM (typically between −70 mV and −120 mV).

8. Turn the CLK adjustment fully **clockwise** and note the reading (near ground, 0 V).

9. Reconnect the FFCLK cables.

10. Set the CLK adjustment so the DVM reading is half way between the readings in steps 7 and 8. Set the voltage within 1.5 mV. If R53 reaches its limit before the voltage is reached, leave it at that point and be sure to do the Testing Procedure below after all adjustments are complete.

11. Disconnect the DVM from J6 and using the cable and adapters, connect the power meter with sensor, through the filter, to J6.

12. Set meter to dB[REF]

13. Adjust GAP (R56) for a maximum power reading. To maintain power meter resolution, it may be necessary to occasionally press dB[REF] on the meter.

    If there is more than one power peak set R56 to the highest.

    If R56 reaches its limit while the power reading is still increasing, set it at the limit and be sure to do the Testing Procedure below when all adjustments are complete.

14. If adjusting both channels, repeat steps 2 through 13 for channel 2 (A7), then go on to step 15. If channel 2 has R22 already shorted go back to step 4. If adjusting one channel, proceed directly to step 15.

CAUTION

The instrument power must not be on while installing or removing jumpers. Improper shorting can cause hardware failure resulting in expensive repair.

15. Set POWER to STBY and remove shorting clips. Set POWER to ON.

16. Press ***more***, ***Utility***, ***Cal Menu***, and ***ADC Reference Cal***.

17. If any adjustment is at its limit, continue with the testing procedure; if not, the adjustment procedure is complete.

Testing Procedure:

If either potentiometer for a channel was at its limit, it is necessary to check the results of the adjustment procedure on that channel. This is done by running some of the self test loops. For channel 1 (A5) run loops 27-31 and for channel 2 (A7) run loops 36-40. Use the following procedure to run the tests.

1. Press ***Exit Cal Menu*** then ***Test Menu***.

2. Press top function key (right edge of display) to select ***RUN FROM LOOP*** and ENTER test #.

3. Press ***RUN FROM LOOP*** to select ***REPEAT LOOP*** and ENTER 1000.

4. Press ***Start Test***.

5. When test has finished press ***Display Errors***. ***Failures*** = should be 0.

6. Press ***Exit Display*** and ***REPEAT LOOP*** to select ***RUN FROM LOOP*** and ENTER the next test number.

7. Press ***RUN FROM LOOP*** to select ***REPEAT LOOP*** then press ***Start Test***.

8. Repeat steps 5 through 7 until all necessary loops have been run.

9. After the necessary test loops have been run, press ***Exit Test Menu***. If any test loop fails, even once out of the 1000 repetitions, repeat the Clock and Gap adjustments for that channel and run the test loops again.

4-9. GAIN AND FLAT ADJUSTMENTS

Description:

There are two low frequency adjustments, GAIN and FLAT. These adjustments compensate for variations is the GaAs sampling circuitry and adjust the low frequency pulse response.

If this adjustment is a result of an assembly replacement (table 4-A), do all other required adjustments then refer to table 3-A for required performance tests. Otherwise, perform the Measurement Accuracy and Offset Accuracy tests (section 3) on channel adjusted.

NOTE

Clock and Gap adjustments may influence the Gain and Flat adjustments. Be sure Clock and Gap adjustments are correct before starting this procedure.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse Generator	≤1% perturbation	Tektronix PG 506
Cable	BNC (m)	HP 10503A

Procedure:

1. Set up the pulse generator with the following parameters.

```
Output select    - Fast rise
Period           - 0.1 ms
  Var            - CCW
Pulse Amplitude - 0.2 V
```

2. Connect the positive FAST RISE OUTPUT (center BNC) of the pulse generator to the CHAN 1 input of the HP 54111D.

3. Press ***Chan 1*** and set or verify that the ***Input Impedance*** is 50Ω. Press AUTOSCALE to establish the signal. Set up the HP 54111D by setting or verifying the following parameters.

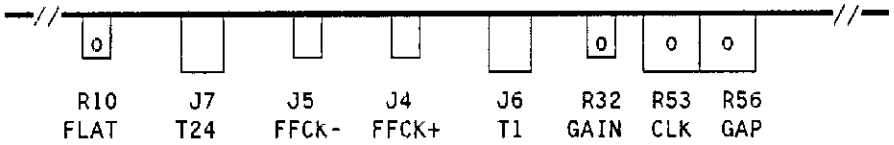
MENU SELECT	FUNCTION SELECT	SETTING
Chan 1,2	VOLTS/DIV OFFSET	20 mvolts/div as required
Timebase	TIME/DIV DELAY Delay Ref at Auto/Trgd Sweep	500 ns/div 2.2 us Center Trgd
Display	Disp Mode Averaging NUMBER OF AVERAGES Screen Graticule	Repetitive ON 8 Single Grid

NOTE

The signal will overdrive the input and the bottom will be clipped by the display. This will have no detrimental effect during these adjustments.

4. Press ***Chan 1*** and ***OFFSET***. Adjust the ***OFFSET*** to put the top of the pulse 3 divisions above center screen. If it is slightly above or below a grid line, flatness deviations will be more readily apparent.

Top view of center section of ADC assembly (A5, A7).



5. On channel 1 ADC assembly (A5), adjust GAIN (R32) for start and end points of the pulse at the same level. To help visualize changes, use ***OFFSET*** to keep waveform close to the grid line.

6. Adjust FLAT (R10) for flattest pulse response.

7. Press ***more***, ***Utility***, ***Cal Menu***, ***ADC Reference Cal***, and ***more***.

8. Repeat the procedure, starting at step 5, until best flatness is achieved.

9. Repeat steps 2 through 8 for channel 2 (A7).

4-10. CALIBRATOR AMPLITUDE ADJUSTMENT

Description:

This procedure adjusts the amplitude of the front panel CAL signal. This signal is used to run calibration routines in the instrument.

The adjustment is done by forcing this signal high and adjusting it while measuring it with an accurate voltmeter. Forcing the signal high is done through a front panel setup. On earlier versions it is necessary to force the output high by using a shorting wire.

The performance test is not necessary after adjustment because the adjustment tolerance is tighter than the performance test tolerance.

If calibrator amplitude is adjusted as a result of replacement of an assembly (table 4-A), see table 3-A for appropriate performance tests. Otherwise, perform the Measurement Accuracy test in section 3 for both channels and the Probe Tip Calibration for TRIG 3 and TRIG 4 in this section.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Voltmeter	Better than 0.05% accuracy	HP 3468A

Procedure A:

1. Connect the DC voltmeter + input to the front panel calibrator signal and – input to ground at the CHAN 1 input BNC.
2. In order, press ***more***, ***Utility***, ***Cal Menu***, ***Timebase Cal*** and ***Timebase Freq Cal*** softkeys.
3. Read the voltmeter. If the measurement is about +0.8 Vdc the instrument is a later version and firmware controlled. Proceed to step 4. If the measurement is about +0.4 Vdc press ***Exit*** and continue with Procedure B on the next page.

Top view of front of Timebase assembly (A1).

4. Adjust R10 as close as possible to +0.8000 V. It must be within ±0.002 Vdc. The adjustment is complete.
5. Press ***Exit***.

Procedure B:

The calibrator output must be forced high with a shorting wire so that it can be measured by a voltmeter.

1. Connect the DC voltmeter + input to the front panel calibrator signal and – input to ground at the CHAN 1 input BNC.

2. The drawing below shows the top front corner of the Timebase assembly A1. The Timebase assembly is the left-most assembly in the card cage. Note the position of R4, specifically the bottom end of this resistor.

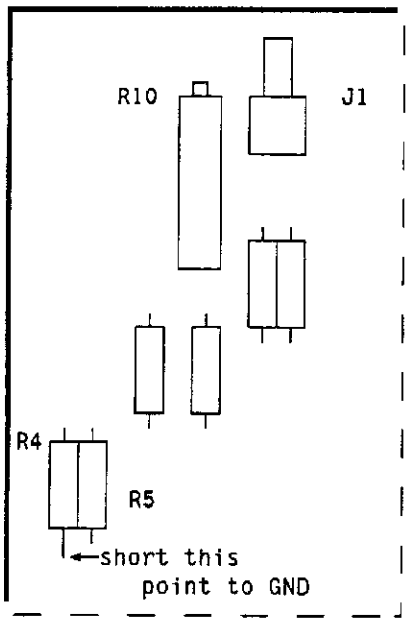
3. Connect one end of a jumper wire to the body of J1 (see picture) on the Timebase. Connect a long grabber to the other end of the jumper.

4. Connect the grabber to the bottom end of R4.

5. Read the measurement on the voltmeter. Adjust R10 as close as possible to +0.8000 V. It must be within ±0.002 Vdc.

6. Disconnect the jumper and DVM.

Top-front corner of Timebase assy. (A1)



4-11. ATTENUATOR ADJUSTMENT

Description:

Channel 1 and channel 2 attenuator assemblies have two compensation adjustments, X10 and X100. These are set at the factory and normally do not require further adjustment.

Since replacement attenuators are adjusted at the factory no further adjustment should be necessary. For other adjustments necessary after attenuator replacement see table 4-A. For performance tests necessary after attenuator replacement see table 3-A. No performance tests are required after only adjusting an attenuator.

NOTE

DO NOT PERFORM THESE ADJUSTMENTS DURING ROUTINE CALIBRATIONS. *It is necessary to partially disassemble the instrument for these adjustments.* ***DO NOT*** *perform these adjustments unless the Low Frequency Input Adjustments have been made and it is desirable to optimize flatness from 50 mV/div to 5 V/div.*

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse Generator	≤1% perturbation	Tektronix PG 506
Cable	BNC (m)	HP 10503A
Adjustment tool	- - - - - - - - - -	HP 8710-1515

Procedure:

1. Without disconnecting any cabling, perform the Front Panel Removal procedure in Section 6A of this service manual. Set the front panel about 10 cm in front of its normal position.

2. With instrument in its normal operating position, remove the screw that fastens the rear of the attenuator to be adjusted. It can be reached from the top. *This screw is not captive.* ***DO NOT*** *allow it to fall into the instrument as it will be difficult to remove.*

3. Set the instrument on its left side and without disconnecting any cabling, slide the attenuator foreward, exposing its bottom. The adjustments are about 1 cm from the front edge. The X100 adjustment is in front and the X10 directly behind.

4. Set up the pulse generator with the following parameters.

   ```
   Output select   - Fast rise
   Period          - 0.1 ms
   Pulse Amplitude - 500 mV
   ```

5. Connect the positive-going FAST RISE OUTPUT of the pulse generator to the input of the attenuator to be adjusted.

6. Press ***Chan X*** (whichever is appropriate) and ensure the ***Input Impedance*** is 50Ω. Press AUTOSCALE to establish the signal. Continue setup of the HP 54111D by setting or verifying the following parameters.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1 or 2	VOLTS/DIV	50 mvolts/div
	OFFSET	100 mV
Timebase	TIME/DIV	5 us/div
	DELAY	20 us
	Delay Ref at	Center
Display	Disp Mode	Repetitive
	Averaging	ON
	NUMBER OF AVERAGES	8
	Screen	Single
	Graticule	Grid

7. Press ***Chan X*** (whichever is appropriate) and ***OFFSET*** and set the the offset to put the top of the pulse 3 divisions above center screen. If it is slightly above or below a grid line, flatness deviations will be more readily apparent.

8. Adjust X10 adjustment (rear capacitor) for best flatness.

9. Set VOLTS/DIV to 500 mV/div.

10. Set pulse generator amplitude to MAX or 5 V, whichever occurs first.

    NOTE: *If you are using a PG 506 the maximum output is about 1 V, so the pulse amplitude will be about 2 divisions. Do not set the HP 54111D for a lower range since 500 mV/div is the lowest that this adjustment covers.*

11. Press ***Chan X*** (whichever is appropriate) and ***OFFSET*** and set the the offset to put the top of the pulse 3 divisions above center screen. If it is slightly above or below a grid line, flatness deviations will be more readily apparent.

12. Adjust X100 adjustment (front capacitor) for best flatness.

13. If the other channel is being adjusted, repeat steps 2 through 12 for it.

14. After adjustments are complete reassemble instrument, reversing the disassembly procedure.

CAUTION

Before installing front panel, be sure three-wire cables at front of attenuators do not become pinched and ensure that all probe sense rings around the input BNCs are inserted into their recesses properly.

4-12. VERTICAL SELF-CALIBRATION

The self-calibration procedures calibrate circuitry with internal routines and adjustments The following procedures are tailored to the Adjustments section and are therefore abbreviated.

If you are doing a complete adjustment procedure, follow the self-calibration completely and in the order given.

4-13. ADC Reference Calibration

Calibrates the ADC references.

Procedure:

1. Press ***more, Utility, Cal Menu***, and ***ADC Reference Cal***.
2. Continue with the next procedure, Vertical Calibration.

4-14. Vertical Calibration

Vertical calibration calibrates vertical sensitivity and offset.

Procedure:

1. Disconnect all inputs to CHAN 1 and CHAN 2.
2. Press the ***Vertical Cal*** and ***Continue***. When calibration is complete the instrument will return to the Cal Menu.
3. Continue with the next procedure, Probe Tip Cal.

4-15. Probe Tip Calibration

The Probe Tip Cal calibrates from the probe tip through the A/D converters.

NOTE

This procedure is usually done for any channel or trigger that has had the probe changed. The vertical specifications for a channel or trigger are only met with the probe it was calibrated with.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Divider Probe	10:1 1 MΩ	HP 10431A/033A/017A

Procedure:

NOTE

You may use the same probe for both channels and both triggers unless you need to calibrate each input to a specific probe (see note on previous page).

1. Press ***Probe Tip Cal*** and ***Calibrate Probe Tip CHAN 1.*** Follow the instructions on the display.
2. When the calibration for CHAN 1 is done calibrate CHAN 2, TRIG 3, and TRIG 4.
3. Press ***Exit*** then continue with the next procedure, DC Gain Adjustment.

4-16. DC GAIN ADJUSTMENT

This adjusts the DC gain to match the high frequency gain.

If DC Gain adjustment is a result of an assembly replacement (table 4-A), see table 3-A for necessary performance tests. Otherwise, perform the Measurement Accuracy and Offset Accuracy tests on the channel adjusted.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Supply	+780 to +820 mV .1 mV resolution	HP 6115A
DC Voltmeter	Better than 0.1% accuracy	HP 3468A
Oscilloscope Probe	10:1	HP 10033A or 10017A

Procedure:

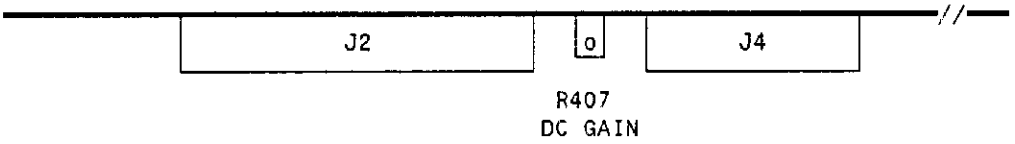
1. Perform a one-key powerup* to set the instrument to default conditions.
   *Power to STBY Press and hold one key Power to ON Release key when "Powerup Self Test Passed!" is displayed.
2. Connect the 10:1 probe to the CHAN 1 input. If you are using an HP 10033A probe, skip the next step.
3. Enter probe attenuation factors. Press ***more, Utility, Probe Menu***, then for both channels; ***CHAN X PROBE ATTN*** and in the ENTRY keys, 10 and ENTER.

4. Set the following additional parameters in the order given.

MENU SELECT	FUNCTION SELECT	SETTING
Display	NUMBER OF AVERAGES Screen	16 Single
Chan 1,2	Display VOLTS/DIV	Chan 1 ON, Chan 2 OFF 10 mvolts/div
Timebase	TIME/DIV	5 us/div
Delta V	V Markers Preset Levels	ON 50-50%

5. Short probe tip to probe ground clip.
6. Press ***Auto Level Set*** and record the ***V(1)***= reading in the lower left corner of the display.
7. Add +800 mV to the reading in step 6.
8. Press ***Chan 1*** and ***OFFSET*** and set offset to the result from step 7.
9. Use the voltmeter to set the power supply to +800 mV ±1 mV.
10. Connect the probe to the output of the supply (probe tip to + and ground to –).

Top view of front end of ADC Control assembly (A4, A6).



11. On Chan 1 ADC Control assembly (A4), adjust DC GAIN (R407) to set the trace at center screen.
12. Disconnect the probe from the power supply and CHAN 1 input and connect it to the CHAN 2 input.
13. Press ***Chan 1***, ***Display (Off)***, ***Chan 2***, ***Display (On)***, and ***VOLTS/DIV***; then in the ENTRY keys, 10 and mV.
14. Press ***Delta V*** and repeat steps 5 to 11, substituting Chan 2 for Chan 1.
15. Perform a one-key powerup to return the instrument to default conditions.
    *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed

4-17. TRIGGER CALIBRATION

Trigger Cal calibrates trigger levels and trigger sensitivity (hysteresis).

Procedure:

1. Press ***Trigger Cal*** and follow the instructions on the display. It could take several minutes for the CHAN 1 and CHAN 2 trigger to calibrate. The arrow will move across the display, showing that the calibration is proceeding.

2. When CHAN 1 and CHAN 2 have calibrated the display will give further instructions. Follow the instructions to calibrate TRIG 3 and TRIG 4.

3. When calibration of the triggers is complete, the instrument will return to the Cal Menu.

4-18. TIMEBASE CALIBRATION

Timebase Calibration consists of Timebase Frequency Calibration and Channel Skew Alignment.

4-19. Timebase Frequency Calibration

The Timebase Frequency Calibration provides an error correction to compensate for a timebase frequency that is different from nominal. It improves the accuracy of time-interval measurements.

If the timebase frequency resulting from this procedure is recorded in the permanent file for this instrument it can be re-entered if the cal factors are inadvertently lost. Nominal is 50.05 MHz

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Frequency Counter *	51 MHz and 50 mV sensitivity 5 digit resolution	HP 5384A
Cable	BNC (m)	HP 10503A

* To maintain a traceable calibration (e.g., U.S. National Bureau of Standards), you must use a traceable frequency counter

Procedure:

1. Press ***Timebase Cal*** and ***Timebase Freq Cal***.

2. **CAUTION!!** This adjustment affects timebase traceability. Press ***Exit*** to preserve present calibration.

3. Follow the instructions on the display.

4. Record the calibration factor in the Performance Test Record or other permanent record for this instrument.

5. Press ***Continue*** to enter the new frequency.

4-20. Channel Skew Alignment

Channel Skew time-aligns the signal that is input to CHAN 1, CHAN 2, TRIG 3, and TRIG 4.

Alignment occurs at the intersection of the input signal's rising edge and the HP 54111D's center horizontal graticule. For each input, this point becomes time-aligned with the zero-delay point.

Alignment includes time delays both internal and external to the HP 54111D, including probe or BNC cable length.

The primary importance in doing the Channel Skew procedure at this time is to set up the instrument for the Trigger Qualifier Adjustments. The setup is designed with that in mind.

For instruments with a serial prefix 2808A and later, the rear panel TIMEBASE CAL output can be used to do skew alignment. Use it instead of the pulse generator

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse generator *	≤500 kHz square wave ≤5 ns risetime	HP 8082A
Cable	BNC (m) (≈3 feet)	HP 10503A
Cables (2)	BNC (m) (9 inch, equal length)	HP 10502A
Adapter	BNC Tee (m)(f)(f)	1250-0781
Adapter (BNC Barrel)	BNC(f) to BNC(f)	1250-0080

* The rear panel TIMEBASE CAL output can be used on instruments with a serial prefix of 2808A or later.

Procedure:

If the instrument to be calibrated has a serial prefix of 2808A or later, it is not necessary to set up the pulse generator when doing only the skew alignment. You can use the TIMEBASE CAL output as a signal, in the same manner as the pulse generator is used. The pulse generator will be used later however, when Trigger Qualifier adjustments are also done.

1. Skip this step if using the rear panel TIMEBASE CAL output. Set up the pulse generator with the following parameters. This setup is not necessary to do just channel skew. The same setup will be used in the Trigger Qualifier adjustments later.

```
Input Mode          - Norm
Pulse               - Normal
Period              - ≥2 us
Width               - Square Wave
Leading edge        - 1 ns
Trailing edge       - 1 ns
Amplitude           - +1.2 V
Offset              - -0.6 V
```

2. Connect the long BNC cable to the left pulse generator output (or HP 54111D TIMEBASE CAL output on prefix 2808A and later) and using the BNC barrel, connect the other end to the center of the BNC Tee.

3. Connect the two 9-inch BNC cables from the BNC Tee to the CHAN 1 and CHAN 2 inputs of the HP 54111D.

4. Press ***Chan 1*** and ***Chan 2*** in turn and set the input impedance on both channels to 50Ω.

5. Press AUTOSCALE to establish the display.

6. Change to or confirm the following on the HP 54111D.

MENU SELECT	FUNCTION SELECT	SETTING when using: Pulse generator	Timebase Cal
Chan 1,2	VOLTS/DIV	200 mvolts/div	30 mvolts/div
	OFFSET	0.00V	-220 mV
Timebase	TIME/DIV	500 ps	500 ps
Trigger	Trigger Mode	Edge	Edge
Chan 1,2	Trig Src	Chan 1	Chan 1
	TRIGGER LEVEL	0.00 V	-220 mV
	Slope	Pos	Pos
Trig 3,4	TRIGGER LEVEL	0.00 V	-220 mV
	Slope	Pos	Pos
	INPUT	50Ω	50Ω

7. Press ***more, Utility, Cal Menu, Timebase Cal***, and ***Channel Skew***.

8. Whichever signal source is being used, the requirements should be met. Press ***Continue*** to start the calibration.

9. Follow any prompts on the display during the procedure.

10. The instrument will align channel 1 and channel 2, then prompt you to move the CHAN 2 signal to TRIG 3 and press ***Continue***.

11. After aligning trigger 3 the display will prompt you to move the TRIG 3 signal to TRIG 4 and press ***Continue***.

12. When alignment is completed the instrument will return to the Cal Menu.

4-21. TRIGGER QUALIFIER ADJUSTMENTS

The Trigger Qualifier adjustments calibrate the time measurement functions of the HP 54111D. There are four adjustments. Some of them can be done individually, but some need to be preceeded by other adjustments. The figure below shows the proper sequence for each adjustment.

No performance tests are required after trigger qualifier adjustment.

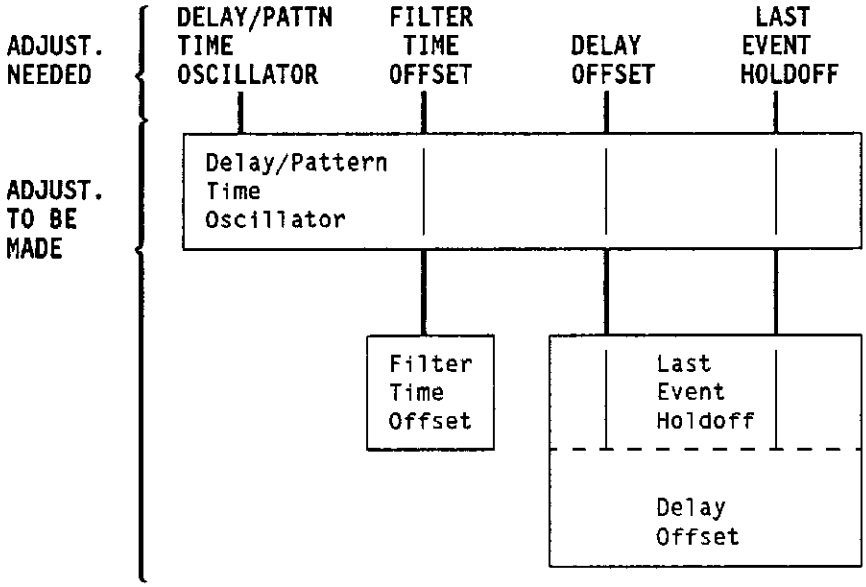


Figure 4-1. Trigger Qualifier Adjustment Sequence.

4-22. Delay/Pattern Time Oscillator Adjustment

Description:

This adjustment controls the frequency of the clock used to measure Trigger Qualifier time delays. It is not connected with the main timebase of the oscilloscope. The 100 MHz oscillator is adjusted for 50 MHz at J14.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Frequency Counter	50 MHz and 50 mV sensitivity 5 digit resolution	HP 5384A
Divider Probe	10:1 1 MΩ	HP 10431A/033A/017A

Procedure:

1. Set the following parameters on the HP 54111D. No other parameters are important.

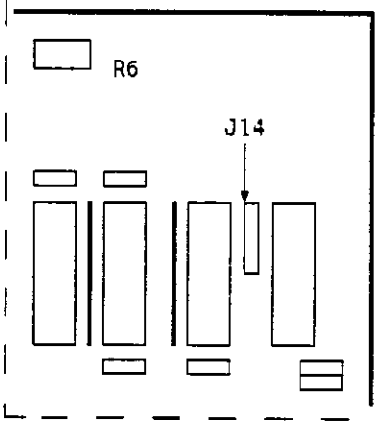
MENU SELECT	FUNCTION SELECT	SETTING
Timebase	Auto/Trgd Sweep	Trgd
Trigger	Trigger Mode Trigger on Pattern When TIME	Pattern X X X X Present > 30.00 ns

2. With the miniature divider probe, connect the frequency counter to J14 on the trigger qualifier assembly (A9). J14 is located at the rear of the board, about 4 cm down from the top edge (see views at right and below. It may be necessary to remove the side cover in order to see where to attach the probe and make the adjustment.

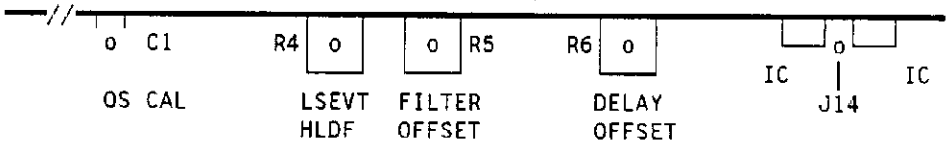
3. Adjust C1 (OS CAL) for a frequency of 50 MHz ±0.02 MHz. C1, the only adjustable capacitor, is near the center of the board, vertically and horizontally.

4. Disconnect the probe from J14.

Top-rear of Trig Qual Assy



Top view of rear end of Trigger Qualifier Assembly (A9)



4-23. Filter Time Offset Adjustment

Description:

Filter Offset is adjusted until oscilloscope will just trigger when a 20 ns pulse is applied.

NOTE

Delay/Pattern Time Oscillator Adjustment must be performed before adjusting the Filter Time Offset.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse generator	300 ns period 20 ns adjustable pulse width 1 - 3 ns risetime and falltime	HP 8082A
BNC-to-BNC cable		HP 10503A

Procedure:

During this and the following procedures, the HP 54111D will use trigger levels and marker levels while making time interval measurements. The procedures are set up to use 0.0 V for both, so the signal generator is set up to swing the signal through 0 V.

If you are using a substitute pulse generator that cannot swing the 1.2 V p-p signal around 0 Volts, be sure to set the correct trigger level and V Markers in the HP 54111D setup (see footnote at bottom of table in step 2).

1. Set up the pulse generator with the following parameters.

```
Input Mode          - Norm
Pulse               - Normal
Period              - 300 ns
Delay               - 0 ns
Width               - 20.0 ns
Leading edge        - 1 ns
Trailing edge       - 1 ns
Amplitude           - +1.2 V
Offset              - -0.6 V
```

2. Perform a one-key powerup* to set instrument to default conditions, then set the following parameters in the order given. If you are doing the entire Trigger Qualifier adjustment procedure, store this setup by pressing SAVE SETUP and a numeric key. Use this SETUP as a starting point for the other procedures, or to recall the setup if the instrument power needs to be turned off.

*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

MENU SELECT	FUNCTION SELECT	SETTING
Display	Disp Mode	Repetitive
	NUMBER OF AVERAGES	4
	Screen	Single
Chan 1	Display	ON
	VOLTS/DIV	200 mvolts/div
	Input Impedance	50Ω
Chan 2	Display	OFF
	VOLTS/DIV	100 mvolts/div
	OFFSET	-380 mvolts
	Input Impedance	50Ω
Timebase	TIME/DIV	5.00 ns/div
	Auto/Trgd Sweep	Trgd
Trigger	Trigger Mode	Edge
	Trig Src	Chan 1
	TRIGGER LEVEL	0.00 volts * (Chan 1,2)
	Slope	Neg (Chan 1,2)
Delta V	V Markers	ON
	MARKER 1 POSITION	Chan 1 0.00 volts *
	MARKER 2 POSITION	Chan 1 0.00 volts *
Delta t	T Markers	ON
	START ON POS EDGE	1
	STOP ON NEG EDGE	1

* The Trigger Level and the V Marker references must be the same. If the pulse generator you are using cannot swing a signal around 0 Volts, set the trigger levels and V Markers to the same voltage, at the vertical center of the 1.2 V peak-to-peak signal.

3. Connect the pulse generator output to channel 1. The display should be pulse whose width is ≈20 ns with an amplitude of 6 divisions peak-to-peak. The trailing edge is at time zero (center screen).

4. Press ***Delta t*** and ***Edge Find*** to measure the width of the pulse. Adjust the pulse generator width to obtain a 20 ns ±100 ps pulsewidth measurement (Δt= 19.9 to 20.1 ns) each time ***Edge Find*** is pressed.

NOTES

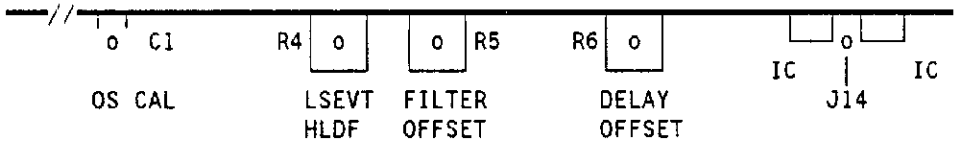
Edge Find uses the V Markers as a reference to measure the pulse. The Measure functions use other parameters which may not be compatible with the adjustment being made.

If the increments of the pulse generator width control are too coarse, use the amplitude control as a fine adjustment of width. Increase amplitude to increase width and vice versa.

5. Change the trigger parameters on the HP 54111D.

MENU SELECT	FUNCTION SELECT	SETTING
Trigger	Trigger Mode Trig On Pattern When Time	Pattern H X X X (default) Present > 20.00 ns

Top view of rear end of Trigger Qualifier Assembly (A9)



6. Adjust FILTER OFFSET (A9R5) until oscilloscope just triggers. Ideally, adjustment should be right on the threshold where the scope is intermittently triggering. This is indicated by slowed acquisition (the dots in the display are not replaced as quickly. Also the advisory "***Awaiting Trigger***" may occasionally appear.

7. If you are doing a complete adjustment procedure go directly to step 6 of the Last Event Holdoff Adjustment, the next procedure.

4-24. Last Event Holdoff and Delay Offset Adjustments

Description:

Last Event Holdoff is adjusted for a 4 ns delay after the second to the last event before main trigger is enabled. Delay Offset is adjusted so trigger will enable on a negative pulse edge which occurs 30 ns after a positive pulse edge.

NOTE

The Last Event Holdoff and Delay Offset adjustments must be preceded by the Delay/Pattern Time Oscillator adjustment.

Equipment Required:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse generator	20 ns adjustable pulse width 300 ns period ≤2 ns risetime and falltime	HP 8082A
Adapter	SMB (f) to BNC (f)	HP 1250-1236
Cable	BNC (m)	HP 10503A

* It is necessary to connect the SMB connector at J13 to the Channel 2 input BNC. Some cables and adapters are part of the HP 54110 Family Support Kit. Use whatever you have that can properly handle the 1 ns risetime pulse from J13.

Procedure:

LAST EVENT HOLDOFF ADJUSTMENT

1. Set up the pulse generator with the following parameters. If you are using a substitute pulse generator that cannot swing the 1.2 V p-p signal around a 0 Volt baseline, be sure to set the appropriate trigger level and V Markers in the HP 54111D set up.

```
Input Mode          - Normal
Pulse               - Normal
Period              - 300 ns
Delay               - 0 ns
Width               - 20.0 ns
Leading edge        - 1 ns
Trailing edge       - 1 ns
Amplitude           - +1.2 V
Offset              - -0.6 V
```

2. Perform a one-key powerup* to set instrument to default conditions, then set the following parameters in the order given. If you saved the setup from the Filter Time Offset, recall it.
*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed" is displayed

MENU SELECT	FUNCTION SELECT	SETTING
Display	Disp Mode	Repetitive
	NUMBER OF AVERAGES	4
	Screen	Single
Chan 1	Display	ON
	VOLTS/DIV	200 mvolts/div
	Input Impedance	50Ω
Chan 2	Display	OFF
	VOLTS/DIV	100 mvolts/div
	OFFSET	-380 mvolts
	Input Impedance	50Ω
Timebase	TIME/DIV	5.00 ns/div
	Auto/Trgd Sweep	Trgd
Trigger	Trigger Mode	Edge
	Trig Src	Chan 1
	TRIGGER LEVEL	0.00 volts * (Chan 1,2)
	Slope	Neg (Chan 1,2)
Delta V	V Markers	ON
	MARKER 1 POSITION	Chan 1 0.00 volts *
	MARKER 2 POSITION	Chan 1 0.00 volts *
Delta t	T Markers	ON
	START ON POS EDGE	1
	STOP ON NEG EDGE	1

* The Trigger Level and the V Marker references must be the same. If the pulse generator you are using cannot swing a signal around 0 Volts, set the trigger levels and V Markers to the same voltage, at the vertical center of the 1.2 V peak-to-peak signal.

3. Connect pulse generator output to channel 1. The display should be a ≈20 ns pulse with an amplitude of 6 divisions peak-to-peak. The trailing edge is at time zero (center screen).

4. Change the trigger parameters on the HP 54111D.

MENU SELECT	FUNCTION SELECT	SETTING
Trigger	Trigger Mode	Pattern
	Trig On Pattern	H X X X (default)
	When	Present >
	Time	20.00 ns

5. Adjust pulse generator pulse width using Width and Amplitude (fine adjust) until the oscilloscope is just on the threshold of triggering.

6. Set channel 1 to OFF, and channel 2 to ON.

7. Remove the short coaxial cable from J13 (DOUT, rear-most coax) on Trigger Qualifier assembly (A9). Connect the SMB-to-BNC cable between J13 and the input BNC of Chan 2. A pulse should be displayed.

8. Press ***Timebase***, and ***TIME/DIV*** and enter ***2.00 ns/div***. Press ***DELAY*** and use the knob to bring leading edge of the positive pulse on channel 2 to precisely center screen.

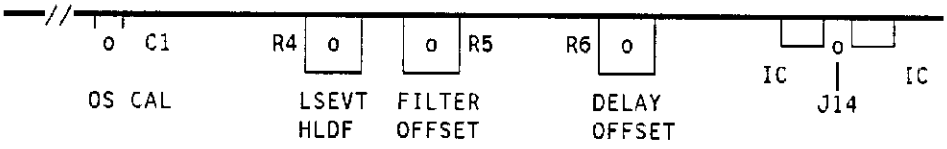
NOTE

Do not change DELAY setting for the following steps.

9. Change HP 54111D trigger to:

MENU SELECT	FUNCTION SELECT	SETTING
Trigger	Trigger Mode After XXX Edge On TRIGGER ON X EVENTS Of XXX Edge On	Events Pos Chan 1 2 Neg Chan 1

Top view of rear end of Trigger Qualifier Assembly (A9)



10. Observe positive transition on channel 2 to the right of center screen and adjust LSEVT HLDF (A9R4) to position edge as close as possible to 2 divisions (4 ns) to the right of center screen. Edge must be between 1.5 and 4 divisions to the right of center screen.

11. Disconnect the SMB-to-BNC cable from J13 and reconnect the short SMB-to-SMB cable.

DELAY OFFSET ADJUSTMENT

NOTE

Do not start this adjustment from this point. Delay/Pattern Time Oscillator Adjustment and Last Event Holdoff Adjustments must be performed before adjusting the Delay Offset (see figure 4-1).

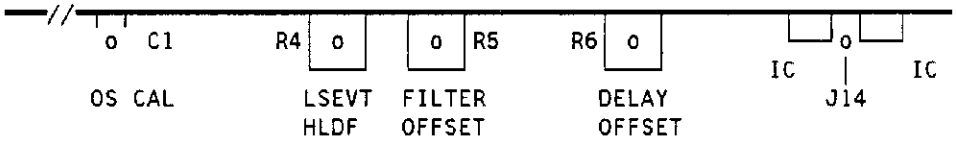
12. Change the following parameters on the pulse generator.

```
Pulse          - Double
Delay          - 50.0 ns
Width          - 30.0 ns
```

13. Change the following parameters on the HP 54111D.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 2	Display	OFF
Timebase	TIME/DIV	20 ns/div
Trigger	Trigger Mode	Edge

Top view of rear end of Trigger Qualifier Assembly (A9)



14. Preset DELAY OFFSET (A9R6) fully clockwise.

15. The display should be two pulses approximately 30 ns wide, with an amplitude of 6 divisions peak-to-peak. The trailing edge of the first pulse is at time zero (center screen).

16. Press ***Delta t*** and ***Edge Find*** to measure the width of the first pulse. Adjust the pulse generator width to obtain a 30 ns ±100 ps pulsewidth measurement (Δt= 30.00 ns) every time ***Edge Find*** is pressed.

NOTES

Edge Find uses the V Markers as a reference to measure the pulse. The Measure functions use other parameters which may not be compatible with the adjustment being made.

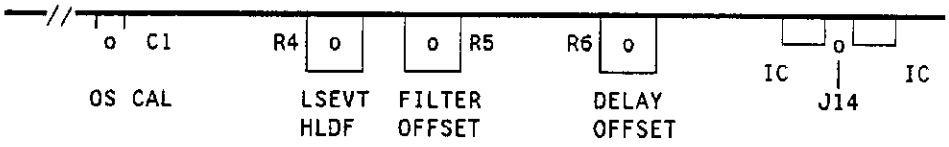
If the increments of the pulse generator width control are too coarse, use the amplitude control as a fine adjustment of width. Increase amplitude to increase width and vice versa.

17. Change HP 54111D trigger to:

MENU SELECT	FUNCTION SELECT	SETTING
Trigger	Trigger Mode After XXX Edge On DELAY XX.XX THEN Trig On XXX Edge On	Time Pos Chan 1 30 ns Neg Chan 1

18. The 54111D should be triggered on the negative edge of the second pulse.

Top view of rear end of Trigger Qualifier Assembly (A9)



19. Adjust DELAY OFFSET (A9R6) to the point where the scope switches from triggering on the second pulse to triggering on the first pulse. Ideally this would be the point where the scope is equally triggered on both negative edges as indicated by two pulses intermittently displayed either side of a stable pulse.

4-25. COLOR CRT MODULE ADJUSTMENTS

NOTE

DO NOT PERFORM THESE ADJUSTMENTS DURING ROUTINE CALIBRATIONS. *The following procedures are provided only for the few extreme cases where either the earth's magnetic field or the user's environment cause an unusable display due to mis-convergence that cannot be corrected by degaussing the entire CRT screen.*

It is recommended that these adjustments be performed only by qualified personnel who are familiar with color CRT convergence procedures.

Before starting adjustments, mark the position where potentiometers are set. This helps in returning adjustments to their original positions if it becomes necessary to restart the procedure.

Description:

The Color CRT Module is adjusted to compensate for magnetic influences causing mis-convergence.

NOTE

DO NOT *continue this procedure before first degaussing the CRT screen using the rear panel degaussing switch. In extreme cases of magnetism, it may be necessary to degauss the CRT using a conventional external television-type degaussing coil.* ***During any of the following adjustments, the CRT module must face west.***

Equipment Required:

Non-metallic Adjustment Tool ..... Sony Part Number 4-367-065-01
HP Part Number 8710-1355

Procedure:

NOTE

The following adjustments are broken down in adjustment groups. The adjustment group sequence must be followed in order due to interaction and dependency. The adjustment group sequence is shown in the adjustment flow diagram on the next page. There will be cases where not all the adjustments groups will be used. For example, if the Geometry Adjustment Group corrects the problem, this will be the only group used.

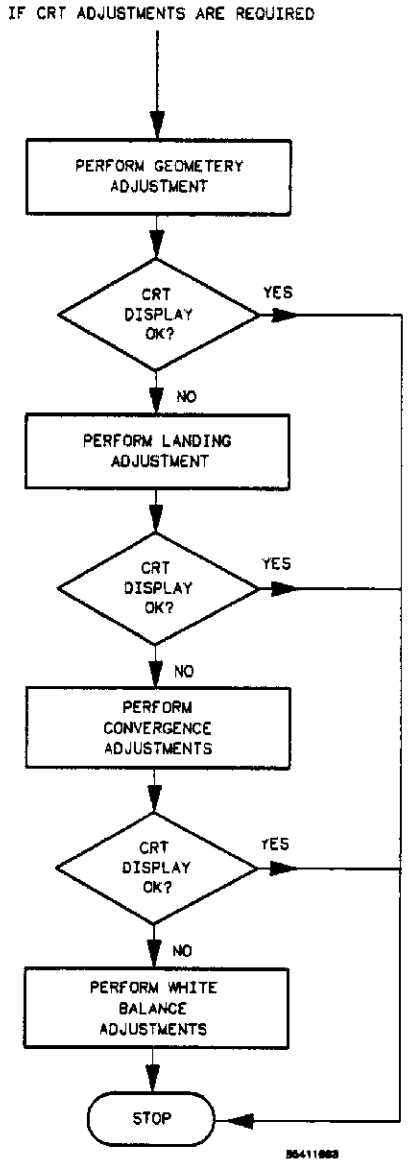


Figure 4-2. CRT Module Adjustment Flow Diagram.

Geometry Adjustments

1. Press ***Utility***, ***CRT Setup Menu***, then ***Pattern*** key as required until the white cross-hatch is displayed on CRT.
2. Preset front panel BACKGROUND control to mechanical center.
3. Preset front panel BRIGHTNESS control maximum clockwise.
4. Preset H.SUB SHIFT (RV006) and V.SUB SHIFT (RV008) located on the bottom PC board to mechanical center.
5. Using a flexible ruler, adjust H.SIZE (RV504) AND V.HEIGHT (RV502) located on the left hand side PC board so that the border of the cross-hatch pattern displayed on the CRT is 120.5 mm (4.74 in.) vertically and 161 mm (6.34 in.) horizontally.
6. Adjust V.CENT (RV510) AND H.CENT (RV503) located on the left hand side PC board to center pattern.
7. Adjust PIN AMP (RV506) located on the left hand side PC board to eliminate pincushion distortion in the vertical lines of the cross-hatch pattern as shown in the next figure.

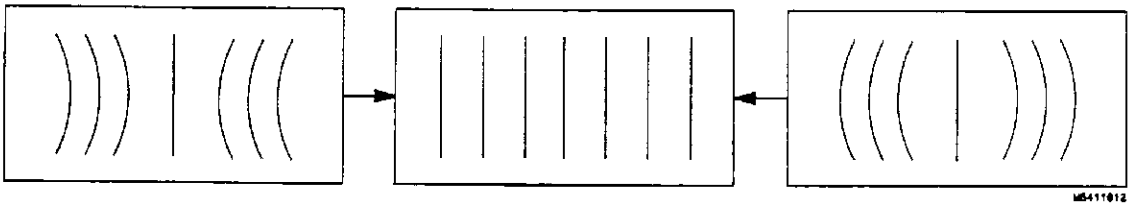


Figure 4-3. PIN AMP Adjustment.

8. Adjust PIN PHASE (RV505) located on the left side PC board to eliminate pin phase distortion in the vertical lines of the cross-hatch pattern as shown in the next figure.

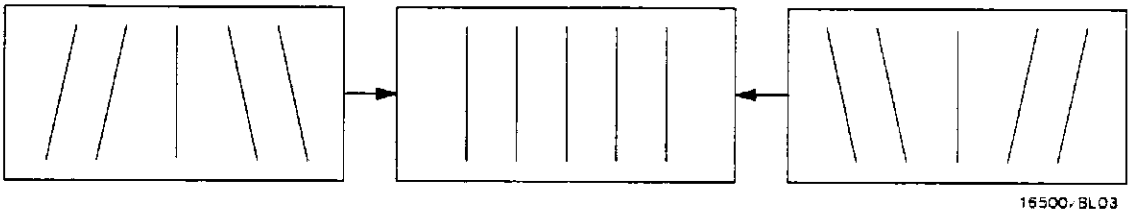


Figure 4-4. PIN PHASE Adjustment.

9. Adjust TOP PIN (RV511) located on the left hand side PC board so that top horizontal line is parallel with the center horizontal line.
10. Adjust BOTTOM PIN (RV512) located on the left hand side PC board so that bottom horizontal line is parallel with the center horizontal line.

Focus, Landing, and Convergence Adjustment Preparation Procedures

NOTE

Note the original routing of all cabling for proper routing when module is re-installed in instrument. Then, re-route the cables from inside the module to the outside (left side) of module for reconnection to the power supply for adjustments.

1. Remove Color CRT Module from the instrument (see section 6A of this service manual).
2. Reconnect instrument front panel and re-install front panel and CRT bezel (use two screws to temporarily hold front panel in place).
3. Loosen deflection yoke clamp screw.
4. With Color CRT Module placed to the left of mainframe, reconnect module.
5. Remove deflection yoke spacers by moving deflection yoke rearward and removing spacers.

NOTE

The deflection yoke spacers are tapered rubber blocks located between front of yoke and rear of CRT funnel.

6. Apply power and allow the instrument to thermally re-stabilize for 20 minutes.

Focus Adjustment

NOTE

Geometry adjustments must be performed before making focus adjustment.

1. In ***Utility*** menu, press ***CRT Setup Menu***, then press ***Pattern*** key as required until the white cross-hatch is displayed on CRT.
2. Adjust FOCUS (RV701) located on the rear PC board for best overall focus.

Landing Adjustment

1. In ***Utility*** menu, press ***CRT Setup Menu***, then press ***Color Purity*** key (fourth key from top) as required until a white raster is displayed on CRT.
2. Turn front panel BRIGHTNESS control fully clockwise.
3. Degauss entire CRT screen by pressing momentary DEGAUSSING switch located on the instrument rear panel.

NOTE

In cases where the user's environment or shipping environment has caused high levels of magnetization to take place, it may be necessary to externally degauss the CRT using a conventional television type degaussing coil to completely degauss the CRT.

4. Set purity magnet tabs to mechanical center (see next figure).

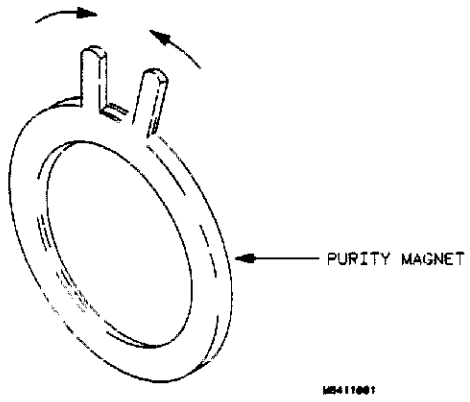


Figure 4-5. Purity Magnet Centering.

5. Press ***Color Purity*** key as required until a green raster is displayed on CRT.

6. Move deflection yoke rearward until left edge of raster turns red and right side of raster turns blue (see figure below).

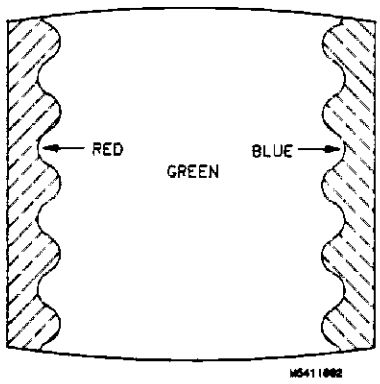


Figure 4-6. Purity Magnet Adjustment Raster.

7. Adjust purity magnets until green is in center of raster with red and blue bands evenly distributed on the sides (see above figure).

8. Move deflection yoke forward until entire raster is green.

NOTE

Landing adjustment is easier if yoke is moved all the way forward and then moved back until raster is completely green.

9. Using ***Color Purity*** key, replace green raster with red and then blue raster each time checking for proper landing adjustment (color purity of each).

10. If landing is not correct in step 9, repeat steps 6 through 9 for best compromise (see next figure).

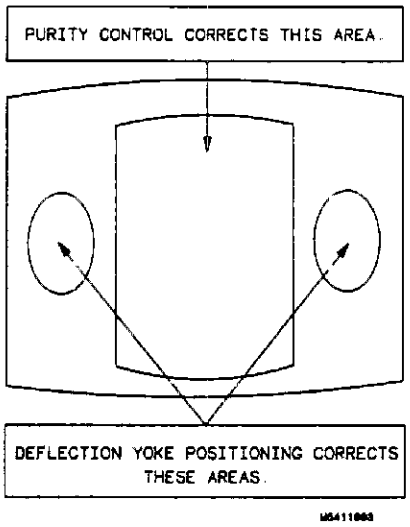


Figure 4-7. Landing and Purity Adjustment Guide.

11. If landing is not correct in step 10, readjust purity magnets for best landing of each color.

12. When landing adjustment is complete, tighten deflection yoke clamp screw just enough to keep yoke from moving. **DO NOT over tighten.**

NOTE

While moving deflection yoke forward and rearward, rotate yoke as necessary to make vertical edges of raster parallel to the sides of the instrument frame.

Static Convergence

1. Preset front panel BACKGROUND control to mechanical center.
2. Preset front panel BRIGHTNESS control maximum clockwise.
3. Temporarily disconnect power from instrument and remove PC board shield cover from rear of Color CRT Module by prying evenly on all four sides.
4. Re-apply power. Press ***more***, ***Utility***, and ***CRT Setup Menu*** keys. Press ***Pattern*** key as necessary to obtain the white cross-hatch pattern.
5. Check the four dots which are located around the center intersection of the cross-hatch pattern for coincidence of the blue, red and green dots. If the dots are not coincident, adjust H.STAT (RV703) located on the rear PC board to obtain horizontal coincidence and V.STAT (RV803) located on the bottom PC board to obtain vertical coincidence (see figure below).

NOTE

Due to interaction, BEAM LANDING will need to be re-adjusted if either H.STAT or V.STAT adjustments are made. Once BEAM LANDING is re-adjusted, repeat step 5 above if necessary to obtain center screen coincidence of the dots.

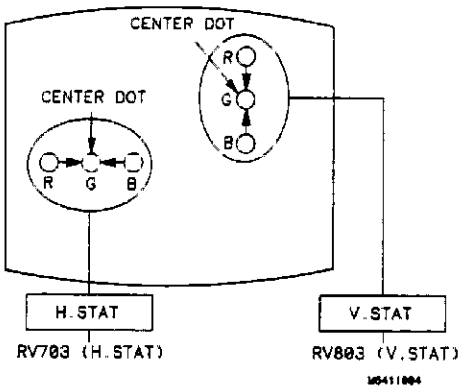


Figure 4-8. Static Convergence.

Dynamic Convergence

1. In ***Utility***, press ***CRT Setup Menu***, then press ***Pattern*** key (second key from top) as necessary to obtain the white cross-hatch pattern.

2. Adjust Y BOW (RV805) located on the bottom PC board to eliminate red, green and blue bowing at the top and bottom of the center vertical line (see next figure).

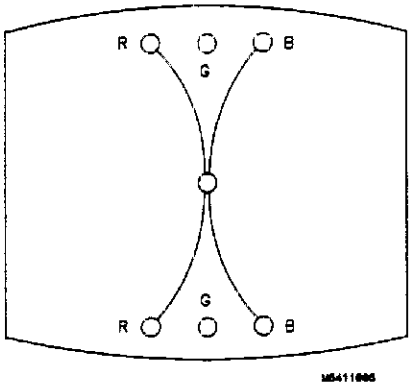


Figure 4-9. Y BOW Adjustment.

3. Adjust Y BOW CROSS (RV804) located on the bottom PC board to eliminate red green and blue orthogonal mis-alignment at the top and bottom of the center vertical line (see next figure).

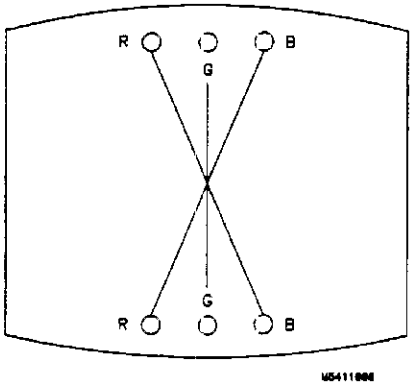


Figure 4-10. Y BOW CROSS Adjustment.

4. Adjust V.STAT TOP (RV801) and V.STAT BOTTOM (RV802) located on the bottom PC board to obtain coincidence of the red, blue and green at the intersection of the top and bottom horizontal lines with the center vertical line (see next two figures).

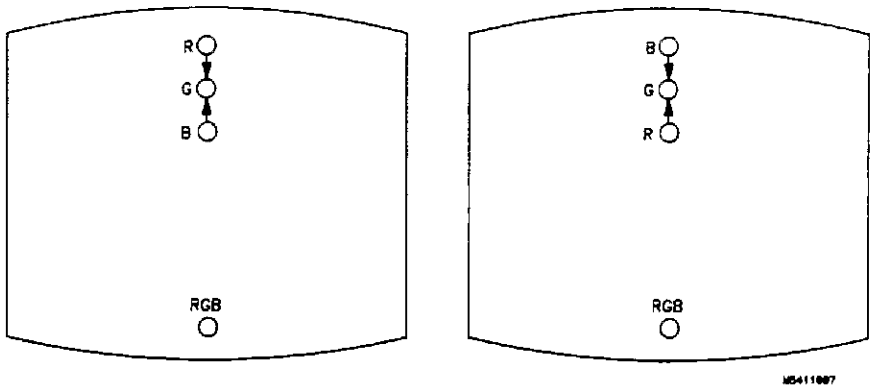


Figure 4-11. V.STAT TOP Adjustment.

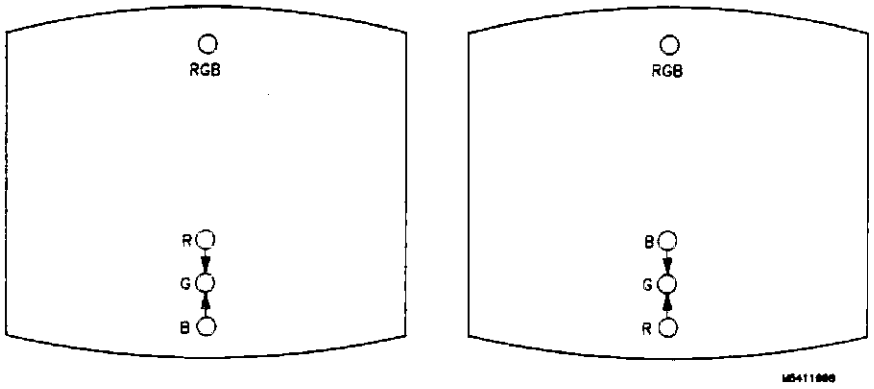


Figure 4-12. V.STAT BOTTOM Adjustment.

5. *Adjust H.AMP (RV807) located on the bottom PC board for equal amounts of mis-convergence at right and left sides of screen (see next figure).*

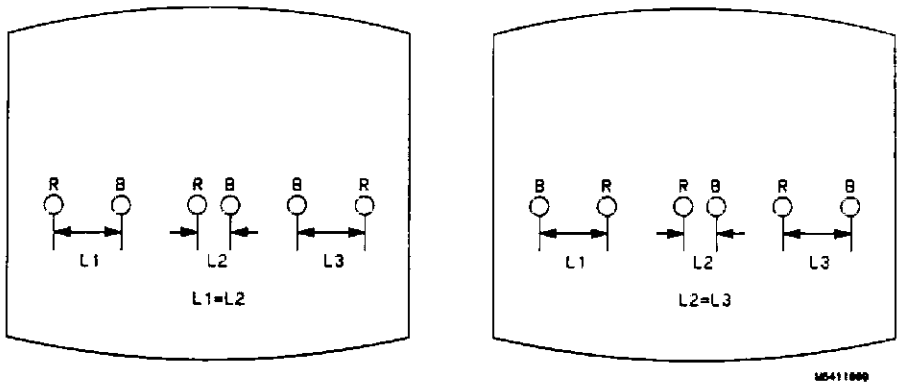


Figure 4-13. H.AMP Adjustment.

6. Adjust H.TILT (RV806) located on the bottom PC board for coincidence of red, green and blue at right and left sides of screen (see next figure).

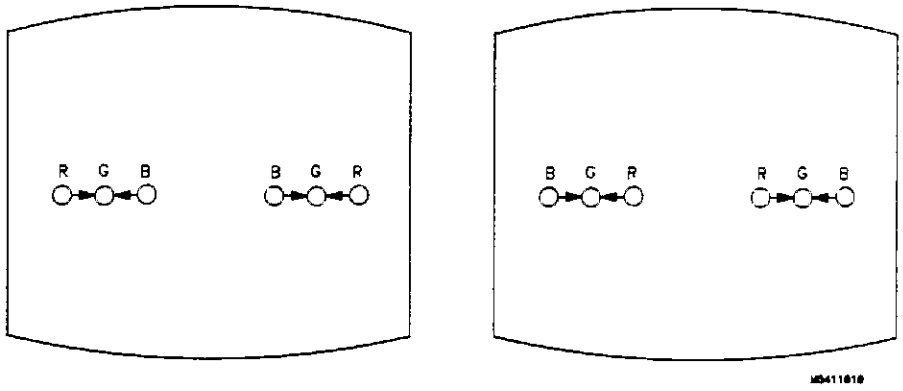


Figure 4-14. H.TILT Adjustment.

White Balance

1. In ***Utility***, press ***CRT Setup Menu***, then press ***Light Output*** key (third key from top) as necessary to obtain a blanked raster.

NOTE

The completely blanked raster will contain the text for the function keys on the right side of the display, however, this will not affect the adjustment.

2. Set front panel BACKGROUND and SUB BRT (RV901) located on the bottom PC board to mechanical center.
3. Set front panel BRIGHTNESS and SUB CONT (RV902) located on the bottom PC board to mechanical center.
4. Set G. DRIVE (RV921), B. DRIVE (RV931) and R. DRIVE (RV911) located on the bottom PC board to mechanical center.
5. Set G. BKG (RV721), B. BKG (RV731) and R. BKG (RV711) located on the rear PC board fully counterclockwise (CCW).
6. Adjust the SCREEN (RV702) located on the rear PC board until either red, green or blue raster just starts to become visible. Note which color becomes visible first and do not adjust the background control (BKG) for that color in the next step.
7. Adjust the other two background controls for best white balance.
8. Press ***Color Purity*** key as necessary to obtain the white raster.
9. Set front panel BRIGHTNESS control at maximum.
10. Observe the screen and adjust the DRIVE controls (RV921, RV931 and RV911) located on the bottom PC board for best white balance.

NOTE

White balance is checked in two ways. First, using an average piece of white photocopy paper, compare the white on the CRT to the paper Second, in the CONFIDENCE TEST function, the gray scale blocks are checked to make sure the block at the far left of the CRT is visible.

11. Repeat steps 1-3 and 6-10 until satisfied with white balance.

NOTES

SECTION 5
REPLACEABLE PARTS

5-1. INTRODUCTION

This section contains information for ordering parts. Table 5-1 lists the abbreviations used in the parts list and throughout this manual. Figure 5- 1, which covers several pages, shows the locations of mainframe parts. Table 5-2 is the list of replaceable mainframe parts. Replaceable parts lists for individual assemblies are included in the HP 54111D Service Data Supplement.

Additional information (about parts or different instrument versions) that may be a consideration when ordering, is given in a history section following the parts list. An asterisk keys affected parts in the parts list.

5-2. ABBREVIATIONS

Table 5-1 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

5-3. PARTS LIST

Table 5-2, the list of replaceable mainframe parts, is organized as follows:

a. Exchange assemblies. These assemblies can be ordered at reduced cost when the inoperative assembly is returned to Hewlett-Packard.

b. External parts. These parts are associated with the outside of the instrument and might be replaced during routine maintenance due to loss or damage

c. Internal parts. These parts are encountered when the instrument is disassembled for repair. It includes assemblies, cables, mechanical parts, hardware, and so fourth.

The following information is given for each part.

a. Hewlett-Packard part number and the check digit (for HP internal use).

b. Total quantity (Qty) in the instrument, given only once, at the first appearance of the part number in the list.

c. Description of the part.

d. A typical manufacturer of a given part in a five digit code. All mainframe parts for this instrument are made by Hewlett-Packard or ordered by description.

e. The manufacturers' number for the part

An asterisk in the parts list is a prompt to look in the history section following table 5-2 for additional information concerning that part.

5-4. EXCHANGE ASSEMBLIES

Some of the parts used in this instrument have been set up on the Blue-stripe exchange program. This allows the customer to exchange his faulty assembly with one that has been repaired, calibrated, and performance-verified by the factory. The cost is significantly less than that of a new part.

Exchangeable parts are listed in a separate section in the replaceable parts table. They have a part number in the form XXXXX-695XX (where the new part would be XXXXX-665XX).

Before ordering a Blue-stripe assembly, check with you're local parts or repair organization for the procedures associated with the Blue-stripe program.

5-5. ORDERING INFORMATION

To order a part listed in the replaceable parts list, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the replaceable parts table, include the instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

5-6. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

a. Direct ordering and shipment from the HP Parts Center.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

Mail-order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 5-1. Reference Designators and Abbreviations.

REFERENCE DESIGNATORS

A	=assembly	F	=fuse	Q	=transistor;SCR; triode thyristor	U	=integrated circuit; microcircuit
B	=fan,motor	FL	=filter	R	=resistor	V	=electron tube; glow lamp
BT	=battery	H	=hardware	RT	=thermistor	VR	=voltage regulator, breakdown diode
C	=capacitor	J	=electrical connector (stationary portion),jack	S	=switch,jumper	W	=cable
CR	=diode;diode thyristor; varactor	L	=coil;inductor	T	=transformer	X	=socket
DL	=delay line	MP	=misc. mechanical part	TB	=terminal board	Y	=crystal unit(piezo-electric or quartz)
DS	=annunciator;lamp,LED	P	=electrical connector (moveable portion),plug	TP	=test point		
E	=misc. electrical part						

ABBREVIATIONS

A	=amperes	DWL	=dowel	MFR	=manufacturer	RND	=round
A/D	=analog-to-digital	ECL	=emitter coupled logic	MICPROC	=microprocessor	ROM	=read-only memory
AC	=alternating current	ELAS	=elastomeric	MINTR	=miniature	RPG	=rotary pulse generator
ADJ	=adjust(ment)	EXT	=external	MISC	=miscellaneous	RX	=receiver
AL	=aluminum	F	=farads;metal film (resistor)	MLD	=molded	S	=Schottky-clamped; seconds(time)
AMPL	=amplifier	FC	=carbon film/ composition	MM	=millimeter	SCR	=screw;silicon controlled rectifier
ANLG	=analog	FD	=feed	MO	=metal oxide	SEC	=second(time),secondary
ANSI	=American National Standards Institute	FEM	=female	MTG	=mounting	SEG	=segment
ASSY	=assembly	FF	=flip-flop	MTLC	=metallic	SEL	=selector
ASTIG	=astigmatism	FL	=flat	MUX	=multiplexer	SGL	=single
ASYNCHRO	=asynchronous	FM	=foam,from	MW	=milliwatt	SHF	=shift
ATTEN	=attenuator	FR	=front	N	=nano(10^{-9})	SI	=silicon
AWG	=American wire gauge	FT	=gain bandwidth product	NC	=no connection	SIP	=single in-line package
BAL	=balance	FW	=full wave	NMOS	=n-channel metal-oxide-semiconductor	SKT	=skirt
BCD	=binary-code decimal	FXD	=fixed	NPN	=negative-positive-negative	SL	=slide
BD	=board	GEN	=generator	NPRN	=neoprene	SLDR	=solder
BFR	=buffer	GND	=ground(ed)	NRFR	=not recommended for field replacement	SLT	=slot(ted)
BIN	=binary	GP	=general purpose	NSR	=not separately replaceable	SOLD	=solenoid
BRDG	=bridge	GRAT	=graticule	NUM	=numeric	SPCL	=special
BSHG	=bushing	GRV	=groove	OBD	=order by description	SQ	=square
BW	=bandwidth	H	=henries;high	OCTL	=octal	SREG	=shift register
C	=ceramic,cermet (resistor)	HD	=hardware	OD	=outside diameter	SRQ	=service request
CAL	=calibrate,calibration	HDND	=hardened	OP AMP	=operational amplifier	STAT	=static
CC	=carbon composition	HG	=mercury	OSC	=oscillator	STD	=standard
CCW	=counterclockwise	HGT	=height	P	=plastic	SYNCHRO	=synchronous
CER	=ceramic	HLCL	=helical	P/O	=part of	TA	=tantalum
CFM	=cubic feet/minute	HORIZ	=horizontal	PC	=printed circuit	TBAX	=tubeaxial
CH	=choke	HP	=Hewlett-Packard	PCB	=printed circuit board	TC	=temperature coefficient
CHAM	=chamfered	HP-IB	=Hewlett-Packard Interface Bus	PD	=power dissipation	TD	=time delay
CHAN	=channel	HR	=hours)	PF	=picofards	THD	=threaded)
CHAR	=character	HV	=high voltage	PI	=plug in	THK	=thick
CM	=centimeter	HZ	=Hertz	PL	=plate(d)	THRU	=through
CMOS	=complementary metal-oxide-semiconductor	I/O	=input/output	PLA	=programmable logic array	TP	=test point
CMR	=common mode rejection	IC	=integrated circuit	PLST	=plastic	TPG	=lapping
CNDCT	=conductor	ID	=inside diameter	PNP	=positive-negative-positive	TPL	=triple
CNTR	=counter	IN	=inch	POLYE	=polyester	TRANS	=transformer
CON	=connector	INCL	=include(s)	POS	=positive,position	TRIG	=trigger(ed)
CONT	=contact	INCAND	=incandescent	POT	=potentiometer	TRMR	=trimmer
CRT	=cathode-ray tube	INP	=input	POZI	=pozidrive	TRN	=turn(s)
CW	=clockwise	INTEN	=intensity	PP	=peak-to-peak	TTL	=transistor-transistor
D	=diameter	INTL	=internal	PPM	=parts per million	TX	=transmitter
D/A	=digital-to-analog	INV	=inverter	PRCN	=precision	U	=micro(10^{-6})
DAC	=digital-to-analog converter	JFET	=junction field-effect transistor	PREAMP	=preamplifier	UL	=Underwriters Laboratory
DARL	=darlington	JKT	=jacket	PRGMBL	=programmable	UNREG	=unregulated
DAT	=data	K	=kilo(10^{3})	PRL	=parallel	VA	=voltampere
DBL	=double	L	=low	PROG	=programmable	VAC	=volt,ac
DBM	=decibel referenced to 1mW	LB	=pound	PSTN	=position	VAR	=variable
DC	=direct current	LCH	=latch	PT	=point	VCO	=voltage-controlled oscillator
DCDR	=decoder	LCL	=local	PW	=potted wirewound	VDC	=volt,dc
DEG	=degree	LED	=light-emitting diode	PWR	=power	VERT	=vertical
DEMUX	=demultiplexer	LG	=long	R-S	=reset-set	VF	=voltage,filtered
DET	=detector	LI	=lithium	RAM	=random-access memory	VS	=versus
DIA	=diameter	LK	=lock	RECT	=rectifier	W	=watts
DIP	=dual in-line package	LKWR	=lockwasher	RET	=retainer	W/	=with
DIV	=division	LS	=low power Schottky	RF	=radio frequency	W/O	=without
DMA	=direct memory access	LV	=low voltage	RGLTR	=regulator	WW	=wirewound
DPDT	=double-pole, double-throw	M	=mega(10^{6}),megohms, meter(distance)	RGTR	=register	XSTR	=transistor
DRC	=DAC refresh controller	MACH	=machine	RK	=rack	ZNR	=zener
DRVR	=driver	MAX	=maximum	RMS	=root-mean-square	°C	=degree Celsius (Centigrade)
						°F	=degree Fahrenheit
						°K	=degree Kelvin

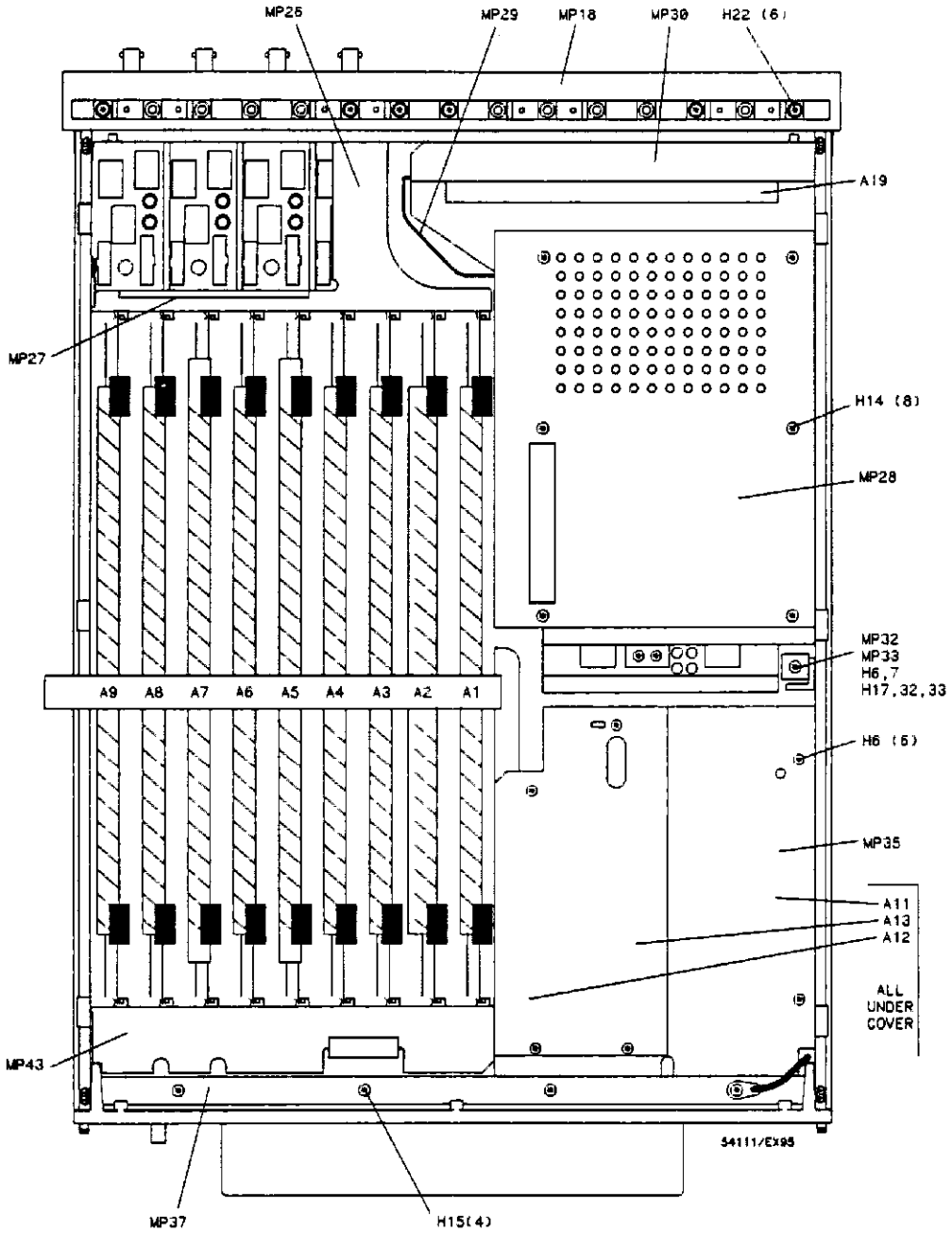


Figure 5-1. Mainframe Parts Locations (sheet 1 of 5)

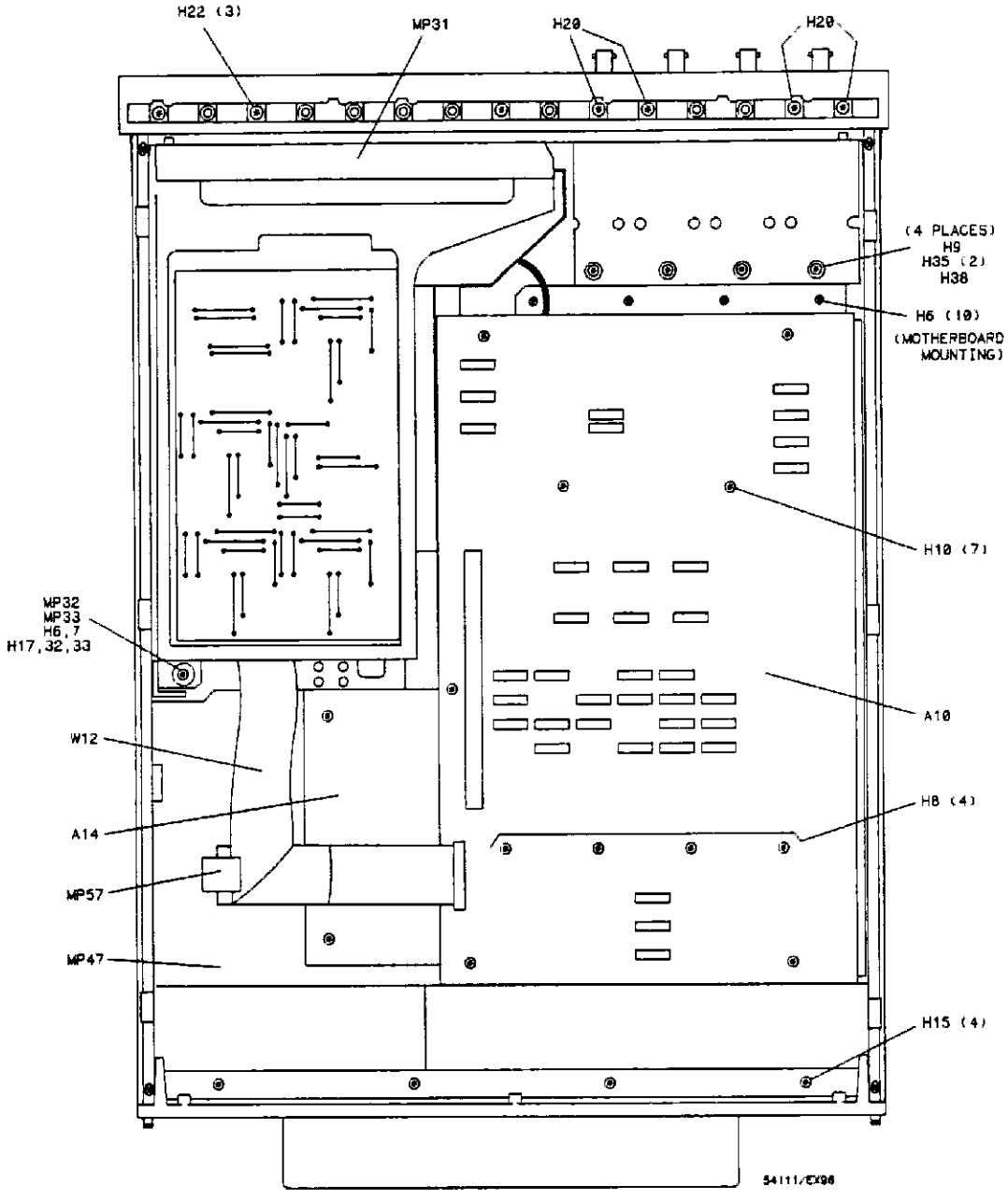


Figure 5-1 Mainframe Parts Locations (sheet 2 of 5)

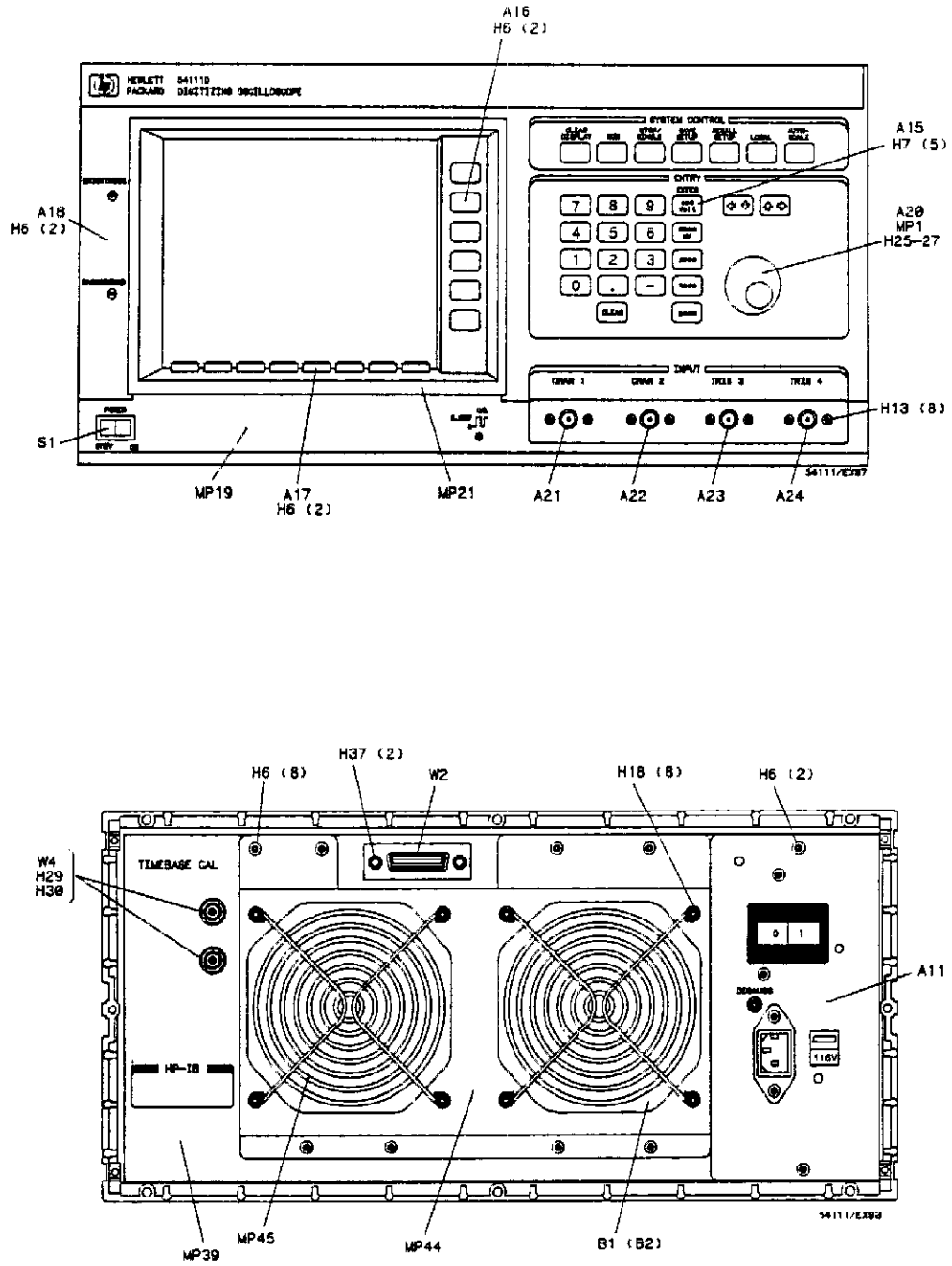
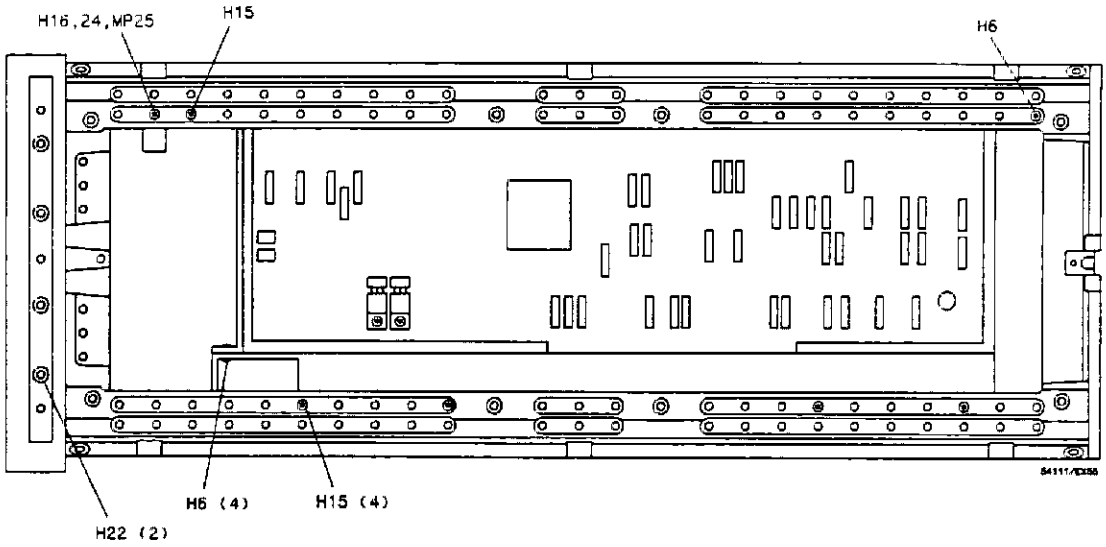


Figure 5-1. Mainframe Parts Locations (sheet 3 of 5)



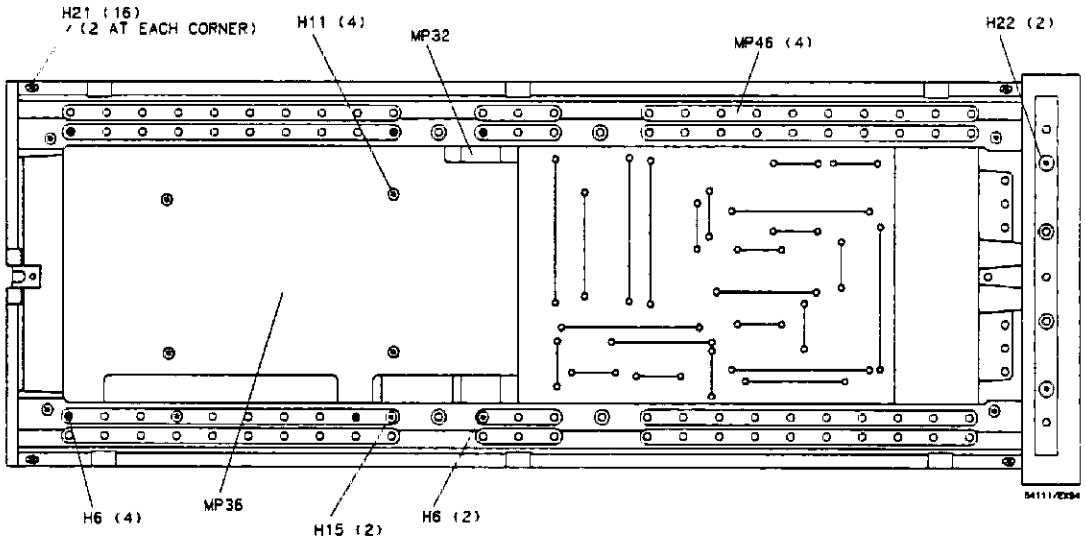


Figure 5-1. Mainframe Parts Locations (sheet 4 of 5)

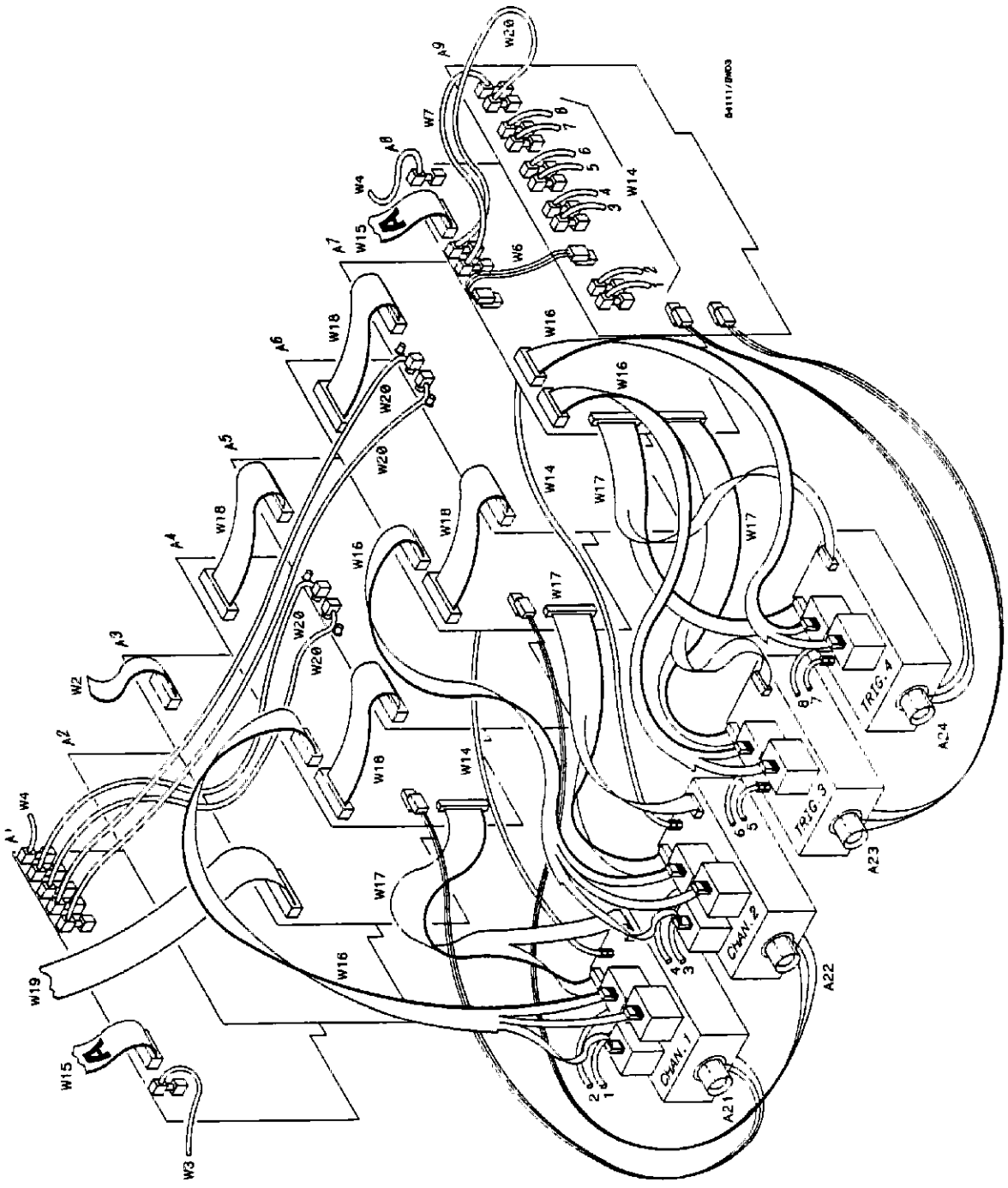


Figure 5-1. Mainframe Parts Locations (sheet 5 of 5)

Table 5-2. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES		
				2640A, 2710A, 2726A, AND 2733A		
				ARE THE SAME AS THE CURRENT LIST		
*A1, A2				See Parts History		
				CURRENT PARTS LIST FOR HP 54111D		
				MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIX 2808A		
EXCHANGE ASSEMBLIES				(See paragraph 5-4 for exchange assembly ordering information)		
*A1	54111-69513	7	1	TIMEBASE ASSEMBLY	28480	54111-69513
*A2	54111-69517	1	1	MICROPROCESSOR ASSEMBLY	28480	54111-69517
A3	54111-69506	8	1	INPUT/OUTPUT ASSEMBLY	28480	54111-69506
A4	54111-69518	9	2	ADC CONTROL ASSEMBLY	28480	54111-69518
A5	54111-69501	3	2	ANALOG-TO-DIGITAL CONVERTOR ASSEMBLY	28480	54111-69501
A6	54111-69518	9		ADC CONTROL ASSEMBLY	28480	54111-69518
A7	54111-69501	3		ANALOG-TO-DIGITAL CONVERTOR ASSEMBLY	28480	54111-69501
A8	54111-69504	6	1	TRIGGER ASSEMBLY	28480	54111-69504
A9	54111-69505	7	1	TRIGGER QUALIFIER ASSEMBLY	28480	54111-69505
A10	54110-69512	5	1	BD ASSY COLOR DISPLAY	28480	54110-69512
A11	54110-69513	6	1	BD ASSY PRIMARY POWER SUPPLY	28480	54110-69513
A12	54110-69510	3	1	BD ASSY ANALOG POWER SUPPLY	28480	54110-69510
A13	54110-69506	1	1	BD ASSY DIGITAL POWER SUPPLY	28480	54110-69506
EXTERNAL PARTS						
E1	8160-0577	4	8ft	GROUND STRIP - RFI	28480	8160-0577
H1	0515-1384	8	2	SCREW-MACH M5 10MM-LG FLAT-HEAD T25	00000	ORDER BY DESCRIPTION
H2	0515-1444	1	4	SCREW-MACH M3.5 25 4MM-LG PAN-HD TXX	00000	ORDER BY DESCRIPTION
H3	0515-1245	0	3	SCREW-MACH M3.5 12MM-LG COVER MOUNTING	28480	0515-1245
H4	0510-1253	0	3	RETAINING RING FOR COVER MOUNTING SCREW	28480	0510-1253
H5				NOT ASSIGNED		
MP1	01650-47401	7	1	KNOB - PPG	28480	01650-47401
MP2	5061-9448	3	1	COVER - BOTTOM	28480	5061-9448
MP3	5040-7201	8	2	FOOT - BOTTOM - FRONT	28480	5040-7201
MP4	5040-7222	3	2	FOOT - BOTTOM REAR - NON SKID	28480	5040-7222
MP5	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP6	8160-0590	1	2	RFI STRIP-FINGERS	28480	8160-0590
MP7	54110-04103	4	1	CVR - TOP	28480	54110-04103
MP8	54111-94301	4	1	CABLE ROUTING DIAGRAM	28480	54111-94301
MP9	5001-0441	2	2	TRIM STRIP - SIDE	28480	5001-0441
MP10	5040-7202	9	1	TRIM STRIP - TOP	28480	5040-7202
MP11	54110-40502	3	4	FOOT - REAR PANEL	28480	54110-40502
MP12	5060-9948	6	1	CVR - PERF LF SIDE	28480	5060-9948
MP13	5061-9523	5	1	CVR - PERF RT SIDE	28480	5061-9523
MP14	5060-9805	4	1	STRAP - HANDLE	28480	5060-9805
MP15	5041-6819	4	1	CAP - STRAP HANDLE (FRONT)	28480	5041-6819
MP16	5041-6820	7	1	CAP - STRAP HANDLE (REAR)	28480	5041-6820
W1	8120-1521	6	1	POWER CORD 125V USA/CANADA	28480	8120-1521
	8120-1703	6		POWER CORD OPTION 900 UNITED KINGDOM	28480	8120-1703
	8120-0696	4		POWER CORD OPTION 901 AUST/NEW ZEALAND	28480	8120-0696
	8120-1692	2		POWER CORD OPTION 902 EUROPEAN CONTINENT	28480	8120-1692
	8120-0698	6		POWER CORD OPTION 904 250V USA/CANADA	28480	8120-0698
	8120-2296	4		POWER CORD OPTION 906 SWITZERLAND	28480	8120-2296
	8120-2957	4		POWER CORD OPTION 912 DENMARK	28480	8120-2957
	8120-4600	8		POWER CORD OPTION 917 SOUTH AFRICA	28480	8120-4600
	8120-4754	3		POWER CORD OPTION 918 JAPAN	28480	8120-4754

See introduction to this section for ordering information

Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
PROBES	10431A	0	2	DIVIDER PROBE - 10:1	28480	10431A
RACK MOUNT KIT	5061-9679	2		RACK MOUNT KIT - OPTION 908	28480	5061-9679
INTERNAL PARTS						
*A1	54111-66513	1	1	TIMEBASE ASSEMBLY	28480	54111-66513
*A2	54111-66517	5	1	MICROPROCESSOR ASSEMBLY	28480	54111-66517
A3	54111-66506	2	1	INPUT/OUTPUT ASSEMBLY	28480	54111-66506
A4	54111-66518	6	2	ADC CONTROL ASSEMBLY CH1	28480	54111-66518
A5	54111-66501	7	2	ADC ASSEMBLY CH1	28480	54111-66501
A6	54111-66518	6		ADC CONTROL ASSEMBLY CH2	28480	54111-66518
A7	54111-66501	7		ADC ASSEMBLY CH2	28480	54111-66501
A8	54111-66504	0	1	TRIGGER ASSEMBLY	28480	54111-66504
A9	54111-66505	1	1	TRIGGER QUALIFIER ASSEMBLY	28480	54111-66505
A10	54110-66512	9	1	COLOR DISPLAY ASSEMBLY	28480	54110-66512
A11	54110-66513	0	1	BD ASSY PRIMARY POWER SUPPLY	28480	54110-66513
A12	54110-66510	7	1	BD ASSY ANALOG POWER SUPPLY	28480	54110-66510
A13	54110-66506	1	1	BD ASSY DIGITAL POWER SUPPLY	28480	54110-66506
A14	54110-66511	8	1	BD ASSY MOTHER	28480	54110-66511
A15	54100-66505	8	1	BD ASSY CONTROL KEYBOARD	28480	54100-66505
A16	54110-66502	7	1	BD ASSY FUNCTION KEYBOARD	28480	54110-66502
A17	54100-66520	7	1	BD ASSY MENU KEYBOARD	28480	54100-66520
A18	54110-66509	4	1	BD ASSY DISPLAY CONTROL	28480	54110-66509
A19	2090-0092	3	1	MODULE - COLOR CRT	28480	2090-0092
A20	01980-61062	5	1	ASSY - RPG	28480	01980-61062
A21	1NC1-0001	7	2	ATTENUATOR ASSEMBLY CHANNEL 1	28480	1NC1-0001
A22	1NC1-0001	7		ATTENUATOR ASSEMBLY CHANNEL 2	28480	1NC1-0001
A23	1NC1-0002	8	2	ATTENUATOR ASSEMBLY TRIGGER 3	28480	1NC1-0002
A24	1NC1-0002	8		ATTENUATOR ASSEMBLY TRIGGER 4	28480	1NC1-0002
B1	3160-0521	3	2	FAN - TUBEAXIAL	28480	3160-0521
B2	3160-0521	3		FAN - TUBEAXIAL	28480	3160-0521
H6	0515-0372	2	39	SCREW-MACH M3 8MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H7	0515-0664	5	7	SCREW-MACH M3 12MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H8	0515-0430	3	4	SCREW-MACH M3 6MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H9	0515-0665	6	8	SCREW-MACH M3 14MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H10	0515-1410	1	7	SCREW-MACH M3 20MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H11	0515-1025	6	4	SCREW-MACH M3 28MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H12				NOT ASSIGNED		
H13	0515-1035	4	8	SCREW-MACH M3 8MM-LG FLAT-HEAD T10	00000	ORDER BY DESCRIPTION
H14	0515-1271	2	8	SCREW-MACH M3 6MM-LG THREAD ROLLING	00000	ORDER BY DESCRIPTION
H15	0515-0433	6	16	SCREW-MACH M4 8MM-LG PAN-HD T15	00000	ORDER BY DESCRIPTION
H16	0515-0383	5	1	SCREW-MACH M4 16MM-LG PAN-HD T15	00000	ORDER BY DESCRIPTION
H17	0515-0641	8	2	SCREW-MACH M4 10MM-LG PAN-HD T15	00000	ORDER BY DESCRIPTION
H18	0515-0435	8	8	SCREW-MACH M4 14MM-LG PAN-HD T15	00000	ORDER BY DESCRIPTION
H18	0361-1272	6	8	FASTENER PUSH-PIN (newer instruments) H31 not used on these instruments	28480	0361-1272
H19				NOT ASSIGNED		
H20	0515-1228	9	4	SCREW-MACH M4 8MM-LG FLAT-HEAD T15	00000	ORDER BY DESCRIPTION
H21	0515-1403	2	16	SCREW-MACH M4 6MM-LG FLAT-HEAD T15	00000	ORDER BY DESCRIPTION
H22	0515-1259	9	17	SCREW-MACH M4 10MM-LG FLAT-HEAD T15	00000	ORDER BY DESCRIPTION
H23	0535-0031	2	8	NUT-HEX M3 W/LOCK WASHER	00000	ORDER BY DESCRIPTION
H24	0535-0043	6	1	NUT-HEX M4 W/LOCK WASHER	00000	ORDER BY DESCRIPTION
H25	2950-0043	6	1	NUT-HEX 3/8-32	00000	ORDER BY DESCRIPTION
H26	3050-1176	3	1	WASHER-FLAT NYLON 3/8	28480	3050-1176
H27	2190-0018	3	1	WASHER-INTERNAL LOCK 3/8	00000	ORDER BY DESCRIPTION
H28				NOT ASSIGNED		
H29	2950-0035	4	2	NUT-HEX 15/32-32	00000	ORDER BY DESCRIPTION
H30	2190-0068	5	2	WASHER-INTERNAL LOCK 1/2	00000	ORDER BY DESCRIPTION
H31	5061-6138	2	8	NUT-INSERT M4 (inst with screw mtd fans)	28480	5061-6138
H32	2190-0763	1	2	WASHER-FLAT METAL 0.141D 0.500	28480	2190-0763
H33	3050-1238	8	2	WASHER-FLAT NEOPRENE 0.149ID 0.478OD	28480	3050-1238
H34				NOT ASSIGNED		
H35	3050-0005	5	8	WASHER-SHOULDER 0.141D 0.375OD	28480	3050-0005

See introduction to this section for ordering information

Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
H36	0380-1902	9	4	STANDOFF-HEX M3	28480	0380-1902
H37	0380-1686	6	2	STANDOFF-HEX HP-IB	28480	0380-1686
H38	0360-0053	7	1	TERMINAL-SOLDER LUG	28480	0360-0053
MP17				NOT ASSIGNED		
MP18	5021-5807	8	1	FRAME - FRONT	28480	5021-5807
MP19	54111-00204	9	1	PANEL - FRONT	28480	54111-00204
MP20	54111-00203	8	1	PANEL - SUB FRT	28480	54111-00203
MP21	54110-40501	2	1	BEZEL - CRT	28480	54110-40501
MP22				NOT ASSIGNED		
MP23	0403-0092	6	1	RUBBER BUMPER (MENU KEYBOARD SUPPORT)	28480	0403-0092
MP24	1400-1362	0	2	CLAMP - CABLE - TWIST TYPE	28480	1400-1362
MP25	1400-0025	0	1	CLAMP - CABLE - TRIG CABLE SUPPORT	28480	1400-0025
MP26	54111-01203	0	1	BKT - CARD CAGE FRT	28480	54111-01203
MP27	0400-0018	0	.4ft	CHANNEL GROMMET - NYLON	28480	0400-0018
MP28	54111-00607	6	1	SHIELD - COLOR CRT MODULE	28480	54111-00607
MP29	4320-0242	6	.3ft	GROMMET - CHANNEL (earlier instruments)	28480	4320-0242
MP29	0400-0010	2	1	GROMMET - ROUND (later instruments)	28480	0400-0010
MP30	54110-01201	7	1	BRACKET - COLOR CRT MOD FRONT-TOP	28480	54110-01201
MP31	54110-01202	8	1	BRACKET - COLOR CRT MOD FRONT-BOTTOM	28480	54110-01202
MP32	54110-01210	8	1	BRACKET - COLOR CRT MOD REAR-ON FRAME	28480	54110-01210
MP33	54110-04702	9	1	BRACKET - COLOR CRT MOD REAR-ON MODULE	28480	54100-04702
MP34				NOT ASSIGNED		
MP35	54111-04104	6	1	COVER - POWER SUPPLY (TOP)	28480	54111-04104
MP36	54110-04106	7	1	COVER - POWER SUPPLY (SIDE)	28480	54110-04106
MP37	5021-5808	7	1	FRAME - REAR	28480	5021-5808
MP38	54110-94302	4	1	LABEL - GROUND CONNECTION WARNING	28480	54110-94302
MP39	54111-00202	7	1	PANEL - REAR	28480	54111-00202
MP40	5958-5582	9	1	LABLE - X-RAY	28480	5958-5582
MP41	7120-4835	0	1	LABEL - CSA CERTIFICATION	28480	7120-4835
MP42				NOT ASSIGNED		
MP43	54111-05201	6	1	DEFL ASSY - AIR	28480	54111-05201
MP44	54110-04108	9	1	HOUSING - FAN	28480	54110-04108
MP45	3160-0092	3	2	FINGER GUARD	28480	3160-0092
MP46	5021-5838	3	4	STRUT - SIDE	28480	5021-5838
MP47	54111-00101	5	1	DECK - MAIN	28480	54111-00101
MP48				NOT ASSIGNED		
MP49	5041-1480	5	2	WIRE MARKER - BROWN	28480	5041-1480
MP50	5041-1481	6	2	WIRE MARKER - WHITE	28480	5041-1481
MP51	5041-1482	7	2	WIRE MARKER - VIOLET	28480	5041-1482
MP52	5041-1483	8	2	WIRE MARKER - BLUE	28480	5041-1483
MP53	5041-1484	9	2	WIRE MARKER - GREEN	28480	5041-1484
MP54	5041-1485	0	2	WIRE MARKER - YELLOW	28480	5041-1485
MP55	5041-1486	1	2	WIRE MARKER - ORANGE	28480	5041-1486
MP56	5041-1487	2	2	WIRE MARKER - RED	28480	5041-1487
MP57	1400-0611	0	1	CLAMP - CABLE - DISPLAY RIBBON CABLE	28480	1400-0611
MP58	1400-0679	0	2	CLAMP - CABLE - MOTHER BD CABLE HOLDER	28480	1400-0679
S1	3101-2911	5	1	SWITCH - ROCKER (Standby)	28480	3101-2911
W2	54111-61612	1	1	CABLE - HPIB	28480	54111-61612
W3	54111-61601	8	1	CABLE - COAX - FRONT PANEL CAL SIGNAL	28480	54111-61601
W4	54100-61610	6	2	CABLE - COAX - LTRIG - TIMEBASE CAL	28480	54100-61610
W5	54100-61612	8	2	CABLE - 3-WIRE - 300VDC PRIMARY POWER	28480	54100-61612
W6	54100-61613	9	1	CABLE - 3-WIRE - HOLDOFF/GATE	28480	54100-61613
W7	54100-61614	0	1	CABLE - COAX - 4 INCH - QUALTRIG(D)	28480	54100-61614
W8	54110-61601	5	1	CABLE - 3-WIRE - COLOR CRT MOD POWER	28480	54110-61601
W9	54111-61611	0	1	CABLE-SHIELDED-FRONT PANEL STBY SWITCH	28480	54110-61611
W10	54111-61610	1	1	CABLE-SHIELDED-REAR CABLE STBY SWITCH	28480	54111-61610
W11	54110-61611	9	1	CABLE - DISPLAY CONTROL	28480	54110-61611
W12	54110-61607	3	1	CABLE - RIBBON - DISP ASSY TO COLOR MOD	28480	54110-61607
W13				NOT ASSIGNED		
W14	54111-61602	9	10	CABLE - COAX - VIN - TCLOCK/LTCLOCK	28480	54111-61602
W15	54111-61603	0	1	CABLE - RIBBON - ATRIG	28480	54111-61603
W16	54111-61604	1	4	CABLE - CHANNEL TRIGGER SOLENOID CABLE	28480	54111-61604
W17	54111-61605	2	4	CABLE - ATTENUATOR/TRIGGER POWER	28480	54111-61605
W18	54111-61606	3	4	CABLE - RIBBON - CONTROL I/O	28480	54111-61606
W19	54100-61601	3	1	CABLE - RIBBON - I/O TO FRONT PANEL	28480	54100-61601
W20	54111-61609	6	5	CABLE - COAX - 12 INCH - TCLK	28480	54111-61609

See introduction to this section for ordering information

5-7. INSTRUMENT AND PART HISTORY

The following provides a brief history of changes in the HP 54111D. Information can be used when ordering parts which may have changed during the manufacturing life of the instrument. It covers such issues as part compatability or part preferences. One key to this section is an asterisk by the reference designator or part number in the parts list.

A new assembly often obsoletes the older one. Because of the Blue- stripe exchange program, there is more chance that an instrument may contain a later version of a part. This also means instrument serial prefix is not a sure indication of the part complement in an instrument.

Even though a part may not have the same part number as the one in your instrument, use the part number in the parts list, along with any following history information, to be sure you are ordering the correct parts to repair your instrument.

1. Serial Prefixes 2640A, 2710A, 2726A, and 2733A

Differences connected with these serial prefixes are virtually transparent to the user and service person. Several assemblies were changed to accomodate manufacturing issues, but all later versions obsolete the earlier ones.

2. Serial Prefix 2808A

This serial prefix change updated the firmware (Microprocessor, A2) and changed the Timebase assembly (A1). The Microprocessor changed from 54111-66507 to -66517. The Timebase changed from 54111-66516 to -66513. The previous assemblies are obsolete.

The new Microprocessor (firmware dated March 10, 1988) directly replaces the old one. However, a Service Note, 54111D-6, describes a difference in the firmware that can affect bus controlled instruments and mentions added features of the new firmware. Check with your HP Customer Service representative.

The new Timebase assembly is not compatable with the old firmware. If the instrument has firmware dated April 22, 1987 (check through the Display Configuration menu), the firmware must be updated to ensure correct operation with the replacement Timebase. Service Note 54111D-4 covers this instance. Check with your HP Customer Service representative.

SECTION 6A
MAINFRAME DISASSEMBLY

6A-1. INTRODUCTION

This section contains removal and replacement procedures for mainframe assemblies. It includes a diagram showing assembly locations and a diagram showing how the instrument is cabled.

6A-2. SAFETY CONSIDERATIONS

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

WARNING

This instrument is equipped with a standby switch on the front panel that DOES NOT de-energize the power supply. To avoid shock hazards capable of causing injury or death, the main power switch on the rear panel must be used to de-energize the instrument or the power cable must be disconnected when the instrument must be de-energized.

WARNING

These procedures are used while repairing an instrument that has protective covers removed and may have had power applied. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Read the Safety Summary in the front of this manual.

CAUTION

Do not remove or replace any of the circuit board assemblies in the instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

CAUTION

The HP 54111D is highly sensitive to Electrostatic Discharge (ESD). Proper ESD precautions should be taken whenever the covers of the instrument are removed and particularly when assemblies are being removed and replaced. Disconnecting and connecting cables can cause ESD into sensitive circuitry.

Use of an anti-static mat and a wrist strap that grounds the service person to the instrument or the mat is recommended. Keep all assemblies in anti-static bags when not installed in an instrument.

6A-3. TOOLS REQUIRED

The hardware requires TORX® type tools for removal and replacement. Sizes required for the procedures in this section are #10 and #15.

If the display must be replaced, an 8 mm wrench or driver is also required.

If an attenuator must be replaced, a 6 mm open end wrench is needed. This wrench is provided in the HP 54100 Family Support Kit.

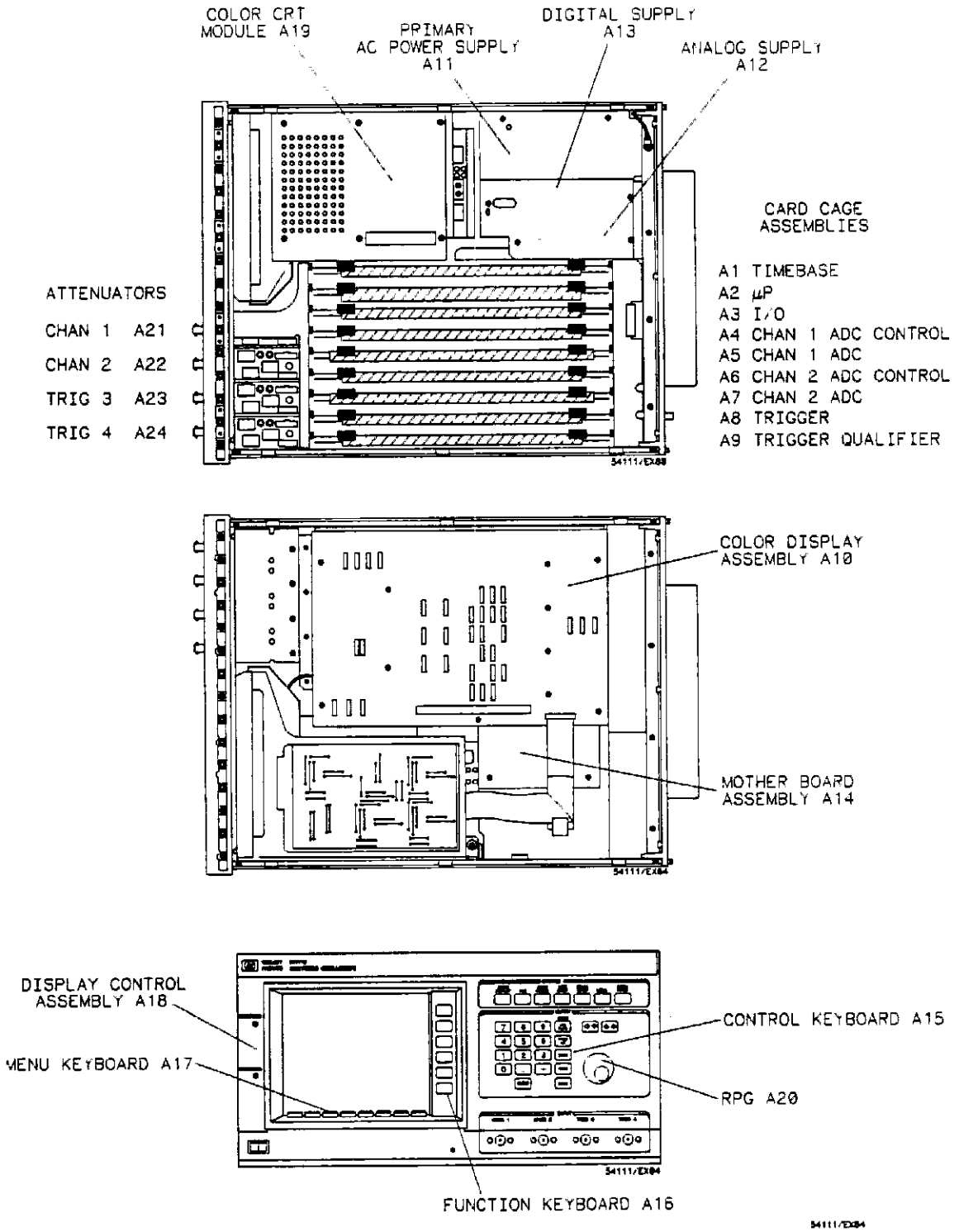


Figure 6A-1. Major Assembly Locations.

6A-4. MAJOR ASSEMBLY REMOVAL PROCEDURES

The following procedures should be followed when disassembling the instrument. Particular care should be taken with the cabling connecting card cage assemblies and attenuators.

6A-5. Card Cage PC Assemblies

REMOVAL

1. Disconnect power cable.
2. Remove the top rear feet, then the top cover.
3. Disconnect any cables from assembly to be removed. Some assemblies have cables along the front edge. These must be removed before the assembly is pulled up.
4. Refer to the illustration on top the power supply. Release PC assembly by pulling the flexible plastic extractors away from the assembly shield, then up.
5. Remove the assembly from the connector by pulling up on the extractors. As the assembly is removed from the instrument, check for cables connected to the center of the assembly and remove them.

REPLACEMENT

1. Insert PC assembly shield edges in proper guides.
2. Keep the extractors up while sliding the assembly in.
3. If the assembly has cabling to its center area, it must be connected as the board is being inserted.
4. If the assembly has cabling to its front edge, it will be easier to connect the cables as soon as the connector is below the top edge of the card cage frame. Refer to the cabling diagram on the instrument top cover or the diagram at the end of this section.
5. While keeping assembly properly aligned in guides, push it in. As the top edge of the assembly becomes level with the top of the card cage the connector will start to engage. Keep assembly level and apply even pressure until connector is seated.

CAUTION

Do not use the extractors to lever the assembly into the connector. *Using the extractors makes it too easy to apply excessive force that might bend misaligned connector pins. If the connector will not seat, remove the assembly and check for bent pins.*

Avoid pinching cabling between the assembly and the mainframe. The coaxial cables that connect to the center of the ADC assemblies are particularly vulnerable to pinching between the assembly and the main deck.

6. Reconnect all remaining cabling. Refer to the diagram on the instrument cover or the diagram at the end of this section.

6A-6. Primary Power Supply

REMOVAL

1. Disconnect power cable.
2. Remove the rear feet from the top right corner and left side.
3. Remove the top and left side covers.

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

4. Through the hole in the top power supply shield, observe the red LED located on the Primary Power Supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding.
5. Remove top power supply shield (six screws).
6. Remove the screw that attaches the ground wire (green/yellow) to top corner of rear frame.
7. Remove the three cables at the top front of the Primary Power Supply PC board.
8. Remove four screws from power supply side cover (figure 6A-2).
9. Remove two screws which attach power supply assembly to rear panel (figure 6A-2).
10. Turn instrument onto its left side. Pull the power supply assembly rearward until the STBY switch cable at the rear of power supply board can be disconnected. Disconnect the cable.
11. Pull supply rearward until it clears the instrument.

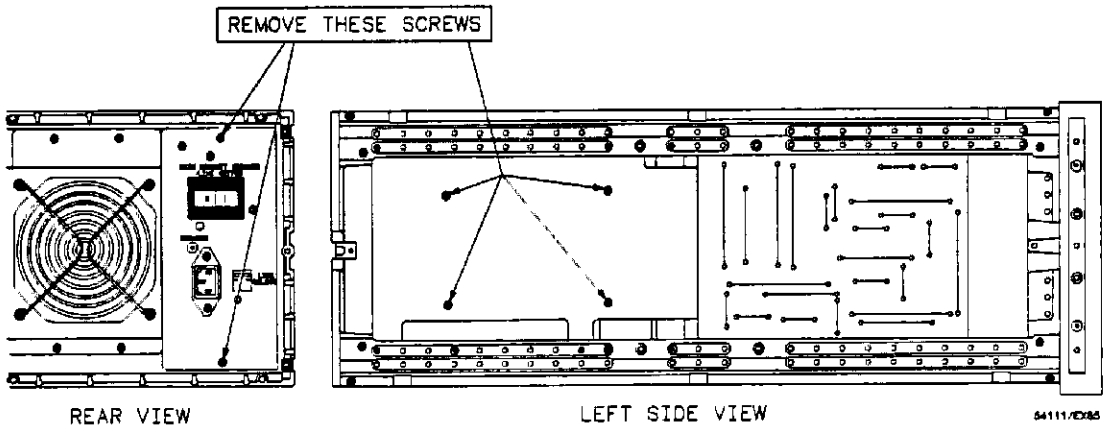


Figure 6A-2. Primary Power Supply Mounting Screws.

PRIMARY POWER SUPPLY REPLACEMENT

Reverse removal procedure to install supply.

WARNING

Power supply safety grounding will be defeated if ground wire removed in step 6 above is not reconnected. To avoid a defeated ground, make sure this green/yellow wire is re-attached to top rear corner of the rear frame.

6A-7. Analog Power Supply

REMOVAL

1. Disconnect power cable.
2. Remove the top rear feet and top cover.

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

3. Through the hole in the top power supply shield, observe the red LED located on the Primary Power Supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding.
4. With the instrument on its left side, remove four screws along the bottom of the fan housing.
5. Set instrument back on its feet and remove the four screws along the top of the fan housing. Lay the fan housing flat, along the back of the instrument. It is not necessary to disconnect the fan power cable.
6. Remove top power supply shield (six screws).
7. Disconnect the Analog Power Supply input cable from the top front corner of the Primary Power Supply.
8. Use a flat-blade screwdriver to loosen the captive screw at the bottom front of the supply.
9. Release power supply board connector by pulling board straight up and off the guide posts.
10. Slide the Analog Power Supply back through the opening in the rear panel.

REPLACEMENT

Reverse the removal procedure to install assembly.

6A-8. Digital Power Supply

REMOVAL

1. Disconnect power cable.
2. Remove top rear feet and top cover.

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

3. Through the hole in the top power supply shield, observe the red LED located on the Primary Power Supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding.
4. Remove top power supply shield (six screws).
5. Set the instrument on its left side. Loosen, approximately four turns, the bottom four fan housing mounting screws. Set the instrument on its feet and remove the top four fan housing mounting screws. This allows the fan housing to tilt back at the top, providing the necessary clearance for removing the Digital Power Supply.
6. Disconnect the Digital Power Supply input cable from the top front corner of the Primary Power Supply.
7. Use a flat-blade screwdriver to loosen the captive screw at the front bottom of the supply.
8. Release power supply board connector by pulling board straight up and off guide posts.
9. Remove the supply from the instrument by lifting front edge of board first then rotating board up and out.

REPLACEMENT

Reverse removal procedure to install board.

6A-9. CRT Bezel, Function and Menu Keyboards

The keyboards at the side and bottom of the CRT can be removed by first removing the CRT Bezel

REMOVAL

1. While pushing down on top edge of bezel (see figure 6A-3), pull top edge away from front panel until holding tabs are clear of the front panel.
2. Lift bezel slightly and pull bottom of bezel away from front panel.
3. Pull bezel away from front panel just far enough to gain access to the ribbon cable connectors on Control Keyboard. They are located just to the right of the bezel opening in the front panel.
4. Disconnect the two ribbon cable connectors from the Control Keybard.

REPLACEMENT

Reverse the removal procedure to install bezel.

NOTE

The ribbon cables must be reconnected as follows: Function Keyboard cable (right side of bezel) to top connector on Control Keyboard and Menu Keyboard cable (bottom of bezel) to bottom connector on Control Keyboard.

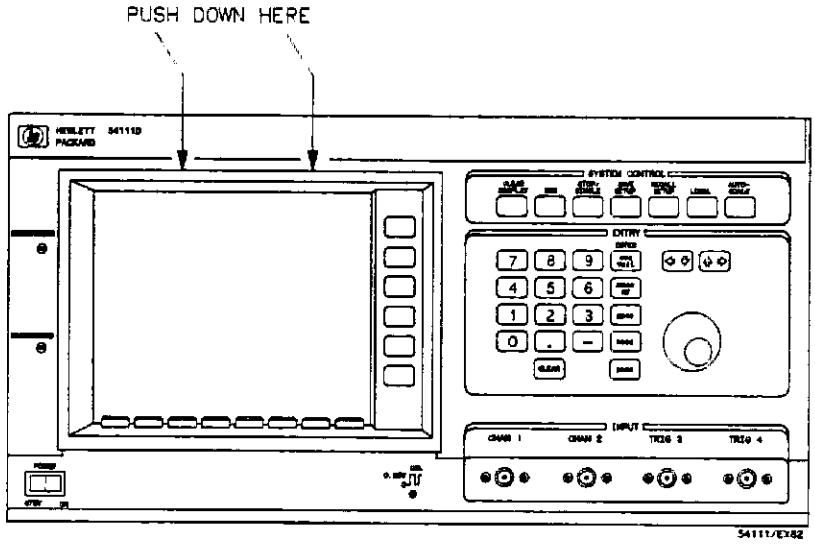


Figure 6A-3. CRT Bezel Removal Pressure Locations.

6A-10. Front Panel, Control Keyboard, and Display Control

Use steps 1 through 11 to remove Front Panel, steps 1 through 12 to remove Display Control, or steps 1 through 11 and steps 13 and 14 to remove Control Keyboard.

NOTE

It is not necessary to remove the front panel to remove the keyboards around the CRT bezel. See the previous removal procedure.

FRONT PANEL REMOVAL

1. Disconnect power cable.
2. Remove the rear feet and the top, bottom, and side covers.
3. Remove top, and side trim strips from the front frame by carefully prying up at the ends of the strips with a flat blade screwdriver.
4. Remove the two front panel screws that were under each side trim strip.
5. Remove the two screws on either side of each of the input BNC connectors.
6. Remove six front panel screws as shown in the following figure.

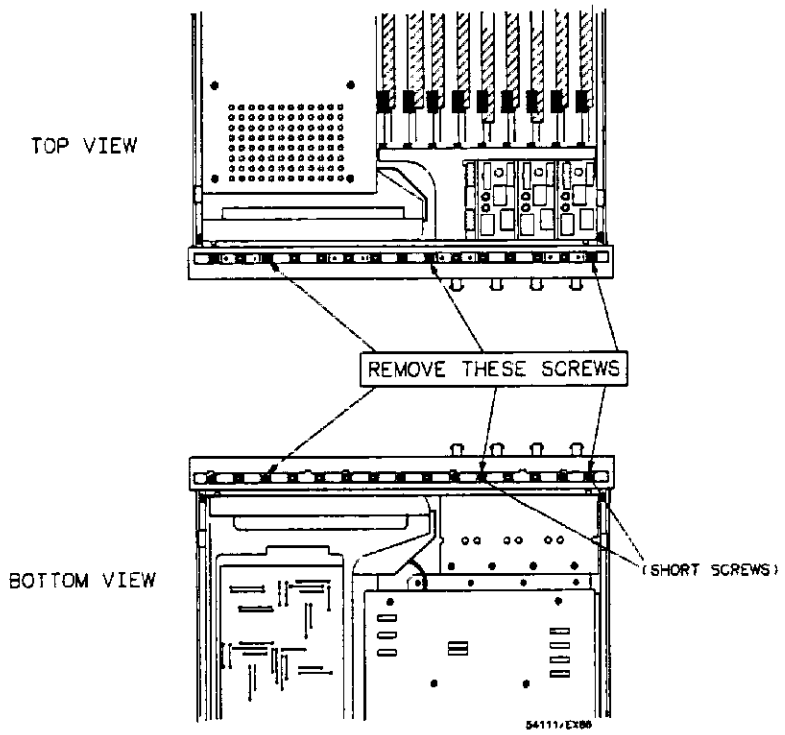


Figure 6A-4. Top and Bottom Front Panel Mounting Screws.

7. Set instrument in its normal operating position.

8 Note the routing of the calibrator signal coax at the front connector on the Timebase assembly (next to the Color CRT Module). Disconnect it at the Timebase and slide it out through the slot in the card cage bulkhead.

9. Disconnect the STBY switch by separating the two-wire interconnect just to the right of the CRT.

10. Pull front panel just far enough to gain access to the cable connector on the CRT Control board (left side of front panel) and disconnect the cable.

11. Open the two cable ties: top left, inside front panel and top right of CRT, and remove the cables.

12. Disconnect the large ribbon cable from the Control Keyboard and remove the front panel from the instrument.

NOTE

At the front of the attenuators is a plastic bushing containing the Probe ID sensing ring. Note the orientation of this bushing and ring. The tabs of the bushing should be horizontal and fit into the recess on the front of the attenuator. Be sure the bushings for all attenuators are properly aligned before replacing the front panel.

DISPLAY CONTROL REMOVAL

13. Remove two screws attaching the Display Control assembly.

CONTROL KEYBOARD REMOVAL

14. Disconnect the RPG cable at the Control Keyboard and the two cables from the CRT bezel keyboards.

    The Menu Keyboard (right side of bezel) cable goes to the top connector and the Function Keyboard (bottom of bezel) cable goes to the bottom connector on the Control Keyboard.

15. Remove five screws and remove board.

    Pass RPG cable through hole in Control Keyboard.

ASSEMBLY REPLACEMENT

Reverse the procedure to replace any of these assemblies.

6A-11. Attenuators

REMOVAL

1. Remove Front Panel (refer to previous paragraph). Set instrument in its normal operating position.

2. Remove the screw at the rear of the attenuator to be removed. This screw is not captive. Don't let it fall into the interior of the instrument because it will be hard to retrieve.

3. Remove the connector for the three-wire cable that connects to the front of the attenuator. The connection is made at the front edge of one of the card cage boards.

3. Remove the connectors from the attenuator solenoids. Channel attenuators have three connectors on the end of each cable and trigger attenuators have two.

4. Remove the cable connectors at the back of the attenuators. Note the orientation of these connectors.

5. Remove the coaxial cables. It is necessary to remove the rear cable first. The HP 54100 Family Support Kit provides a 6 mm open-end wrench for removing these cables. The attenuator should now be free of the instrument.

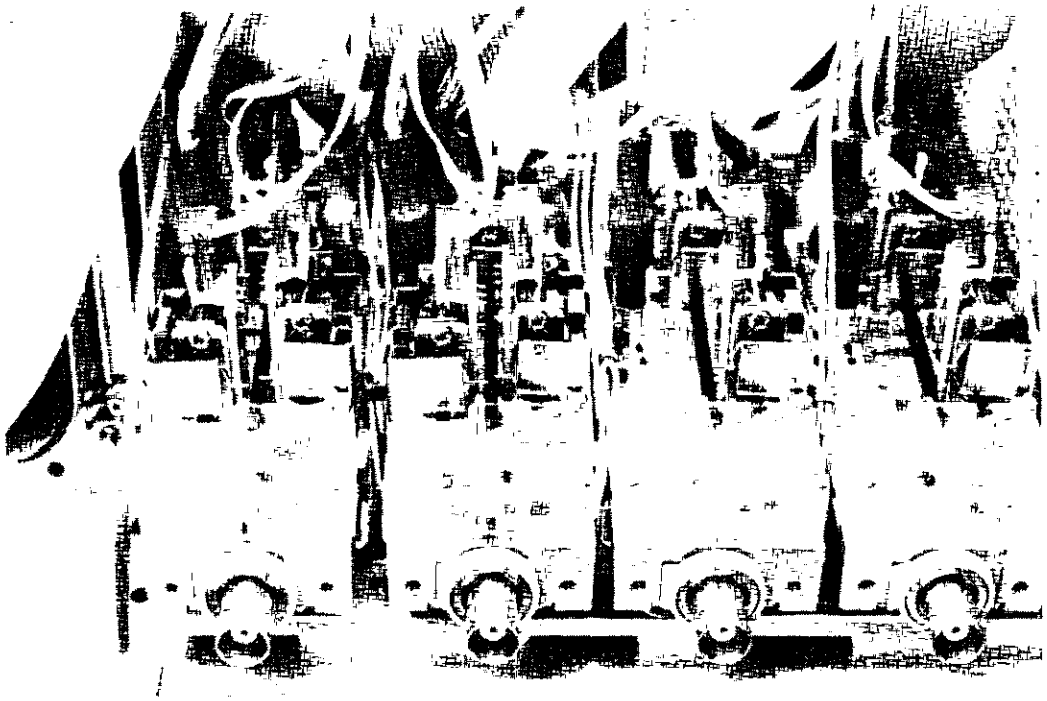


Figure 6A-5. Channel and Trigger Attenuators.

REPLACEMENT

The replacement procedure is essentially the reverse of removal.

1. Connect the coaxial cables to the attenuator.

NOTE

The two cables on the side are the trigger connections. The cable at the rear is the vertical signal connection. Only the Channel attenuators have this signal connector. The trigger cables have a colored marker at each end. Connect the cables to the attenuator using the following chart.

ATTENUATOR	FRONT CONNECTOR	REAR CONNECTOR
CHAN 1	Brown	Red
CHAN 2	Orange	Yellow
TRIG 3	Green	Blue
TRIG 4	Violet	White

In the event that the cables were inadvertently removed at the Trigger Qualifier, they should be re-installed in order of color, front to back, following the standard color code. You can also use the diagram on the cover of the instrument or at the back of this section.

2. Connect the rear ribbon cables to the attenuator. The connectors are keyed.

3. Carefully connect the cables to the solenoids. The connectors are keyed but the keying can be defeated by excessive force. Use the cabling diagram on the inside of the instrument top cover or the figure at the end of this section.

4. Connect the three-wire cable to the front of the appropriate card cage assembly. Use the cabling diagram for reference. Route the cable along the right side of the attenuator.

5. Insert the rear mounting screw into the hole at the rear of the attenuator. Slide the attenuator into place and rest the mounting screw on the standoff. Hold the attenuator in line with the others while inserting the screw.

   NOTE *Leave the rear screw slightly loose so the attenuator will align with the front panel when front screws are tightened. Rear screw is tightened last.*

6. Recheck the routing of all cables, especially the three-wire cable. It can become pinched when the front panel is installed.

7. Check the alignment of the BNC sensing ring on all attenuators. It should fit into the recess in the front of the attenuator.

8. Install the front panel and reassemble the rest of the instrument. Use the appropriate procedures in this section.

6A-12. Color CRT Module

The Color CRT Module is replaceable only as a complete unit.

COLOR CRT MODULE REMOVAL

1. Remove Front Panel (refer to the appropriate paragraph in this section).
2. Disconnect the flat wide ribbon cable from the Color Display Assembly and remove cable from clip.
3. Remove four screws that attach the Color Display Module to the front frame (see figure below).
4. Remove two screws attaching side of module to left side corner struts (see figure below).
5. Slowly pull module forward until the power cable (small three-wire) can be disconnected at the Primary Power Supply board.
6. Continue pulling module forward until it clears the instrument.

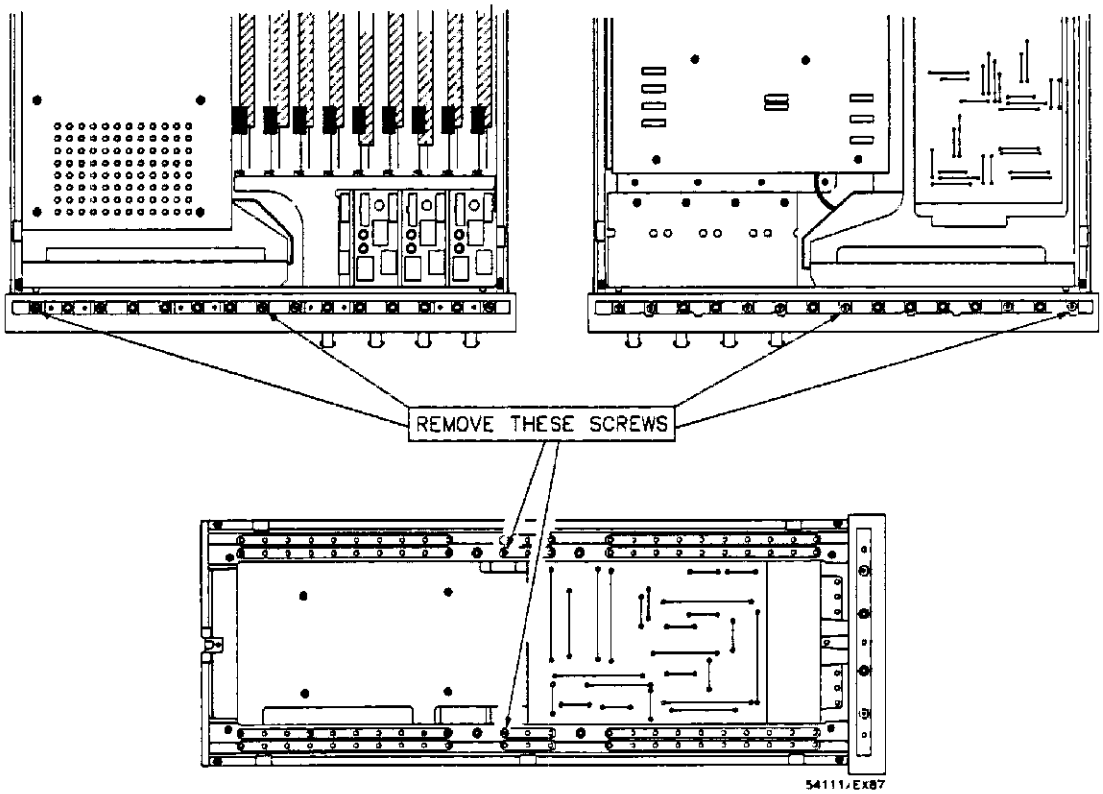


Figure 6A-6. Color CRT Module Mounting Screws.

REPLACEMENT

It is necessary to remove several items from the inoperative Color CRT Module and install them on the new one. Use the following procedure to do that and install the new module.

TRANSFER PARTS TO NEW MODULE

1. Remove the eight small screws that hold the shield to the top and side of the inoperative module.

   THESE SCREWS ARE SPECIAL self-tapping screws, different from the screws in the rest of the instrument. They must be used for mounting the shield on the new module. Do not use them for any other purpose.

2. Use an 8 mm wrench to remove the four nuts on the front of the inoperative module and remove the shield.

3. Remove the front mounting brackets and put the 8 mm nuts back on the module.

4. Remove the 8 mm nuts from the new module, do not remove any other hardware, and install the front mounting brackets.

5. Install the shield on the new module. Place it over the two front mounting screws and front mounting brackets.

6. Install the four 8 mm nuts but leave them loose so the shield can move.

7. Use the special self-tapping screws (step 1) to fasten the top and side of the shield. They will be hard to start while they are tapping the holes. Be careful that excessive tightening does not strip the self- tapped holes.

8. Tighten the 8 mm nuts at the front of the module.

9. The rear bracket is two brackets connected together by shock mounting hardware. Remove the two screws that hold the bracket assembly to the rear of the inoperative module.

   THESE SCREWS ARE SPECIAL self-tapping screws that must be used for mounting the bracket assembly on the new display. Do not use them for any other purpose.

10. Mount the rear bracket assembly on the new module. The screws will be hard to start because they must self-tap the mounting holes. Be careful that excessive tightening does not strip the self-tapped holes.

11. Note the routing of the power cable and CRT Control cable and <u>one at a time</u>, remove them and install them on the new module.

12. Remove the wide flat ribbon cable from the old module and install it on the new one.

INSTALL NEW MODULE

13. Install the new module most of the way into the instrument. Avoid pinching cables as module is being installed.

14. Connect the power cable to the appropriate connector at the top front corner of the Primary Power Supply and slide module the rest of the way in.

15. Install, but do not tighten, the two rear and four front mounting screws (see figure 6A-6).

16. Install the front panel. Use the steps given in the front panel procedure except for steps 3, 2, and 1.

17. Push the module foreward, closing as much as possible the gap between the CRT and the bezel. Tighten the two rear and four front mounting screws.

18. Complete the rest of the instrument assembly by doing steps 3, 2, and 1 of the front panel procedure.

6A-13. Fans

REMOVAL

1. Disconnect power cable.

2. Remove bottom rear feet and bottom cover.

3. Disconnect fan power cable from rear corner of Mother board.

4. Remove fan housing mounting screws as shown in the figure.

5. While noting fan cable routing, carefully remove fan housing from instrument.

6. Disconnect power cable connector from defective fan and remove fan from housing.

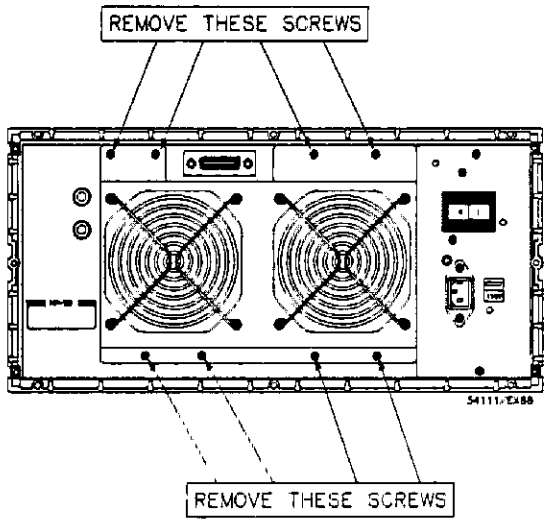


Figure 6A-7. Fan Housing Mounting Screws.

REPLACEMENT

Reverse removal procedure to install fan. Be sure fan power cable does not get pinched between fan and rear panel.

6A-14. Color Display Assembly

REMOVAL

1. Disconnect power cable.
2. Remove bottom rear feet and bottom cover.
3. Disconnect wide ribbon cable from Color Display assembly.
4. Remove assembly mounting screws as shown in the figure below.
5. Carefully lift board straight up to disengage Mother board connector.

NOTE

The Display assembly to Mother Board connector will exhibit some removal resistance while the board is being removed. It is recommended the major lifting force be exerted on the edge of the Color Display Assembly at the connector.

REPLACEMENT

Reverse removal procedure to install assembly. Use additional care when inserting the connector pins into connector on Mother board.

NOTE

Power for the Color Display Assembly is obtained from the Mother board via the four short mounting screws. Their positions are marked +5 and GD on the board. These mounting screws must be installed and tightened before proper operation of the instrument can be expected.

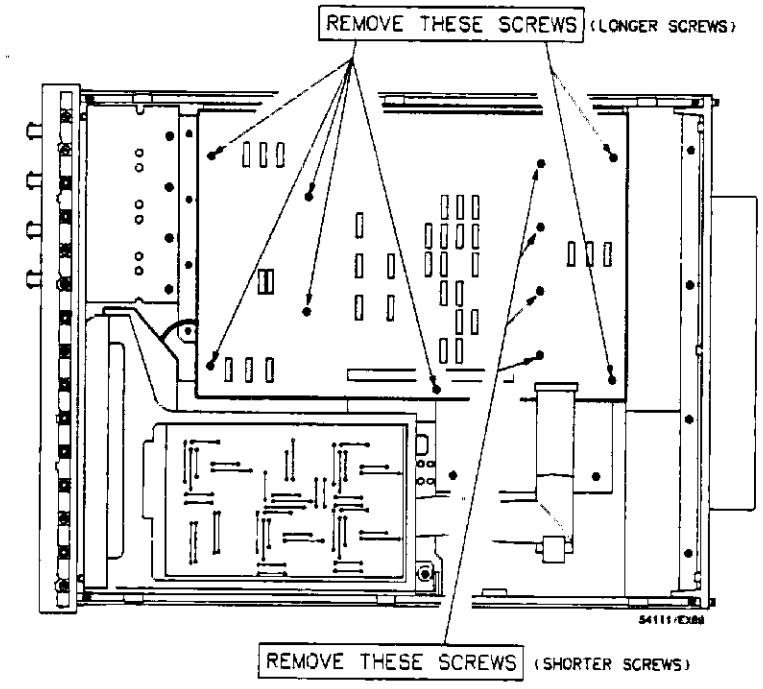


Figure 6A-8. Color Display Assembly Mounting Screws.

6A-15. Mother Board

REMOVAL

1. Disconnect power cable.
2. Remove rear feet and all covers.
3. Remove all card cage PC boards (refer to earlier paragraph).
4. Remove Analog Power Supply and Digital Power Supply (refer to earlier paragraphs).
5. Remove Color Display Assembly (refer to earlier paragraph).
6. Disconnect fan power cable connector from corner of Mother board.
7. Loosen the STBY switch cable by removing the two nylon cable clamps from bottom of Mother board. Squeeze the clamps and pull them from the holes in the board.
8. Remove the remaining mounting screws and remove board (see figure below).

REPLACEMENT

Reverse removal procedure to install board.

NOTE

The Mother board and Display board share some of the same mounting screws. Therefore, when installing the Mother board install only the screws removed in step 8 above (shown in figure below).

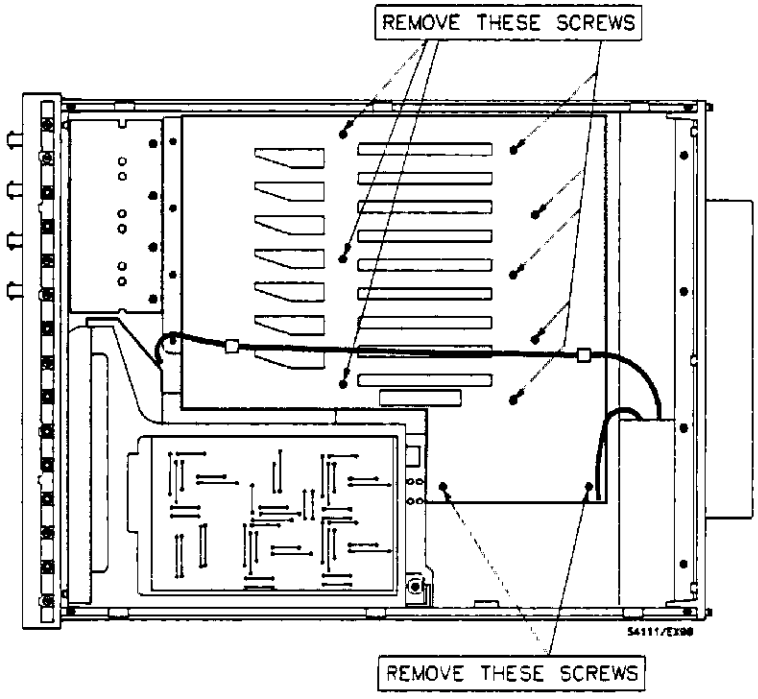


Figure 6A-9. Mother Board Mounting Screws.

6A-16. CABLING DIAGRAM

The following cabling diagram should be used when removing and replacing boards and assemblies.

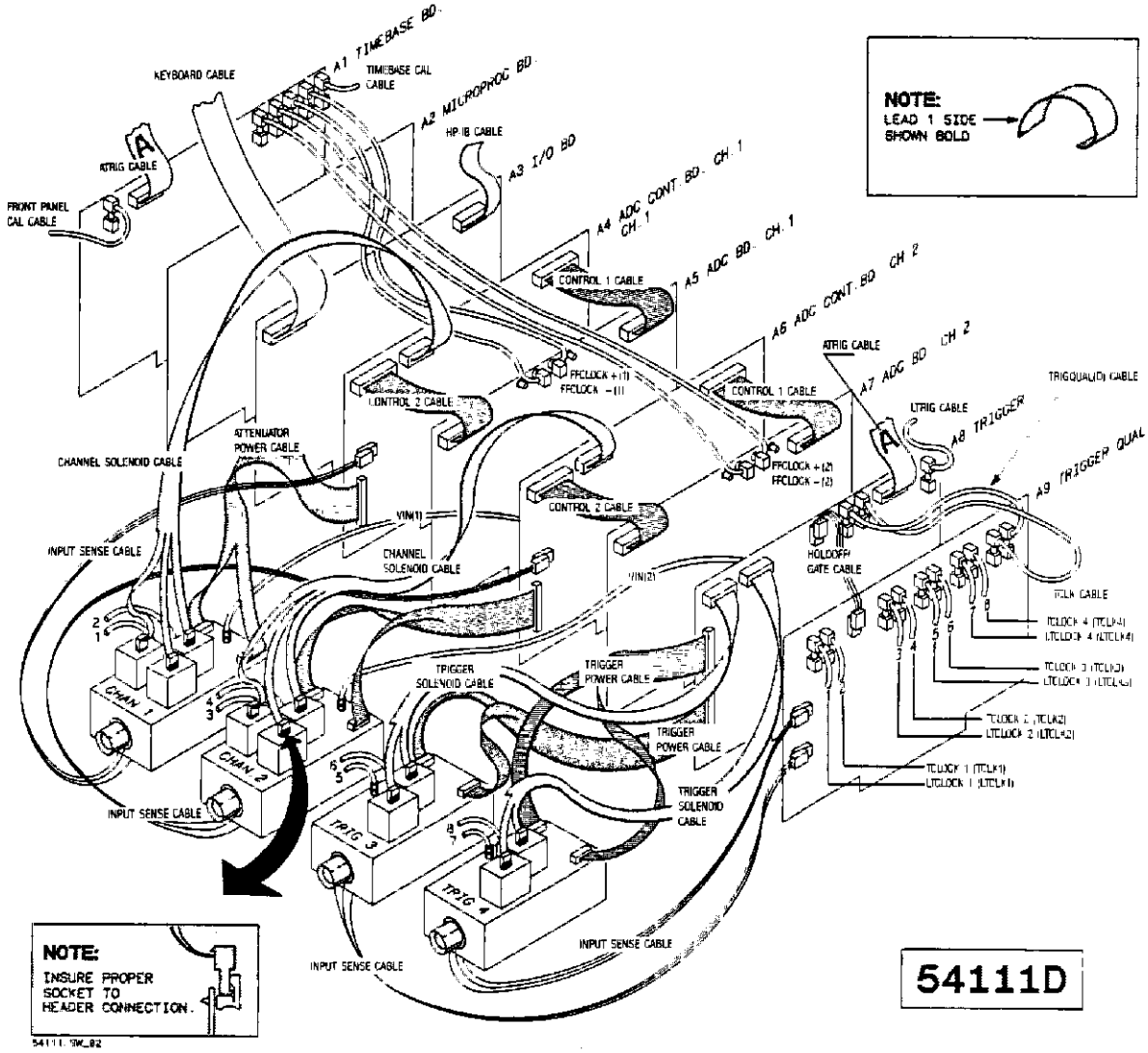


Figure 6A-10. HP 54111D Cabling Diagram.

NOTES

SECTION 6B
THEORY OF OPERATION

6B-1. INSTRUMENT LEVEL THEORY

The HP 54111D is a digitizing oscilloscope with up to 1 GS/s sampling rate and 500 MHz repetitive bandwidth. It has two input channels, which are digitized and provide internal trigger. There are two additional external trigger channels.

The mainframe consists of power supplies, color monitor assembly, and display assembly. The card cage holds the acquisition system (except attenuators) as well as the Microprocessor assembly and Input/Output assembly.

The acquisition system consists of four attenuator assemblies (including two trigger attenuators), two Analog to Digital Converter (ADC) assemblies, two ADC Control assemblies, and the Trigger, Timebase, and Trigger Qualifier assemblies. The attenuators are located between the card cage and the front panel.

Refer to the Instrument Level Block Diagrams for the following discussion.

6B-2. TYPICAL DATA ACQUISITION CYCLE

The acquisition cycle begins on the Timebase assembly. Before the acquisition cycle begins, the RUN/HALT flip-flop is set to HALT. This forces the LRUN/HALT line high. The pre- and post-trigger delay times are then loaded into the timebase IC.

To begin the cycle, LRUN/HALT is brought low, and the timebase IC then asserts ARUN (Asynchrounous RUN). Data taking begins.

After two cycles of the pre-trigger delay clock, generated by the timebase IC, the pre-trigger delay counter begins counting down from its preloaded value. When it reaches zero, TRIG ARM is asserted by the Timebase.

The Timebase then waits for ATRIG to be asserted by the Trigger assembly, indicating that a trigger event has occurred. After ATRIG, the fine interpolator is started. The fine interpolator in the timebase IC counts until the fine interpolator gate ceases being asserted. This time interval is proportional to the amount of time between the trigger event and the next subsequent sample clock. The dual slope interpolator circuit has acted as a time-interval stretcher.

Two post-trigger delay clock counts after the fine interpolator control has been de-asserted by the timebase IC, the post-trigger delay counter begins counting down to zero. When it gets to zero data taking stops.

When the fine interpolator gate ceases being asserted by the dual slope interpolator, the processor reads the coarse and fine interpolation counters. Then it reads the contents of the interleaved A/D memory by rapidly advancing the memory to the beginning of the data, then single-stepping through it.

Acquired data is read sequentially from the four A/D memories (FISO) in a "round-robin" fashion, into RAM on the I/O assembly. After the FISOs are read, the Timebase IC asserts LIRQ1 and the microprocessor resets the Timebase IC by setting the LRUN/HALT flip-flop to HALT.

The cycle then repeats.

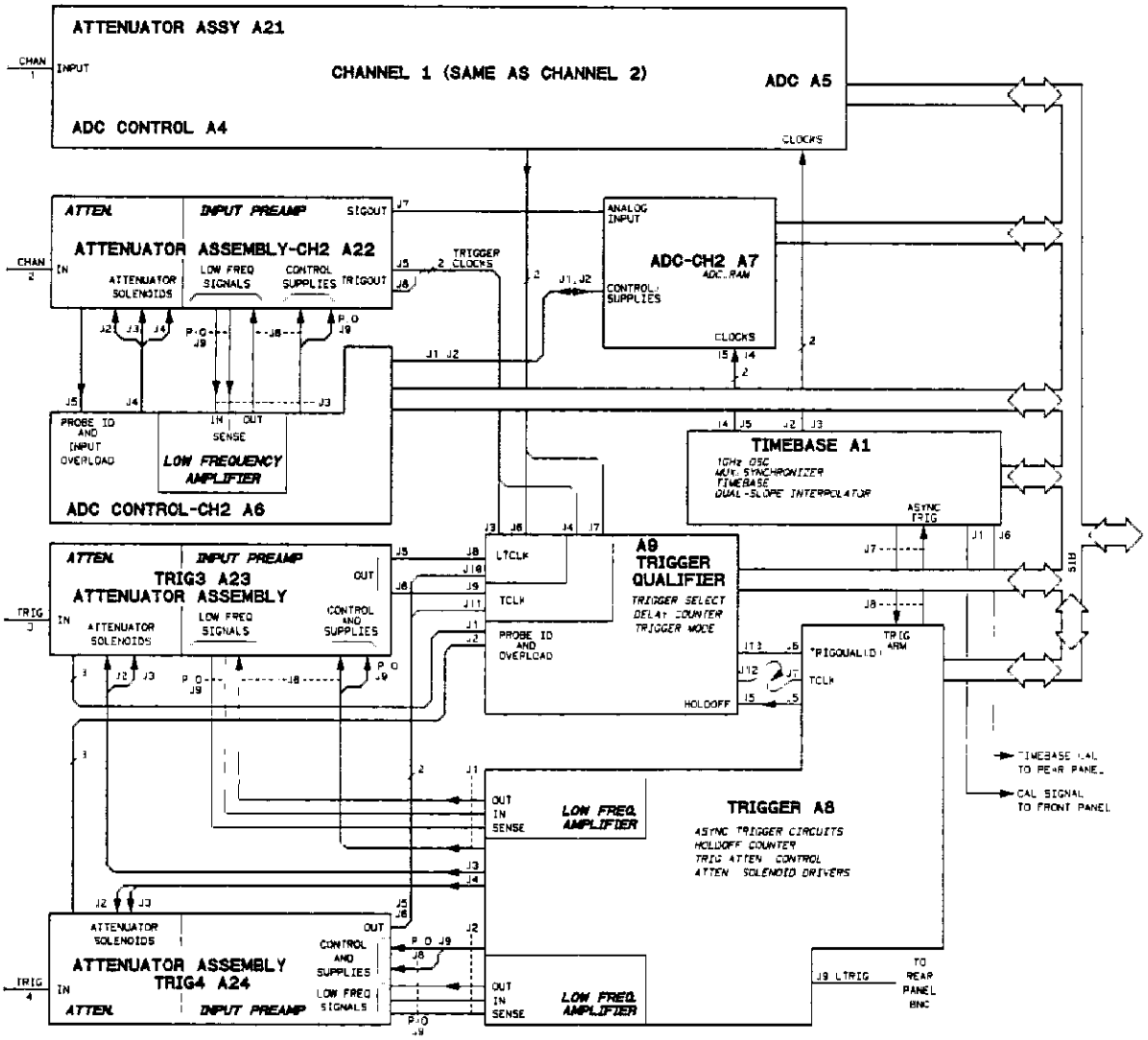


Figure 6B-1. Instrument Block Diagram, Acquisition System

6B-3. Acquisition

Channel 1 acquisition is identical to channel 2 acquisition. Use the Instrument Block Diagram, Acquisition System, for reference.

CHANNEL ATTENUATOR. The channel attenuator provides signal conditioning between the front panel channel input and the analog-to- digital converter. The outputs are a ±0.64 V single-ended signal, representative of the input signal, and two complementary trigger signals whose edges represent the desired trigger point for the channel. The ADC Control provides power supplies, control signals, and the low frequency amplifier, and it receives the probe ID and input overload signals.

ANALOG-TO-DIGITAL CONVERTER. The Analog-to-Digital Converter (ADC) digitizes and stores the channel input signals. It gets control and supplies from the ADC Control and sample clocks from the Timebase. The ADC flash converter outputs into FISO (fast in/slow out) sequential memory and the output from memory goes to the system interface bus (SIB).

ADC CONTROL. The ADC Control provides control for the attenuator and ADC assemblies. Interface to the SIB provides the control. Supply voltages are developed for the attenuator and ADC assemblies. The ADC Control carries the low frequency amplifier for the attenuator assembly.

6B-4. Triggering and Sample Clocking

TRIGGER ATTENUATORS. The trigger attenuator assemblies provide nearly the same functions as the channel attenuator assemblies. Part of the attenuator section is not used and the signal output is not used. The complementary trigger signals, probe ID, and overload are sent to the Trigger Qualifier. The Trigger provides the low frequency amplifier, control signals, and power supplies.

TRIGGER QUALIFIER. The Trigger Qualifier uses the trigger signals from the channel and trigger attenuator assemblies to provide edge and pattern recognition. Trigger delay circuitry is also a part of the Trigger Qualifier. HOLDOFF is an input from the Trigger. The Trigger Qualifier develops TCLK (trigger clock) and TRIGQUAL (D) (trigger qualifier) for the Trigger circuits. Probe ID and overload signals are inputs from the attenuator assemblies to the Trigger Qualifier.

TRIGGER. The Trigger provides the asynchronous trigger to the Timebase. Asynchronous trigger provides a time reference for, or terminates (after a time delay), the data acquisition.

TCLK clocks TRIGQUAL(D) (trigger qualifier) through the trigger circuitry. If holdoff is being used, as soon as a trigger occurs the holdoff counter (by events or time) disables the trigger circuitry until the counter times out.

The Trigger assembly includes the control circuitry and supplies for the trigger attenuators and low frequency amplifiers.

TIMEBASE. The Timebase generates the sample clocks for the ADC assembly. A 1 GHz oscillator provides the base sample rate. Frequency dividers provide sample rates down to 50 Hz. The trigger interpolator measures the time from the trigger to each sample when repetitive sampling is used.

After the pre-trigger delay, TRIGARM (trigger arm) enables the ATRIG signal to reach the timebase.

The Timebase provides a vertical calibration signal to a connector on the front panel. It provides either of two signals to a rear panel BNC. When the instrument is running in the acquisition modes, the signal is 500 KHz referenced to the system clock. In Timebase Cal mode it is 50 MHz referenced to the acquisition clock. In a small group of early instruments the rear panel signal is always referenced to the acquisition clock and varies with the sample rate.

6B-5. Instrument Control

Use the Instrument Block Diagram, Mainframe, for reference.

MICROPROCESSOR. The Microprocessor uses a 68000 16-bit processor to handle all processing on the system interface bus (SIB). The assembly includes 512K bytes of ROM and 32K bytes of non-volitile CMOS RAM. Bus buffers, interrupt logic, a time-out counter, and a bus arbitration circuit are part of the Microprocessor assembly. Because of the single controller in the HP 54111D, the bus arbitration circuitry is not used.

INPUT/OUTPUT. The Input/Output (I/O) assembly combines several functions on one PC board. The dynamic RAM on this assembly is used for basic operation of the instrument and to store waveforms. The keyboard control provides scanning and reading of the three keyboards and RPG (rotary pulse generator). The HP-IB interface couples the system interface bus (SIB) to the HP-IB port on the rear panel. An oscillator and divider circuit provides 16, 8, 4, and 2 MHz clocks for the system. The battery back-up provides battery power to the non-volitile RAM on the microprocessor assembly. The Power Test circuitry monitors the supplies on the SIB. The output of the circuit is a status bit that the microprocessor reads. If all supplies are greater than 50% it registers as passing. The Power-On Reset provides a glitch-free reset pulse to the SIB for use by any circuitry on the bus.

FRONT PANEL ASSEMBLIES. Front panel assemblies include three keyboards, an RPG (rotary pulse generator), and the Display Control. The Control Keyboard allows direct entry of values into the field selected on the CRT. The Function and Menu keyboards, to the right of and below the CRT respectively, give control of functions noted on the display. The RPG provides the digital equivalent of a potentiometer as well as sequential stepping through incremental functions. The Display Control provides analog brightness and background control of the display.

COLOR DISPLAY ASSEMBLY. The Color Display Assembly provides interface between the SIB and the Color CRT Module. It includes graphics RAM, character generation, and RGB generation. Horizontal sync, vertical sync, and blanking also drive the Color CRT Module.

COLOR CRT MODULE. The Color CRT Module includes the color CRT and its associated driving circuitry. It uses H and V sync, blanking, and red, green, and blue video from the Color Display assembly. The Color CRT Module is considered one replaceable part.

6B-6. Power Supplies

PRIMARY SUPPLY. The Primary supply provides an unregulated 300Vdc primary voltage to the switching supplies. It can be set for 115 or 230 V line input (-25%, +15%). A circuit breaker provides rear panel switching of the line input. The STBY (standby) switch on the front panel controls a 120 Vdc switching regulator which supplies the Color CRT Module as well as an on/off control voltage to the Analog and Digital supplies.

DIGITAL SUPPLY. The Digital Supply switching regulator provides +5 V and -5.2 V to most of the digital circuitry. It uses the 300 Vdc primary from the Primary Supply and is controlled (on/off) by an output from the 120 V Supply. These supplies are designated +5 and -5 on the SIB and are referenced to DGND of the SIB.

ANALOG SUPPLY. The Analog Supply switching regulator provides ±8.5 Vdc and ±18.5 Vdc to much of the analog circuitry. It uses the 300 Vdc primary from the Primary Supply and is controlled (on/off) by an output from the 120 V Supply. Many of the assemblies in the instrument use local regulation of these supplies to provide decoupling from system noise. These supplies are designated ±8 and ±18 on the SIB and are referenced to AGND of the SIB.

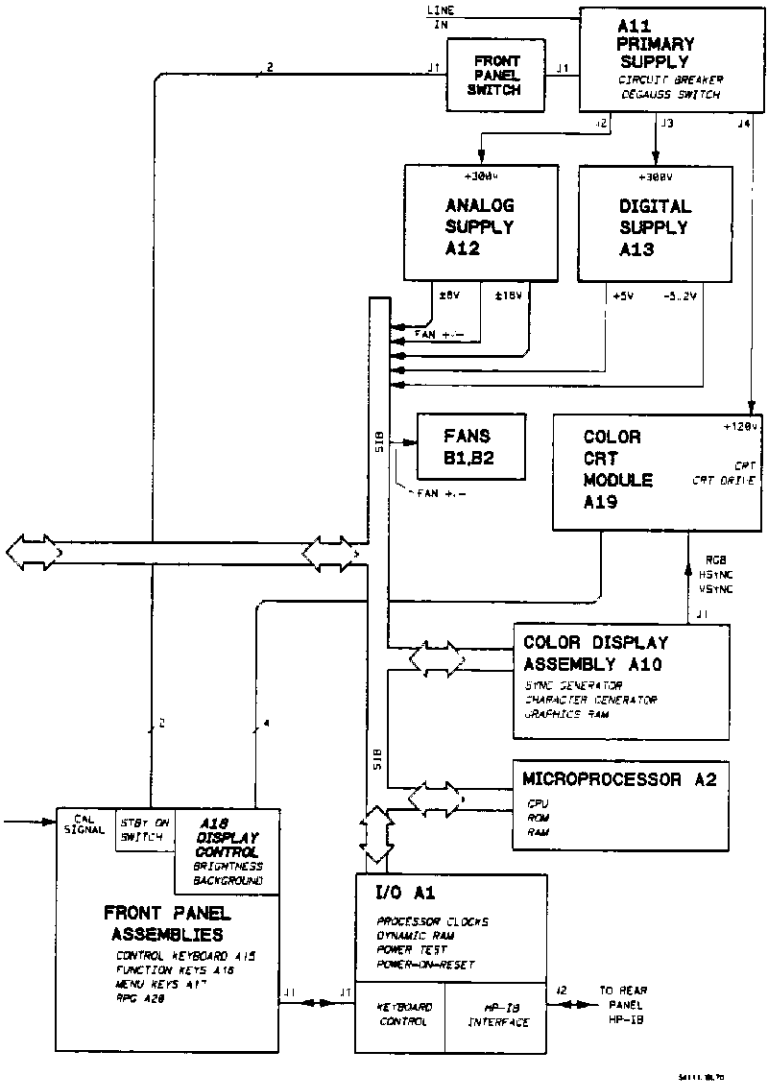


Figure 6B-2. Instrument Block Diagram, Mainframe

6B-7. ATTENUATOR ASSEMBLY THEORY

6B-8. Channel Attenuators

The Channel Attenuator assemblies consist of two main sections, the attenuator and the preamplifier. The Channel Attenuator assemblies get power and control from the ADC Control assembly for their respective channel. Refer to the Attenuator Assembly Block Diagram for the following discussion.

INPUT ATTENUATOR. The input attenuator section provides 50Ω or 1MΩ impedance switching and two ÷10 sections which can be cascaded for ÷100. Magnetically latching solenoids control the switching. A ring on the input BNC connector provides means for identifying high impedance 10:1 voltage divider probes. A sample of the input signal from a tap on the 50Ω input termination is used to control an overload protection circuit. The microprocessor removes the 50Ω termination if the input is overloaded.

PREAMPLIFIER. The preamplifier hybrid consists of several sections, a high-pass filter and FET and associated circuitry, the main preamplifier with trigger circuitry, the driver amplifier, and a differential-to-single converter.

At the input to the preamp, the low frequency component of the input signal is sent to the low frequency amplifier on the ADC Control assembly. AC/DC coupling and DC offset are incorporated in the low frequency amplifier.

Upon return to the attenuator assembly, the low frequency and high frequency signals are recombined and fed to the input FET of the preamplifier. The preamplifier incorporates most of the gain changing and the trigger conditioning. Three incremental gain ranges, ÷1, ÷2, and ÷4 affect the signal before trigger pick-off. Vernier gain affects the signal after trigger pick-off. Other signals control trigger functions.

The output of the preamplifier chip is fed to the driver chip. The gain of the driver can be increased by a factor of five for increased sensitivity.

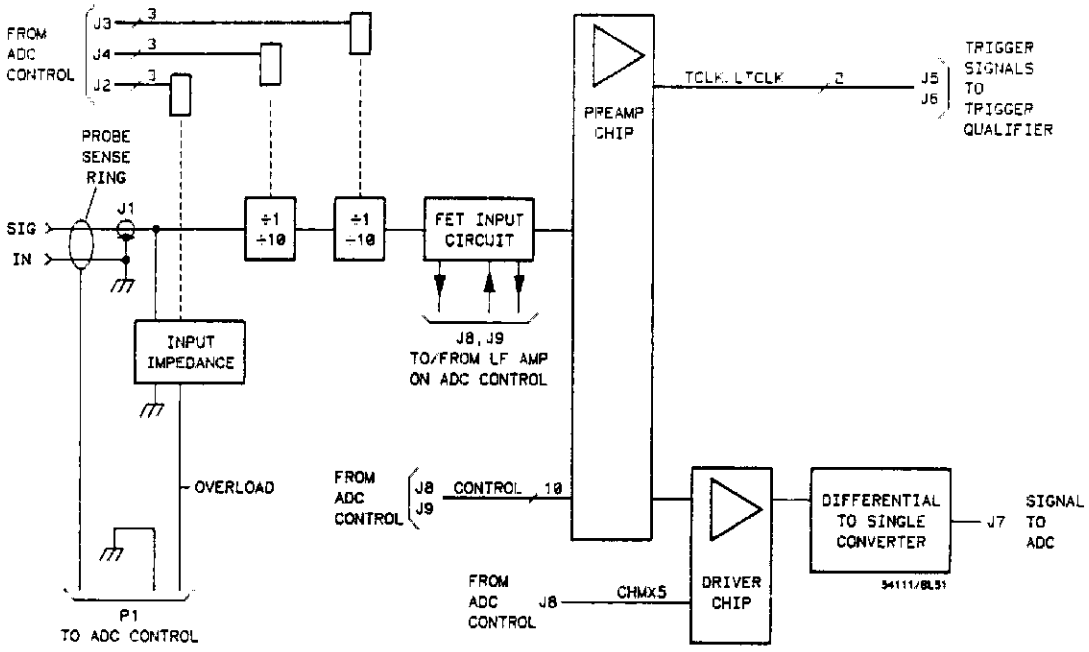
The output of the driver feeds the differential-to-single converter. The output of the converter is a coaxial connector which is connected by cable to the ADC assembly and analog-to-digital converter hybrid.

The trigger signals are two complementary signals whose edges represent the selected trigger point of the input signal. They are conducted via two coaxial cables to the Trigger Qualifier assembly.

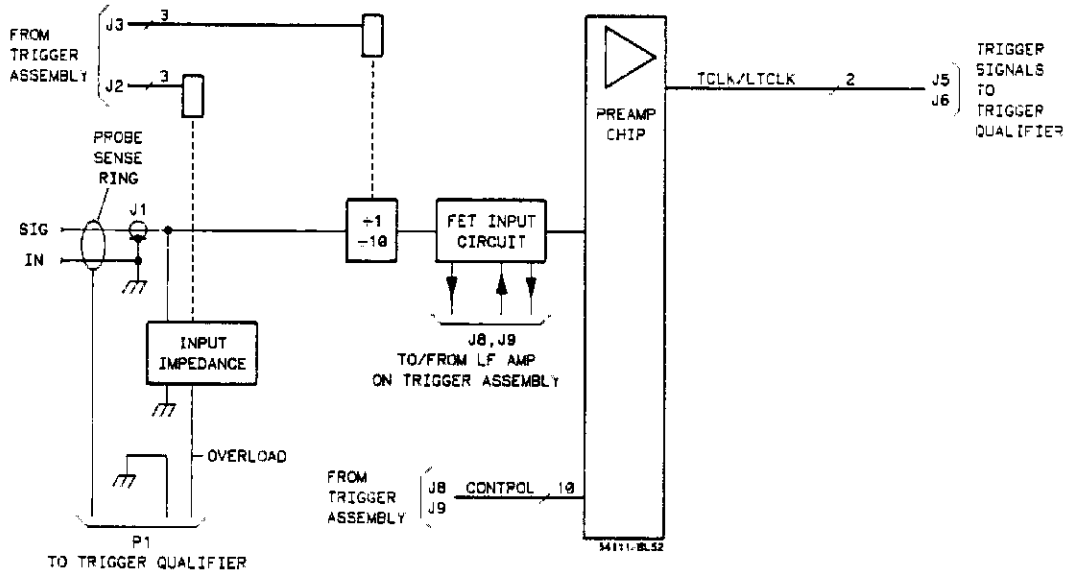
6B-9. Trigger Attenuators

The Trigger Attenuator assemblies are nearly the same as the Channel Attenuator assemblies. There are two major differences. First, there is a single divide-by-ten function at the attenuator input. Second, there is no main signal output. Only the two trigger signals are used. Also, the preamplifier is kept in the ÷4 gain mode.

Both Trigger Attenuator assemblies get power and control from the Trigger assembly. The low frequency amplifiers are also on the Trigger assembly. The trigger signals, probe ID, and input overload signals are sent to the Trigger Qualifier assembly.



CHANNEL ATTENUATOR ASSEMBLY BLOCK DIAGRAM



TRIGGER ATTENUATOR ASSEMBLY BLOCK DIAGRAM

Figure 6B-3. Attenuator Assembly Block Diagrams

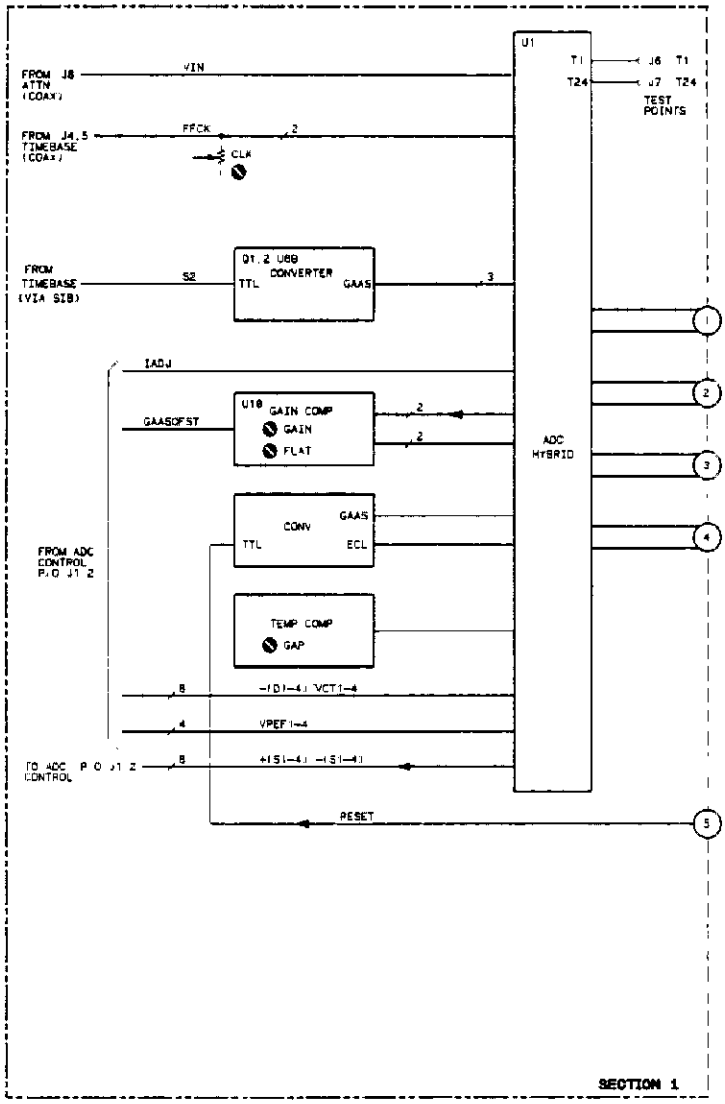


Figure 6B-4. ADC Assembly Block Diagram (part 1)

6B-10. ADC ASSEMBLY THEORY

The Analog-to-Digital Converter (ADC) assembly samples one channel input signal and stores it in memory.

Use the Analog-to-Digital Converter Assembly Block Diagram for the following discussion. The block diagram is laid out in two sections, corresponding to the two schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

Section 1

The ADC hybrid is a multi function part. The input signal to each channel is sampled using a GaAs diode sampling bridge. The output of this sampler is distributed to four second-rank samplers, each of which drives a six bit flash ADC. These six bit converters run in four phaases at rates of up to 250 MSa/s, one fourth the sample rate. Each converter outputs gray-code data to one memory IC.

Each flash converter consists of an array of comparators, of which one input of each is connected to the input signal, and the other input is connected to a tap on an accurate voltage divider stick. A reference voltage is applied to the divider stick. At the time of the sample, the outputs of the comparators are latched. The amplitude of the signal determines which comparator outputs were high or low and logic circuitry then converts the comparator outputs to a 6-bit binary gray code.

VIN, the analog signal input, comes through a coaxial cable from the attenuator assembly. FFCK+/-, the complementary sample clocks, come from the Timebase assembly through coaxial cables. The CLK adjustment sets the differential offset. S2 is a control signal, also supplied by the Timebase. It is converted from TTL to GaAs levels by Q1, Q2, and part of U8. The RESET signal comes from the Timebase via the SIB and Section 2 of the block diagram.

The rest of the ADC support circuitry controls dc levels in the hybrid. The source for external input is the ADC control assembly. There is temperature compensation and four adjustments. For control of the voltage divider sticks there are 12 inputs from and eight outputs to the ADC control assembly.

The output of the ADC hybrid is four sets of 6-bit data, each set with its own clock. Each data bit and clock is a complementary signal pair, so there are 14 lines for each data set.

Section 2

The FISO (fast in, slow out) memory is 2K bytes (16K bits). It is written and read serially. Each memory IC stores data from one of the four flash converters in the ADC hybrid. Seven pairs of complementary signals, six data bits and a clock, write data into one memory IC at one fourth the sample rate. The memory is eight bits wide. The remaining two data bits are used for a dither function.

Data is read from memory using the same clock signals, but at a rate compatible with the microprocessor. The outputs of the memories are paralleled and are run through a gray-to-binary code converter. The output of the converter is buffered onto the lower byte of the SIB data bus. The Timebase assembly puts "0"s on the upper byte of the data bus.

The Control Data Latch latches FISO control signals from the upper byte of the SIB. ADCR/LW, ADCRST, and LADCMEMRD control read/write and reset of the memory. ADCRST is also used to reset the ADC hybrid and FISO memory.

The circulating clock, FISOPHA-D, synchronizes reading data out of the memory. The microprocessor can read them to determine which FISO is being read.

DITHERING

As the information is read from the four ADCs, a digital bias is applied at the input of the FISO memory. That is, the data from each converter is augmented from six to eight bits, these least significant bits being either 00, 01, 10, or 11 (in straight code). The resulting eight bit words are then passed through a six, seven, or eight-bit filter, resulting in a certain amount of bandwidth and S/N ratio for each filter. This process is called dithering.

If the signal is significantly oversampled, eight effective bits of resolution can be achieved at bandwidths of up to 25 MHz single-shot with 1 GSa/s sampling.

Without going into the mathematical detail of how dithering works, it effectively moves the thresholds of each A/D converter, making each converter's thresholds 1/4 LSB different from the the one before it. This small noise signal is then filtered out by the chosen interpolation filter. The result is better resolution out of the same number of hardware bits.

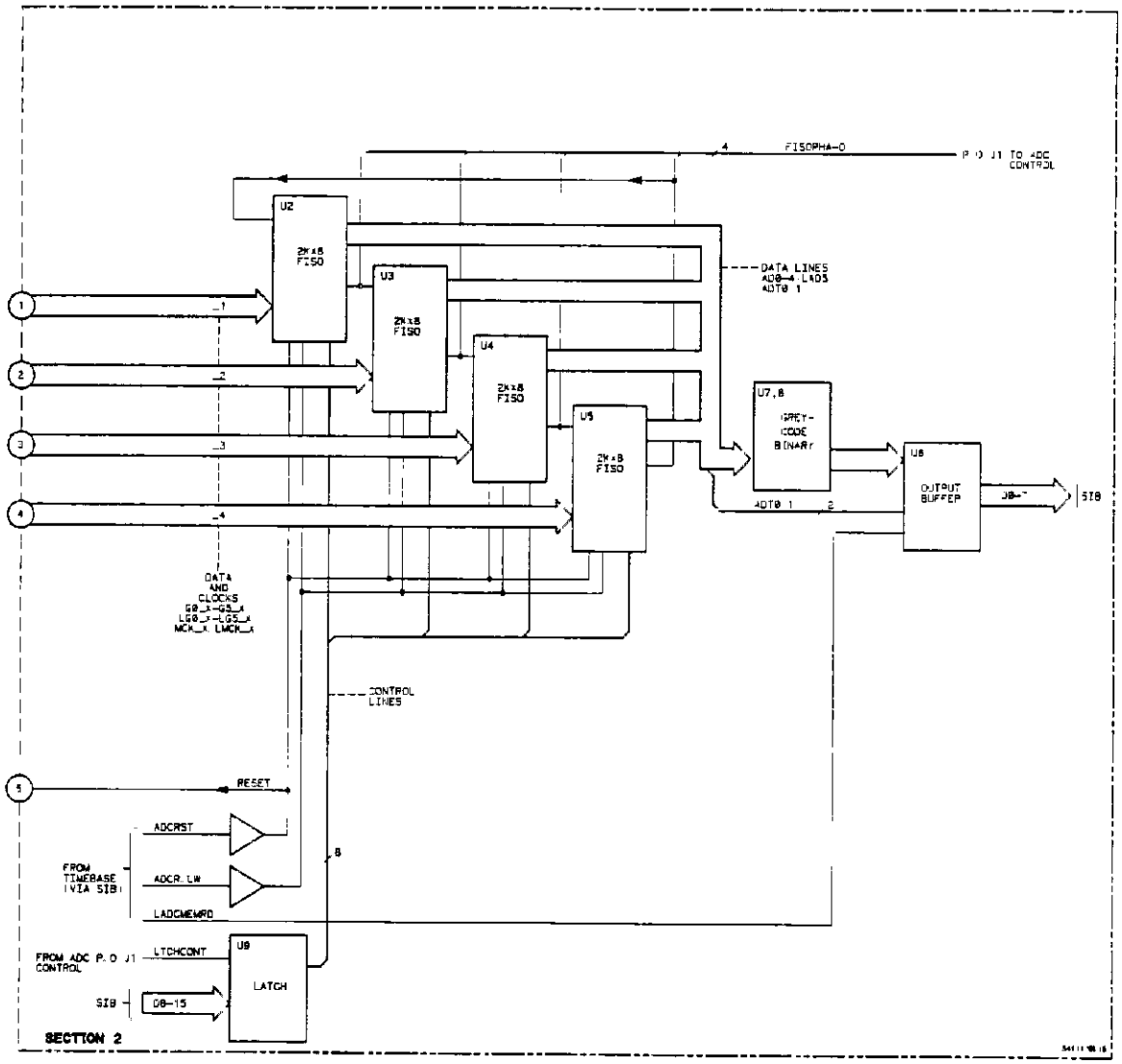


Figure 6B-5. ADC Assembly Block Diagram (part 2)

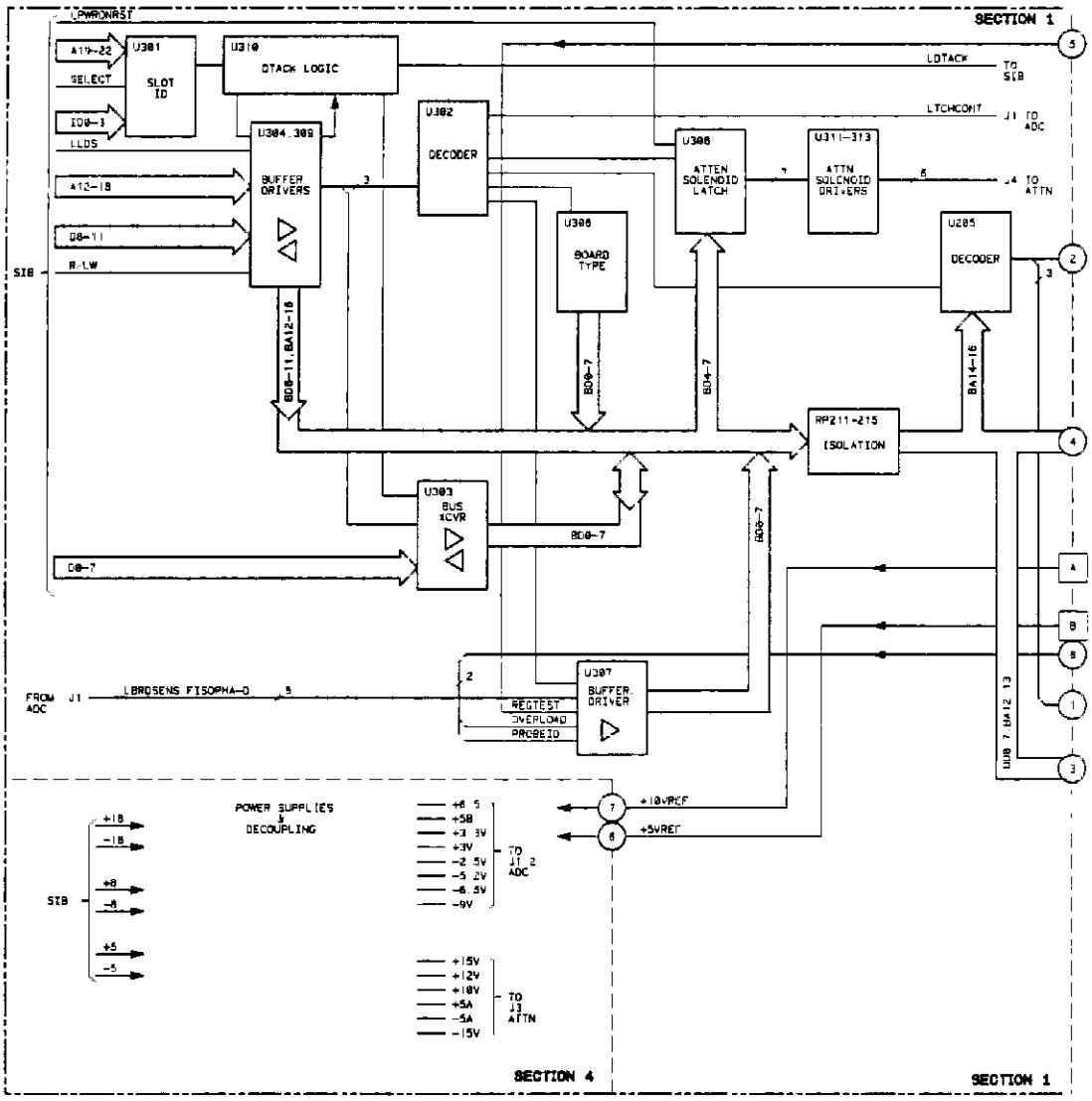


Figure 6B-6. ADC Control Assembly Block Diagram (part 1)

6B-11. ADC CONTROL ASSEMBLY THEORY

The ADC Control assembly provides supplies and most of the control for the Analog-to-Digital Converter (ADC) assembly.

Use the ADC Control Assembly Block Diagram for the following discussion. The block diagram is laid out in four sections, corresponding to the four schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

Section 1

SLOT ID. U301 is a 4 bit comparator which compares address lines A19-22 with slot ID codes ID0-3. Slots are made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U301 output goes high, enabling other circuitry.

DTACK LOGIC. Data transfer acknowledge circuitry buffers the output of the slot ID and develops the LDTACK signal.

BUFFER/DRIVERS. U304 and U309 improve the fan-in of several signals to prevent loading of the SIB.

DECODER U302. With address lines A17 and A18 and the R/LW line, U302 decodes read and write functions of this assembly.

BOARD TYPE. When board type is requested by the microprocessor, this assembly responds with a code over the data bus. The input pins of buffer U305 are encoded with the board type. Enabling U305 reads the code.

ATTENUATOR SOLENOID LATCH. U308 latches the channel attenuator setup data. This sets the attenuator input impedance and division ratio. A low on the LPWRONRST line keeps the driver circuitry from changing the attenuators during power-up.

ATTENUATOR SOLENOID DRIVERS. The solenoid drivers provide drive signals to input impedance and division ratio solenoids on the channel attenuators. The solenoids are magnetically latched, so only a short duration signal is needed to change settings.

DECODER U205. This decoder provides control signals for DACs and latches in the analog control circuitry.

ISOLATION. Resistors in the address and data lines isolate the analog circuitry from the digital circuitry.

BUS TRANSCEIVER. U303 buffers read/write data from/to the data bus of the SIB.

BUFFER/DRIVER U307. U307 buffers several signals from this assembly and the ADC assembly, onto the lower byte of the data bus.

Section 4

Several power supply voltages are generated on this assembly. They use the supplies from the SIB and isolate circuitry on this assembly from the rest of the system. They also supply all the voltages for the ADC assembly and the channel attenuator.

Section 2

Circuitry in this section controls the channel attenuator preamplifiers and part of the ADC. The low frequency amplifier for the attenuator preamp is also included here.

LATCHES U203/U204. U204 latches data from the data bus for control of the channel attenuator preamp. The output of U203 are also ANDed in U206 for test purposes. U203 latches data for control of circuitry in this section.

REGISTER TEST. Outputs from U203 and U204 are ANDed in U206 for internal testing purposes.

TRIGGER LEVEL DAC. This DAC provides a trigger level signal to the attenuator preamp. The bilateral switch in its output changes the trigger level range.

CAL/OFFSET DAC. This DAC provides the channel offset signal during acquisition and a calibration voltage during calibration procedures initiated by firmware. The reference output is also used for other purposes on this assembly and the attenuator preamp.

QUAD DAC. The quad DAC provides four analog signals. Two signals are for the ADC hybrid on the ADC assembly, one controls the attenuator vernier and the other controls the trigger sensitivity.

LOW FREQUENCY AMP. The low frequency amplifier is part of the input signal path. The low frequency component of the signal is picked off, amplified, and reinserted between the ÷10 attenuators and the preamp hybrid of the attenuator assembly. The ac/dc coupling and offset functions are accomplished in the low frequency amplifier.

PROBE ID/INPUT OVERLOAD. A sense ring at the input BNC identifies when a standard 10:1 probe is being used. The instrument automatically adjusts the vertical scaling to suit. A line from the channel attenuator monitors the signal on the 50Ω input termination resistor. The overload circuit provides an interrupt to the microprocessor over the IRQ2 line and a flag onto the data bus. Once the overload is cleared, the microprocessor sends a reset signal through U205 (section 1) which resets the sense circuit.

Section 3

This section controls the divider sticks of the flash converter ADCs (see ADC assembly theory). There are four sets of control circuitry, one for each divider stick. Two quad DACs and a latch, controlled by calibration routines, set up the levels on the sticks.

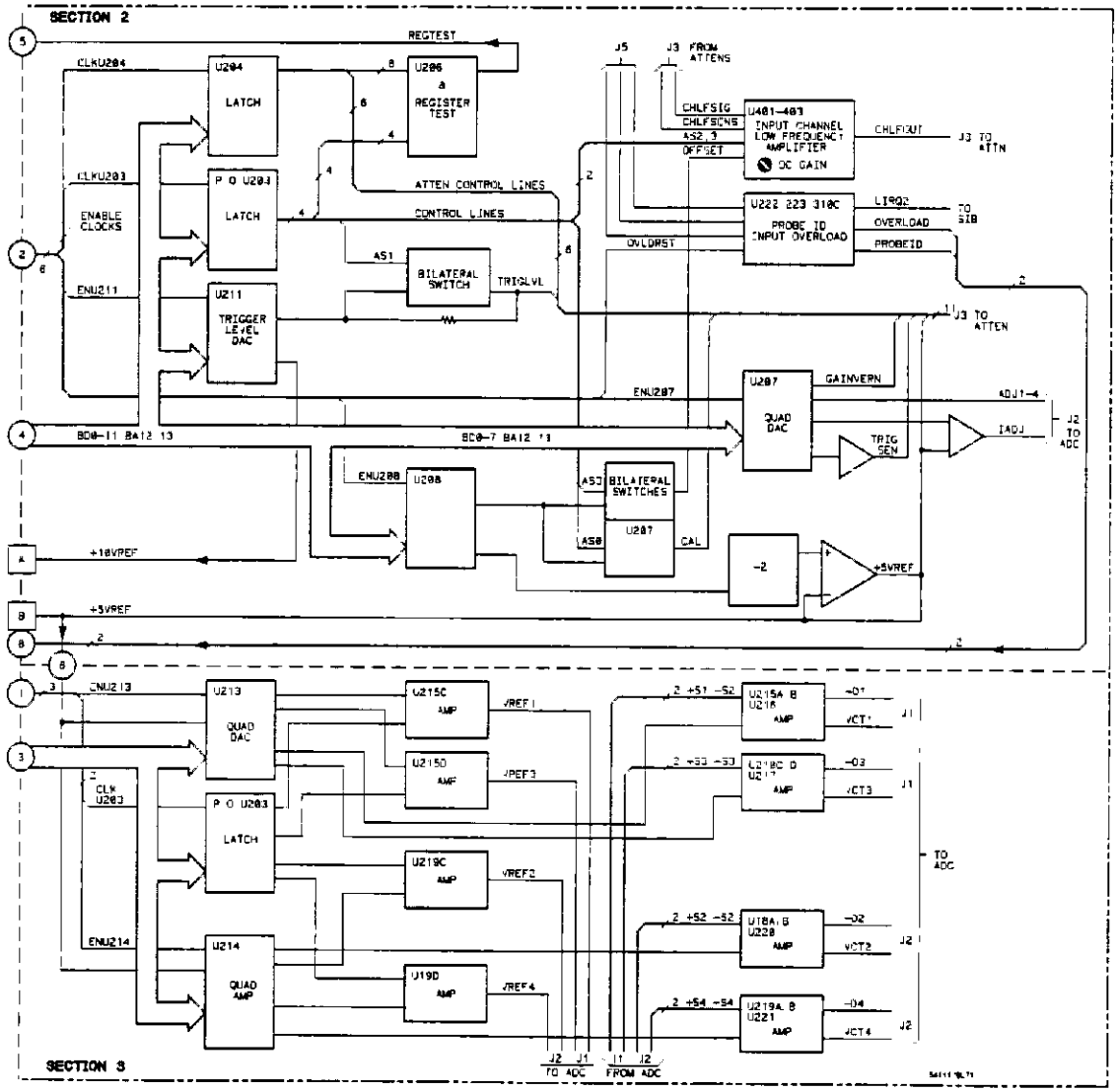


Figure 6B-7. ADC Control Assembly Block Diagram (part 2)

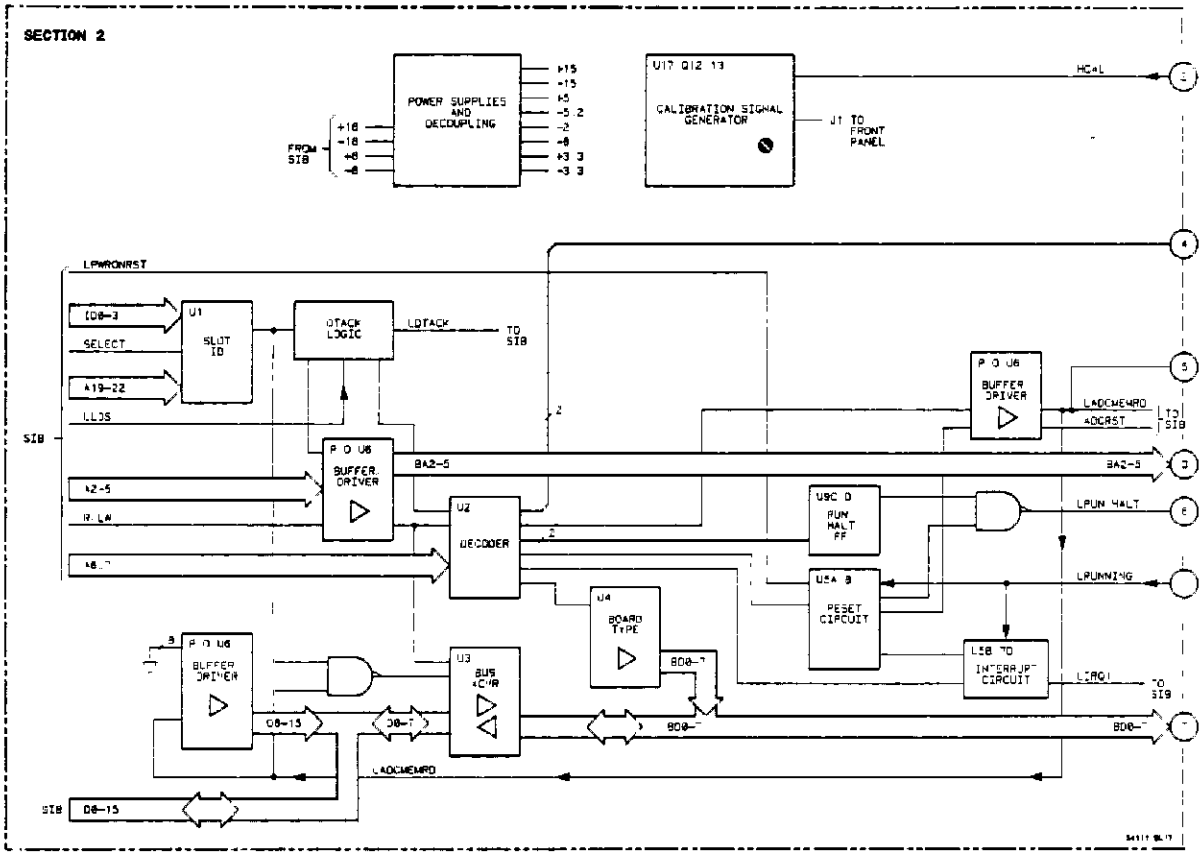


Figure 6B-8. Timebase Assembly Block Diagram (part 1)

6B-12. TIMEBASE ASSEMBLY THEORY

The Timebase assembly provides the acquisition sample clock. It provides several control signals to the Trigger and ADC assemblies as well as several other outputs.

Use the Timebase Assembly Block Diagram for the following discussion. The block diagram is laid out in two sections, corresponding to the two schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

Section 2

Circuitry in section two provides control for the timebase and part of the ADC.

SLOT ID. U1 is a 4 bit comparator which compares address lines A19-22 with slot ID codes ID0-3. Slots are made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U1 output goes high, enabling other circuitry.

DTACK LOGIC. Data Transfer Acknowledge circuitry buffers the output of the slot ID and develops the LDTACK signal.

BUFFER/DRIVER U6. U6 improves the fan-in of several signals to prevent loading of the SIB. It also buffers the memory read and ADCRST signals.

DECODER. With address lines A6 and A7 and the R/LW line, U2 decodes read and write functions of this assembly.

BUFFER/DRIVER U10. When the acquisition data is being read from the FISO memory onto the lower byte of the SIB data bus, U10 puts all zeros on the upper byte of the bus.

BUS TRANSCEIVER. U303 buffers read/write data from/to the data bus of the SIB.

BOARD TYPE. When board type is requested by the microprocessor, this assembly responds with a code over the data bus. The input pins of buffer U4 are encoded with the board type. Enabling U4 reads the code.

RUN/HALT F-F. The run/halt flip-flop uses two lines of decoder U2 to enable or disable the LRUN/HALT signal.

RESET CIRCUIT. The reset circuit provides a timed reset sequence for the acquisition system.

INTERRUPT CIRCUIT. The interrupt circuit drives the LIRQ2 line on the SIB.

POWER SUPPLIES. Several power supplies use the SIB power buses to derive specialized operating voltages for the circuitry in section 1. They also isolate this circuitry from the rest of the instrument environment.

CALIBRATION SIGNAL GENERATOR. This 2 KHz oscillator provides a square-wave signal to the front panel. When the instrument is in the Timebase Cal mode the output is forced high and the amplitude can be measured or adjusted to 0.8000 Vdc.

On some earlier instruments the signal is forced high by another method.

Section 1

Circuitry in section one develops the acquisition sample clock. It also does the trigger interpolation.

During sampling, acquired data must be correlated to the trigger point. Each acquisition cycle has a different relationship to the trigger. Correlation is done by the trigger interpolator. It makes a high precision time interval measurement which is used to position the acquired data.

1 GHZ OSCILLATOR. The 1 GHZ oscillator uses a SAWR (surface acoustic wave resonator) to generate the basic acquisition sample clock.

MUX/SYNCHRO. The multiplexer/synchronizer IC provides the high frequency division ratios for the acquisition sample clock. Sample rates developed here are 1 GHz, 500 MHz, and 250 MHz. A 100 MHz output goes to the timebase IC for further division.

TIMEBASE IC. The timebase IC is a multifunction IC. It provides the majority of the sample clock rates, from 100 MHz down to 50 Hz. It divides the 100 MHz output of the multiplexer/synchronizer IC in a 1, 2, 4, 10 sequence. It feeds the divided rate back into the mux/synchro for output to the ADC assembly. It also provides counters and gating for coarse and fine interpolators and the pre- and post-trigger delay counters.

FINE INTERPOLATOR. The trigger interpolator consists of coarse and fine interpolators. The coarse interpolator is part of the timebase IC. The fine interpolator uses a dual slope technique to increase the accuracy of the time interval measurement. It is gated by the timebase IC and its output controls a counter in the timebase IC.

TEST SIGNAL LOGIC. This circuitry is a multiplexer and divider combination that selects one of two signals and outputs them to the rear panel. HCAL from the timebase IC selects the signal. When the instrument is in an acquisition mode, the rear panel output is the 2 MHz system clock from the SIB divided by four. When the instrument is in the Timebase CAL mode, the output is the 100 MHz output of the timebase IC divided by two.

HCAL from the timebase IC also controls the Calibration Signal Generator. When the instrument is in the Timebase Cal mode, HCAL forces the front panel CAL signal to 0.8 Vdc so that it can be measured or adjusted during performance tests or adjustment procedures respectively.

On a few earlier instruments the above circuitry is different. The rear panel signal is only a signal that is a divide-by-two function of the sample rate and the front panel CAL signal is forced high by another method.

LOGIC U14. Several signals are combined to develop S2, a signal that controls the high/low frequency modes of the ADC hybrid.

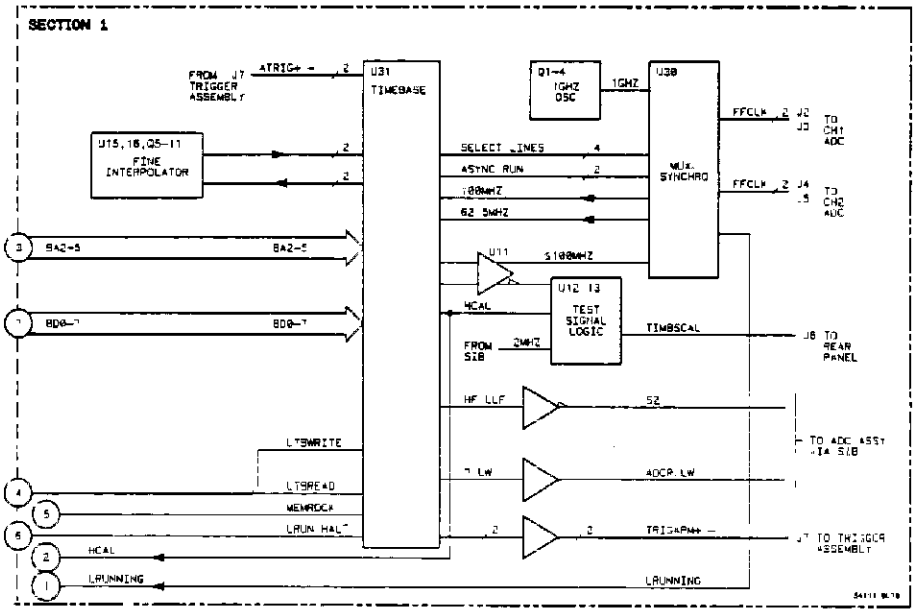


Figure 6B-9. Timebase Assembly Block Diagram (part 2)

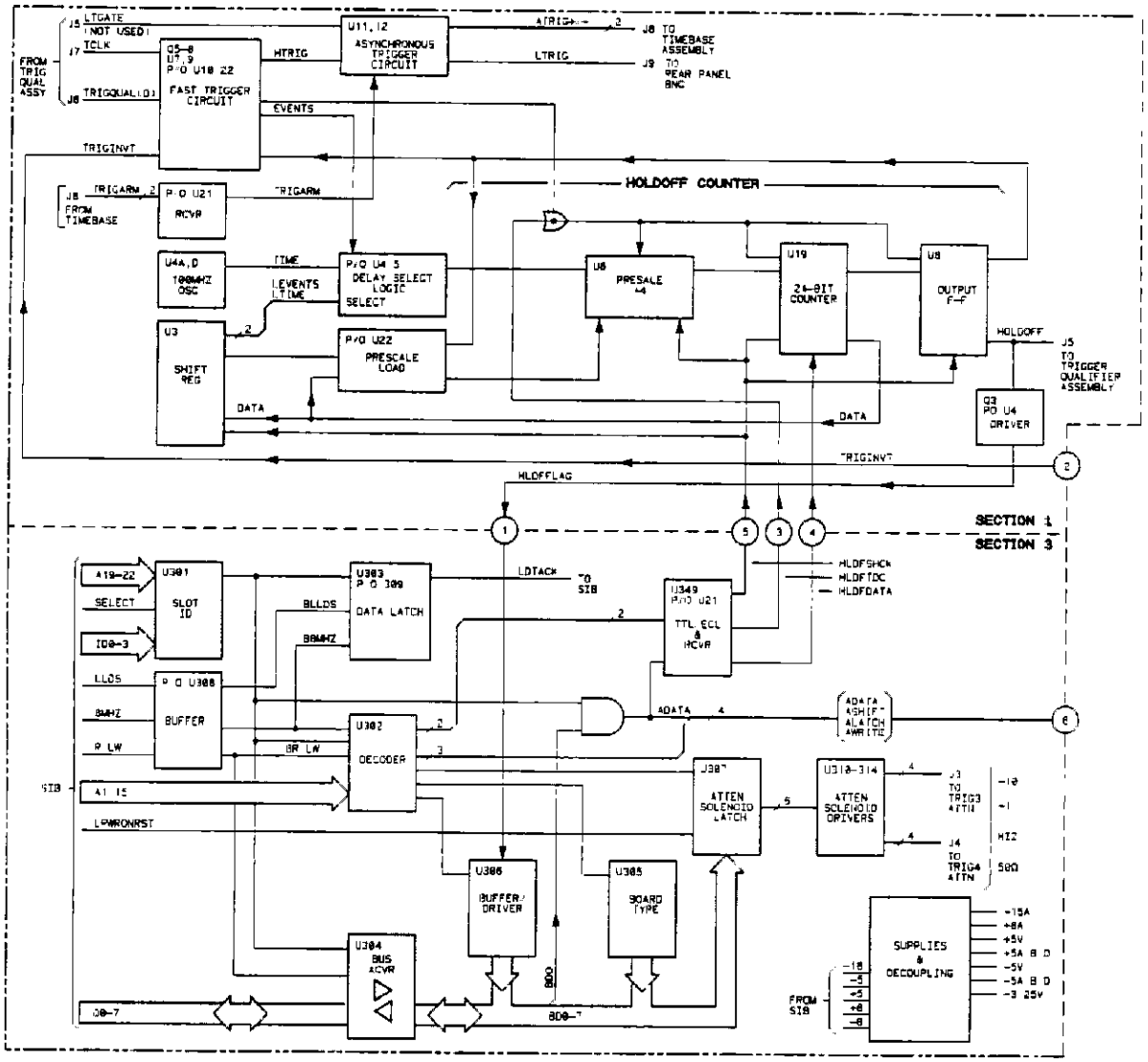


Figure 6B-10. Trigger Assembly Block Diagram (part 1)

6B-13. TRIGGER ASSEMBLY THEORY

The Trigger assembly establishes the trigger point for an acquisition cycle and establishes the holdoff period. It also provides control and supplies, trigger level, sensitivity, and slope for the TRIG 3 and TRIG 4 attenuators.

Use the Trigger Assembly Block Diagram for the following discussion. The block diagram is laid out in three sections, corresponding to the three schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

Section 1

FAST TRIGGER CIRCUIT. Logically ORs three input lines (only one is used, TCLK) to produce edges representing trigger events. TCLK clocks TRIGQUAL (D) (from the Trigger Qualifier) through the fast trigger circuit. TRIGQUAL (D) functions at the "D" input of the Fast Trigger flip-flop.

The holdoff circuitry keeps the Fast Trig F-F set until the end of the holdoff period. When TRIGQUAL (D) is true, the Fast Trig F-F generates an HTRIG edge on the first TCLK edge after the end of holdoff.

INVERT is used to invert the trigger signal for pattern entered triggering.

ASYNCHRONOUS TRIGGER FF. Trigger enable signal TRIGARM enables asynchronous trigger flip-flop U11. U11 then produces ATRIG after it receives the next HTRIG edge.

HOLDOFF OSCILLATOR. Generates a crystal controlled 100 MHz signal for holdoff by time.

HOLDOFF COUNTER. Counts a 100 MHz signal for time holdoff, or TCLK transistions for events holdoff.

Section 3

SLOT ID. U301 is a 4 bit comparator which compares address lines A19- 22 with slot ID codes ID0-3. Slots are made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right When the slot this assembly is in is addressed, the two codes are equal and U301 output goes high, enabling other circuitry.

DTA LATCH. The Data Transfer Acknowledge Latch signals the microprocessor when the Slot ID output is true.

BUFFER. Improves the fan-in of several signals to prevent loading of the SIB.

DECODER. With address lines A1 and A15 and the R/LW line the read and write functions of this assembly are decoded.

BUS TRANSCEIVER. Buffers read/write data from/to the data bus of the SIB.

TTL/ECL AND RCVR. The sensitive high frequency trigger circuitry is isolated from the rest of the digital circuitry by the TTL/ECL converter and line receiver. Serial data and control signals pass through this isolation circuitry.

HOLDOFF FLAG. Enabling buffer U306 reads HLDFFLAG, the status of the holdoff circuit.

BOARD TYPE. When board type is requested by the microprocessor, this assembly responds with a code over the data bus. The input pins of buffer U305 are encoded with the board type. Enabling U305 reads the code.

ATTENUATOR SOLENOID LATCH. U307 latches TRIG 3 and TRIG 4 attenuator setup data. This sets the attenuator input impedance, 1MΩ or 50Ω and division ratio, ÷1 or ÷10. A low on the LPWRONRST line keeps the attenuators from changing during power-up.

ATTENUATOR SOLENOID DRIVERS. The solenoid drivers provide drive signals to input impedance and division ratio solenoids on the TRIG 3 and TRIG 4 attenuators. The solenoids are magnetically latched, so only a short duration signal is needed to change settings.

POWER SUPPLIES. Several power supply voltages are generated on this assembly. They use the supplies on the SIB and isolate circuitry on this assembly from system noise.

Section 2

Circuitry in this section controls the TRIG 3 and TRIG 4 attenuators. The low frequency amplifiers for the attenuator preamp are also included here.

SHIFT REGISTERS. The shift registers convert serial data to parallel for loading in the attenuator control circuitry. U201 and U202 provide a data bus for the DACs and control for loading data. The outputs of U203 and U204 control several attenuator preamp hybrid functions as well as ac/dc and invert functions in the low frequency amp on the Trigger assembly.

DECODER. U205 decodes three output lines from U201 and controls the loading of data into shift registers U203 and U204 and DACs U207, 208, and 211.

DACS. Single-output DACs U208 and U211 provide the trigger level voltage to the low frequency amplifier. Dual DAC U207 provides trigger sensitivity (gain) signals to the preamp hybrid on the attenuators, for calibration.

LOW FREQUENCY AMPS. The low frequency amplifiers are part of the input signal path. The low frequency component of the signal is picked off, amplified, and reinserted at the gate of the FET. The ac/dc coupling and trigger level functions are accomplished in the low frequency amplifier.

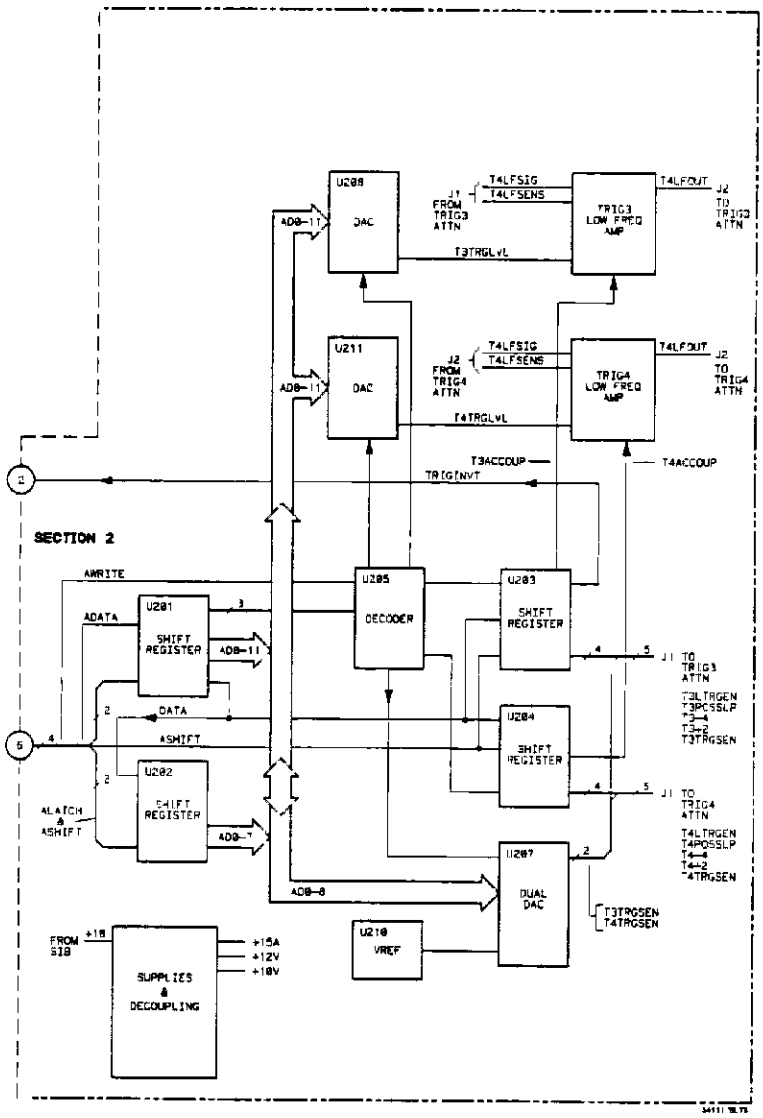


Figure 6B-11. Trigger Assembly Block Diagram (part 2)

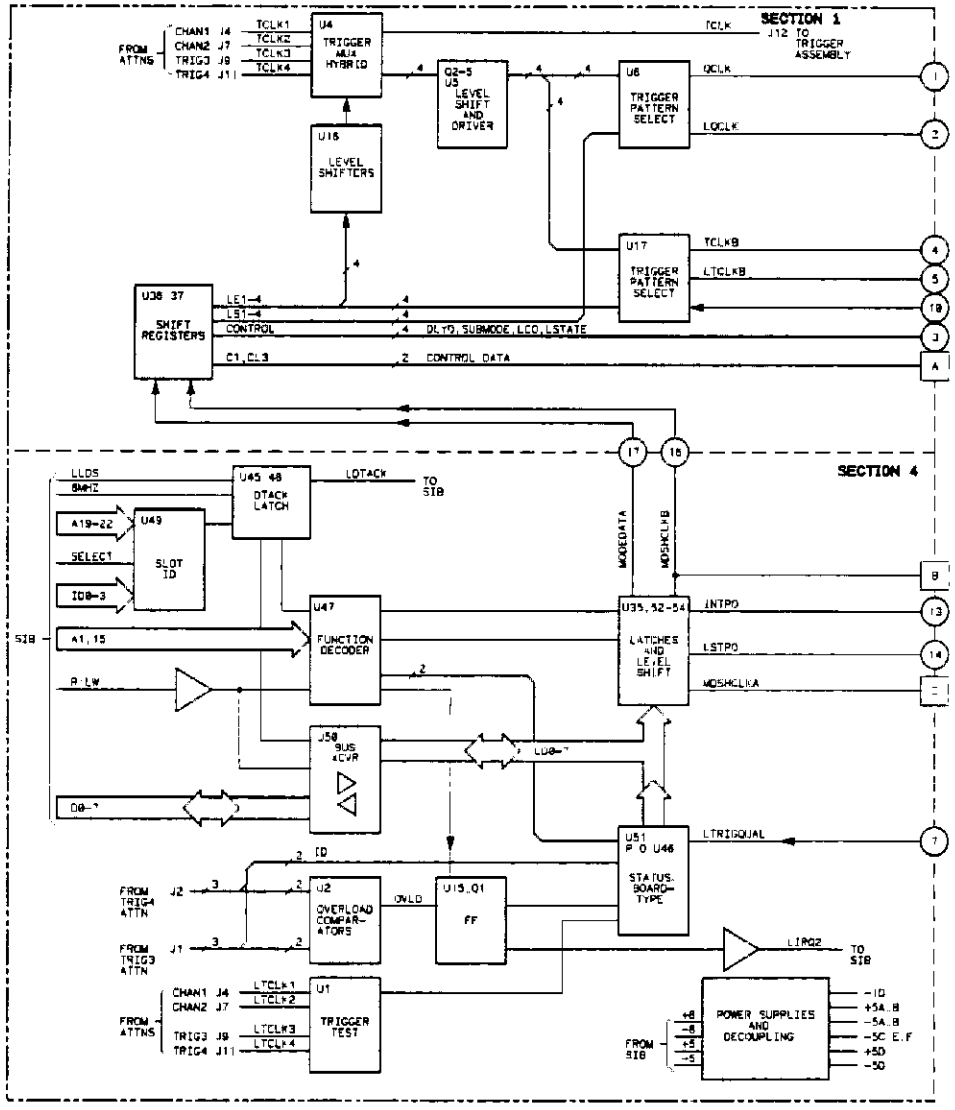


Figure 6B-12. Trigger Qualifier Assembly Block Diagram (part 1)

6B-14. TRIGGER QUALIFIER ASSEMBLY THEORY

The Trigger Qualifier uses the trigger signals from the channel and trigger attenuators to provide edge and pattern recognition. Trigger delay circuitry is also a part of the Trigger Qualifier.

HOLDOFF is an input from the Trigger assembly. The Trigger Qualifier develops TCLK (trigger clock) and TRIGQUAL (D) (trigger qualifier) for the Trigger assembly circuitry. Probe ID and overload signals are inputs from the attenuators to the Trigger Qualifier.

Use the Trigger Qualifier Assembly Block Diagram for the following discussion. The block diagram is laid out in four sections, corresponding to the four schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

Section 1

SHIFT REGISTERS. The shift registers convert serial data to parallel to provide control functions for trigger selection. Lines LE1-4 and LS1-4 select TCLK1-4 for trigger combinations. The other lines control various functions of the pattern recognition circuitry.

LEVEL SHIFTERS. The level shifters convert the levels out of the CMOS shift registers to the level needed by the trigger multiplexer hybrid.

TRIGGER MULTIPLEXER HYBRID. The LE1-4 lines, after level shifting, select the combination of TCLK1-4 signals to use as a trigger. This combination becomes TCLK which carries the 500 MHz trigger capability to the Trigger assembly. The transitions of TCLK are used to generate all acquisition triggers. TCLK1-4 signals are also sent through buffers in the multiplexer. These outputs are used for trigger pattern processing.

LEVEL SHIFT AND DRIVERS. Transistors Q2-5 level shift and drive the trigger pattern selectors U6 and U17.

TRIGGER PATTERN SELECT U6. Trigger select lines LS1-4 select a combination of the buffered TCLK1-4 signals. The QCLK and LQCLK signals are used for event-delay, time-delay and state modes of trigger qualification.

TRIGGER PATTERN SELECT U17. Trigger select lines LE1-4 select a combination of the buffered TCLK1-4 signals. The TCLKB and LTCLKB signals, which are logically equivalent to the TCLK signal, are used for event-delay and pattern present modes of trigger qualification.

Section 4

SLOT ID. U49 is a 4 bit comparator which compares address lines A19-22 with slot ID codes ID0-3. The slot is made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U49 output goes high, enabling other circuitry.

DTACK LATCH. When this assemblyd is addressed, the latch enables function decoder U47 and bus transceiver U50. The latch also sends out LDTACK over the SIB.

FUNCTION DECODE. Decodes R/LW, A1 and A15 to enable various functions on this assembly.

TRIG INPUT OVERLOAD CIRCUIT. Lines from the TRIG 3 and TRIG 4 attenuators monitor the signals on the 50Ω input termination resistors. If the signals are too high, overload comparators provide an interrupt to the microprocessor over the IRQ2 line and a flag onto the data bus. When the voltage returns to within limits, the microprocessor sends a clear signal through U47 which resets the circuit.

TRIGGER TEST. The complementary trigger outputs from the attenuators, LTCLK1-4, are used for internal testing. A simulated signal is generated in the attenuator circuitry. The trigger test comparators sense activity on the trigger lines and the output of the comparators is

read by the microprocessor. This provides additional information for fault location.

STATUS/BOARD TYPE. U51 and parts of U46 function to read status lines or board type onto the data bus. One output of the decoder U47 enables reading status, another enables reading board type. The status lines read are LTRIGQUAL, TRIG 3/TRIG 4 probe IDs, and input overload. A sense ring on the TRIG 3/4 input BNCs pulls the ID line down when a standard 10:1 probe is installed. The instrument automatically adjusts triggering factors for the 10:1 probe.

LATCHES AND LEVEL SHIFT. This circuitry controls and loads data into the time and event qualifying circuitry. It is an interface between the TTL bus interface and the ECL and CMOS circuitry it drives. It also isolates the controlled circuitry from the bus environment. The outputs are serial data, two clocks, and two control lines.

POWER SUPPLIES. The power supplies and decoupling isolate the trigger qualifier circuitry from the SIB power buses.

Section 2

MODE CONTROL LOGIC. This circuitry controls the set-up of the various resources available for trigger qualification. To control the set-up the microprocessor loads 45 bits of serial data through shift registers U36 and U37 (section 1) and shift register U38 and counter U26 (section 3). Mode control logic set-up is loaded through shift registers U36 and U37.

100 MHZ TRIGGER. Dual D flip-flop U19 is used to start the 100 MHz oscillator and 29-bit counter when they are used in time delay or event delay modes.

STARTABLE OSCILLATOR This 100 MHz oscillator is used as a reference for delay-by-time and pattern present-for-time functions.

TRIGGER SELECT AND DRIVERS. OR/AND gate U7 selects the desired source for the qualified trigger in state and event delay modes. In time delayed modes the output of U8 is the source. The Outputs of U7 and U8 are ORed (effectively) and used to drive common-base transistors Q6 and Q12 which drive the TRIGQUAL (D) and LTRIGQUAL lines respectively.

Section 3

Section three, a 29-bit counter, is a subfunction of section two. It is a 150 MHz counter used for counting time or events in various trigger modes. It is comprised of a one-bit, a four-bit, and a 24-bit counter. For short counts, the microprocessor uses the control lines to disable unneeded sections of the 29-bit counter.

RESTART CIRCUIT. With the restart circuit set, the counter always starts at the beginning of the count sequence, regardless of the previous state of the rest of the logic. This gives a 10 ns reload time.

CONTROL LOGIC. The control logic selects the counters to be used for the division ratio.

PRESCALER. The prescaler U23B allows a quick response when the count is from 1 to 4 It is only one bit, but counts 3 and 4 are accomplished by how it is set up.

4-BIT COUNTER. The 4-bit counter, with the prescaler, is used from counts 5 to 36. The 24-bit counter takes too long to load for these counts.

24-BIT COUNTER. The 24-bit counter, with the other counters, is used for counts greater than 36. In this mode all counters are running.

OUTPUT F-F U20A. The output flip-flop provides a pulse with a duration dependant on the counting time.

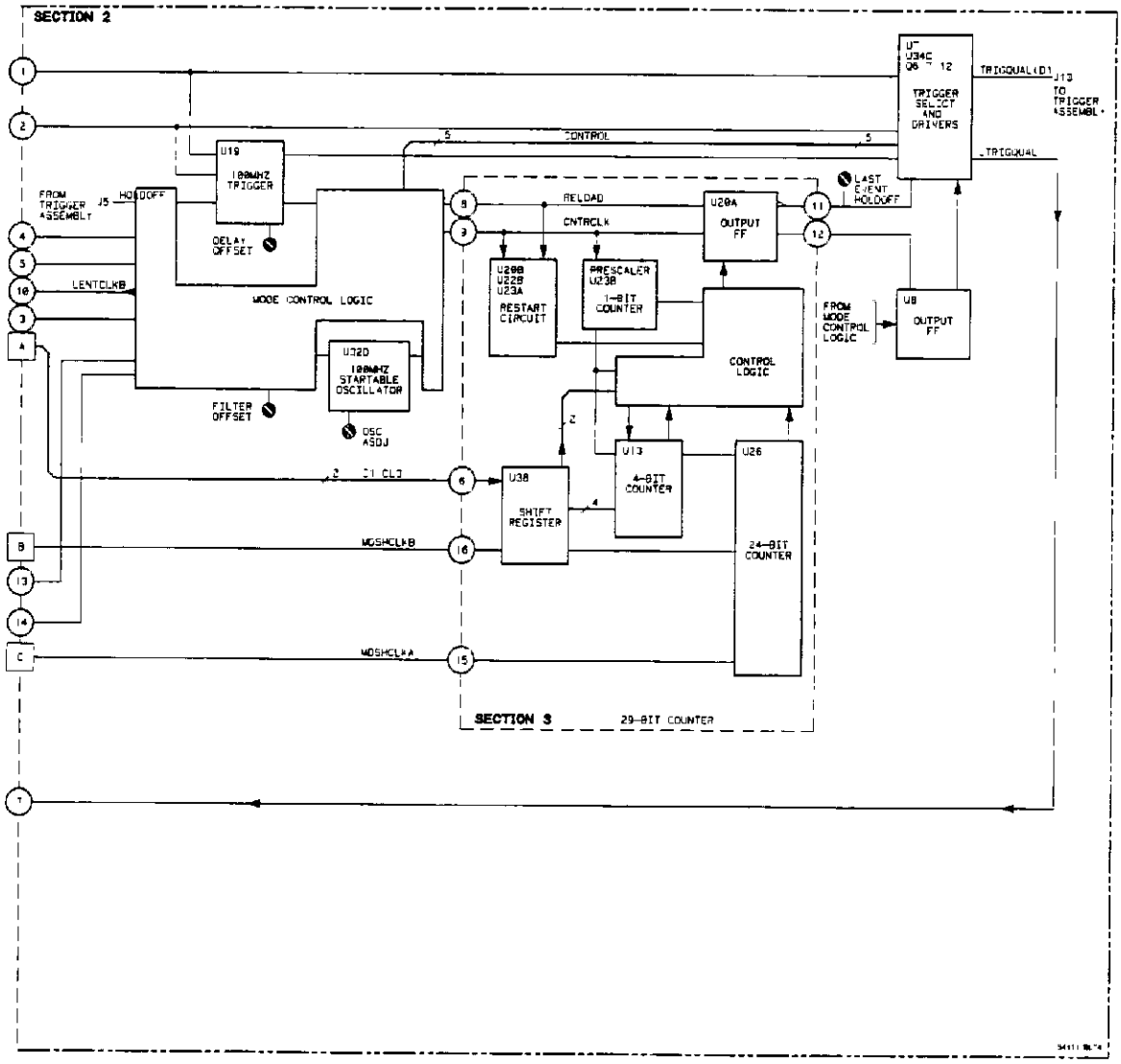


Figure 6B-13. Trigger Qualifier Assembly Block Diagram (part 2)

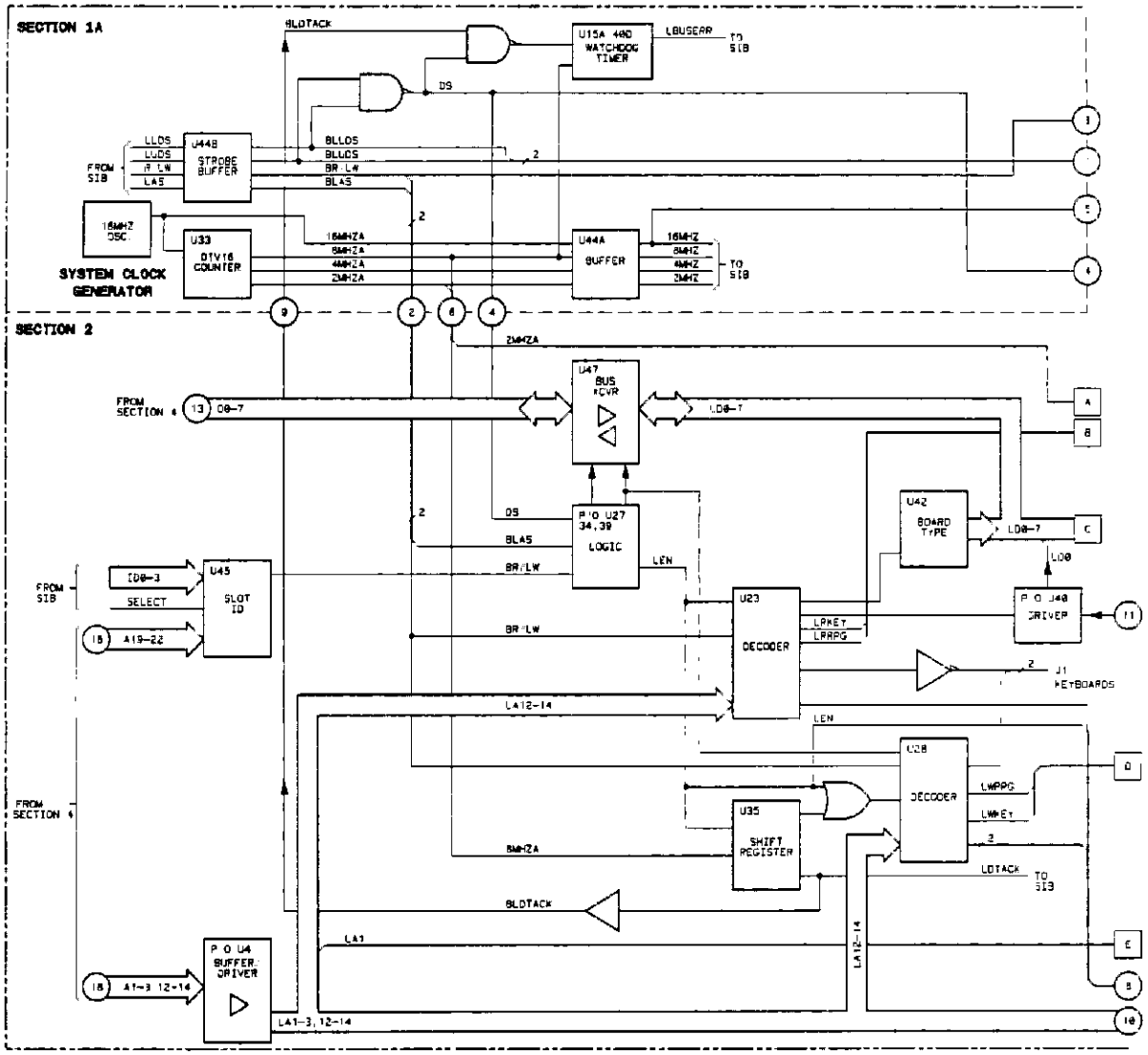


Figure 6B-14. I/O Assembly Block Diagram (part 1)

6B-15. INPUT/OUTPUT ASSEMBLY THEORY

The I/O assembly serves several purposes. First it provides instrument interface to keyboard and HP-IB through ribbon cables. It provides 256K words of dynamic RAM for waveform storage and other purposes. It provides several system functions, all of which are described below. In addition the I/O provides passive pull-up resistors for data, address, and control lines for the System Interface Bus, (SIB).

Use the I/O Assembly Block Diagram for the following discussion. The block diagram is laid out in five sections, corresponding to the five schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

Section 1A

STROBE BUFFER. Buffer U44B provides increased fan-out for the data and address strobes and the read/write line.

SYSTEM CLOCK GENERATOR. A crystal controled 16 MHz oscillator supplies the system clock. A binary counter divides this down into 8 MHz, 4 MHz and 2 MHz. All four signals are buffered onto the System Interface Bus (SIB).

WATCH DOG TIMER. Under normal operation U18 should be reset by LDTACK before a time constant set by R19 and C40 times out. If U18 is not reset it generates LBUSERR which keeps the microprocessor from getting hung up in an instruction cycle. This could happen if any addressed assembly does not generate LDTACK or if the microprocessor tries to access a nonexsistent assembly.

Section 2

SLOT ID. U45 is a 4 bit comparator which compares address lines A19-22 with slot ID codes ID0-3. Slots are made unique by grounding appropriate pins at the mother board connector. Slots are numbered 0000 to 1001 from left to right. When the slot this assembly is in is addressed, the two codes are equal and U45 output goes high, enabling other circuitry.

BUFFER/DRIVER. Buffer/driver U46 buffers several of the address lines into the control circuitry on this assembly.

LOGIC CIRCUIT. The logic circuit of parts of U27, U34, and U39 use several signals to control read and write functions.

BUS TRANSCEIVER. U47 buffers data off of and on to the SIB.

BOARD TYPE. When board type is requested by the microprocessor, this assembly responds with a code over the data bus. The input pins of buffer U305 are encoded with the board type. Enabling U305 reads the code.

DRIVER U40. U40, under control of read decoder U23, buffers the power test signal onto the local data bus.

DECODERS. Decoders U23 and U28 decode address lines LA12-14 to provide enables for the various functions on the I/O assembly. U23 provides read enables and U28 write enables.

SHIFT REGISTER. U35 generates LDTACK which is sent back to the microprocessor indicating data was received. This signal also resets the watchdog timer (section 1). Another signal from U35 helps enable the write decoder U28.

KEYBOARD CONTROLLER. U21 sees a keyclosure and interrupts the microprocessor by IRQ4 line. U21 detects which key was pressed by scanning column lines with pulses and sensing rows for a return path. U21 converts key closure scan data to parallel data and places this on the local data bus when enabled.

KEYBOARD DMUX. This demultiplexer drives the keyboard columns using the three scan lines out of the keyboard controller.

RPG READ. The RPG outputs two out-of-phase pulses. Direction of rotation is determined by the difference in phase angle

between both pulses. The pulse frequency is a function of rotation speed and this tells the microprocessor what size of incremental steps to take. Part of U13 detects RPG activity, and interrupts the microprocessor by IRQ3 line.

Section 1B

HP-IB. U1 interprets HP-IB commands and controls direction of data flow from an external controller to local data bus. One side of U1, LD0- 7, connects to the local data bus. The other side of U1 connects to two bidirectional data transceivers, U4 for data and U5 for control commands. The data transceivers buffer between the HP-IB and the HP-IB controller.

Section 3

POWER TEST. The power test circuitry monitors all six supplies on the SIB. The CPU reads the output of this circuit during self test.

POWER ON RESET. Power on reset circuit provides a glitch-free pulse shortly after power up and power down. This sets many devices to a known state and prevents the microprocessor from taking damaging action during power up. A pushbutton switch also provides a manual means to reset the system without powering down the instrument.

BATTERY CIRCUITS. A battery provides power for the non-volitile RAM memory on the microprocessor assembly. It can retain basic setup information and system configuration for several years. The circuit also keeps the battery charged and provides for smooth transfer of power from battery to power supplies after power up.

Section 4

Section four is comprised of the control circuitry for the dynamic RAM. Dynamic RAM is addressed in rows and columns and must be refreshed to maintain memory.

RAM ID. From the CPUs perspective the dynamic RAM is a "slot" by itself, irrespective of the slot for the I/O assembly. The other assemblies are IDd by the slot ID code. U51 is a 4 bit comparator which compares address lines A19-22 with code 10 decimal which is hard-wired on the other comparator input. The CPU sees the dynamic RAM at "slot" 10 no matter which slot the I/O assembly is in.

BUS XCVRS. The bus transceivers and associated logic buffer data between the dynamic RAM and the SIB.

COLUMN STROBES. The column strobes and associated ciruitry provides the column address strobes, LCAS1-8, for the dynamic RAM.

ROW STROBES. The row strobes and associated ciruitry provides the row address strobes, LRAS1-4, for the dynamic RAM.

ADDRESS MUX. U30 and U38 multiplex 16 of the SIB address lines into the eight memory address lines of the dynamic RAM.

CONTROL AND REFRESH. The control and refresh circuitry provides the necessary timing to write and read from memory while keeping the memory refreshed at the proper interval.

REFRESH COUNTER. The refresh counter activates the memory address lines during the refresh cycle.

Section 5.

Section 5 consists of an array of 16, 64K by 4 bit dynamic RAMs. The addressing and refresh circuitry is covered in section 4.

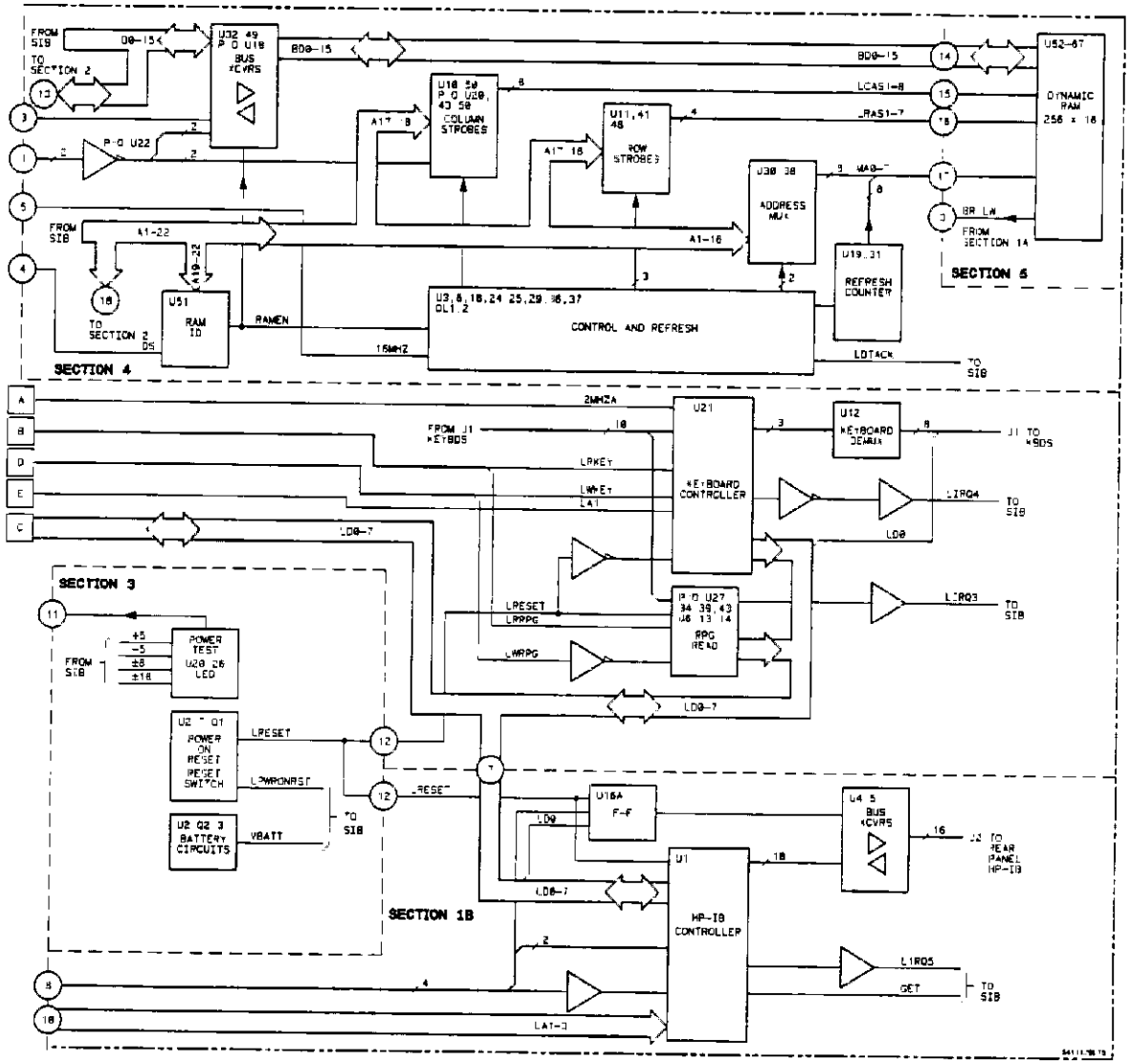


Figure 6B-15. I/O Assembly Block Diagram (part 2)

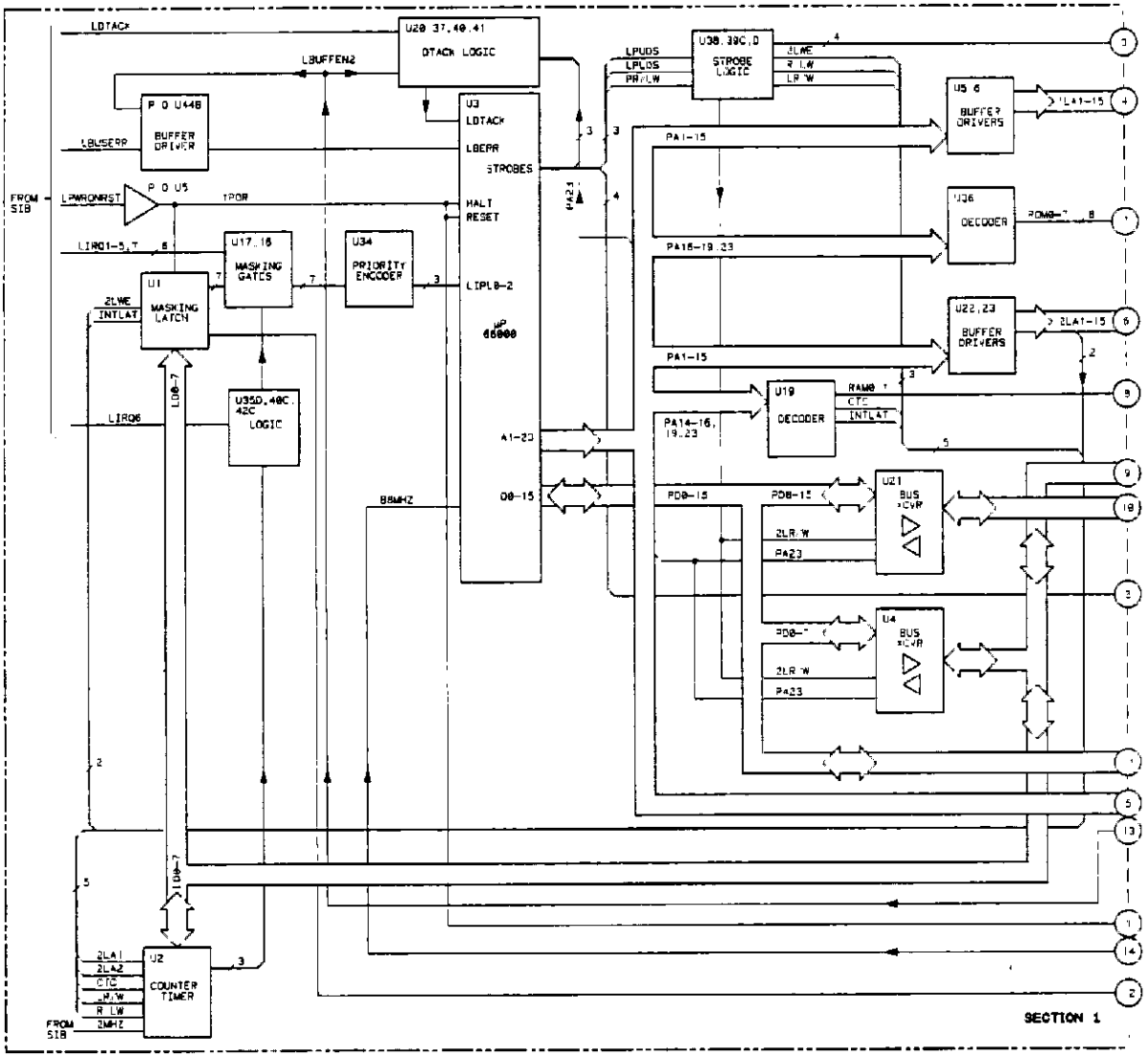


Figure 6B-16. Microprocessor Assembly Block Diagram (part 1)

6B-16. MICROPROCESSOR ASSEMBLY THEORY

The Microprocessor assembly controls the operation of the instrument. At initial power up, power on reset insures the μP starts up in a known condition. The μP then runs several routines, some of which are: determine which assembly is in which slot, system self diagnostics, and setup display information. The μP then responds to system interrupts, HP-IB, keyboard, or RPG.

Use the Microprocessor Assembly Block Diagram for the following discussion. The block diagram is laid out in three sections, corresponding to the three schematic diagrams in the Service Data Supplement. The circled numbers correspond to the interconnections between schematics. The discussion is covered here by sections.

To the μP, all system assemblies look like memory locations. Address line A23 separates local memory from system memory. When A23 is high system memory is being accessed over the SIB. When A23 is low local processor memory is being accessed. After the μP sends data over the SIB, LDTACK comes back from the addressed assembly, which tells the μP the information was received. This LDTACK also goes to the I/O assembly and resets the watchdog timer. If the watchdog timer is not reset, then BUSERR is sent to the μP which displays an error message on the CRT.

The μP starts a data acquisition cycle by setting a bit on the Timebase assembly. When the acquisition cycle is finished, the microprocessor moves data from ADC memories to display memories. The microprocessor does signal post-processing, making measurements on the signal and digital signal filtering, averaging, etc.

Section 1

μP. The Motorola 68000 microprocessor runs at 8 MHz. Main characteristics are: 16 bit data bus, 23 bit address bus, and 3 interrupt lines.

INTERRUPT CIRCUITRY. The μP communicates with the bus through the interrupt circuitry. Any of the seven interrupt lines on the SIB can be masked by the μP.

Counter/Timer. The counter/timer contains three programmable counters. It is used primarily as a time-out device. The microprocessor programs and reads each counter over LD0-7 lines. Each counter has an output which is used as an interrupt to the microprocessor. All three counter outputs are ORed through U35 and U42. This result, through U40, shares an interrupt line with LIRQ6 from the SIB.

Masking Latch. The masking latch latches data from LD0-7 to set masks on the seven interrupt lines. The output of the latch is OR'ed with the interrupt so a high out of the latch masks the interrupt signal.

Masking Gates. The gates of U17 and U18 OR the interrupt with the output of the masking latch. A high from the latch masks the interrupt.

Priority Encoder. Encodes all seven incoming interrupt lines into three lines for the microprocessor. If more then one interrupt occurs at the same time, U34 prioritizes them so the interrupt with the highest priority is processed first. When an interrupt occurs, the system is vectored to a predetermined firmware location.

STROBE LOGIC. The strobe logic combines the upper and lower data strobes and read/write from the microprocessor into read and write enables for local use.

BUFFER DRIVERS. Buffer/drivers U5, 6, 22, and 23 drive the ROM and RAM with address lines LA1-15. U22 also provides 2LA1 and 2LA2 to the counter/timer.

DECODERS. U19 and U36 decode certain address lines into RAM and ROM select lines. U19 also provides two control lines to the counter/timer.

BUS TRANSCEIVERS. Bus transceivers U4 and U21 control read and write to the ROM and RAM on the microprocessor assembly.

Section 2

Section two covers the μP ROM and RAM. The ROM and RAM ICs have 8 bit data lines. To acheive 16 bit data words, 16 bit words are divided into a lower portion LD0-7, and an upper portion LD8-15. ROMs or RAMs are read in pairs.

Firmware instructions for the μP are contained in ROM memory. There is space for eight ROM pairs, but some instruments may use fewer ROMs.

The non-volatile battery backed-up RAM contains stack registers, status registers, scratch pad memory, and soft cal information. Several setup registers save front panel setup information.

Section 3

BUS ARBITRATION LOGIC. The microprocessor assembly contains circuitry so it can operate in a multiprocessor system. With only one microprocessor being used, bus request and bus grant signals are tied to the proper logic levels to ensure this board has control over the SIB when required.

BUFFER DRIVER U44. U44B buffers the upper and lower data strobes and the address strobe onto the SIB.

BUS TRANSCEIVERS. The bus transceivers, U48 and U49, interface the microprocessor data bus and the SIB data bus.

BUFFER/DRIVERS U45-47. These buffers isolate the microprocessor address bus from the SIB address bus. LIACK, interrupt acknowledge, and R/LW are buffered by U45.

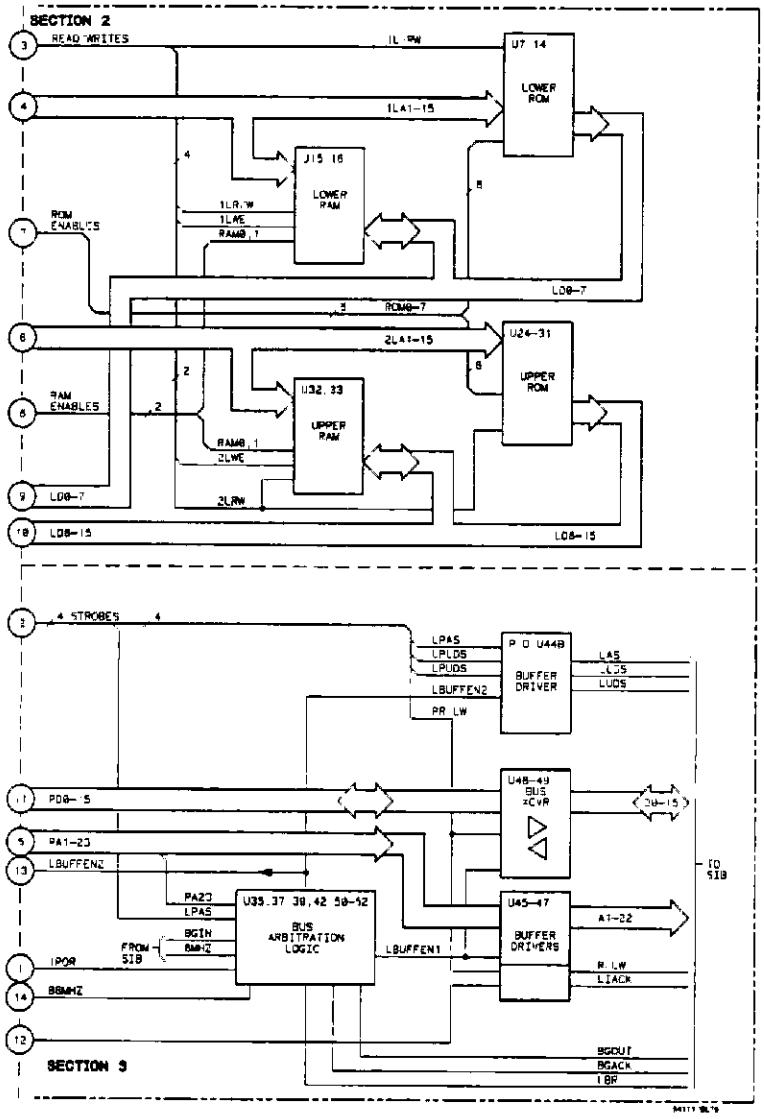


Figure 6B-17. Microprocessor Assembly Block Diagram (part 2)

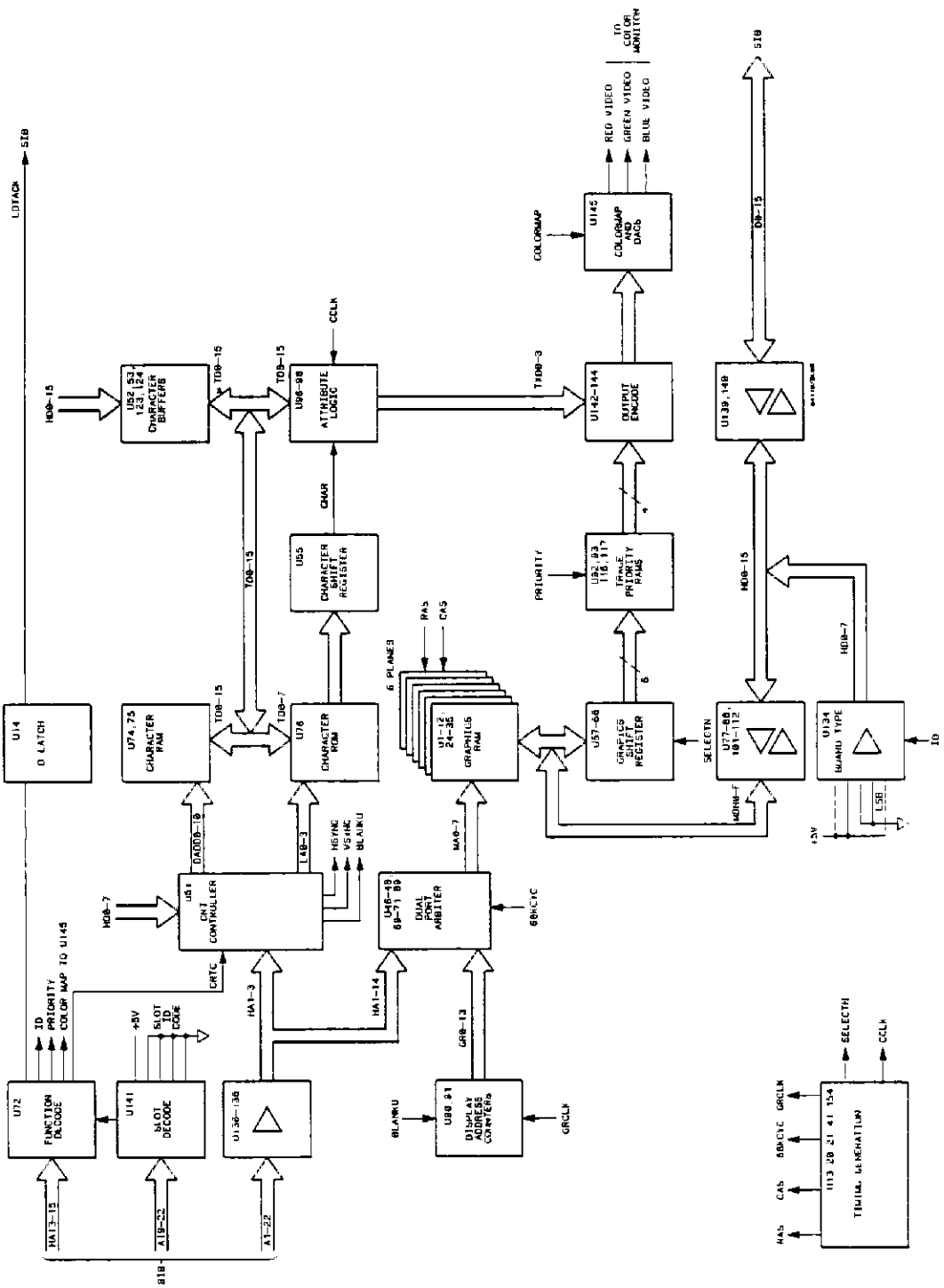


Figure 6B-18. Color Display Assembly Block Diagram

6B-17. COLOR DISPLAY ASSEMBLY THEORY

This assembly is the interface between the microprocessor and Color CRT Module. It contains graphics memory, timing generator, character generator, prioritization circuitry, color map, and output DACs.

TIMING GENERATION. Controls timing functions for the Color Display assembly.

FUNCTION DECODER. Decodes HA13-15 to enable various board functions, these are: CRTC for the CRT controller, ID for board type, COLOR MAP for the color map and output DACs, priority for RAM.

D LATCH. Outputs LDTACK over the SIB, indicating data was accepted.

SLOT DECODE. A 4 bit comparator, U141, compares slot address lines A19-22, to the slot ID code hard wired on the board. When board is addressed, the codes are equal and U141 helps enable the function decoder.

CRT CONTROLLER. Controls timing signals for the Color Display Module, blanking, horizontal and vertical drive, and character control.

CHARACTER RAM. Characters are stored here as 16 bit words, 8 bits for the character and 8 bits for character attributes.

Bit number	Function
TD0-6	ASCII character
TD7	Not used
TD8	Inverse video
TD9	Blink
TD10	Underline
TD11-14	Color
TD15	Priority bit

CHARACTER ROM. Functions as a character generator by decoding ASCII data, TD0-7, from character RAM.

CHARACTER SHIFT REGISTERS. Converts parallel character data to serial character video.

ATTRIBUTE LOGIC. Converts TD8-15 to attributes, 4 bits for color and 4 bits for other attributes. Above table defines these bits.

DISPLAY ADDRESS COUNTERS. 4-bit counters which generate address lines GA0-13.

DUAL PORT ARBITER. Outputs addresses from either the host microprocessor or an outside controller to place graphics on screen.

GRAPHICS RAM. Six planes of dynamic memory which store graphics data.

Plane	Information
0	Graticules
1	Stored Traces
2	Channel 1
3	Channel 2
4	Not Displayed
5	Not Displayed

GRAPHICS SHIFT REGISTERS. Parallel loaded with graphics data and serially outputs graphics video.

TRACE PRIORITY RAM. A high speed RAM which maps outputs from the graphics planes into unique address locations for the color map. It also provides arbitration when more then one plane tries to illuminate the same pixel location Plane 0 has the lowest priority and plane 3 the highest. Planes 4 and 5 are scratch pad memory and not displayed, so have no priority significance.

OUTPUT ENCODE. Generate addresses for the color map using graphics data or character and attribute data

COLOR MAP AND OUTPUT DAC. Three RAMs convert encoded addresses to a digital color value: red, green, or blue. There is one output DAC for each RAM. The output DACs convert the digital value to red, green, or blue levels for the Color CRT Module.

BOARD TYPE. When the microprocessor requests board type, this buffer is enabled and the response is "25" over the LD0-7 lines.

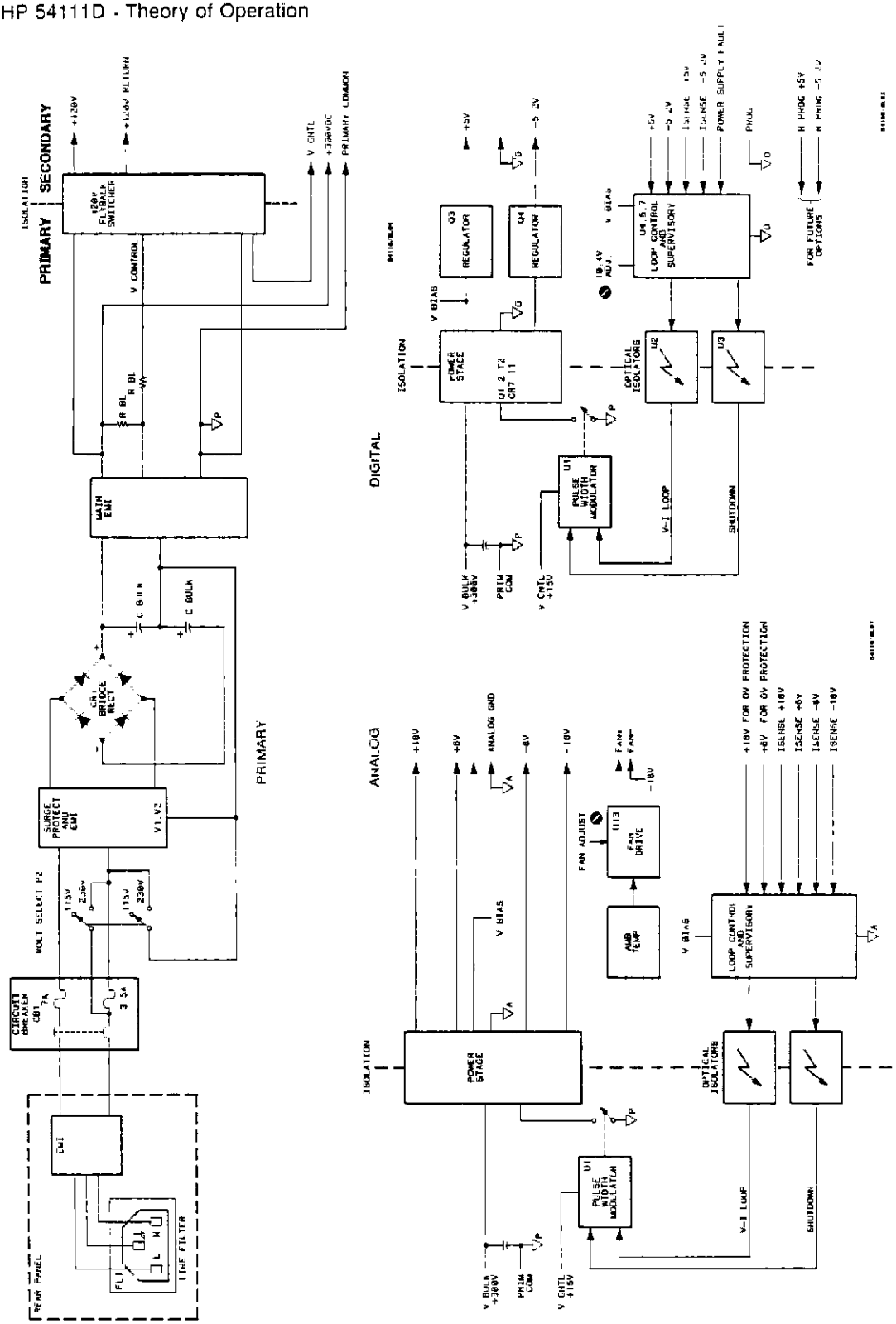


Figure 6B-19. Power Supply Block Diagrams

6B-18. POWER SUPPLY THEORY

6B-19. Primary Power Supply

The primary board rectifies and filters the input ac voltage. When the voltage select switch is in the 230V position, the ac is bridge rectified and filtered to yield approximately 300V dc and 120V dc. 120V dc is generated by an isolating switching regulator, and is used to power the color monitor. 300V dc is used for the digital and analog supplies. The input voltage is doubled in the 115V position to yield the same dc voltages.

The primary board has surge protection circuitry that protects against ac line voltage transients and current surges. Over voltage crowbar devices trip the circuit breaker for sustained input over-voltage conditions.

The pulse width modulator (PWM) circuitry is powered by a bleeder resistor on one of the bulk storage capacitors. The main EMI (electromagnetic interference) filter is located in a dc current path to reduce component size and to increase effectiveness of the filter.

6B-20. Digital Power Supply

The digital power supply is a dc to dc converter which converts 300V dc to +5V and -5.2V dc.

PULSE WIDTH MODULATOR (PWM). Is used to achieve voltage and current regulation by changing the PWM's turn-on time. It has an operating frequency of 68 kHz.

POWER STAGE. Performs the actual conversion of 300V dc to +5V and -5.2V dc. Digital and primary ground planes are kept isolated through transformer T2.

OPTICAL ISOLATORS. Isolates the primary and digital ground planes. Voltage and current feedback control is sent through U2, to control the duty cycle of the PWM. Power supply shutdown is sent through U3.

LOOP CONTROL AND SUPERVISORY. When excessive output voltage is detected, circuitry sets a latch in the PWM which can only be reset by cycling the circuit breaker off for 60 seconds, or an instantaneous reset by cycling the front panel power switch. Circuitry also senses the current and activates foldback current limiting for excessive current loading.

6B-21. Analog Power Supply

The analog power supply is a dc-to-dc converter which converts 300V dc to +18V, +8V, -8V, and -18V dc.

PULSE WIDTH MODULATOR (PWM). Is used to acheive voltage and current regulation by changing the PWM's turn on time. It has an operating frequency of 68 kHz.

POWER STAGE. Performs the actual conversion of 300V dc to +18V, +8V, -8V, and -18V dc. Plus a fan drive output that increases fan speed with ambient temperature. Analog and primary ground planes are kept isolated through transformer T2.

OPTICAL ISOLATORS. Isolates the primary and analog ground planes. Voltage and current feedback control is sent through U2, to control the duty cycle of the PWM. Power supply shutdown is sent through U3.

LOOP CONTROL AND SUPERVISORY. When excessive over-voltage is detected, circuitry sets a latch in the PWM which can only be reset instantaneously by cycling the front panel power switch to standby and then to on, or by turning the circuit breaker to the off position for 60 seconds. +18 volts is regulated and the other outputs are semi-regulated outputs which follow the +18 volts. Each output is current limited. The -8 volt output has foldback current limiting.

NOTES

SECTION 6C
SERVICE MENUS/KEYS

6C-1. INTRODUCTION

This section describes the service menus and keys that are available for calibration, troubleshooting and CRT display alignment. A basic understanding of these will be helpful in troubleshooting failures, however, Self-Test and Troubleshooting is covered specifically in Section 6D.

6C-2. SERVICE MENUS

The service menus are part of the Utility menu, in the second level of the menu softkeys. Once Utility is pressed, six function keys will be displayed: Probe Menu, HP-IB Menu, Cal Menu, Test Menu, Color Menu, and CRT Setup Menu.

PROBE MENU. The Probe Menu is used to set the attenuation factor before the input of the instrument. This sets the instrument scaling factors for a special probe or other device. This is not a service menu though the functions may be used during service procedures. Further use of this menu is covered in the Operating and Programming and other user manuals.

HPIB MENU. The HPIB Menu provides keys that are used to set the HPIB attributes. These attributes are address number, Talk/Listen, and EOI. This menu is discussed in detail in the Operating and Programming and other user manuals.

CAL MENU. The Cal Menu is used to calibrate the instrument. The calibration factors are stored in non-volitle memory. Use of this menu is covered in the *HP 54111D Operating and Programming Manual.* Basic functions of the Cal menus are covered in this section.

TEST MENU. The Test Menu provides several functions used to set up and run internal diagnostics test and view the results. Use of these functions is covered briefly in following paragraphs and comprehensively in the Self-Tests/Troubleshooting, section 6D.

COLOR MENU. The Color Cal Menu provides functions used to set the characteristics of the colors displayed. These characteristics include hue, saturation, and luminosity. This menu is covered in detail in the Operating and Programming and other user manuals.

CRT SETUP. The CRT Setup Menu provides several functions that provide confidence testing as well as test patterns for adjusting the Color CRT Module. These functions are discussed in following paragraphs.

6C-3. ONE-KEY POWER UP

A one-key power up is often performed to return the instrument setup to default conditions. This is done as follows:

1. Set the front panel POWER switch to STBY,
2. Press and hold one front panel key,
3. Turn front panel POWER switch to ON.
4. Release key when display shows "Powerup Self Test Passed!" or Failed.

6C-4. TWO-KEY POWER UP

CAUTION

Using the two-key power up will leave the instrument uncalibrated. Effort needed for recalibration should be considered before using this mode to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.

A two-key power up is a basic reset of the entire operating system of the HP 54111D. All volatile and non-volatile RAM is cleared. As a result, all calibration factors are purged and the instrument must be recalibrated.

All calibration except the Timebase Cals can be done with just the front panel CAL signal and the self-cal menus. For further information about Timebase Cal read later paragraphs in this section. The two-key power up is performed in much the same way as the one-key power up.

1. Set the front panel POWER switch to STBY.
2. Press and hold the top and bottom keys in the group at the right edge of the display.
3. Turn front panel POWER switch to ON.
4. Release keys when display shows "Powerup Self Test Passed!" or Failed.

6C-5. CAL MENUS

6C-6. ADC Reference Cal

ADC Reference Cal calibrates the comparator stick references in the ADC hybrid (see theory of operation). Since the ADC is composed of four separate convertors, they must calibrated so they all convert the same input voltage to the same digital value. If they do not, the digitized input will appear in the display as two or more traces.

ADC Reference Cal can be set to manual or automatic modes. It can be performed at any time by pressing ***ADC Reference Cal*** in the Cal menu. It is also done automatically as part of the Vertical Cal.

See the *HP 54111D Operating and Programming Manual*, the chapter on utility menus, for further information about this function.

ADC Reference Cal uses internal hardware to provide a level for digitizing.

6C-7. Probe Tip Cal

The Probe Tip Cal uses a triggering technique to measure where the CAL signal from the front panel triggers the system. The front panel CAL signal is calibrated independently from the operating system. The cal factors are stored and used to manipulate acquired data.

The vertical specifications of the HP 54111D are based on calibration of the vertical system through the probe. Changing the probe at an input nullifies the calibration of that channel or trigger. Restoring calibration at that input requires a Probe Tip Cal of that input.

Use of Probe Tip Cal in service procedures is accompanied by instructions appropriate to the procedure. Other information about Probe Tip Cal can be found in the Utility Menu chapter of the *HP 54111D Operating and Programming Manual*.

6C-8. Vertical Cal

Vertical Cal sets gain and offset coefficients in firmware for vernier control. Front panel inputs aren't needed. Internal signals are supplied through an internal input to the attenuator preamp.

6C-9. Trigger Cal

Trigger Cal is a trigger level and sensitivity calibration. There are no input signals used for this calibration and the user needs only to follow the prompts on the screen to remove any signals before the routine is run.

The firmware sets the trigger level and hysteresis (sensitivity).

6C-10. Timebase Cal

6C-11. CHANNEL SKEW

Channel Skew compensates the time differences between the channel displays and triggers. A common signal is applied to the CHAN 1 input and the other inputs, CHAN 2, TRIG 3, and TRIG 4 in turn. A measure routine finds the edges of the signals, and the time difference between them is stored and used to time-align displayed signals and triggers.

For the vertical channels, the reference points are the offset voltage (vertical center screen) for the displayed signals and the trigger levels for the triggers.

For the trigger channels, the reference is the trigger level.

The procedure for this calibration is covered in the Adjustment procedures, the *HP 54111D Operating and Programming manual*, or you can follow the prompts on the display in the Channel Skew menu.

6C-12. TIMEBASE FREQ CAL

Timebase Frequency Cal is used to improve the accuracy of the instrument timebase. The timebase reference is a 1.001 GHz oscillator. It sets the sample rates for acquisition, and is therefore the timing standard in the instrument.

By measuring this frequency, and entering the measurement at the menu provided, the firmware in the instrument can compensate timing measurements for any error in the oscillator.

Restoring Timebase Frequency Cal may require using a traceable frequency counter if instrument use warrants it. If the cal factor was recorded when the instrument was last calibrated, calibration can be restored by re-entering the cal factor. If the cal factor is not known it is necessary to re-measure the Timebase Cal signal and enter the new value. Use the procedure in this section or follow the directions in the Timebase Freq Cal menu of the instrument.

The frequency measured is nominaly 50.05 MHz, the timebase reference divided by 20. When the Timebase Freq Cal menu is entered the signal is provided at a rear panel connector. The exact frequency should be measured with an accurate frequency counter and the resulting value entered in the menu.

The procedure for this calibration is covered in the Adjustment procedures, the *HP 54111D Operting and Programming Manual*, or you can follow the instructions in the Timebase Freq Cal menu.

6C-13. TEST MENU

Five sub-menus are available when the Test Menu is selected. The menus allow the user to access and run internal diagnostics and view the results. In addition, the position of each of the printed circuit boards located in the main card cage can be read and displayed.

Use of the test menus is covered in depth in section 6D, Troubleshooting.

6C-14. Repeat Loop/Run From Loop

The top key toggles between REPEAT LOOP and RUN FROM LOOP. These keys in conjunction with Loop # = [0-80], # Repetitions = [1-1000 or Infinite], and Start/Stop Test key will execute internal self-test diagnostic routines. All input signals must be disconnected from the instrument for these tests.

REPEAT LOOP. Selecting this mode will continuously execute the Loop # entered at RUN FROM LOOP. Pressing ***Start Test*** will start execution and the loop will continuously run until the ***Stop Test*** key is pressed. Pressing ***Display Errors*** will show how many times the loop was executed and the number times the loop failed.

Entering a value in # Repetitions will cause the firmware to run the designated loop that many times and stop. Start the test at REPEAT LOOP.

There are a number of loops that will blank or over-write the Stop Test key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

RUN FROM LOOP. Selecting this mode will start execution from the loop entered and will proceed to execute all higher numbered loops. Upon reaching the last test, the cycle will be repeated.

If any test should fail, the instrument will change from RUN FROM LOOP to REPEAT LOOP and will repeatedly execute the loop that failed.

Starting tests at RUN FROM LOOP will set the number of repetitions (entered at REPEAT LOOP) to infinite.

6C-15. Extended Tests

When this key is pressed, one of twenty-one internal instrument tests may be selected by entering the test number with the entry devices. The tests are numbered 0 through 20. All input signals must be disconnected from the instrument for these tests.

Many of the extended tests are useful only at the factory. Those that are of use to field service personnel are covered in the troubleshooting in section 6D.

6C-16. Start/Stop Test

This key is used to initiate any test where a test number is entered by one of the entry devices. Once the test number is entered, pressing ***Start Test*** initiates the test and the key toggles to ***Stop Test***. Pressing ***Stop Test*** stops the test in progress and the key toggles back to ***Start Test***.

A number of tests will blank or over-write the ***Stop Test*** key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

6C-17. Display Errors

Pressing this key will display the number of any loops which failed while one of the following tests was run:

- Powerup self test
- INTERFACE tests
- REPEAT and RUN FROM LOOP tests
- HP-IB commanded self test

This display shows the current loop or last loop executed, the number of times the loop was executed, and the number of times that it failed. The bottom portion of the display shows all loops that failed starting with the first loop failure.

The four STATUS x = xxxxx lines in the Display Errors field are primarily for factory use. Any field usable information in this part of the display is covered in the troubleshooting, section 6D.

To return to the Test Menu, press ***Exit Display Menu*** key.

6C-18. Display Configuration

Most major assemblies used in the HP 54111D have circuitry allowing them to be interrogated directly by the microprocessor. The exceptions are the Analog to Digital Converter (ADC) assemblies. The HP 54111D card cage has 9 slots. When ***Display Configuration*** is pressed, the resulting display shows the location of card cage assemblies, except the ADCs. The Microprocessor assembly will not be noted on the display either.

The display also shows the firmware date, such as Wed April 22 09:07:02 MST 1987.

To return to the Test Menu, press ***Exit Display Menu*** key.

6C-19. CRT SETUP MENU

When CRT Setup Menu is selected, four keys are displayed that allow access to CRT setup displays. The keys available are, from top to bottom, Confidence Test, Pattern Off, Light Output Off, Color Purity Off, and at the bottom, Exit CRT Setup Menu.

Even though some of the patterns overwrite the key display, the functions can be selected The bottom key can be pressed at any time to exit the CRT Setup Menu.

6C-20. Confidence Test

This function displays a three-part confidence test pattern. At the top of the screen is a complete character set, in the center is a group of seven color blocks, and at the bottom a seven block grey-scale.

The top four lines of the character set display include the complete character set. The bottom line displays three sets of numerals The first set is displayed in inverse video, the second set flashes between normal and inverse video and the third set is normal video and underlined.

The seven color blocks displayed at the center are, from left to right; beige, grey, red, yellow, green, amber, and cyan.

NOTE

Since color perception is subjective, any slight variation in colors from what is described here should be disregarded.

At the bottom of the CRT a seven block grey-scale is displayed, with increasing luminosity from left to right. This grey-scale display is used if Color CRT Module adjustments are necessary.

6C-21. Pattern

These patterns are used when Color CRT Module adjustments are necessary. When CRT Setup Menu is selected, this key is initially ***Pattern Off***.

Pressing ***Pattern Off*** once will display a white cross-hatch pattern over the entire CRT and the Pattern Off key changes to Pattern White. Inside the cross-hatch pattern there are dots at the center, corners, and at the 12, 3, 6 and 9 o'clock positions. Additionally, there are test matrices in the center and corners.

Pressing ***Pattern White*** key changes the pattern color to red and the key changes to Pattern Red. Successive pressings of this key will change the color of the pattern to green then blue, the name of the Pattern key is the color displayed.

Pressing ***Pattern Blue*** key changes the display to the white cross- hatch pattern on the top half of the CRT and white with a dark cross-hatch on the bottom. The key then changes to Pattern HV Reg. This test is used primarily by the factory, however it may indicate the need for service if there are severe high voltage problems.

Pressing ***Pattern HV Reg*** changes the display to a solid white screen with dark cross hatch lines. The key changes to Pattern I White. Successive pressing of this key changes the color to red, green and then blue, the name of the Pattern key is again the color of the display.

Pressing ***Pattern I Blue*** changes the display to a white cross- hatch pattern with the inside flashing between solid white and cross- hatch. The key changes to Pattern Bounce. This test is primarily used by the factory, however, it may indicate the need for service if there are severe high voltage problems.

Pressing ***Pattern Bounce*** exits this set of tests and returns the CRT Setup Menu.

6C-22. Light Output

These displays are used by the factory.

Pressing ***Light Output White*** displays a horizontal band of white half the height of the display. The key display is not overwritten. Successive pressing of this key will change the color of this band to red, green, blue and then a grey-scale. Each time the key is pressed it also changes to the appropriate description.

Pressing ***Light Output Grey-Scale*** exits this set of tests and returns the CRT Setup Menu.

6C-23. Color Purity

Pressing ***Color Purity Off*** displays a full white raster. Successive pressing of this key changes the color of the raster to red, green and then blue. At each color display the name of the key changes to the appropriate description. These displays are used when Color CRT Module adjustments are necessary.

Pressing ***Color Purity Blue*** exits this set of tests and returns the CRT Setup Menu.

NOTES

SECTION 6D
SELF-TESTS/TROUBLESHOOTING

6D-1. INTRODUCTION

This section describes the self-tests and troubleshooting routines that service personnel can use to locate failures to the assembly level. A basic understanding of the service menus and keys will be helpful in troubleshooting failures and is covered specifically in Section 6C.

The material presented in this section is in only a general order of importance, or use. Depending on the problem encountered, troubleshooting may progress back and fourth within the section but should start with the Main Troubleshooting Procedure.

Following are the troubleshooting sections in order of appearance:

- Main Troubleshooting
- "No Display" Troubleshooting
- Power Supply Troubleshooting
- Color CRT Module Failure Isolation
- Firmware Troubleshooting
- Core Subsystem Troubleshooting
- Data Acquisition Troubleshooting
- Front End Troubleshooting
- Hints, Tricks, and Arcana

6D-2. FAILURE INDICATIONS

The majority of failures in the HP 54111D are initially indicated in one of several ways: improper display (blank, distorted, or random) on the CRT after power-up, the keyboard is locked after power up, or "Powerup Self Test Failed !" is displayed on the CRT.

Other failures may be apparent during normal operation, but most problems are caught by the internal self-test routines and will result in one of the indications mentioned.

Loop failures may occur occasionally due to system or environmental noise. This may result in intermittent power-up failure messages. Loops must fail a certain percentage of the time to be considered a true failure and must be specially tested if random failures are occuring. See Main Troubleshooting for further information and procedures.

NOTE

In addition to the front panel power switch (STBY), there is a main breaker power switch located on the rear panel. Before troubleshooting a "no display" failure, make sure the rear panel switch has not been inadvertently turned off.

6D-3. TEST EQUIPMENT REQUIRED

The HP 54100 Family Product Support Kit consists of assembly and cable extenders and other tools. Some of the parts in this kit are necessary for certain assembly level diagnostic procedures. These procedures aid in troubleshooting, but are not necessary for troubleshooting most failures.

In addition, other than the equipment required for performance tests and adjustments, all that is needed is a general purpose 300 MHz oscilloscope such as the HP 54201A.

6D-4. ONE-KEY POWER UP

A one-key power up is often performed to return the instrument setup to default conditions. This is done as follows:

1. Set the front panel POWER switch to STBY.
2. Press and hold one front panel key.
3. Turn front panel POWER switch to ON.
4. Release key when display shows "Powerup Self Test Passed!" or Failed.

6C-5. TWO-KEY POWER UP

CAUTION

Using the two-key power up will leave the instrument uncalibrated. Effort needed for recalibration should be considered before using this method to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.

A two-key power up is a basic reset of the entire operating system of the HP 54111D. All volatile and non-volatile RAM is cleared. As a result, all calibration factors are purged and the instrument must be recalibrated.

All calibration except the Timebase Cals can be done with just the front panel CAL signal and the self-cal menus. The two-key power up is performed in much the same way as the one-key power up.

1. Set the front panel POWER switch to STBY.
2. Press and hold the top and bottom keys in the group at the right edge of the display.
3. Turn front panel POWER switch to ON.
4. Release keys when display shows "Powerup Self Test Passed!" or Failed.

6D-6. MAIN TROUBLESHOOTING

Figure 1, Main Troubleshooting Flow Diagram, should be used as the initial and primary troubleshooting procedure.

CAUTION

If the instrument you are servicing is traceably calibrated, try to record the TIMEBASE FREQUENCY CALIBRATION FACTOR before the two-key powerup. This procedure deletes this cal factor! Once the instrument is repaired, the traceable calibration can be restored by reentering the cal factor, or recalibration with a traceable frequency counter.

6D-7. Powerup Self Tests

When instrument power is applied the powerup self tests will be initiated, and the message "Power-up Self Test in Progress" will be displayed. As the tests progress, the message "Last Loop Completed nn" will be displayed. The number "nn" is the loop number of the present test. Many tests run too quickly to recognize the number. For firmware dates later than April 22, 1987, the number of any failed test will appear in red and a slight delay will allow the test number to be recognized. If they have been disabled (see extended Test 22), the message "Powerup Self Test Disabled !" will be displayed.

Unless the instrument warmup function has occured (see Instrument Warmup), failed tests result in the message "Powerup Self Test Failed" on the display.

6D-8. Instrument Warm-up

Under certain conditions the message "Instrument Warm-up in Progress mm:ss" may appear, in red, in the display. The time, in minutes and seconds, starts at 15:00 and counts down to zero. If the instrument passes all power-up tests at initial turn on there will be no warm-up indication on the display.

This message has no relationship with instrument temperature. If the instrument fails any of certain powerup self tests, specifically loops 26-31 (channel 1) or 35-40 (channel 2), the instrument will first assume that failure is due to lack of warm-up and display the message. If any of test loops 41,42 (channel 1) or 43,44 (channel 2) also fail, and if these additional failures are in the same channel as the first failures, the instrument will assume these failures are connected with the first and treat them the same. The instrument will not display a "Powerup Self Test Failed !" message for warm-up specific failures but will display it if other tests fail.

For example: if any of loops 26-31 and 41 or 42 (channel 1) fail, with no other failures, only the warmup message will be displayed. If

loops 43 or 44 also fail, there will be both warmup and self test failed messages.

At five minute intervals of the timer, the instrument will initiate the power-up self-test routine. If the specific tests pass, the warm-up message will end. If the tests do not pass, the warmup message will stay and the timer will start where it left off before the self-test routine was initiated. If loops 26-31 or 35-40 pass but 41-44 are still failing, the warmup message will end but the self test failed message will be displayed.

There will be a final initiation of powerup self tests at 00:00 of the timer. If the instrument still does not pass these tests, only the "Powerup Self Test Failed !" message will be displayed.

If the Automatic Warmup Retest (Extended Test 10) has been turned OFF, failure of these warmup dependent tests will result in display of "Powerup Self Test Failed !"

6D-9. Connectors

Most instruments are sensitive to connectors and assemblies that are not completely seated. So one of the initial steps, before starting troubleshooting, should be to make a mechanical check of all the connectors and assemblies to make sure that everything is properly seated.

Check the coaxial connectors, ensure that the ribbon connectors are completely snapped in place, and press down firmly on card cage assemblies to ensure proper seating.

6D-10. System Lock-up

After running the power-up self tests the instrument may be locked up by a system error, it will not respond to the keyboard. This can be a random failure or a hard failure. An error message such as one of the following,

```
SYSTEM  ERROR! Zero Divide XXXXXXH
SYSTEM  ERROR! Bus Error XXXXXXH
SYSTEM  ERROR! Address Error XXXXXXH
```

will be displayed on screen, followed by

```
To clear, cycle power with one front-panel key
pressed. If the error condition remains please
consult the service manual.
```

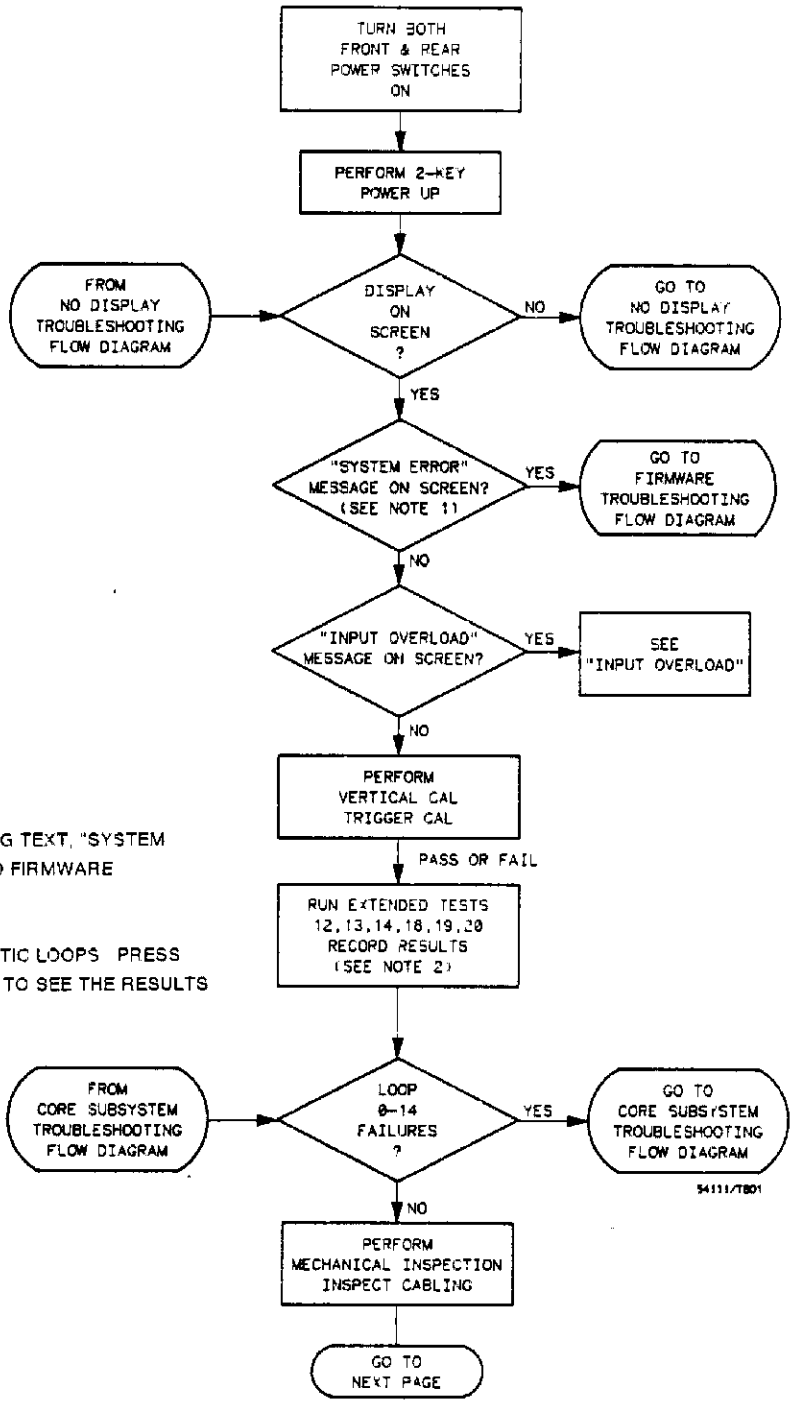
Note the hex number (XXXXXXH) after the error message. This may be useful if help from an HP Service Center is needed later.

Try to use the one key power-up to reset the instrument. If the instrument is failing after a one key power-up and calibration traceability need not be maintained, try a reset using the two key power-up.

CAUTION

Using the two-key power up will leave the instrument uncalibrated. Effort needed for recalibration should be considered before using this mode to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.

If the instrument is still failing, try to obtain information about the failure mode by "breaking in" to the power-up routine before the system becomes locked. Go to Firmware Troubleshooting for further information.



NOTES

1 SEE MAIN TROUBLESHOOTING TEXT, "SYSTEM LOCK-UP", BEFORE GOING TO FIRMWARE TROUBLESHOOTING

2 TEST 12 RUNS THE DIAGNOSTIC LOOPS PRESS THE "DISPLAY ERRORS" KEY TO SEE THE RESULTS

Figure 6D-1. Main Troubleshooting Flow Diagram (part 1)

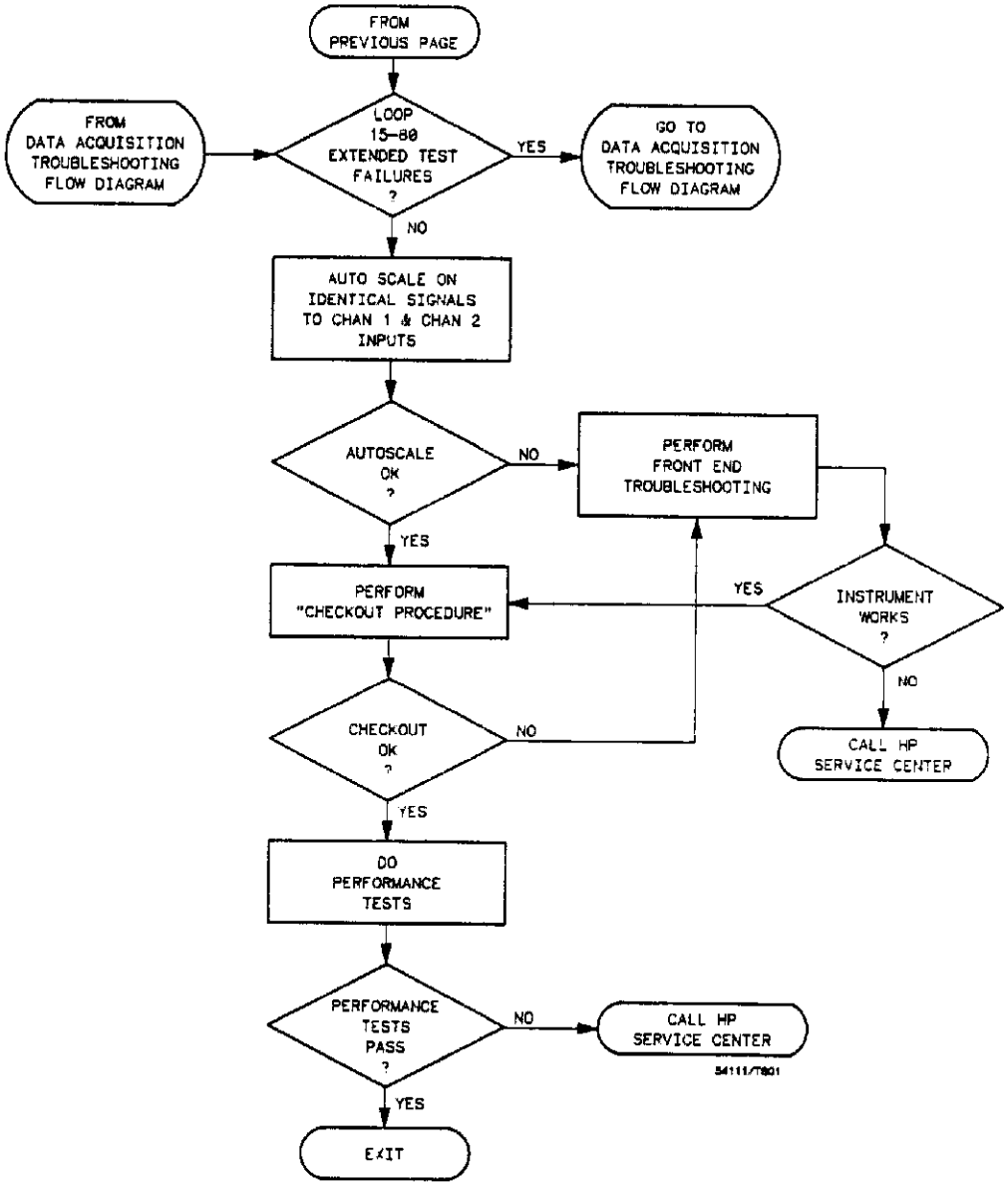


Figure 6D-2. Main Troubleshooting Flow Diagram (part 2)

6D-11. Input Overload

If an Input Overload message is displayed on screen immediately after power-up the cause is usually an input sense cable that has become disconnected or mis-connected. This failure also results in lock-up of the instrument; there will be no response to the keyboard.

NOTE

Do not do any other troubleshooting until the problem causing this Input Overload message has been corrected.

CAUTION

Do not perform a two-key powerup. The instrument will be harder to return to proper operation.

Use the following procedure to check for this problem.

1. Turn the POWER to STBY.

2. Remove the covers (see section 6A).

3. Ensure that all of the input sense cables are properly connected. (See the diagram on the cover of the instrument or at the end of section 6A.)

4. If the instrument still fails to power up properly, continue with troubleshooting based on known symptoms.

If a two-key powerup was performed, it may be necessary to clear the non-volitile RAM manually by using the following procedure.

1. Turn POWER to STBY.

2. Pull the Microprocessor assembly clear of the motherboard. This separates the RAM from its battery supply on the I/O assembly. Leave separated for several seconds.

3. Re-insert Microprocessor assembly and apply power. Instrument should power up and display a message that calibration is needed.

6D-12. Intermittent Failures

Loop failures that are intermittent may not be true failures. A loop must fail more than one percent of the time to be considered a true failure. If a loop seems to be intermittent it should be run in the REPEAT LOOP mode to determine the failure percentage.

Use the following procedure to check the failure percentage of a given loop.

1. Press ***more***, ***Utility***, and ***Test menu***.

2. Press the top softkey to get ***RUN FROM LOOP*** and ENTER the Loop # with the ENTRY keys.

3. Press ***RUN FROM LOOP*** to get ***REPEAT LOOP*** and ENTER the # Repetitions with the ENTRY keys. The number of repetitions must be high enough to get a proper sampling. Checking for one percent of errors will need several hundred repetitions for a good sample.

4. Press ***Start Test***. Several hundred samples may take a few minutes to complete. You can press ***Stop Test*** then ***Display Errors*** to check on the progress of the test but starting the test again will start it at the beginning.

5. When the display returns to the test menu press ***Display Errors*** to check the error rate. If ***Failures*** = is greater than one percent of ***Executions*** = the loop has a true failure.

6D-13. NO-DISPLAY TROUBLE-SHOOTING

Check to see whether the power supply is functioning correctly by checking the four LEDs that indicate supply function. One is located on the I/O assembly (A3), and the others are located on the primary, digital, and analog power supply assemblies. If any of these LEDs is not lit, proceed directly with the Power Supply Troubleshooting procedures.

Use a voltmeter to check the voltages at the test points on the power supply. If voltages are not correct (see Power Supply Troubleshooting) proceed with the Power Supply Troubleshooting procedure.

If the supplies are correct and there is still no display, cycle the power with the front panel switch. If the display produces a normal flash at powerup and powerdown, the Color CRT Monitor is probably working. If it does not light at all, check if the 120 V LED at the front of the Primary Supply is lit. If it is, outrig a working Color CRT Module (see Color CRT Module Outrigging). Replace Color CRT Module if outrigged module works. If outrigged module does not work, see Power Supply Troubleshooting procedure.

If the display lights, determine whether the problem is in the Color Display assembly or in the Color CRT Module, as follows.

1. Check the voltage on the 120 Volt pin on the Color CRT Module; also check the Red, Blue, and Green Video signals. If these signals are correct (see Color CRT Module Failure Isolation) then outrig a new Color CRT Module and test it. If it works, replace the module.

2. If they are not correct, the display assembly is suspect. Check the +/- 5 Volts on the display assembly and the Vertical and Horizontal Sync signals coming from the display assembly. If these are not present, the Color Display assembly is suspect. Remove assemblies not in the core subsystem and proceed with verifying its operation (see Core Subsystem Troubleshooting).

If you have not been able to find the problem using these techniques, call your HP Service Center.

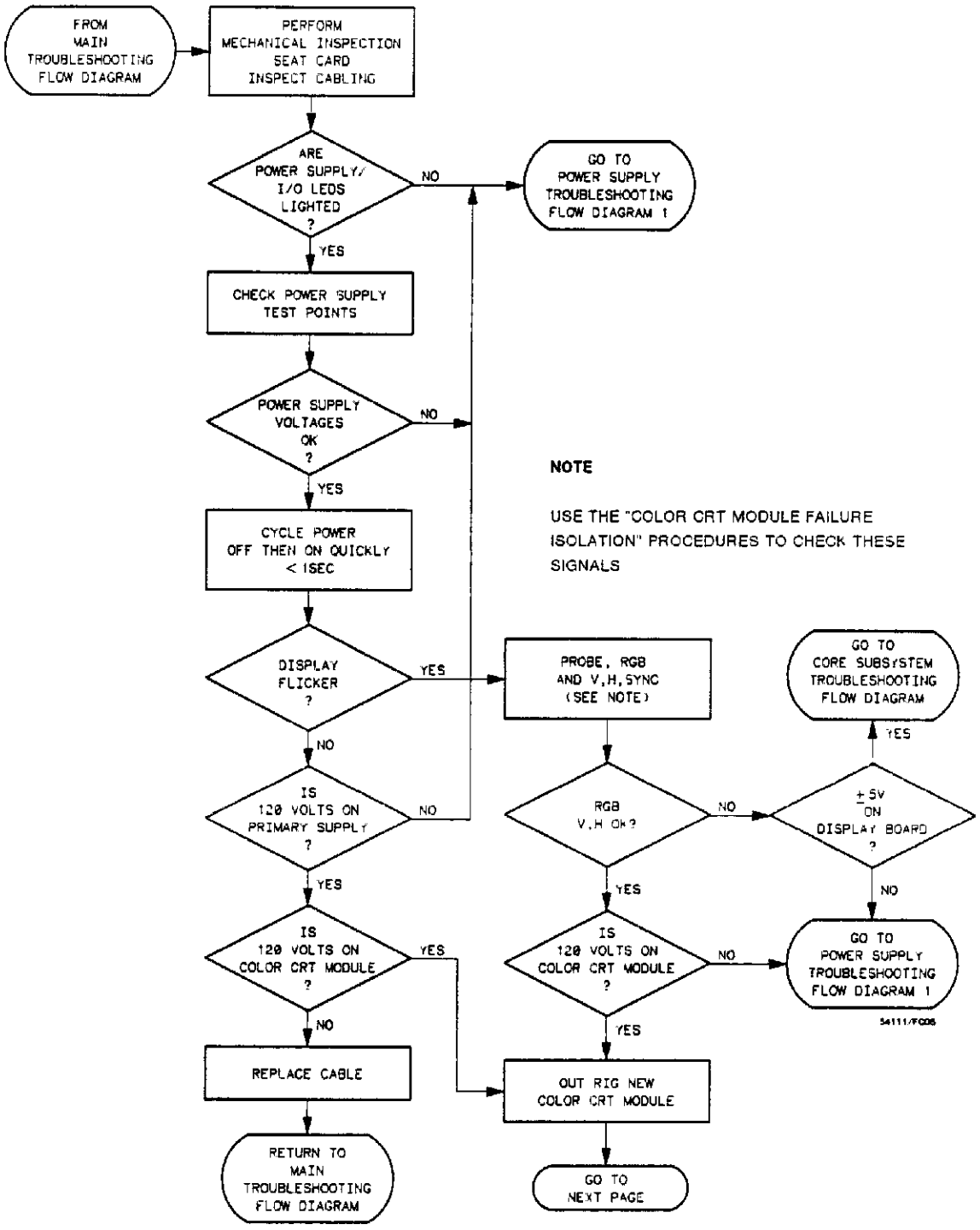


Figure 6D-3. No Display Troubleshooting Flow Diagram (part 1)

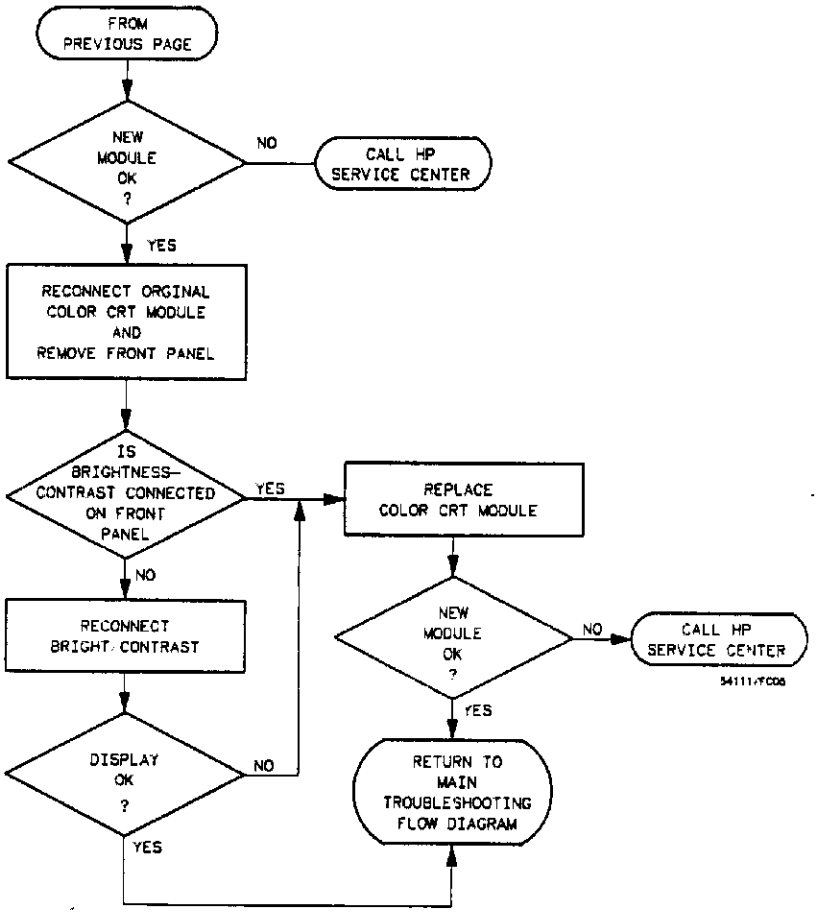


Figure 6D-4. No Display Troubleshooting Flow Diagram (part 2)

NOTES

6D-14. POWER SUPPLY TROUBLE-SHOOTING

When a power supply problem is suspected, it is first important to make sure that no unusual load is keeping the supply in a current limited condition. The table below shows which supplies are used on each assembly.

1. If the 300V LED on the Primary Supply is not lit go directly to the Power Supply Troubleshooting Flow Diagram on the next page.

2. If the 300V LED is lit, find the LEDs on the Analog and Digital supplies and I/O assembly. They are near the top-front of each assembly, so if you cannot see them they are probably not lit.

3. If the LEDs are lit and you still suspect a supply problem, go to the Power Supply Troubleshooting Flow Diagram on the next page.

4. If the LEDs are not lit continue with this procedure before going to the Power Supply Troubleshooting Flow Diagram on the next page.

CAUTION

Always turn front panel POWER to STBY before removing and inserting assemblies and be sure to use proper ESD precautions.

5. At the right side of the instrument, pull up the Trigger Qualifier assembly until it clears the motherboard connector, about one half inch.

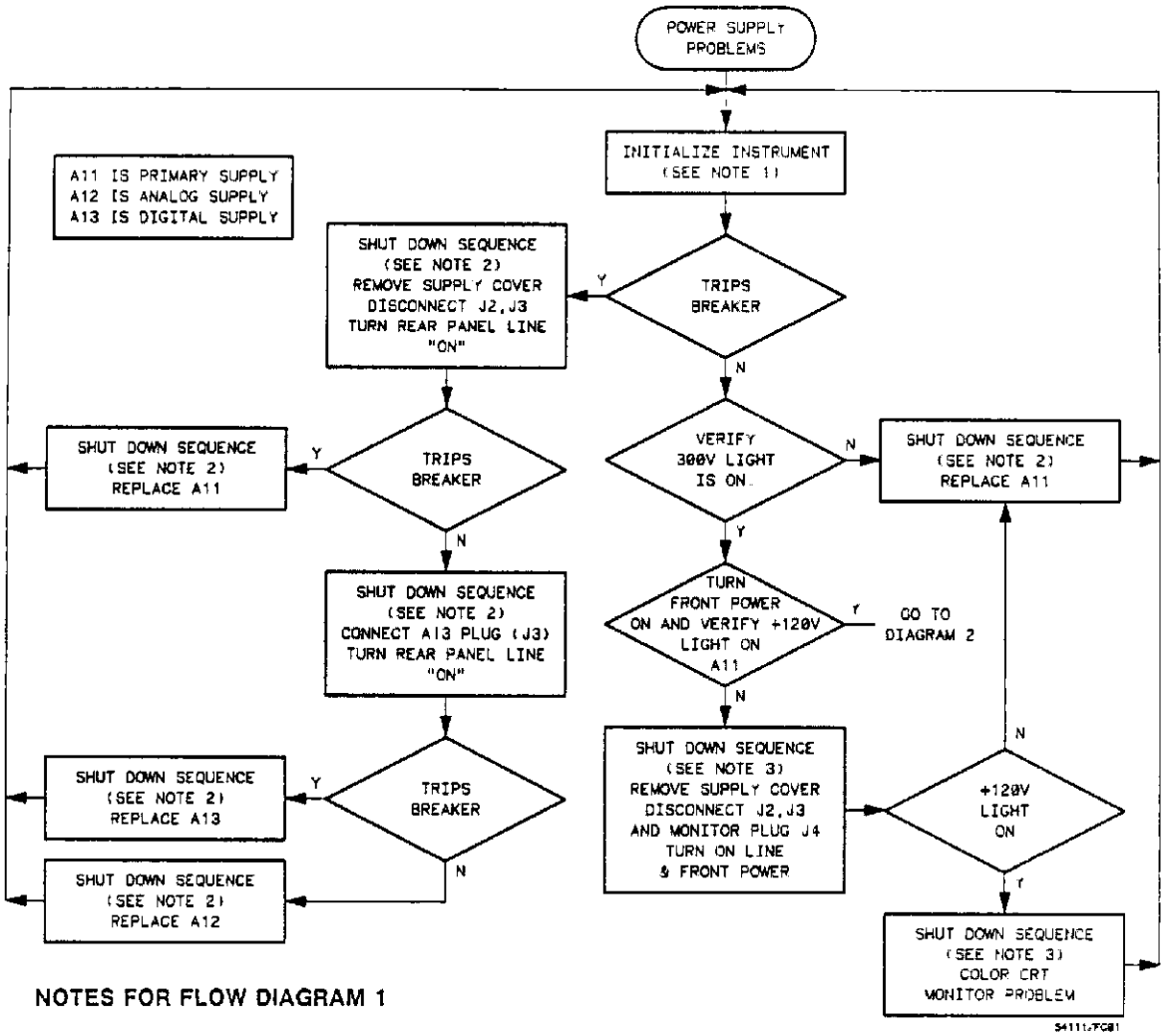
6. Check to see if the LEDs are lit. If the LEDs are lit troubleshoot the Trigger Qualifier for excessive loading. If they are not lit, leave the assembly up and go to the next step.

7. Working from right to left, pull up each card cage assembly while watching for the LEDs to light. If they light, troubleshoot for excessive loading, the last assembly pulled up.

8. After the I/O assembly is pulled up, watch only for the supply LEDs. If all nine card cage assemblies are up, and the supply LEDs are not lit, go to the following Power Supply Troubleshooting Flow Diagram.

Table 6D-1. Power Supply Distribution.

	+5V	-5V	+18V	+8V	-8V	-18V	+120V
TIMEBASE	*		*	*	*	*	
MICROPROCESSOR	*						
INPUT/OUTPUT †	*	*	*	*	*	*	
CH1 ADC CONT	*	*	*	*	*	*	
CH1 ADC	*		*		*	*	
CH2 ADC CONT	*	*	*	*	*	*	
CH2 ADC	*		*		*	*	
TRIGGER	*	*	*	*	*	*	
TRIGGER QUAL	*	*		*	*		
COLOR DISPLAY	*						
COLOR CRT MOD.							*



NOTES FOR FLOW DIAGRAM 1

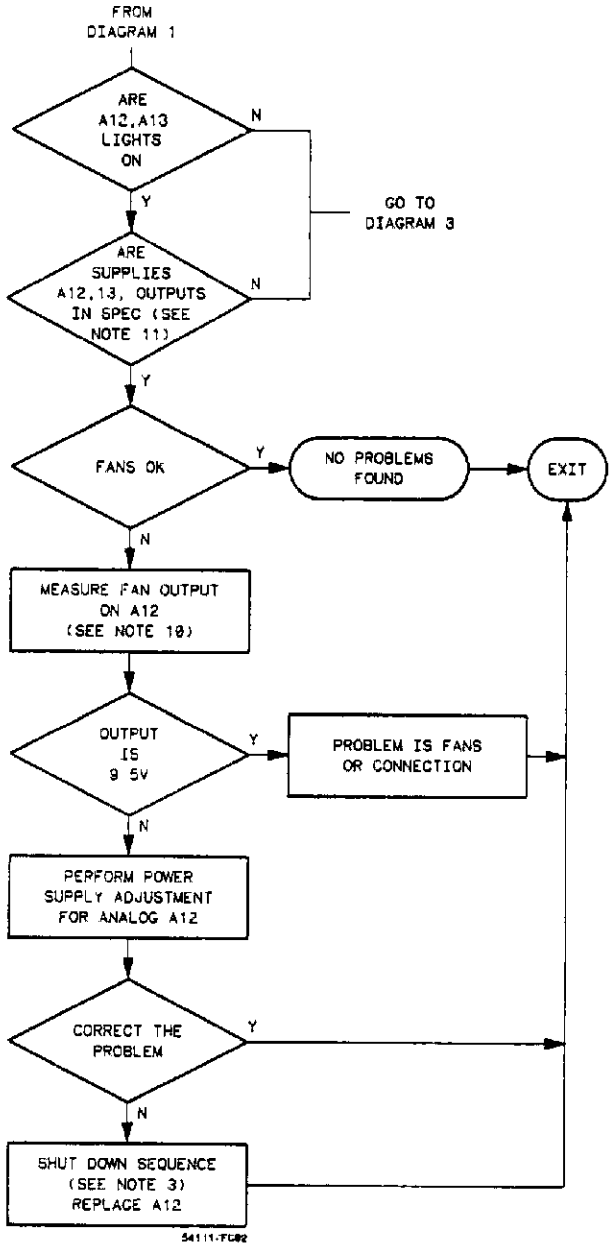
1) A. FRONT PANEL POWER SWITCH SHOULD BE IN STANDBY
   B. REAR PANEL LINE SWITCH SHOULD BE OFF "0"
   C. CONNECT AC POWER SOURCE
   D. TURN REAR PANEL LINE SWITCH TO ON "1"

2) A. TURN REAR PANEL LINE SWITCH TO OFF "0"
   B. ALWAYS UNPLUG AC POWER SOURCE
   C. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

WARNING
EXTREME CAUTION MUST BE TAKEN WHEN REMOVING POWER SUPPLY COVER.

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

Figure 6D-5. Power Supply Troubleshooting Flow Diagram 1.



NOTES FOR FLOW DIAGRAM 2

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

10) CONNECT THE VOLTMETER (+) LEAD TO THE "FAN" TEST POINT AND THE (-) LEAD TO THE -18V TEST POINT. THE READING SHOULD BE 9 5V. THIS VOLTAGE WILL INCREASE WITH INCREASING AMBIENT TEMPERATURE. SEE THE POWER SUPPLY ADJUSTMENT PROCEDURE FOR THE ANALOG SUPPLY.

11) FOR POWER SUPPLY TEST POINTS AND SPECIFICATIONS SEE TABLE BELOW

DIGITAL SUPPLY TST PTS (+) LEAD	(-) LEAD	VOLTAGE
+5V	GND	+5.10 ±0.1V
-5V	GND	-5.30 ±0.1V
+14B	GND	>+5V
ANALOG SUPPLY TST PTS (+) LEAD	**(-) LEAD**	**VOLTAGE**
+18V	GND	+18.5 ±0.3V
+8V	GND	+8.9 ±1V
-8V	GND	-8.5 ±1V
-18V	GND	-18.5 ±0.3V
FAN	-18V	+9.5 ±0.3V
+26B	GND	>+5V

Figure 6D-6. Power Supply Troubleshooting Flow Diagram 2.

NOTES FOR FLOW DIAGRAM 3

3) A TURN FRONT PANEL SWITCH TO STANDBY
   B TURN REAR PANEL LINE SWITCH TO OFF "0"
   C ALWAYS UNPLUG AC POWER SOURCE
   D **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

4) THE NOMINAL OUTPUT FOR +14B IS 21V HOWEVER, WHEN THE SUPPLY IS OPERATING IN THE CURRENT LIMIT MODE, IT CAN BE AS LOW AS +5V THE NOMINAL OUTPUT FOR +26B IS 26V IT TOO CAN BE AS LOW AS +5V WHEN IN CURRENT LIMIT

5) MEASURE OUTPUTS +5V AND -5V ON THE DIGITAL POWER SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES. IF OUTPUTS ARE GREATER THAN HALF THE ANSWER IS NO.

7) MEASURE OUTPUTS ±18V AND ±8V ON THE ANALOG SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES IF OUTPUTS ARE GREATER THAN HALF THE ANSWER IS NO

8) THE TEST POINTS TO MEASURE +14.6V ARE AT THE BACK OF THE BOARD CLOSE TO THE TOP CONNECT THE VOLTMETER COMMON LEAD TO THE COM TEST POINT ON THE BOARD **CAUTION!!!** ***USE CAUTION WHEN MEASURING THIS VOLTAGE. IT IS NOT ISOLATED FROM THE LINE (MAINS) INPUT AND THE PRIMARY SUPPLY IS EXPOSED WITH THE POWER SUPPLY COVER REMOVED.***

9) BY REMOVING THE CONNECTORS AT J2 AND J3 YOU ARE CHECKING IF EITHER THE ANALOG OR DIGITAL SUPPLY IS LOADING VCNTL.

   EXTREME CAUTION MUST BE TAKEN WHEN MEASURING VCNTL ON THE PRIMARY SUPPLY. THE TOP PIN ON CONNECTORS J2 AND J3 IS VBULK WHICH IS +300V. THE PINS BELOW ARE VCNTL, THEN GROUND

   TO MEASURE VCNTL, TURN THE POWER OFF AND MAKE SURE THE +300V LAMP (NEAR TOP OF BOARD) IS OFF. CONNECT THE VOLTMETER (+) LEAD TO VCNTL (SECOND PIN FROM TOP) AND THE (-) LEAD TO GROUND (BOTTOM PIN). APPLY POWER AND OBSERVE THE METER READING. WITH ONE SUPPLY CONNECTED THE READING SHOULD BE ABOUT +25V AND WITH NEITHER CONNECTED ABOUT +42V. TURN OFF POWER (+300V LAMP IS OFF) BEFORE REMOVING THE VOLTMETER LEADS

---

6) WHEN THE SUPPLIE(S) ARE RUNNING IN THE CURRENT MODE THIS MEANS THAT AN EXTERNAL LOAD IS PULLING DOWN THE SUPPLY OUTPUT(S). AN EXTERNAL LOAD COULD BE AN ASSEMBLY IN THE CARD CAGE OR THE COLOR DISPLAY ASSEMBLY (NOT THE COLOR CRT MODULE). THE ONLY WAY TO ISOLATE THE COLOR DISPLAY ASSEMBLY IS TO COMPLETELY REMOVE IT FROM THE MAINFRAME. THE FANS CAN ALSO PUT THE ANALOG SUPPLY INTO THE CURRENT MODE. YOU CAN DISCONNECT THE FANS BY REMOVING THE BOTTOM COVER AND DISCONNECTING THE FAN CABLE.

	+5V	-5V	+18V	+8V	-8V	-18V	+120V
TIMEBASE	*		*	*	*	*	
MICROPROCESSOR	*						
INPUT/OUTPUT †	*	*	*	*	*	*	
CH1 ADC CONT	*	*	*	*	*	*	
CH1 ADC	*		*		*	*	
CH2 ADC CONT	*	*	*	*	*	*	
CH2 ADC	*		*		*	*	
TRIGGER	*	*	*	*	*	*	
TRIGGER QUAL	*	*		*	*		
COLOR DISPLAY	*						
COLOR CRT MOD.							*

†ONLY THE +5V IS USED FOR POWER. THE OTHER SUPPLIES CONNECT FOR POWER TEST ONLY AND ARE HIGH IMPEDANCE POINTS. LIKELYHOOD OF LOADING THESE SUPPLIES IS LOW

TO ISOLATE A CURRENT PROBLEM, REMOVE ONE LOAD AT A TIME UNTIL THE PROBLEM IS FOUND. PROBLEMS COULD INCLUDE BENT PINS ON THE MOTHERBOARD OR A BAD COMPONENT ON A PC ASSEMBLY. SEE THE ADJACENT TABLE FOR POWER DISTRIBUTION TO THE VARIOUS ASSEMBLIES

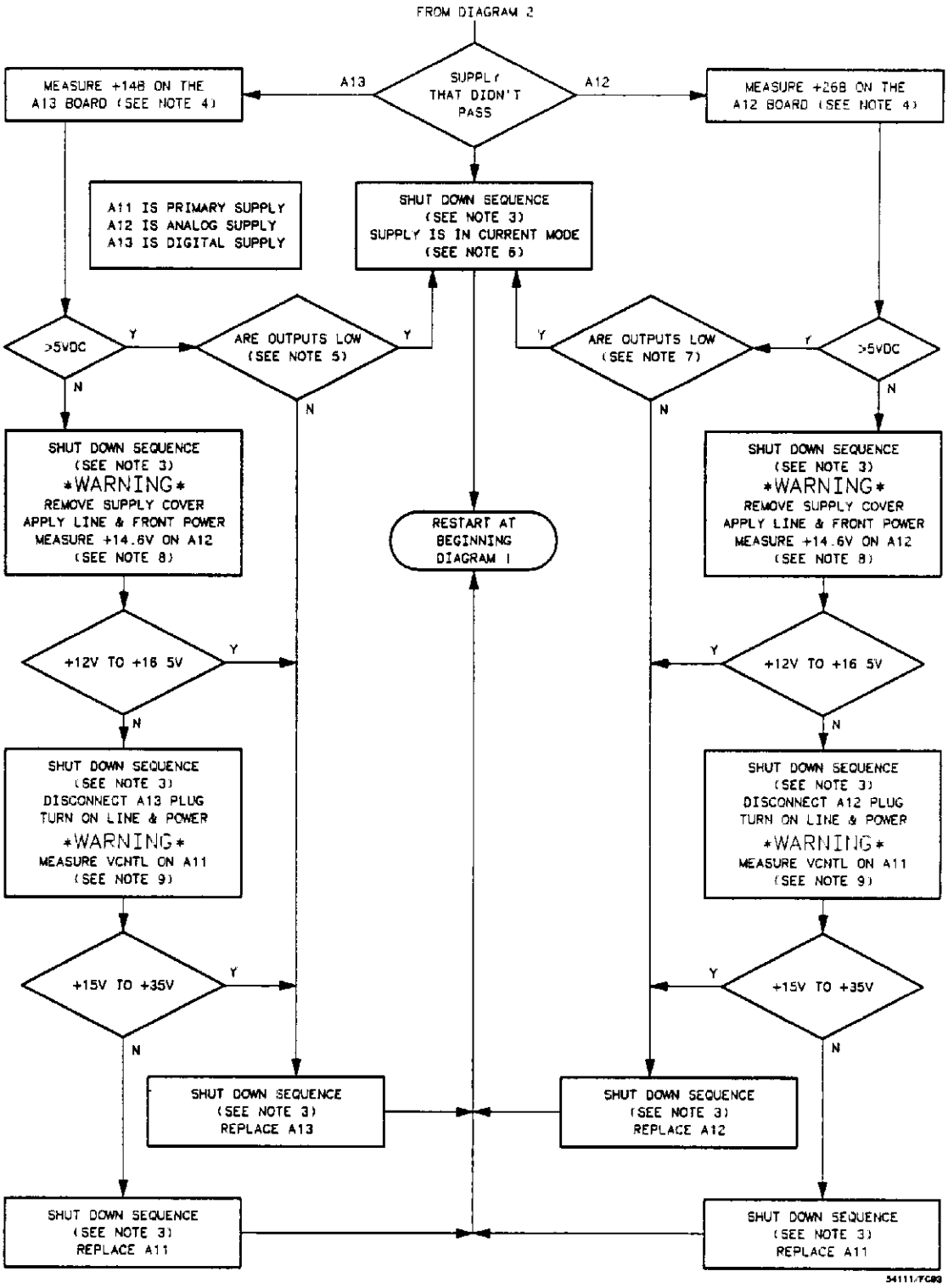


Figure 6D-7. Power Supply Troubleshooting Flow Diagram 3.

6D-15. COLOR CRT MODULE FAILURE ISOLATION

The following procedure causes the processor to write a known pattern of video to the module. The video waveforms, the vertical and horizontal sync signals, and the +120V primary module power are checked at the module inputs. If the inputs are present and correct, use the Color CRT Module Outrigging procedure to ensure that replacement of the module will correct the problem.

6D-16. Troubleshooting Procedure

1. Turn instrument to STBY using the front panel power switch.

2. Remove covers (see Instrument Disassembly, section 6A).

3. Turn power on and check the +120 V module power at the module power input connector (see next figure). The correct voltage will be between +118 and +122 volts. If the +120 V supply voltage is incorrect, see the power supply troubleshooting procedures.

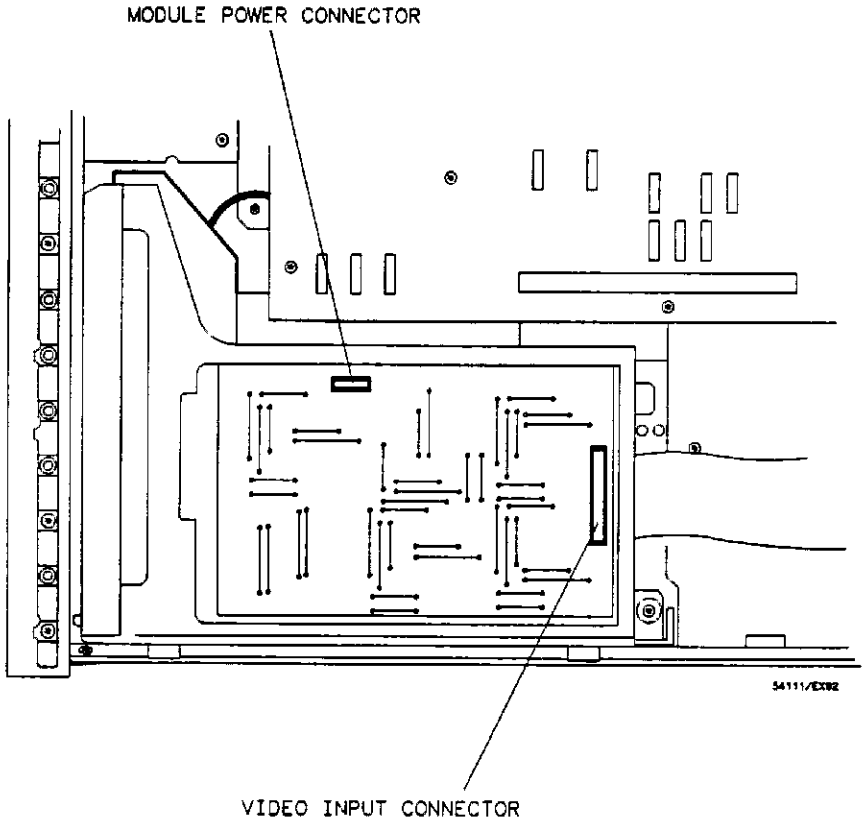


Figure 6D-8. Color CRT Module Input Connections

4. Move clear plastic board shield on bottom of Color CRT Module by pushing rearward until it clears front frame and hinge it away from the board.

5. With 10:1 divider probes, connect channel 1 of the monitor oscilloscope to vertical sync test point VD (located on module video input connector, pin 3) and channel 2 of the monitor oscilloscope to horizontal sync test point HD (located on module video input connector, pin 7). These test points are located on the Color CRT Module (A19). The vertical and horizontal sync signals are TTL levels and should resemble the waveforms in the following figure. The vertical sync is on the top and the horizontal sync on the bottom.

6. To see if the Color CRT Module is loading the signals, disconnect the wide ribbon cable at the Color Display assembly and check the signals at the two labled test points (VSYNC, HSYNC near U119) on the Color Display assembly.

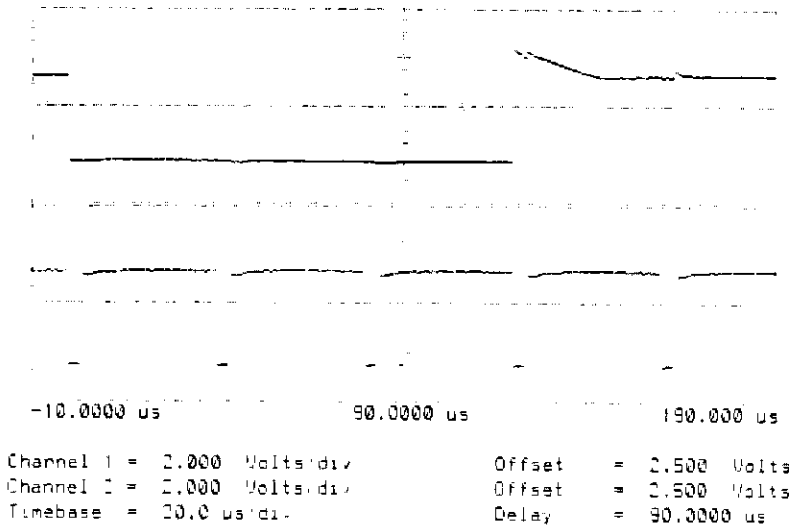


Figure 6D-9. Vertical and Horizontal Sync Waveforms

7. It is helpful to try to get a known display before checking the video waveforms. If the display is operating, press ***more, Utility, CRT Setup Menu***, and ***Color Purity***. This will give a white raster so all video signals will be at maximum.

   If there is no display, try to get the same signals using the following procedure.

   a. Turn instrument off, then on, then press the following softkeys, in order given.

   b. In bottom row press:
      Key at extreme right
      Key second from right
   c. In vertical column press:
      Key at bottom
      Key third from bottom

8. Check the red, green, and blue video signals at the module video input connector at pins 21, 29, and 37 respectively (see Color CRT Module Input Connections drawing).

   The video signals have a 0 V baseline and will vary in amplitude from 0 V to approximately +600 mV, depending on the characteristics of the colors displayed.

9. Video signals can be adversely loaded by input circuit failures within the Color CRT Display Module. Therefore, before assuming Color Dispaly assembly failures, repeat this test with the video cable disconnected from the Color CRT Module and the measurements taken at the pins of U145 on the Color Display assembly. The red, green, and blue signals are on U145 pins 14, 18, and 22 respectively.

6D-17. Incorrect Display Color

Using the CRT Setup Menu, then pressing the ***Color Purity*** key it is easy to locate a potentially defective CRT write gun or associated electronics. By pressing the ***Color Purity*** key several times the primary colors will be displayed. The colors displayed on the measurement screens are user definable, while the color purity check displays fixed primary colors.

6D-18. Module Outrigging Procedure

Due to the amount of work and time involved in changing the Color CRT Module it is prudent to verify the defective module diagnosis by outrigging a good module. Required parts which are part of the 54100 Family Support Kit are: Color CRT Module power cable, Display Control assembly, and Display Control Cable. Also necessary is a working Color CRT Module which is not part of the service kit.

1. Turn power off and remove instrument power cable.

2. Remove covers (see Instrument Disassembly, section 6A).

3. Disconnect Color CRT Module power cable at the primary power supply.

4. Connect the Color CRT Module power cable from the support kit to the primary power supply.

5. On the bottom of the instrument, disconnect the wide ribbon cable from the the suspect Color CRT Module and extend it as far as possible from the instrument when it is in a normal operating position.

6. Set the working Color CRT Module next to the instrument.

7. Connect the wide ribbon cable to working module.

8. Connect the module power cable to the mating connector towards the front of the CRT Module. This connection can be verified by noting that the connector is labled B-4 on the bottom of the PC board at the connector.

9. Connect the Display Control Cable from the support kit to the mating connector which is toward the rear of the module. This connector is labled B-2 on the bottom of the PC board.

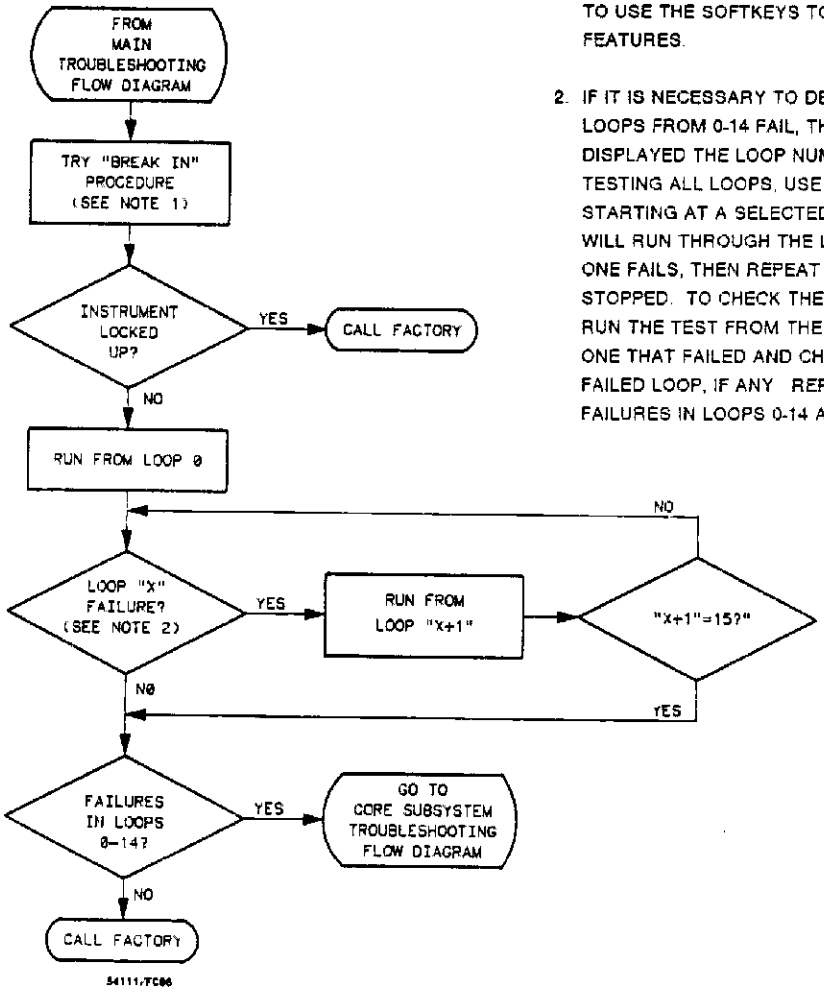
10. Connect the CRT Brightness Control from the support kit to the other end of the Display Control Cable.

11. Re-connect the power cord and turn instrument on.

12. Verify display operation.

6D-19. FIRMWARE TROUBLE-SHOOTING

Firmware troubleshooting is used to evaluate a firmware problem that prevents the instrument from displaying self-test information by locking up the keyboard. This routine is entered from the Main Troubleshooting Flow Diagram.



NOTES

1. THIS PROCEDURE MAY ALLOW YOU TO "BREAK IN" TO AN INSTRUMENT THAT IS LOCKING UP DURING THE POWERUP CYCLE. IT IS NECESSARY TO INTERRUPT THE POWERUP CYCLE BEFORE IT LOCKS UP THE INSTRUMENT.

   IF THE INSTRUMENT IS LOCKING UP, CYCLE THE POWER WITH THE STBY SWITCH. JUST AFTER "LAST LOOP " DISAPPEARS, DURING THE POWERUP ROUTINE, PRESS THE STOP/SINGLE KEY. TIMING IS IMPORTANT HERE AND IT MAY TAKE SEVERAL TRIES TO "BREAK IN".

   WHEN BREAK IN IS SUCCESSFUL, YOU WILL BE ABLE TO USE THE SOFTKEYS TO ACCESS THE SELF TEST FEATURES.

2. IF IT IS NECESSARY TO DETERMINE WHICH OF THE LOOPS FROM 0-14 FAIL, THE INSTRUMENT HAS NOT DISPLAYED THE LOOP NUMBERS OR STOPS BEFORE TESTING ALL LOOPS, USE "RUN FROM LOOP" STARTING AT A SELECTED LOOP. THE INSTRUMENT WILL RUN THROUGH THE LOOPS UNTIL THE NEXT ONE FAILS, THEN REPEAT THAT LOOP UNTIL STOPPED. TO CHECK THE REST OF THE LOOPS, RUN THE TEST FROM THE LOOP AFTER THE LAST ONE THAT FAILED AND CHECK FOR THE NEXT FAILED LOOP, IF ANY. REPEAT THIS UNTIL ALL FAILURES IN LOOPS 0-14 ARE FOUND.

Figure 6D-10 Firmware Troubleshooting Flow Diagram

6D-20. CORE SUBSYSTEM TROUBLE-SHOOTING

GENERAL

It is best to attempt to get the instrument to pass all the Core Tests before going on to fix more complex loops. Occasionally, bent motherboard pins or defects in other system elements will cause these loops to fail. By making a system of the Microprocessor assembly, I/O assembly and one other assembly, it is possible to determine which socket or assembly may be causing an interaction that causes one of the core loops to fail. Using this technique, seat each assembly into the motherboard one at a time. Be sure to turn the power off before raising or seating an assembly into the motherboard.

If only the Microprocessor and I/O assemblies are seated, the system will go into a repeating multicolored routine with about a two second cycle. This is useful in certain troubleshooting situations but no loop error information will be available.

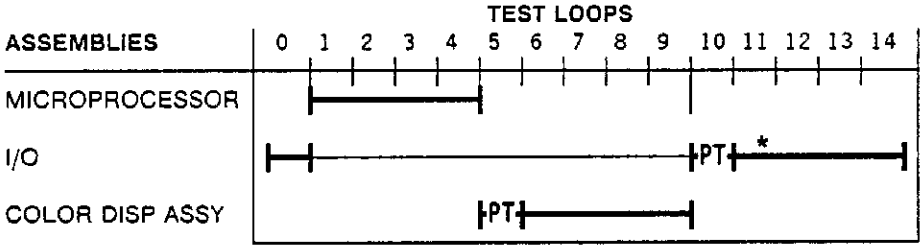
LOOP 11

Loop 11, which can test every addressable location in the DRAM on the I/O assembly, is a special case. Using RUN FROM LOOP does not completely execute this test because that would take about 18 minutes to complete. Instead, RUN FROM LOOP tests a random block of this memory.

The REPEAT LOOP mode will run the complete Loop 11 test, but only once due to its length. A complete test of DRAM should be done only if the I/O assembly is suspected of failing and there is not enough proof, or if loop 11 has an intermittent failure. This test takes about 18 minutes to run.

Table 6D-2. Core Subsystem Diagnostic Routines.

NOTE: *For the Core Subsystem tests to be available and meaningful, the power supplies, Color CRT Module, and Color Display assembly must be working, and the Microprocessor, I/O, and one other assembly must be present with partial function.*



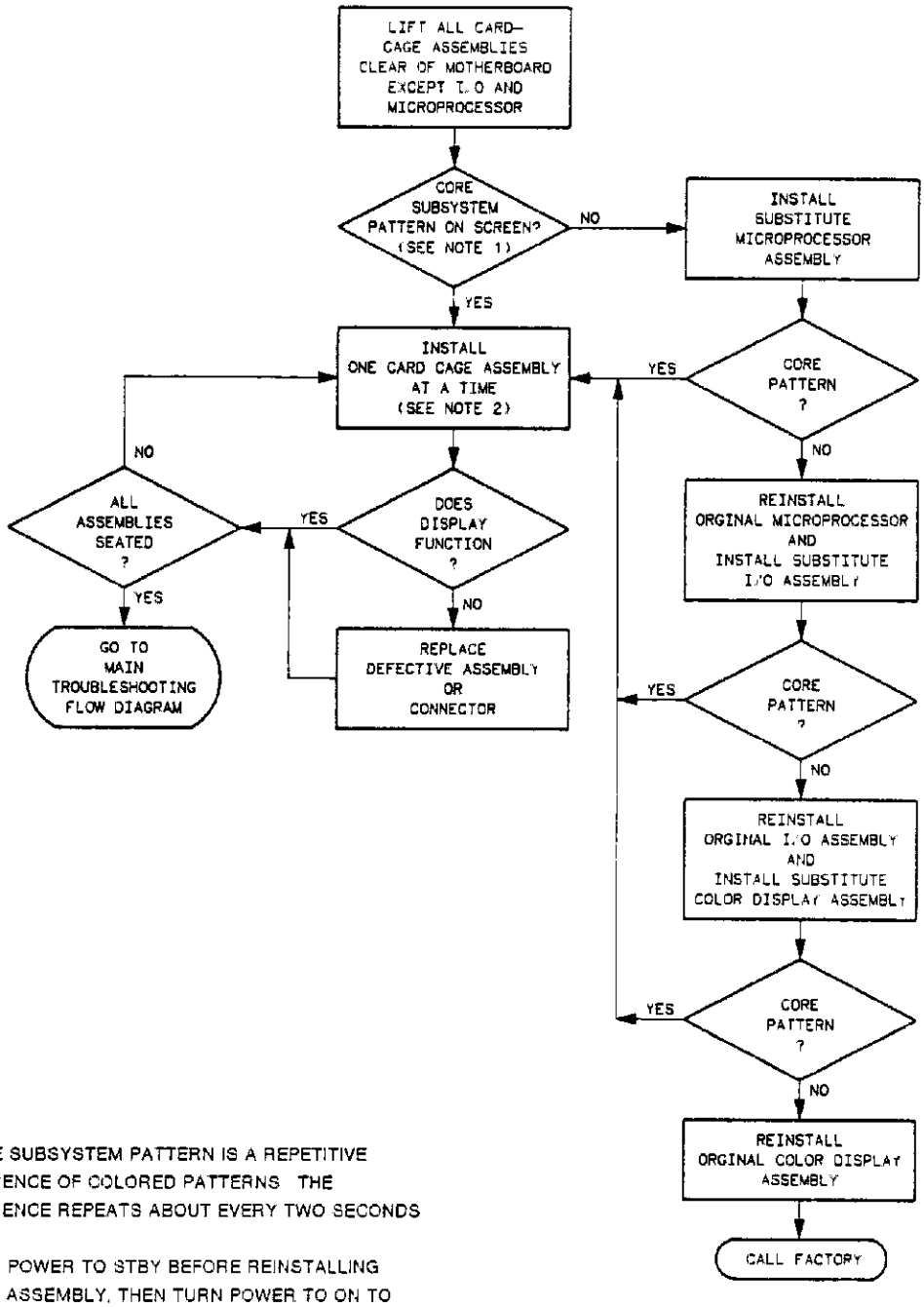
KEY:

|PT| Presence test. If the diagnostic firmware fails to find the assembly, this loop fails and all other self tests that include this assembly are skipped

This assembly must work for the test to be successful. The test will be skipped and will not show a failure if the assembly is not present

The I/O assembly provides the system clock which must work for any test to be run. It also provides the watchdog timer, which must work or Loop 0 will lock up the instrument.

* See Loop 11 text above



NOTES

1. CORE SUBSYSTEM PATTERN IS A REPETITIVE SEQUENCE OF COLORED PATTERNS. THE SEQUENCE REPEATS ABOUT EVERY TWO SECONDS.

2. TURN POWER TO STBY BEFORE REINSTALLING EACH ASSEMBLY, THEN TURN POWER TO ON TO CHECK DISPLAY.

Figure 6D-11. Core Subsystem Troubleshooting Flow Diagram

6D-21. DATA ACQUISITION SUBSYSTEM TROUBLESHOOTING PROCEDURE

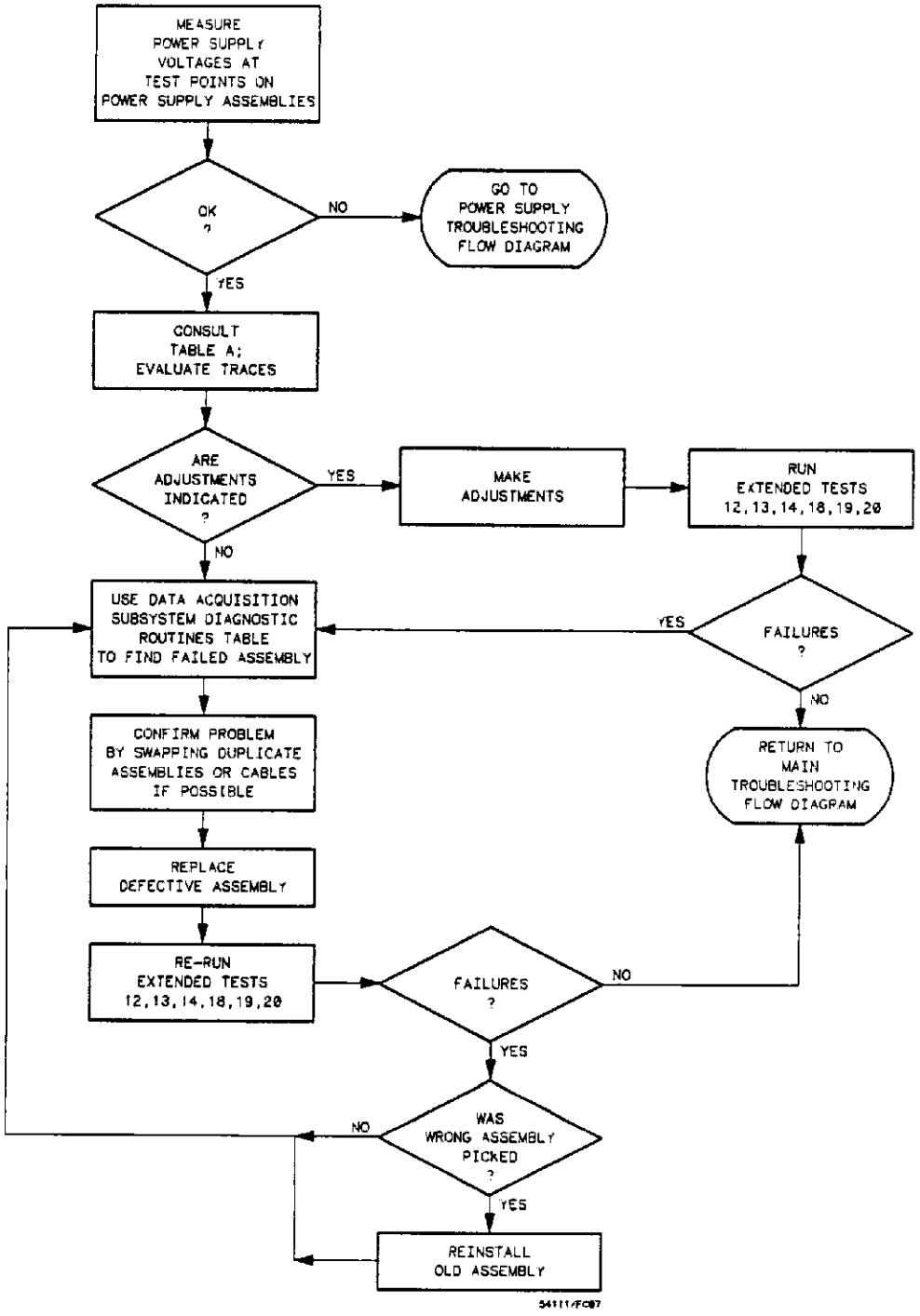


Figure 6D-12. Data Acquisition Subsystem Troubleshooting Flow Diagram.

6D-22. Data Acquisition Subsystem Diagnostic Routines

The Data Acqusition Diagnostics consists of several groups of tests:

- Timebase Assembly Tests
- ADC Control Assembly Tests
- ADC (Digitizing) Assembly Tests
- Offset Tests

- Factory Test
- Trigger Assembly Tests
- Trigger Qualifier Assembly Tests
- Extended Tests

The tests are arranged in a meaningful order. The more complex and complete tests are located at the end of the group. The firmware executes the tests in numerical order.

Troubleshooting the Data Acquisition Subsystem is based on the Data Acquisition Subsystem Diagnostic Routines table, table 6D-3. The areas tested are shown across the top of the table. Various letters indicate a function of the card in a particular test. If a particular card is not present, its presence test fails, and the tests for that assembly are skipped. Loop numbers are shown at the top and bottom of the table.

Information about instrument loop errors is accessed by pressing ***Utility***, ***Test Menu***, and ***Display Errors***. The display shows only the numbers of failed loop tests. Once an error appears on the Display Errors screen the error will stay until the power is cycled or until extended test 12 is run, even if the fault has been corrected.

NOTE

It is best to disconnect all front panel inputs from the instrument while using the self-test loops for troubleshooting. Some of the loops can be affected by a signal at a front panel BNC.

Some loop failures may be caused by misadjustment. use the following table to check for these failures.

TABLE A

Loop	Adjustments
03	Self-calibration required: Probe Tip, Vertical, Trigger, and Timebase Cals
26-31	Channel 1 CLK, GAP
35-40	Channel 2 CLK, GAP
41/42	Channel 1 GAIN, FLAT, CLK, GAP
43/44	Channel 2 GAIN, FLAT, CLK, GAP
78	Trigger Qual: DELAY/PATT oscillator

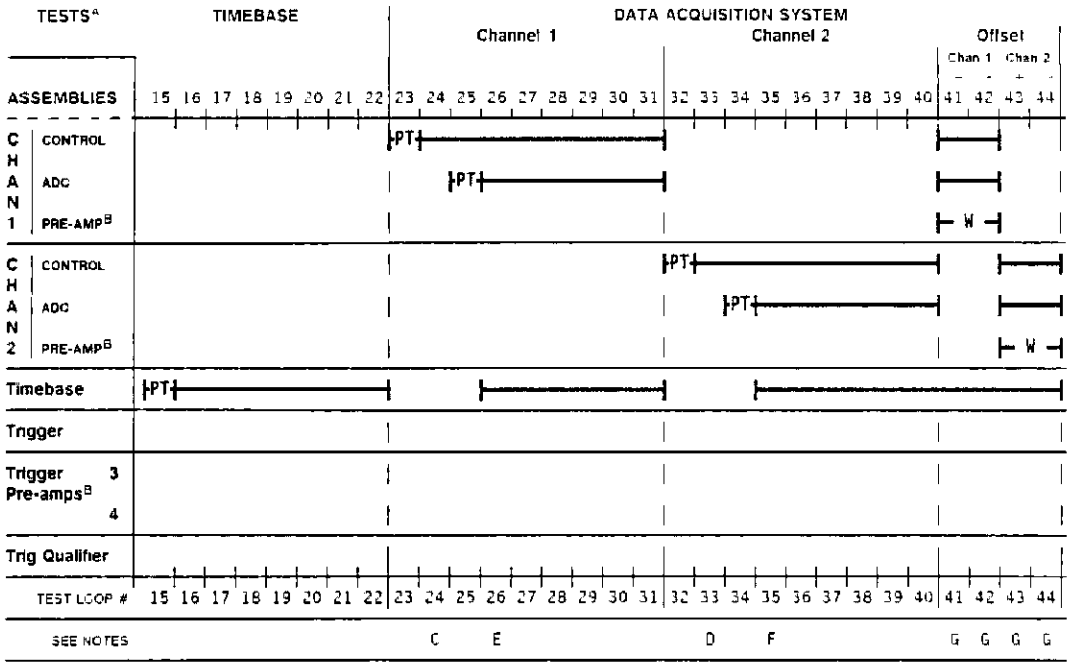
6D-23. How To Use The Diagnostic Routines Table

This table relates diagnostic loop test and extended test results to replaceable assemblies. It provides a technique for rapidly and correctly identifying an assembly to replace when loop failures have occurred. Most true hardware failures result from the failure of a single circuit element on a single assembly, though they can cause several loops to fail. The correct use of this table allows the reader to confidently determine the most probable cause of the observed set of loop failures.

After running the powerup self-tests (or extended test 12) and extended tests 13, 14, 18, 19, and 20, you will have a set of test results, consisting of a "pass" or "fail" for each loop. It is important to emphasize that passing a loop test is valuable information, even though only failures are displayed. If a loop is not listed in the "Loop failures" list on the DISPLAY ERRORS screen, it has passed all the times it was run since power-up or Extended Test #12 was run.

Comparing these test results to the information in the table often yields an immediate, clear indication of the most probable cause of failure. For example, when loops 24 through 31 have failed, and all other loops and extended tests have passed, the most probable cause is failure of the channel 1 ADC Control assembly. This can be verified by swapping the channel 1 and channel 2 ADC Control assemblies (carefully recabling). Then you should see loops 33 through 40 fail, and all others pass. In this case, replacement of the defective ADC Control assembly is clearly indicated.

Table 6D-3. Data Acquisition Subsystem Diagnostic Routines



KEY:

- |-PT-| Presence test. If the diagnostic firmware fails to find the assembly, this loop fails and all other self tests that include this assembly are skipped.
- |—| This assembly must work for the test to be successful. The test will be skipped and will not show a failure if the assembly is not present.
- |-W-| This assembly must work for the test to be successful. However, in this test there is no presence test for this assembly, the diagnostics assume that it is there. If the assembly is not present, then the loop will fail just as if the assembly functions failed.
- |-0-| Only one of the input pre-amplifiers will be used for the input signal during this test. Starting from the top of the table, the test selects the first pre-amp that has passed all previous tests and uses it for the test. The pre-amp that is used can be determined from the status of the particular loop.

NOTES:

A. The Microprocessor, I/O, and Color Display assemblies must work for these tests to be valid.

B. The Pre-amp is part of the Attenuator assembly.

C. This test must pass for the results of test loops 25-31, 41, and 42 to be valid.

D. This test must pass for the results of test loops 34-40, 43, and 44 to be valid.

E. This test must pass for the results of test loops 27-31, 41, and 42 to be valid.

F. This test must pass for the results of test loops 36-40, 43, and 44 to be valid.

G. The ADC assembly (A4 and A6) adjustments, GAIN, CLK, and GAP must be adjusted fairly well for these test loops to consistently pass.

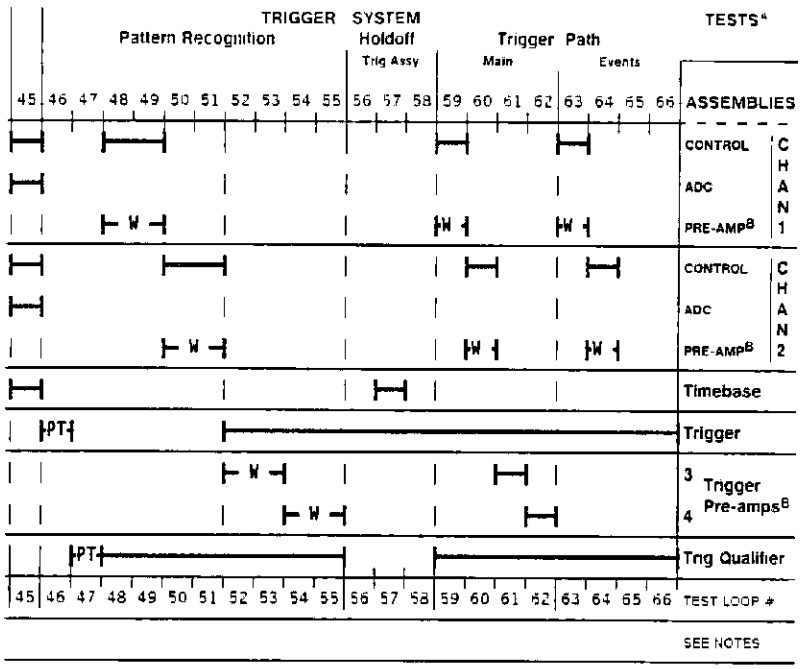
H. This test loop usually fails due to incorrect adjustment of the Delay/Pattern Time oscillator on the Trigger Qualifier assembly. Adjust the oscillator and repeat the test.

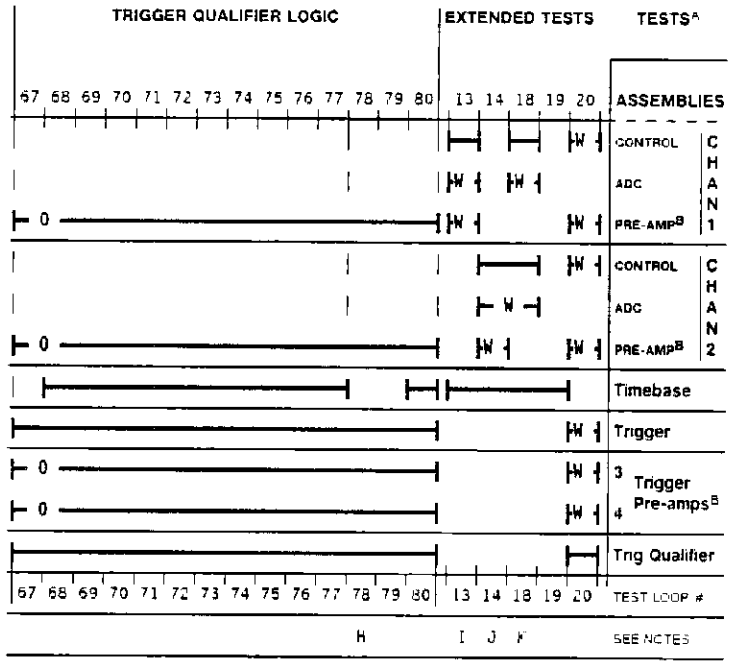
I. For the results of this test to be valid, loop 26 must pass.

J. For the results of this test to be valid, loop 35 must pass.

K. For the results of this test to be valid, loops 26 and 35 must pass.

Table 6D-4. Data Acquisition Subsystem Diagnostic Routines (con't.)





In some cases, several assemblies appear to be suspect from looking at the list of loop failures. In such cases, noting which loops have successfully completed before the first failure often allows you to conclude that at least part of one of the suspect assemblies is working. For example, when loops 41 and 42 fail, the Timebase, ADC, ADC Control and channel attenuator assembles for channel 1 all are suspect. However, if no other loops have failed, the extended test results (particularly 13, 18, and 20) are helpful. In this case, loops 23 through 31 testing channel 1 ADC and ADC Control assemblies have successfully completed before loops 41 and 42 ran. This means that two assemblies that might be suspect are in some sense working. Thus, it is best at this point to focus attention on the channel attenuator assembly, perhaps swapping with channel 2 to see whether loops 43 and 44 then fail.

In any case, if unexpected failures, or no changes result from swapping two assemblies, the cause is probably elsewhere. Factory experience has shown that careful rechecking of the interconnections of the swapped assemblies, or restoring the orginal setup and swapping related assemblies (the ADC assemblies in the example immediately preceeding), are the most effective courses in this situation.

Sometimes the loop failures will not make any sense at all. Try The Core System Plus One (following) to isolate individual assemblies into a "suspect bad" or "known good" status.

If the failure still cannot be isolated, more information is available from the status fields for each loop, and can be analyzed by the factory. If you can not resolve your loop test results, we encourage you to call your nearest HP Service Center. They will help you or obtain information from the factory to resolve the problem.

6D-24. The Core System Plus One

Occasionally, the indications from the loop errors, the extended tests and the display can be so confusing that it is difficult to determine where to start the trouble shooting process. When this happens, it's sometimes best to start with the Core System which means that all assemblies are pulled up except the I/O assembly, microprocessor assembly and one other assembly, usually the Timebase.

CAUTION

Always turn power OFF when seating an assembly, and be sure to use proper ESD precautions.

Once you get this system working with no loop errors associated with the Timebase assembly, then one more assembly or a pair of assemblies, like an ADC and its control assembly, can be reinserted. Again, check for associated loop errors with these particular assemblies.

Once a small system is successful other assemblies can be put down one at a time. Always rerun extended test 12 to write the current loop failures into display memory.

Another useful technique is to put the core subsystem in place, plus one assembly, and check it. If it functions correctly, then remove that assembly and reinsert another assembly (or a pair of assembies) and check them. Using the diagnostic table you should be able to quickly draw some good conclusions about the status of all the assemblies in the system.

Note that if an assembly is not present, after it fails its presence test none of the remaining tests that include that assembly are run.

6D-25. Timebase Tests — Self Test Loops 15 - 22

The system interface circuitry must be functioning properly for most of the rest of the loops (15 -- 80) to be meaningful. The Timebase test uses the 1GHz Oscillator, the Mux/Sync, and the Timebase IC, all of which are on the Timebase assembly. The 100 MHZ originates at the Mux/Sync. Loop 20 tests the 62.5 MHz path, all others test the 100 MHz Mux/Sync path (except 15).

15 Test for Timebase Presence Only
16 Test the Operation of the Pre-Trigger Delay Clock on the Timebase IC
17 Test the Pre-Trigger Delay Time in the Timebase IC
18 Test the Reset of the Coarse and Fine Interpolators
19 Test the Count of the Fine Interpolator at 100 MHZ
20 Test the Count of the Fine Interpolator at 62.5 MHZ
21 Test the Count of the Coarse Interpolator on the Timebase IC at 100 MHZ
22 Test the Count of the Post Delay Counter at 100 MHZ

6D-26. ADC Control Assembly Tests — Self Test Loops 23, 24, 32, 33

The ADC Control assembly performs most of interface and control functions for the ADC assembly. The ADC assembly does not have an address in the same sense as the other assemblies; its address is handled through the Contol 1 cable. The ADC assembly SIB slot locations are not shown in the Display Configuration Screen. There are two control assembly tests for each channel. The interface circuitry to the control assembly and status registers that control the pre-amps (in the attenuator assemblies) are checked in these tests. If either 24 or 33 fail the additional failures associated with the appropriate ADC Assembly are meaningless.

23 Test for ADC Control Assembly 1 Presence Only
24 Test ADC Control Assembly 1 Interface
32 Test for ADC Control Assembly 2 Presence Only
33 Test ADC Control Assembly 2 Interface

6D-27. ADC (Digitizing) Assembly Test — Self Test Loops 25 - 31, 34 - 40

Two identical sets of loops tests both ADC assemblies. Loops 25 - 31 are associated with Channel 1 and loops 35 - 40 are associated with Channel 2. The first test is for presence. The second loop (26, 33) resets the ADC assembly and reads and checks the FISO (Fast In Slow Out memory) phases. These two tests (26, 33) must pass before the remaining ADC tests are meaningful. If both channels have identical failures, then the timebase may be at fault (SEE Diagnostic Table). While it is not imperative that the CLK, GAP and GAIN adjustments are perfect it is a good idea to check them when these loop failures are encountered. The cables can also cause these loops to fail. The remaining loops test the ADC assembly at ever increasing frequency. The higher the frequency, the more critical the clock and gap adjustments become.

Chan 1	Chan 2	Test
25	34	Presence only
26*	35*	FISO low speed reset and read **
27	36	ADC at 10 MHZ
28	37	ADC at 100 MHZ
29	38	ADC at 250 MHZ
30	39	ADC at 500 MHZ
31	40	ADC at 1 GHZ

* Must pass before the remaining loops in this section and Extended Tests 13, 14, and 18 are valid.

** For Firmware Codes after Apr 22 1987 also tests dither bit fan-out

6D-28. Offset Tests — Self Test Loops 41 - 44

This is a more complete test of the data acquisition subsystem. The firmware starts this test with an ADC Reference Cal. Then a DAC on the ADC Control assembly outputs a signal to the pre-amp (in the Attenuator assembly). The ADC assembly digitizes the signal which is compared to the "right answer". The tests consist of a negative and positive signal for each vertical channel.

For firmware date Apr 22 1987 this test can catch stuck FISO Fan-out, ADC or gray-code converter bits. The test does not test the entire FISO memory; this is done using Extended Test 18. For firmware dates after Apr 22 1987 the FISO fan-out test is moved to Extended tests 13 and 14 for data bits and loops 26 and 35 for dither bits.

41 Test Channel 1 with Positive Offset
42 Test Channel 1 with Negative Offset
43 Test Channel 2 with Positive Offset
44 Test Channel 2 with Negative Offset

NOTE: The CLK, GAP, and GAIN must be adjusted properly for these loops to pass. Passing the test does not guarantee that the adjustments are optimal.

6D-29. Factory Test — Self Test Loop 45

45 This test is useful only at the Factory

6D-30. Trigger Tests — Self Test Loops 46 - 66

Each of the four triggers in the HP 54111D has four paths to follow. Three of these paths are associated with the TCLK (TCLOCK_) path: State, Pattern, and Edge.

The fourth path is the trigger complement, LTCLK (LTCLOCK_), brought to the Trigger Qualifier assembly to reduce system noise and for testing. This signal does not go beyond the Trigger Qualifier assembly. The LTCLOCK signals from each trigger source are wire-anded together. A malfunction (or miscabling) of one may, depending on failure mode, generate a self test loop error on all of the LTCLOCK test paths and control circuitry on the Trigger assembly.

The holdoff tests are rather unique in that only the core subsystem and the Trigger assembly are involved (56, 58). This loop tests the system's ability to transmit a signal from the pre-amp (in Attenuator assembly) through the Trigger Qualifier assembly over to the Trigger assembly (via the TCLK cable). If any of the loop tests labeled TCLOCK1 pass, then the signal is arriving at the Trigger Qualifier input and any other loop failure involving that path is a problem other than the pre-amp and cable.

Failure of loops 63-66 only indicates that the Trigger Qualifier assembly is defective.

TRIGGER TESTS

46 Test for Trigger Assembly Presence
47 Test for Trigger Qualifier Assembly Presence
48 Test Channel 1 Trigger through State Mode
49 Test Channel 1 Trigger through LTCLK Status
50 Test Channel 2 Trigger through State Mode
51 Test Channel 2 Trigger through LTCLK Status
52 Test Trigger 3 Trigger through State Mode
53 Test Trigger 3 Trigger through LTCLK Status
54 Test Trigger 4 Trigger through State Mode
55 Test Trigger 4 Trigger through LTCLK Status

ATRIG CABLE TEST

57 Test the interface between the Time base and the Trigger assembly (ATRIG)

HOLDOFF TESTS

56 Test the events hold off counter on the Trigger assembly
58 Test the hold off by time counter on the Trigger assembly

MAIN TRIGGER PATH TESTS

59	Test the main trigger path from Channel 1 to the Trigger flip-flop on the Trigger Assembly.	TCLOCK1 Path
60	Test the Main trigger path from Channel 2 to the Trigger flip-flop	TCLOCK2 Path
61	Test the main trigger path from Trigger 3 to the Trigger flip-flop	TCLOCK3 Path
62	Test the main trigger path from Trigger 4 to the Trigger flip-flop	TCLOCK4 Path

EVENTS DELAY TESTS

63	Test Channel 1 events delay path	TCLOCK1 Path
64	Test Channel 2 events delay path	TCLOCK2 Path
65	Test Trigger 3 events delay path	TCLOCK3 Path
66	Test Trigger 4 events delay path	TCLOCK4 Path

6D-31. Trigger Qualifier Tests — Self-Test Loops 67 - 80

This series of loops tests various modes on the Trigger Qualifier assembly. The diagnostics select the first attenuator assembly that passes it's tests, as a signal source for these tests. The selected source must have passed its three previous tests for the true side of the trigger (TCLK). In the unlikely event that all 4 sources failed the previous tests, this series of tests is not run.

Failure of loop 78 usually indicates that the 100 MHZ Oscillator needs to be adjusted. Loop 78 has the tightests specification, but test failures of 79 and 80 could also indicate a similar adjustment problem.

67 Test State Not Present (State Present Tested Previously)
68 Test Zero-Hold Time of State Present/Not Present
69 Test Delayed by Events = 0
70 Test Delayed by Events = 1
71 Test Delayed by Events = 2
72 Test Delayed by Events = 3
73 Test Delayed by Events = 4
74 Test Delayed by Events = 5
75 Test Delayed by Events = 36
76 Test Delayed by Events = 37
77 Test Delayed by Events = 69
78 Test Delayed by Time = 500 us. Failure is usually due to adjustment problem
79 Test Pattern Present > 100 us (Same as 63 -66)
80 Test Pattern Present < 200 us

6D-32. Extended Tests

Not all Extended Tests are of use to field service personnel. Also, only a few tests are part of the diagnostic table.

The extended tests must be individually executed by the service person. The Extended Tests are part of the Test Menu. To select a test, press ***Extended Test***, ENTER the test number, and press ***Start Test***. The results of the test appear in a few seconds. To exit the test, press ***Stop Test***. Errors or problems appear in red on the screen after the test.

TESTS 0-9. These tests check the interface between the microprocessor and other assemblies and are for factory use.

TEST 10. Test 10 is not really a test but the control of a special function of the warm-up cycle. If certain loop failures occur at initial power up, and continue during the next 15 minutes, a warmup message will be displayed. Every five minutes the instrument will initiate the powerup self test routine (see Instrument Warm-up).

Extended Test 10 can turn the warm-up function on or off. Pressing ***Start Test*** for Extended Test 10 will toggle the function to ***OFF*** or ***ON***, depending on the previous state. Press ***Stop Test*** to return to the test menu.

The default setting is ON. When the warmup function is OFF, failure of the warmup dependent loops will result in the message "Powerup Self Test Failed !", rather than "Instrument Warm-up in Progress mm:ss".

TEST 11. Extended Test 11 is used to verify that all front panel keys and RPG are working. When the test is entered and initiated a keyboard mockup is displayed on the CRT. The mockup consists of boxes corresponding to each key on the front panel. A box lights when it's key is pressed. The RPG mockup consists of a set of radial lines representing a circle. When the RPG is rotated, an O cursor rotates around the circle.

To exit this test at any time the third key from the top, along the right edge of the display, must be pressed twice.

TEST 12. Test 12 resets the system and initiates the powerup self test. The test ends with the instrument in the acquisition menus. If the advisory message "Powerup Self Test Failed" should appear on the display, the failing loops may be found by pressing ***Utility***, ***Test Menu***, then ***Display Errors*** keys.

TESTS 13, 14. These tests (13 and 14 for Channels 1 and 2 respectively) check for stuck bits in the acquisition circuitry. The offset DAC is incremented slowly and the output of the ADC is checked for proper progression of codes. The acquisition circuitry must be working and fairly closely calibrated to obtain valid results from these tests.

For firmware codes later than April 22, 1987, additional data is collected during the test that checks fan-out in the FISO IC. Fan-out is slowing the speed and widening the format of data before storage. Failure of the fan-out test indicates a problem with a FISO or another problem in the data path.

TEST 15. This test is for factory use. It slews all of the DAC outputs so that they can be checked for smooth outputs. Checking DAC outputs is only usefull for component level troubleshooting which is not supported in this document.

TEST 16. Test 16 repeats loops 6-9 continually. It is similar to the test that runs when all of the acquisition assemblies are removed. This is an alternative to removing the assemblies; however it is usually better to remove the assemblies while troubleshooting the core subsystem because the CPU interface to the data acquisition subsystem is eliminated.

TEST 17. This test is for factory use only.

TEST 18. The FISO Test (18) checks the core memory of each FISO. A few errors in a FISO indicates a FISO problem. However, if a whole FISO fails or all FISO bits on one channel, another cause should be suspected; for example, a defective FFCLOCK signal or ADC assembly. The only part of the digitizing hybrid used is the clock signal. Loop 26 must pass for the FISO test information to be valid on Channel 1 and loop 35 for Channel 2.

TEST 19. Test 19 evaluates only the Timebase assembly

TEST 20. Test 20 uses the pattern recognition path on the Trigger Qualifier assembly to determine which trigger source (channels or triggers) is connected to which trigger clock input and with what polarity (differential signals).

This test also checks the FET at the input of the Attenuator assembly preamp. It uses the offset path (channels) or trigger level path (triggers) and checks for a change at the trigger out of the Attenuator assembly. If a problem exists in the signal path in front of the FET, (the passive attenuators) test 20 will not show a defect.

Changes

The following two tests are included in instruments with a firmware code date after April 22, 1987.

TEST 21. Test 21 is for factory use.

TEST 22. Test 22 is not really a test but the control of the powerup self test function. When power is applied the instrument automatically runs all the self tests. This takes time and may not be necessary if the instrument was off for only a short time and is known to be functioning properly.

Extended Test 22 will disable or enable the powerup self tests. The default setting is ENABLED. Pressing ***Start Test*** for Extended Test 22 will toggle the function to ***ENABLED*** or ***DISABLED***, depending on the previous state. Press ***Stop Test*** to return to the test menu.

When the self tests are disabled, the message in the display after powerup self tests are attempted is "Powerup Self Test Disabled!", rather than "Powerup Self Tests Passed!" or Failed.

It should be noted that disabling the tests will also prevent catching warmup failures (see Instrument Warmup).

6D-33. FRONT END TROUBLE-SHOOTING

Once all loop errors and extended test failures have been eliminated, some symptoms may persist. Most of the remaining problems will be found in the front-end subsystem, the channel and trigger attenuators. Below are identified some common symptoms and their causes, and a checkout procedure to ensure that the front end subsystem is functioning properly.

6D-34. Remaining Symptoms

INSTRUMENT WON'T TRIGGER AFTER TRIGGER CAL, OR TRIGGER CAL WON'T COMPLETE

Most probable cause: trigger output failure from a channel or trigger attenuator assembly.

To verify, apply a signal to the suspect attenuator and view the TCLOCK+ output on an oscilloscope. The display should be a square wave with approximately 50% duty cycle. Use cables and adapters from the HP 54100 Family Support Kit to connect to the oscilloscope. If no output signal appears, check cable continuity by swapping cables with another assembly. If problem persists, replace the failed channel or trigger attenuator assembly.

ONE CHANNEL HAS A STRAIGHT TRACE WHICH CAN BE MOVED WITH OFFSET

Most probable cause: FFCLOCK Failure.

Check cable continuity by swapping cables between channels. If the problem does not move with the cable, check the 1 GHz FFCLOCK output of the Timebase assembly. Use a power meter (HP 436A with 8482A sensor) and cables and adapters from the HP 54100 Family Support Kit. If power on suspect output is 3 dB below other outputs on the Timebase assembly, replace the Timebase assembly.

Check with HP Customer Service if the Timebase assembly appears to be working normally and no loop or cable failures are found.

6D-35. Checkout Procedure

If any front end assembly (channel or trigger attenuator assembly) has been replaced, or if other front-end problems are suspected, use this check-out procedure to verify operation of the front end subsystem. Normally, it is not needed unless the front-end is suspected of failure.

INITIAL SELF-CALIBRATION

Perform Probe Tip Cal, Trigger Cal, and Vertical Cal.

AUTOSCALE TEST

1. Attach two 10033A probes (or those supplied with instrument) to channels 1 and 2, and connect to the front panel cal signal. Press AUTOSCALE.

2. The result should be two identical traces of the front panel cal signal, displayed on a dual trace screen. If autoscale does not work there can be several reasons: the front panel cal signal may not work or one or both of the probes may not work. These can be checked by observing the front panel cal on another oscilloscope using the probes.

3. Once the signal is known to be present, and the HP 54111D still does not autoscale, the most probable cause is the failure of trigger calibration. Check for improper cabling as a potential cause of this failure, particularly the solenoid control cables.

IDENTICAL SIGNAL TEST

Once two reasonably similar waveforms have been established on channels 1 and 2, check the vertical sensitivity and offset on each channel to see that they are similar. If the scale factors are not identical, check to see that the probe attenuation factors are set at 10:1

If there is still a problem, the most probable cause of failure is probe-tip calibration failure,

unless other loops have begun to fail. Check for other loop failures and if any are found, refer to the Data Acquisition System Troubleshooting Procedures. If none are found, perform a Probe Tip Cal. If this fails to solve the problem, contact HP Customer Support.

TRIGGER ATTENUATOR TEST

Using the front panel CAL signal and HP 10033A probes, trigger the instrument from triggers 3 and 4. Use a vertical channel for the display. Ensure that positive and negative trigger slopes both work on high sensitivity. It may be necessary to adjust the trigger level to about 400 mV to get the instrument to trigger.

If the instrument will not trigger on triggers 3 or 4, the most probable cause is miscabling of the trigger assembly. Check cabling after referring to cabling diagram. Check for unconnected or misconnect solenoid control cables.

CLICK TESTS

This tests the operation of the solenoid operated switches in the passive dividers of the attenuator assembly.

1. Check to see that the 50Ω/1MΩ switches work. Remove probes from front panel, and switch between 50 and 1M ohm at each channel or trigger menu. A click should come from the attenuator assembly as impedance is switched.

2. If there is no click, check the attenuator cabling for loose, miscabled, or detached connectors, and for debris such as loose screws or other conductive material on top of the attenuators.

3. Check the operation of the vertical sensitivity solenoids on the channel attenuators by varying the vertical sensitivity on each channel, as follows:

   Be sure the probes are disconnected and attenuation factors are 1:1. With a single display, and when using the increment/decrement (arrow) keys, clicks will occur on the channel attenuator assemblies when switching between vertical sensitivities of 20 and 50 mV/div and between 200 and 500 mV/div.

   Normally a click is heard when switching both ways through these transitions. Different circuitry is used when switching up than when switching down. However, if one switching direction is faulty the solenoid will stay in the first direction it switches to and no clicks will be heard at that range transition. If any clicks are not present, check cabling and look for debris in the solenoids.

4. Check the sensitivity solenoids on the trigger attenuators by changing between LO SENS and HI SENS in the trigger menu Select the appropriate channel as the trigger source and use the arrow keys. Clicks should be heard when sensitivity is changed. Failure modes would be the same as those for channel attenuators.

It is usually not be necessary to remove attenuators while determining if the attenuator, cable, or control is causing a failed click test. Use swapping techniques to isolate the fault. Swap one end of the solenoid cables (connected at the top of the Acquisition assembly) and try to control the suspect attenuator with a different channel menu; or swap the entire cable.

6D-36. Attenuator Outrigging

It is possible to quickly check the effect of replacing a channel or trigger attenuator by outrigging a substitute. The following procedure shows how this is done. The required cables are in the 54100 Family Support Kit.

NOTE

If necessary, use the cabling diagram on the top cover of the instrument or the end of section 6A to recable the instrument during or after this procedure.

1. Turn off power and remove top cover.
2. Remove Power Cable from suspect assembly at the attenuator and card cage assembly.
3. Connect two or three (depending on attenuator) Coaxial Cables to the good attenuator assembly.
4. Disconnect the Solenoid Cable at the suspect attenuator.
5. Connect the Solenoid Control Cable to the good attenuator.
6. Extend the Attenuator Power Cable using the extender cable from the support kit.
7. Connect the extended power cable to the proper card cage assembly.
8. Connect the signal and trigger coaxial cables to the proper locations
9. Verify proper operation.

6D-37. HINTS, TRICKS, AND ARCANA

6D-38. Multiplicity of Function

Many parts of the HP 54111D are duplicated. This allows part swapping to troubleshoot for a defective assembly. There are two ADC assemblies, two ADC Control assemblies, and two channel and two trigger attenuator assemblies. Multiple inputs and outputs on these assemblies allow part swapping or recabling to be effective troubleshooting tools.

CLOCK SIGNALS

Two pairs of clock signals (FFCLKs) originate at the Timebase assembly. If the timebase assembly is suspected as a probable cause for a defect and only one channel is affected, it is easy to switch pairs of timebase outputs to the ADC assembly and see whether the symptoms change. If the problem follows the change, then you have correctly identified the Timebase assembly as defective.

The converse is also true, if the problem stays at the same channel, then you have identified the potential problem in either channel. Naturally, it is a good idea to check the CLK, GAIN, and GAP adjustments with any ADC assembly problem.

CONNECTORS AND CABLES

The many identical cables on the HP 54111D can be interchanged to test suspected defective cables.

TRIGGERS

Two signals per channel are used as trigger signals to the Trigger Qualifier assembly. Channel pairs can be interchanged isolate a potential Trigger Qualifier problem or a potential triggering problem in an Attenuator assembly.

For example, suppose you suspect a problem with the channel 1 trigger on the Trigger Qualifier assembly. If Extended Test 20 passed, the channel attenuators must work. If Extended Test 20 failed because of no TCLK #1, swap the trigger pair coaxes for the channel attenuators and run the test again. If the test still fails TCLK #1 the problem is the Trigger Qualifier. If TCLK #1 passes but TCLK #2 fails, the problem is in the channel 1 Attenuator assembly or its control. Swap

entire Attenuator assemblies (by recabling) to finalize the fault location.

The TCLK signals can also be checked with an oscilloscope, comparing the suspect attenuator assembly to a known good one.

DIGITIZING SUBSYSTEM

The digitizing subsystem is composed of the ADC assembly and the ADC Control assembly. At times it is difficult to tell which of the two assemblies is defective. Swapping is a quick and easy way of separating cause.

TRIGGER ATTENUATORS

It is relatively simple to verify a defective trigger attenuator by simply interchanging the cabling, all of it, going to the trigger attenuators. This cabling interchange consists of the trigger solenoid cable, the input sense cables, the TCLOCK and the LTCLOCK cables, as well as the attenuator power cables. The result of this cable interchange will be that the system thinks that Trigger 4 is really Trigger 3. Keeping this in mind and viewing the screen for the symptoms, it's easy to track where the defect moves. The channel attenuators can be interchanged similarly, but the VIN cable location on the ADC assembly makes the process slightly more complicated.

6D-39. System Interface Bus

All the slots in the motherboard are identical except for the slot ID and have identical voltages or signals associated with each pin. This means that defective motherboard slots can be found by rearranging the assemblies in the card cage. The assemblies have been arranged in the order that gives the lowest system noise, but any of the assemblies can work in any of the slots.

Rearranging the assemblies is of course limited by the cabling, which may not accomodate some arrangements.

NOTES

HEWLETT PACKARD

SERVICE MANUAL

HP 54112D

DIGITIZING OSCILLOSCOPE

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed:

2735A

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

Manual Part No. 54112-90903
Microfiche Part No. 54112-90803

PRINTED: December 1987

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

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For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CWA584

GEWERBEAUFSICHTSAMT STUTTGART

- Zentrale Stelle für Sicherheitstechnik und Vorschriftenwesen in Baden-Württemberg -

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Stuttgart, den 02.06.1986
Fernsprecher
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Durchwahl 2050 - 4798
Aktenzeichen: Z 5108/Hewlett-
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Betr.: Durchführung der Rontgenverordnung (RöV)
hier: Bauartzulassung gem. § 7 Abs. 2 RöV

Bezug: Ihr Antrag vom 22.05.1986; PSD US-ab

N a c h t r a g 1

zum Zulassungsschein Nr. BW/218/86/Ro

Aufgrund des § 7 Abs. 2 der Rontgenverordnung vom 1.3.1973 (BGBl. I S. 173) wird die der Firma Hewlett-Packard GmbH, Herrenberger Straße 110, 7030 Böblingen, erteilte Zulassung Nr. BW/218/86/Rö vom 16.01.1986 wie folgt erweitert:

Gegenstand:	Digital-Oszilloskop
Firmenbezeichnung:	HP Typ 54 111 D HP Typ 54 112 D HP Typ 54 120 A
Bauartunterlagen:	Service Manuals Nr. 54 111 - 90 902 vom 21.94.86 Nr. 54 112 - 90 902 vom 24.04.86 Nr. 54 120 - 90 902 vom 26.04.86

Die für den Strahlenschutz wesentlichen Merkmale entsprechen der bereits zugelassenen Ausführung.

Typenbezeichnung der Bildröhre, Auflagen, Hinweise und Befristung ergeben sich aus dem Zulassungsschein Nr. BW/218/86/Rö vom 16.01.1986.

Dieser Nachtrag gilt nur im Zusammenhang mit dem vollständigen Text des o.g. Zulassungsscheins.

Reutter

GEWERBEAUFSICHTSAMT STUTTGART

Dieses Gerät wurde nach den Auflagen der Zulassungsbehörde einer Stückprüfung unterzogen und entspricht in den für den Strahlenschutz wesentlichen Merkmalen der Bauartzulassung. Die Beschleunigungsspannung beträgt maximal 22,3 kV.

Hewlett-Packard
1900 Garden of the Gods Road
Colorado Springs
Colorado 80907, USA

GEWERBEAUFSICHTSAMT STUTTGART

- Zentrale Stelle für Sicherheitstechnik und Vorschriftenwesen in Baden-Württemberg -

Gewerbeaufsichtsamt · Jägerstr. 22 · Postfach 705 · 7000 Stuttgart 1

Stuttgart, den 16.01.1986

Fernsprecher
(0711) 2050 1 (Behördenzentrum)
Durchwahl 2050 - 4798

Aktenzeichen: Z 5108/HP/Ws/Hh
(Bitte bei Antwort angeben)

Firma
Hewlett Packard GmbH
Herrenberger Str. 110/130

7030 Böblingen

Zulassungsschein Nr. BW/218/86/Rö

Gemäß § 9 der Röntgenverordnung vom 01.03.1973 (BGBl. I S. 173) wird die Zulassung der Bauart durch den Bauartzulassungsbescheid vom 16.01.1986 mit Aktenzeichen Z 5108/HP/Ws/Hh für den nachfolgend aufgeführten Störstrahler bescheinigt:

Gegenstand	:	Digital-Oszilloskop
Firmenbezeichnung	:	HP Typ 54110D
Bildröhre	:	Sony Typ M23 JHU 15X
Hersteller	:	Hewlett-Packard 1900 Garden of the Gods Road Colorado Springs Colorado 80907, USA
Betriebsbedingungen	:	Hochspannung: max. 22,3 kV Strahlstrom: max. 0,4 mA
Zulassungskennzeichen	:	BW/218/86/Rö

Die Bauartzulassung ist befristet bis 16.01.1996.

Für den Strahlenschutz wesentliche Merkmale

1. Die Art und Qualität der Bildröhre,
2. die der Hochspannungserzeugung und -stabilisierung dienenden Bauelemente.

Auflagen:

1. Die Geräte sind bezüglich der für den Strahlenschutz wesentlichen Merkmale entsprechend den vorgestellten und geprüften Mustern und Antragsunterlagen herzustellen.

2. Die Geräte sind einer Stückprüfung daraufhin zu unterziehen, ob sie bezüglich der für den Strahlenschutz wesentlichen Merkmale der Bauartzulassung entsprechen.

   Die Prüfung muß umfassen:

   a) Kontrolle der Hochspannung an jedem einzelnen Gerät,

   b) Messung und Dosisleistung nach Festlegung im Bauartzulassungsbescheid.

3. Die Herstellung und die Stückprüfung sind durch den von der Zulassungsbehörde bestimmten Sachverständigen überwachen zu lassen.

4. Die Geräte sind deutlich sichtbar und dauerhaft mit dem Kennzeichen

   BW/218/86/Rö

   zu versehen sowie mit einem Hinweis folgenden Mindestinhalts:

   "Die in diesem Gerät entstehende Röntgenstrahlung ist ausreichend abgeschirmt.
   Beschleunigungsspannung maximal 22,3 kV."

Hinweis für den Benutzer des Geräts:

Unsachgemäße Eingriffe, insbesondere Verändern der Hochspannung oder Auswechseln der Bildröhre können dazu führen, daß Röntgenstrahlung in erheblicher Stärke auftritt. Ein so verändertes Gerät entspricht nicht mehr dieser Zulassung und darf infolgedessen nicht mehr betrieben werden.

Reutter

GEWERBEAUFSICHTSAMT STUTTGART

Dieses Gerät wurde nach den Auflagen der Zulassungsbehörde einer Stückprüfung unterzogen und entspricht in den für den Strahlenschutz wesentlichen Merkmalen der Bauartzulassung. Die Beschleunigungsspannung beträgt maximal 22,3 kV.

Hewlett-Packard
1900 Garden of the Gods Road
Colorado Springs
Colorado 80907, USA

SAFETY CONSIDERATIONS

GENERAL - This is a Safety Class I instrument (provided with terminal for protective earthing)

OPERATION - BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNING

- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates hazardous voltages.

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

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SECTION 1
GENERAL INFORMATION

1-1. INTRODUCTION

This Service Manual contains information necessary to test, adjust, and service the Hewlett-Packard 54112D Digitizing Oscilloscope. This manual is divided into 6 sections as follows:

1 - General Information

2 - Installation

3 - Performance Tests

4 - Adjustments

5 - Replaceable Parts

6A - Instrument Disassembly

6B - Theory of Operation

6C - Service Menus/Keys

6D - Self-Tests/Troubleshooting

Information for operating, programming, and interfacing the HP 54112D is contained in the *HP 54112D Operating and Programming Manual* supplied with each instrument.

The General Information Section includes a description of the HP 54112D Digitizing Oscilloscope, its specifications, characteristics, options, and available accessories.

Listed on the title page of this manual is a Microfiche part number. This number can be used to order 4 X 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement as well as pertinent Service Notes.

1-2. DESCRIPTION

The HP 54112D is a fully programmable, real-time digitizing oscilloscope. It uses sample rates up to 400 Megasamples/second, and has a real-time bandwidth of 100 MHz.

The inputs include four vertical signal channels and an external trigger. The channel inputs can be set up for 50 Ohm impedance with dc coupling or 1 MOhm at 6.5 pf with ac or dc coupling. The signals from the vertical channels and external trigger can be used to provide a qualified trigger for the instrument and can be a pattern of levels and/or edges (see table 1-2).

The color display of the HP 54112D provides 16 colors which are mapped to provide specific colors for specific functions. For example, channel 1 is displayed in yellow, channel 2 in green, channel 3 in orange, channel 4 in pink, and error messages are displayed in red.

To ensure proper operation, extensive self-tests have been designed into the instrument, in addition to internal diagnostics which aid in efficient fault locating and repair should a failure occur.

1-3. SPECIFICATIONS

Instrument specifications are listed in table 1-1. These specifications are the performance standards against which the oscilloscope is tested.

1-4. OPERATING CHARACTERISTICS

Table 1-2 is a listing of the instrument's operating characteristics. These are not specifications, but are typical operating characteristics included as additional information for the user.

1-5. GENERAL CHARACTERISTICS

Table 1-3 gives environmental limits, input power requirements, and mechanical dimensions.

1-6. SAFETY CONSIDERATIONS

This product is a Safety Class 1 instrument (provided with a protective earth terminal). Review the instrument and manual for safety markings and instructions before operating. A page, Safety Considerations, covering general safety concerns, is in the front of this manual. Specific warnings, cautions, and instructions are placed wherever applicable throughout the manual. These precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this instrument. Hewlett-Packard assumes no liability for the customer's failure to comply with these requirements.

1-7. INSTRUMENTS COVERED BY MANUAL

The oscilloscope serial number is located on the rear panel. Hewlett-Packard uses a two-part serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter **(0000A00000).** The prefix is the same for all identical oscilloscopes and changes only when a modification is made that affects parts compatibility. The suffix is assigned and is different for each oscilloscope. This manual applies directly to oscilloscopes with the serial prefix shown on the title page.

An oscilloscope manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial prefix indicates the oscilloscope is different from those described in this manual. The manual for this newer oscilloscope is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer oscilloscope.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-8. OPTIONS

In addition to power cord options, the following options are available for the HP 54112D:

- W30: Additional two years "return to HP" service support commencing at the end of the standard warranty.
- 090: Deletion of the four 10:1 divider probes.
- 908: Rack mounting kit.
- 910: Extra manuals, consisting of a set of operating and programming manuals and a service manual.

1-9. ACCESSORIES SUPPLIED.

The following accessories are supplied with the HP 54112D:

- Four 10:1 divider probes, HP Model No. 10033A.
- One power cord.
- One set of operating and programming manuals.
- One service manual.

1-10. RECOMMENDED TEST EQUIPMENT

Equipment recommended to maintain the HP 54112D is listed in table 1-4. The function for which a piece of equipment is needed (Performance Tests, Adjustments, or Troubleshooting), is also given in the table.

Table 1-1. Specifications

VERTICAL (VOLTAGE)

Bandwidth (-3 dB) **dc-coupled**	dc to 100 MHz
ac-coupled	10 Hz to 100 MHz
Transition Time (10% to 90%)	See "Operating Characteristics"
Deflection Factor (full-scale=8 div)	5 mV/div to 5 V/div continuous
Resolution (% of full scale)	8 bits with averaging to 100 MHz, (0.4%) 6 bits to 100 MHz, (1.6%)
DC Gain Accuracy	±2% of full-scale [1]
DC Offset Accuracy	±1.5% of setting ±0.2 div [2]
DC Measurement Accuracy **single data point**	±Gain Acc. ±Offset Acc. ±Resolution
between data points on same waveform	±Gain Acc. ±2 × Resolution
DC Offset Range	±1 V (5 mV/div to 49 mV/div) ±10 V (50 mV/div to 499 mV/div) ±40 V (500 mV/div to 5 V/div)
Input Coupling	ac/dc/dc-50 Ω
Input Resistance	1 Megohm nominal, or 50 ohms (dc) ±1%
Maximum Safe Input Voltage	±40 Volts @ 1 MΩ (dc + peak ac), 5 Vrms @ 50 Ω

NOTE: *All voltages in the table correspond to a 1:1 attenuation setting. If a 10:1 probe is attached, multiply all voltages by 10. The HP 10033A has a maximum voltage of ±200 V.*

1 When calibrated to probe tip using the front panel calibration source. Applies to major ranges (5 mV/div, 10 mV/div, 20 mV/div, 50 mV/div, 100 mV/div, 200 mV/div, 500 mV/div, 1 V/div, 2 V/div). All settings other than these ranges are ±3% of full-scale.

2 Increases to ±0.4 divisions at 5 mV/div to 9 mV/div

Table 1-1. Specifications (cont.)

HORIZONTAL (TIME)

Digitizing Rate	400 MS/s to 50 S/s
Deflection Factor	2 ns/div to 1 s/div
Memory Depth per Channel	64K max (160 µs @ 400 MS/s)
Pre-trigger Delay Range	−160 µs @ timebase settings 249 ns/div and faster, increasing to −1200 s @ 1 s/div.
Post-trigger Delay Range	160 ms @ timebase settings 500 ns/div and faster, increasing to 10,000 s @ 1 s/div.
Measurement Accuracy	
single channel	2 to 24.9 ns/div - ±500 ps ±0.002% of reading 25 ns/div and slower - ±0.2% of time range[1] ±0.002% of reading
dual channel	2 to 24.9 ns/div - ±1 ns ±0.002% of reading 25 ns/div and slower - ±0.4% of time range[1] ±0.002% of reading

NOTE: *All delta time measurement accuracy specifications include: (1) Timebase accuracy (% of Delta t), (2) Aperture uncertainty and sample clock phase jitter, (3) Reconstruction filter uncertainty, (4) Trigger interpolator jitter (repetitive only), (5) Channel to channel skew (dual channel only).*

1 Time range is TIME/DIV x 10

TRIGGERING

Sources	**Internal Channels 1,2,3,4**	**External Rear Panel Input**
Sensitivity	0.1 of full-scale, dc to 100 MHz	100 mV p-p (1:1) dc to 50 MHz
Trigger Level Range	±3 x full-scale [1,2]	±5 V (1:1) [3]
Input Resistance	NA	200K ohms (nominal) [4]
Maximum Safe Input Voltage	NA	±40 volts (dc + peak ac)
Input Operating Range	NA	±5 V (1:1) dc + peak ac

1 The trigger level range is centered on the Offset level.

2 Trigger level range is limited to ±600 mV from 25 to 49 mV/div inclusive, ±6 V from 250 to 499 mV/div inclusive, and by the maximum safe input voltages at 2 V/div and above.

3 The ±25 mV of hysterisis in the external trigger is not included in this specification.

4 When the external trigger is used with a 1 Mohm 10:1 probe intended for 1 Mohm inputs (HP 10017A/033A/431A) and instrument menus are set up to reflect the 10:1 probe, the software provides the correct scaling to compensate for the difference in input resistance.

Table 1-2. Operating Characteristics.

VERTICAL

Real-time Mode Transition Time (10% to 90%): 3.5 ns.
Calculated by measuring a 3.5 ns risetime source. In the filter mode, a 3.5 ns input risetime is measured as; 4.95 ns = $\sqrt{(3.5)^2 + (3.5)^2}$.
Input Capacitance: 6.5 pF at 1 MOhm input resistance.
Input Protection: 50 ohm input resistor is protected where input rating is exceeded.
Dynamic Performance (typical):

Input Frequency	1 MHz	10 MHz	40 MHz	100 MHz
Effective Bits of Resolution	5 5	5.5	5.2	5.0

Channel-to-channel Isolation: 60dB at 100MHz.

HORIZONTAL

Delay Between Channels: Difference in delay between channels can be front panel calibrated.
Reference Location: The reference point can be located at the left edge, center, or right edge of the display. The reference point is the trigger plus the delay time.

TRIGGER

Trigger Modes
Edge trigger: on any source.
Pattern trigger: A pattern can be specified for all sources. Each source can be specified as high, low, or don't care. Trigger can occur on the last edge to enter the specified pattern or the first edge to exit the specified pattern.
State trigger: A pattern can be specified for any of the sources. Trigger can be set to occur on an edge of either polarity on the source specified as the clock (not one of the pattern sources) when the pattern is present or not present. Setup time for the pattern to be present prior to the clock edge is <4 ns; hold time is zero.

Delayed Trigger
Events-delayed mode: The trigger can be armed by an edge on any source, then triggered by the nth edge on any other source. The number of events, n, can be set from 1 to 16,000,000. Maximum event counting rate is 35 MHz.
Time-delayed mode: The trigger can be armed by an edge on any source, then triggered by the first edge on any other source after a specified time from 50 ns to 160 ms has elapsed.
External Trigger Filter
High Frequency Reject provides an external trigger bandwidth from dc to approximately 4 KHz.

DISPLAY

Data Display Resolution: 501 points horizontally by 256 points vertically.
Data Display Formats
Quad Screen: Channel displays are two divisions high. Each channel is displayed separately.
Dual screen: Channel displays are four divisions high. Channels 1 and 3 are overlaid on the top display and channels 2 and 4 on the bottom.
Full screen: Channel displays are eight divisions high and all are overlaid.

Table 1-2. Operating Characteristics (cont.)

DISPLAY (cont.)

Display Modes

Variable persistence: The time that each data point is retained on the display can be varied from 200 ms to 10 seconds, or it can be displayed in the infinite persistence mode.

Averaging: The number of averages can be varied from 1 to 64. On each acquisition, 1/n times the new data is added to (n-1)/n of the previous value at each time coordinate. Averaging operates continously; the average does not converge to a final value after n acquisitions, except over HP-IB.

Graticules: Full grid, axes with tic marks, frame with tic marks, or graticule off.

Data Reconstruction: On sweep speeds when less than 500 points are acquired across the screen, a built-in digital filter will automatically reconstruct the data in the real-time acquisition modes (single-shot acquisition). The filter "off" position in the display mode will display raw data.

Display Colors: A default color selection is set up. Different colors are used for display background, channels, functions, background text, highlighted text, advisories, markers, overlapping waveforms, and memories. If desired, colors may be changed either from the front panel or over HP-IB.

HP-IB

Data Transfer Rate: 80k bytes/s

MEASUREMENT AIDS

Markers: Dual voltage markers and dual time markers are available. Voltage markers can be assigned to channels, memories, or functions.

Automatic Edge Finders: The time markers can be assigned automatically to any displayed edge of either polarity on any channel. The voltage markers establish the threshold reference for the time markers in this mode.

Automatic Pulse Parameter Measurements: The following pulse parameter measurements are performed automatically (as defined by IEEE standard 194-1977, "IEEE Standard Pulse Terms and Definitions").

Frequency	Overshoot
Period	Peak-to-peak voltage
Duty Cycle	Average voltage
Pos Pulse Width	RMS voltage
Neg Pulse Width	Top voltage *
Rise time	Base voltage *
Fall time	Maximum voltage
Preshoot	Minimum voltage

* only available over the HP-IB.

Waveform Math: Two independent functions are provided for waveform math. The operations provided are +, −, and invert. The vertical channels or any of the waveform memories can be used as operands for the waveform math.

SETUP AIDS

Presets: Vertical deflection factor, offset, and trigger level can be preset independently on each channel for ECL and TTL levels.

Auto-Scale: Pressing the Auto-Scale button causes the vertical and horizontal deflection factors and the trigger source to be set for a display appropriate to the signals applied to the inputs. Requires a duty cyle greater than 0.1% and frequency greater than 50 Hz. Operative only for relatively stable input signals.

Save/Recall: Ten front panel setups may be saved in non-volatile memory. If Auto-Scale is inadvertently pressed, pressing Recall followed by Auto-Scale, restores the instrument to the state prior to the first Auto-Scale.

Table 1-3. General Characteristics

ENVIRONMENTAL CONDITIONS

Temperature
Operating: 0°C to +45°C (+32°F to +113°F)
Non-operating: −40°C to +75°C (−40°F to +167°F)

Humidity
Operating: up to 95% relative humidity (non-condensing) at +40°C (+104°F)
Non-operating: up to 90% relative humidity at +65°C (+149°F).

Altitude
Operating: up to 4600 meters (15,000 ft)
Non-operating: up to 15,300 meters (50,000 ft).

Vibration:
Operating: Random vibration 5-500 Hz, 10 minutes per axis, −0.3 Grms.
Non-operating: Random vibration 5-500 Hz, 10 minutes per axis, −2.41 Grms; resonant search 5 to 500 Hz swept sine, one octive/minute sweep rate, 5 minute resonant dwell at 4 resonances per axis.

POWER REQUIREMENTS

Voltage: 115/230 V ac, −25% to + 15%, 48-66 Hz.
Power: 350 watts maximum, 700 VA maximum.

WEIGHT

Net: approximately 25 kg (56 lb).
Shipping: approximately 32 kg (70 lb).

DIMENSIONS

Refer to the outline drawings.

NOTES:

1. *Dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP field engineer.*
2. *Dimensions are in millimetres and (inches).*

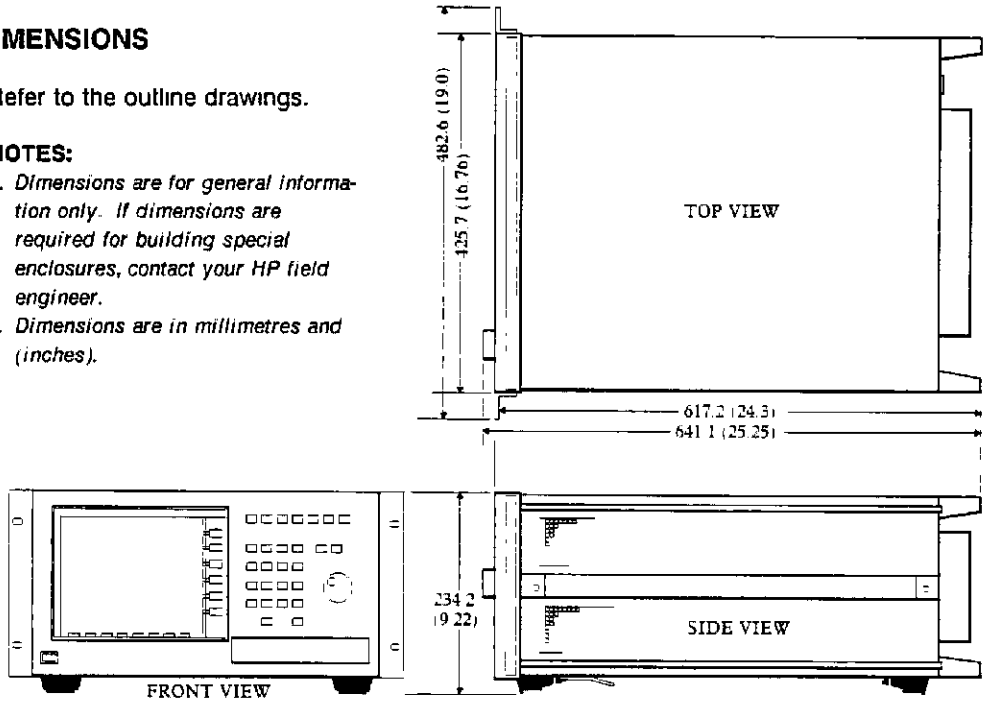


Table 1-4. Recommended Test Equipment.

Equipment Required	Critical Specifications	Recommended Model	Use*
Signal Generator	100 KHz to 100 MHz, <-34 dBm to >+12 dBm, timebase within 5 ppm	HP 8656B check time-base to be within 5 ppm	P
Power Meter and Sensor	100 KHz to 100 MHz, <-28 dBm to >+9 dBm	HP 436A/8482A	P
DC Supply	±175 mV to ± 100V, 0.1 mV resolution	HP 6115A	P,A
Digital Multimeter	Better than ±0.05% accuracy	HP 3468A	P,A,T
Pulse Generator	≤1% perturbation after 10 ns 0 to -300 mV output	Tektronix PG 506	A
Oscilloscope	General purpose 300 Mhz bandwidth	HP 54201A	T
Power Splitter	Outputs differ by <0.15%	HP 11667A	P
Attenuator	10 ±0.6 dB at 50 MHz	HP 8491B	P
Divider Probe	10:1, 1 MΩ	HP 10431A/033A/017A	P,A,T
Termination	BNC 50Ω feedthrough	HP 10100C	P,A
Cables (2)	BNC (m) >36 inch (equal Length)	HP 10503A	P,A
Cable	Type N (m) 24 inch	HP 11500B	P
Adapter (2)	N (m) to BNC (f)	HP 1250-0780	P
Adapter	N (m) to BNC (m)	HP 1250-0082	P
Adapter	N (f) to BNC (m)	HP 1250-0077	P
Adapter (2)	BNC (f) to banana (m)	HP 1251-2277	P
Adapter	BNC tee (m) (f) (f)	HP 1250-0781	P,A
Adjustment tool	Non-metallic (for display)	HP 8710-1355	A
Adjustment tool	(for attenuator)	HP 8710-1515	A
Product Support Kit	No substitute	HP 54100-69006	T

* P = Performance Tests, A = Adjustment Procedures, T = Troubleshooting

SECTION 2
INSTALLATION

2-1. INTRODUCTION

This section contains the initial operation information for the HP 54112D Digitizing Oscilloscope. Included are power and grounding requirements, operating environment requirements, cleaning methods and storage and shipment requirements.

2-2. PREPARATION FOR USE

POWER REQUIREMENTS. The instrument requires a power source of either 115 or 230 VAC, -25% to +15%; single phase, 48 to 66 Hz; 350 watts, 700 VA maximum.

CAUTION

The instrument may be damaged if the Line Voltage Select Switch is not properly set to match the input line voltage.

LINE VOLTAGE SELECTION. Before turning ON the instrument verify that the Line Voltage Select Switch on the rear panel matches the input line voltage.

POWER CABLE. This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See table 2-1 for option numbers of power cables and plug configurations available. Part numbers for each cable option are also listed in the parts list in Section VI.

2-3. OPERATING ENVIRONMENT

The operating environment is noted in table 1-3. Note should be made of the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Protection should be provided against internal condensation.

2-4. CLEANING REQUIREMENTS

When cleaning the instrument, CAUTION must be exercised on which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE damaged.

CAUTION

BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuitry if it seeps under the keys.

2-5. STORAGE AND SHIPMENT

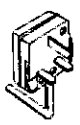
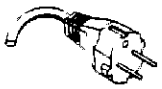
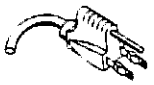
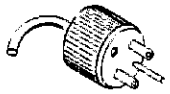
2-6. Environment

The instrument may be stored or shipped in environments within the following limits:

Temperature: -40 to +75° C (-40 to +167° F)
Humidity: Up to 90% at 65° C (+149° F)
Altitude: Up to 15,300 metres (50,000 feet)

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause malfunction if the instrument is operated under these conditions.

Table 2-1. Power Cord Configurations

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 250V 900 	8120-1351 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore
OPT 250V 901 	8120-1369 8120-0696	Straight *NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray	Australia, New Zealand
OPT 250V 902 	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So Africa, India (Unpolarized in many nations)
OPT** 125V 903 	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical) UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Mexico, Philippines, Taiwan,
OPT** 250V 904 	8120-0698	Straight *NEMA6-15P	90/228	Black	United States, Canada
OPT 250V 905 	8120-1398 8120-1625	CEE22-V1 (System Cabinet Use) 250V	30/76 96/244	Jade Gray	For interconnecting system components and peripherals. United States and Canada only
OPT 250V 906 	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 220V 912 	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark
OPT 250V 917 	8120-4211 8120-4600	Straight SABS164 90°	79/200 79/200	Jade Gray	Republic of South Africa India
OPT 100V 918 	8120-4753 8120-4754	Straight Mitl 90°	90/230 90/230	Dark Gray	Japan

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug
**These cords are included in the CSA certification approval of the equipment
E = Earth Ground
L = Line
N = Neutral

AC CABLES3

2-7. Packaging

TAGGING FOR SERVICE. If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

ORIGINAL PACKAGING. If the original packing material is not available or is unserviceable, material identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for servicing, attach a tag showing owner (with address), model number, complete instrument serial number, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials.

a. Wrap instrument in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION 3
PERFORMANCE TESTS

3-1. INTRODUCTION

The procedures in this section test the instrument's electrical performance using specifications in Section I as performance standards. The specification is also listed at the beginning of the test for reference.

3-2. CALIBRATION CYCLE

This instrument requires periodic verification of performance. The instrument should be checked using the following performance tests yearly or every 2000 hours of operation. Amount of use, environmental conditions, and the user's experience concerning need for calibration will contribute to performance verification requirements.

3-3. CALIBRATION REQUIREMENTS

To fully calibrate the HP 54112D, follow these steps:

1. Ensure front panel CAL signal is 800 ±2 mV. Follow the Calibrator Amplitude Adjustment procedure, section 4, but do not adjust unless outside the 2 mV tolerance.

2. Check the Flatness Adjustment, section 4. Do not adjust unless needed.

3. Perform these procedures per section 4:
   - Vertical Cal
   - Probe Tip Cal
   - Offset Cal
   - Trigger Cal
   - Channel Skew Alignment

4. Perform all Performance Test procedures and record the results.

For a MIL STD calibration, do all performance tests first and record results in the performance test record. Then perform the calibration as above.

3-4. TESTS AFTER REPLACEMENTS

Some performance tests may be necessary after replacement of an assembly, though it may not be necessary to test the entire instrument. Table 3-1 (next page) gives the minimum performance testing required after replacement of major assemblies.

3-5. EQUIPMENT REQUIRED

Equipment required for performance tests is listed in table 1-4. Any equipment that satisfies critical specifications given in the table may be substituted.

3-6. PROBES USED DURING TESTS

The HP 54112D uses a ring around the input BNC to sense a grounded contact pin on certain 10:1 probes, such as the HP 10431A, or other probes shipped with the instrument. The HP 54112D scales the input properly when those 10:1 probes are being used.

Some parameters of the HP 54112D are specified with the instrument calibrated through a probe to the front panel CAL signal or a 10 V supply. Therefore, some of the performance tests require the use of a 10:1 divider probe and using the Probe Tip Cal to calibrate the instrument with that probe.

In the event that the probes shipped with the HP 54112D are not available for performance tests, any probe with comparable specifications may be used, whether it has the grounded contact pin or not. Probe Tip Cal assumes that a 10:1 probe is being used so the calibration is properly done. The performance test procedures are written to allow use of unsensed probes, such as the HP 10017A.

Calibration with the probe is a user function. The HP 54112D can be calibrated to other probes once it is returned to the user.

Table 3-1. Performance Tests Required After Assembly Replacement.

PERF. TEST / ASSEMBLY	Calibrator Amplitude	Input Res.	Measurement Accuracy	Offset Accuracy	Band-width	Timebase Accuracy	Trigger Sens.
Acquisition			RCO	RCO	RCO		
Timebase/Trig	#					X	EXT Trig only
Attenuator		RCO	RCO	RCO	RCO		RCO

NOTE: The **Microprocessor, Input/output,** and **Color Display** assemblies, **Color CRT Module**, and **Power Supplies** do not require any performance tests after replacement.

KEY: RCO Replaced Channel Only. Perform the test only on the channel in which the assembly was replaced

\# Timebase/trigger assembly replacement calls for calibrator amplitude adjustment. Adjustment sets calibrator amplitude with greater accuracy than the performance test requires so the performance test is unnecessary.

X This test must be performed.

3-7. PERFORMANCE TEST RECORD

Results of performance tests may be entered in the Performance Test Record (table 3-2) at the end of the procedures. The Test Record lists the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and when testing after repairs or adjustments.

3-8. ONE-KEY POWER UP

A one-key power up is a procedure where any one key is held depressed when the power is turned on. The key is held depressed until the power up cycle completes; "Powerup Self Test Passed!" (or Failed) is displayed. This is done to preset or reset the instrument to default conditions and prevent previous setups from interfering with the next test. It also simplifies the instrument setup procedure.

The one-key power up is a part of many procedures and should be performed like any other procedural step.

You can save some time by performing the first one-key power up then storing the setup. This avoids the wait for actual power up. The procedures however, expect the instrument to be in a certain menu after power up. After recalling the stored setup the instrument will not be in the same menu as it would be after the power up. The next steps in the procedure, if they involve keystrokes, may need to be altered to reflect the different starting point. This method is recommended for experienced users of the instrument.

3-9. PERFORMANCE TEST PROCEDURES

Performance test procedures start with the next paragraph. Any one, or all procedures may be done in any order.

NOTE

Allow instrument to warm up for at least 15 minutes prior to beginning performance tests.

3-10. CALIBRATOR AMPLITUDE

Description:

This procedure checks the amplitude of the front panel calibrator. This signal is used to run calibration routines in the instrument.

When being adjusted, this signal has a tighter specification than that required for passing this test. This is done to maintain the performance specification for the entire calibration cycle (see Calibration Requirements).

Specification:

+0.8 ±0.004 Vdc

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Voltmeter	Better than 0.05% accuracy	HP 3468A

Procedure:

1. Connect the voltmeter input to the front panel calibrator signal. Connect the voltmeter ground to the CHAN 1 input BNC ground.
2. With the softkeys, press ***more, Utility, Test Menu, Extended Tests***, 21 and ENTER, and ***Start Test***.
3. The CAL signal should be +0.8 ±0.004 Vdc; record the value.
4. Press ***Stop Test*** then ***Exit Test Menu*** to return to normal functions.

3-11. INPUT RESISTANCE

Description:

A four-wire resistance measurement is used to verify accuracy of the channel 50Ω input resistance.

Specification:

50Ω ±1%

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Multimeter	Measure resistance better than 0.25% accuracy	HP 3468A
Cables (2)	BNC	HP 10503A
Adapter	BNC Tee (m)(f)(f)	HP 1250-0781
Adapter (2)	BNC (f) to banana (m)	HP 1251-2277

Procedure:

1. Set up the multimeter to make a 4-wire resistance measurement.
2. Connect the BNC tee to the CHAN 1 BNC of the HP 54112D and connect the BNC cables to the female ends of the BNC tee.
3. Use the BNC-to-banana adapters to connect the free ends of the BNC cables to the 4-wire resistance connectors on the multimeter.
4. Press ***Chan 1*** and verify or set ***Input Impedance*** of ***50Ω***. The reading on the multimeter should be 50Ω ±0.5Ω.
5. Repeat steps 2 through 4 for channels 2, 3, and 4.

3-12. VOLTAGE MEASUREMENT ACCURACY

Description:

This test verifies the voltage measurement accuracy of the instrument with a 10:1 probe at the input. Accuracy consists of gain accuracy and resolution. The test uses positive and negative DC levels so that any OFFSET errors are nulled.

If any part of this test fails on a channel, perform the Flatness Adjustment and vertical software cals (Vertical Cal, Probe Tip Cal, Offset Cal, section 4) for that channel and retest.

Specification: [1]

Averaging: ±2.8% of full scale[2] [2% gain + 2 × resolution(0.4%)]
Real-time:[3] ±5.2% of full scale[2] [2% gain + 2 × resolution(1.6%)]

1 - Major ranges only and with a 10:1 probe at the input; 2 - Full scale = 8 div × V/div; 3 - Not tested

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Supply	±175 mV to ±70 Vdc 0.1 mV resolution	HP 6115A
DC Voltmeter	Better than 0.1% accuracy	HP 3468A
Oscilloscope Probe	10:1	HP 10431A/033A/017A

Procedure:

A positive, followed by a negative, voltage is applied at each V/div range. Each voltage is measured and the difference is used to check gain on that range. With a supply like the HP 6115A, polarity is changed by floating the supply and reversing the connection of the probe to get the negative value. If you are using a supply with switchable polarity reversing the probe connection is not necessary.

1. Perform a one-key power up* to set instrument to default conditions, then set the following additional parameters.

*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1,2,3,4	Display	Chan 1 On/Chan 2,3,4 Off
Timebase	TIME/DIV	2 us/div
Display	NUMBER OF AVERAGES Screen	64 Single
Delta V	V Markers	On

2. Connect the 10:1 divider probe to the CHAN 1 input of the HP 54112D and the front panel CAL signal and press ***more.***

3. If you are using an HP 10431A or 10033A probe, skip this step. Press ***Utility, Probe Menu,*** and ***CHAN 1 PROBE ATTN,*** then in the ENTRY keys, 10 and ENTER.

4. Calibrate the HP 54112D to the 10:1 probe being used for the test. Press ***Utility, Cal Menu, Probe Tip Cal, Calibrate Probe Tip CHAN 1,*** and ***Continue.*** When calibration is done press ***Exit, more, Chan 1,*** and ***VOLTS/DIV.***

5. Set the power supply to 0.0 V and remove any connection between the output and ground.

6. Use the following table for steps 7 through 17. For the first V/div setting it is necessary to set the supply within ±0.1 mV with the voltmeter.

SCOPE V/div	INPUT VOLTAGE SETTINGS#	Δ	MEASURED Δ VOLTAGE LIMITS TOLERANCE	MIN		MAX
50 mV	±175 mV*	350 mV	±12 mV	338 mV	_____	362 mV
100 mv	±350 mV	700 mV	±24 mV	676 mV	_____	724 mV
200 mv	±700 mV	1.40 V	±50 mV	1.35 V	_____	1.45 V
500 mV	±1.75 V	3.50 V	±120 mV	3.38 V	_____	3.62 V
1 V	±3.5 V	7.00 V	±240 mV	6.76 V	_____	7.24 V
2 V	±7.0 V	14.0 V	±500 mV	13.5 V	_____	14.5 V
5 V	±17.5 V	35.0 V	±1.2 V	33.8 V	_____	36.2 V
10 V	±35.0 V	70.0 V	±2.4 V	67.6 V	_____	72.4 V
20 V	±70.0 V	140 V	±5 V	135 V	_____	145 V

#For a supply without a polarity switch (like the HP 6115A) polarity is changed by switching the probe tip and ground of the 10:1 probe

*Confirm this setting with the voltmeter

7. Connect the probe to the output of the supply (probe tip to +, ground clip to −).

8. Press ***Chan 1*** and ENTER the SCOPE V/div range with the ENTRY keypad.

9. Set the supply to the positive value of the voltage in the INPUT VOLTAGE - SETTINGS column of the table and press CLEAR DISPLAY to restart averaging.

10. Press ***more, Delta V,*** and ***MARKER 2 POSITION.*** When ***#Avgs*** = 64, use the knob and cursors to set the marker over the trace. With the marker at best overlap the most overlap color will show.

11. Set the supply to the negative value of the voltage in the INPUT VOLTAGE - SETTINGS column of the table (or reverse the probe connections, probe tip to − and ground clip to +) and press CLEAR DISPLAY.

12. Press ***MARKER 1 POSITION*** and overlap the trace with the marker.

13. Read and record the ΔV= in the lower right corner of the screen. It should fall within the specified limits in the table above.

14. If you are using a supply with no polarity switch reverse the probe connection (probe tip to +, ground to −).

15. Press ***more*** and repeat steps 7 through 14 with the rest of the V/div rannges in the table.

16. Press ***more, Chan 1, Display (Off), Chan 2***, and ***Display (On)***.

17. Repeat steps 2 through 15 for the remaining channels, substituting channel numbers appropriately.

18. Set the dc power supply to 0.0V.

19. If you are doing the Offset Accuracy tests next, skip this step. If probe attenuation factors (step 3) were entered, set them back to 1.000 to avoid improper results in further tests. Press ***more, Utility, Probe Menu***; then, for all channels, ***CHAN X PROBE ATTN*** and in the ENTRY keys, 1 and ENTER.

3-13. VERTICAL OFFSET ACCURACY

Description:

This test verifies vertical offset accuracy. Resolution is a part of the specification for this test.

Offset Cal, a front panel software cal which can be done by the user, can affect the outcome of the Vertical Offset Accuracy test. If the Offset Cal is done with an inaccurate dc source the instrument may fail this test. If the test fails, for each failed channel perform the Offset Cal (section 4) then repeat the Vertical Offset Accuracy test before troubleshooting the instrument.

Specification:

With a 10:1 probe at the input.

Averaging: ±1.5% of setting ± 0.2 div[1] ±Resolution[0.4% of full scale (8 div.)]
Real-time:[2] ±1.5% of setting ± 0.2 div[1] ±Resolution[1.6% of full scale (8 div.)]

1 - ±0.4 div from 50 to 90 mV/div; 2 - Not tested

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Supply	±300 mV and ±9.5 V 1.0 mV resolution	HP 6115A
Oscilloscope Probe	10:1	HP 10431A/033A/017A

Procedure:

1. Perform a one-key power up* to set instrument to default conditions, then set the following additional parameters.

   *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1,2,3,4	Display	Chan 1 On/Chan 2,3,4 Off
Timebase	TIME/DIV	2 us/div
Display	NUMBER OF AVERAGES Screen Graticule	64 Single Grid

2. Connect the 10:1 probe to CHAN 1 of the HP 54112D.

3. If you are using an HP 10431A or 10033A probe skip this step. Press ***more, Utility, Probe Menu***, and ***CHAN 1 PROBE ATTN***, then ENTER 10.

4. If you just did the Voltage Measurement Accuracy tests skip this step. Calibrate the HP 54112D to the 10:1 probe being used for the test. Press ***Utility, Cal Menu, Probe Tip Cal, Calibrate Probe Tip CHAN 1***, and ***Continue***. When calibration is done, press ***Exit, more, Chan 1***, and ***VOLTS/DIV***.

5. Use the following table for steps 6 through 13.

SUPPLY VOLTAGE	MEASUREMENT LIMITS TOLERANCE	MAX		MIN
0.00 V	±24 mV	-24 mV	_____	24 mV
300 mV	±28 mV	272 mV	_____	328 mV
-300 mV	±28 mV	-272 mV	_____	-328 mV
-9.50 V	±170 mV	-9.33 V	_____	-9.67 V
9.50 V	±170 mV	9.33 V	_____	9.67 V

6. Connect the probe ground clip to the probe tip.

7. Press ***VOLTS/DIV*** and ENTER 100 mV.

8. Press ***OFFSET*** and use the arrow keys to set the trace exactly to center screen when ***#Avgs = 64***. The ***Offset*** reading should be within the specification for 0.00 V in the table. Record the reading.

9. Set the supply to 0.00 V then connect the voltmeter and probe to the output of the supply (probe tip to + and ground clip to −).

10. Set the supply voltage and scope offset to the next value in the table. It is easiest to enter the offset value directly, using the key pad.

11. Adjust the offset using the knob and arrow keys until the trace is at center screen when ***#Avgs = 64***.

12. The ***Offset*** = value should be within the limits given in the table. Record the reading.

13. Repeat steps 10 through 12 with the other values in the above table. If using a supply with no polarity switch, for negative voltages reverse the probe tip and ground at the supply.

14. Remove the probe from the power supply and connect the probe ground to the probe tip.

15. Use the following table for steps 16 through 23. Follow steps 16 through 21 for a pass/fail test, or steps 16 and 17a through 20a for a precise test. The pass/fail test is faster. If a range is close to the specification for a pass/fail test, make a precise test of that range.

V/div	PASS/FAIL LIMITS(div)	PRECISE LIMITS		
50 mV	±0.4	-22 mV	_____	+22 mV
100 mV	tested previously			
200 mV	±0.2	-47 mV	_____	+47 mV
500 mV	±0.2	-120 mV	_____	+120 mV
1 V	±0.2	-240 mV	_____	+240 mV
2 V	±0.2	-470 mV	_____	+470 mV
5 V	±0.2	-1.2 V	_____	+1.2 V
10 V	±0.2	-2.4 V	_____	+2.4 V
20 V	±0.2	-4.7 V	_____	+4.7 V

NOTE

Note that the minor division marks on the display are at 0.25 division increments and the specifications in the PASS/FAIL column of the table are 1.0, 0.4, and 0.2 divisions.

16. Press ***VOLTS/DIV*** and ENTER 50 mV.

PASS/FAIL TEST

17. Press ***OFFSET*** and ENTER 0 V.

18. Check the distance of the trace from the center horizontal axis. It should be within the DIVISIONS limits shown in the table above when ***#Avgs = 64***.

19. If trace is within limits in step 18, record the range as passing. If it appears to be outside the limits, make a precise test of this range (steps 17a and 18a at right), then continue with step 20.

20. Repeat steps 18 and 19 for each V/div range in the table.

21. After checking all ranges go to step 22.

PRECISE TEST

17a. Press ***OFFSET*** and use the cursor keys to set the trace to exactly center screen when ***#Avgs = 64***.

18a. Check that the Offset reading is within the specification in the LIMITS - VOLTAGE column. Record the reading and set offset to 0.0 V.

19a. Repeat steps 17a and 18a for each V/div range in the table. If if you are doing a precise test of all ranges it is not necessary to set the offset to 0.00 V (step 18a) after each range check.

20a. After checking all ranges go to step 22.

22. Press ***Chan 1***, ***Display (Off)***, ***Chan 2***, and ***Display (On)***.

23. Repeat steps 2 through 22 for channels 2, 3, and 4 substituting channel references as appropriate.

24. If probe attenuation factors (step 3) were entered, set them back to 1.000 to avoid improper results in further tests. Press ***more, Utility, Probe Menu***; then for all channels ***CHAN X PROBE ATTN*** and in the ENTRY keys, 1 and ENTER.

3-14. BANDWIDTH

Description:

This test checks the -3 dB bandwidth of the HP 54112D. If the test fails, consult an HP Customer Service representative.

Specification: (-3dB bandwidth point)
dc coupled, 0 to 100 MHz; ac coupled*, 10 Hz to 100 MHz
* Not tested

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Signal Generator	100 KHz to 100 MHz -22 to +12 dBm	HP 8656B
Power Meter/Sensor	100 KHz to 100 MHz <-28 dBm to >+8 dBm	HP 436A/8482A
Power splitter	Outputs differ by <0.15dB	HP 11667A
Cable Adapter	Type N(m) 24 inch N(m) to BNC(m)	HP 11500B HP 1250-0082

Procedure:

1. Zero and calibrate the power meter using the Power Reference on the meter and the REF Cal Factor on the power sensor.

2. Connect the equipment as shown in the following diagram.

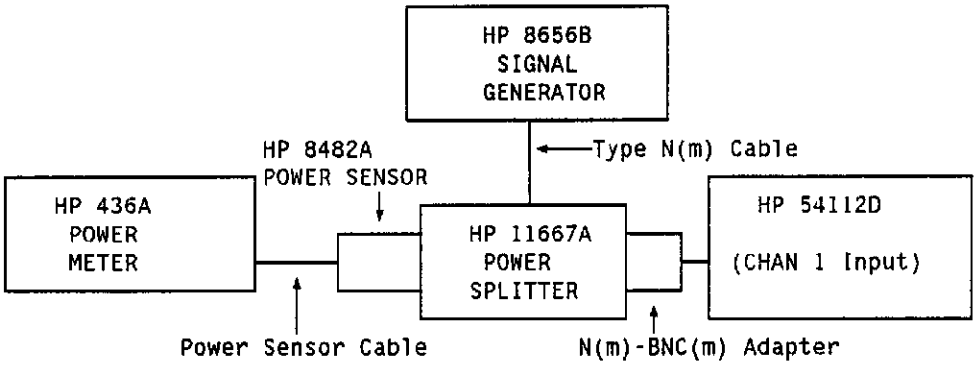


Figure 3-1. Bandwidth Test Connections.

3. Perform a one-key power up* to set instrument to default conditions, then set the following additional parameters in the order given.
*Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed

MENU SELECT	FUNCTION SELECT	SETTING
Display	Disp Mode NUMBER OF AVERAGES Screen	Repetitive 8 Single
Chan 1,2,3,4	Display VOLTS/DIV Input Impedance	Chan 1 On/Chan 2,3,4 Off 200 mvolts/div 50Ω
Timebase	TIME/DIV	2 us/div
Trigger	Trig Src	Chan 1
Delta V	V Markers Preset Levels	On 0-100%

4. Set up the 8656B signal generator with a 100 kHz signal at +12 dBm. The HP 54112D should display two cycles of a sinewave signal.

5. Set power meter Cal Factor % to 100 kHz value from the cal chart on the probe and press dB[REF] to set a 0 dB reference.

6. Press ***more***, ***Delta V*** and ***Auto Level Set***. The V Markers will mark the top and bottom of the signal. Note the ΔV= value at the bottom of the screen.

7. Change the frequency of the signal generator to 100 MHz and change the power meter Cal Factor to the 100 MHz % value from cal chart.

8. Press ***more***, ***Timebase*** and ***TIME/DIV*** and ENTER 5 ns.

9. Press ***more*** and ***Delta V***. Increment the signal generator output amplitude while occasionally pressing ***Auto Level Set*** on the HP 54112D.

10. When the ΔV= value (bottom of screen) is the same as noted in step 6, read and record the level on the power meter. It should be less than +2.85 dB from the zero reference.

11. Connect the signal to the CHAN 2 BNC input. Press ***more*** and set the following on the HP 54112D.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1 Chan 2	Display Display	Off On
Timebase	TIME/DIV	2 us/div
Trigger	Trig Src	Chan 2

12. Repeat steps 4 through 11 for channels 2, 3, and 4, substituting channel references as appropriate. Omit step 11 after channel 4 has been tested.

3-15. TIME MEASUREMENT ACCURACY

Description:

Time measurement accuracy is checked by correlating time measurements with a frequency-stable signal.

Channel Skew Alignment is a front panel firmware calibration that can be done by the user and it will affect the channel-to-channel time accuracy of the instrument. The user may calibrate the time reference between channels to suit his measurements. If the Channel-to-Channel Accuracy part of the Time Measurement Accuracy tests is done without recalibrating Channel Skew, the test will be done with the users calibration and the instrument may fail.

To return the instrument to traceable calibration before the Time Measurement Accuracy tests, use the Channel Skew Alignment procedure in the adjustment procedures, section 4 of this service manual. Channel Skew can be done without affecting any other performance tests or adjustments.

If the tests fail after Channel Skew is calibrated, consult an HP Customer Service representative.

Specification:

Single Channel:

2 to 24.9 ns/div - ±500 ps ±0.002% of reading
25 ns/div and slower - ±0.2% of time range* ±0.002% of reading

Dual Channel:

2 to 24.9 ns/div - ±1.0 ns ±0.002% of reading
25 ns/div and slower - ±0.4% of time range* ±0.002% of reading

* Time range is TIME/DIV x 10

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Signal Generator	1.0 MHz and 50 MHz time base accuracy - 5 ppm	HP 8656B-check time base to be within 5 ppm
Power splitter	----------	HP 11667A
Cable Adapter (2)	Type N(m) 24 inch N(m) to BNC(f)	HP 11500B HP 1250-0780
Cables (2) Termination	BNC(m) >24 inch (equal length) BNC 50Ω feedthrough	HP 10503A HP 10100C

Procedure:

1. Set the signal generator frequency to 50 MHz and amplitude to 120 mV.

2. Connect the signal generator to the input of the power splitter with the type N cable. With the N-to-BNC adapters and the BNC-to-BNC cables, connect the outputs of the power splitter to the CHAN 1 and CHAN 2 inputs.

3. Perform a one-key power up* to set instrument to default conditions.
   *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed

4. Press ***Chan 1, 2, 3, 4*** menu keys in turn and set the ***Input Impedance*** on all to 50Ω.

5. Press AUTOSCALE to establish the display, then set or confirm the following parameters in the order given.

MENU SELECT	FUNCTION SELECT	SETTING
Display	NUMBER OF AVERAGES Screen	8 Single
Chan 1,2,3,4	Display VOLTS/DIV OFFSET	Chan 1 On/Chan 2,3,4 Off 20 mvolts/div 0.00 V
Timebase	TIME/DIV	5 ns/div
Trigger Ch 1,2,3,4 Ext. Trig	Trig Src TRIGGER LEVEL Slope	Chan 1 0.00 V (all channels and ext) Pos (all channels and ext)

SHORT DELAY - TIMEBASE ACCURACY

6. Press ***Trigger*** and ***TRIGGER LEVEL***. Adjust Chan 1 Trigger Level so the positive edge crosses exactly at center screen.

7. Press ***Timebase*** and ***DELAY***. With the entry keys, set Delay to each setting in the following table. Check that the positive edge crosses the horizontal graticule line within the "Divisions" specification from center screen. Record a pass or fail for each delay setting.

   If you want to measure the error, for each Set Delay value adjust the delay to make the positive edge cross at center screen. Record the difference between the instrument reading and the Set Delay value. Each should be within the "Time" specification.

Set Delay	Specification Divisions	Specification Time	Record
20 ns	±0.1	±501 ps	_____
40 ns	±0.1	±501 ps	_____
60 ns	±0.1	±502 ps	_____
80 ns	±0.1	±502 ps	_____
100 ns	±0.1	±502 ps	_____
1.0 µs	±0.1	±520 ps	_____
15.0 µs	±0.16	±800 ps	_____

NOTE. 0.2 div = one minor horizontal graticule division

CHANNEL TO CHANNEL ACCURACY

8. Further set up the HP 54112D with the following parameters.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 2	Display	On
Timebase	Delay	0.00 s
Delta V	V Markers	On
	MARKER 1 POSITION	Chan 1 0.00 V
	MARKER 2 POSITION	Chan 2 0.00 V
	Preset Levels	50-50%
Delta t	T Markers	On
	START ON XXX	POS
	EDGE X	1
	STOP ON XXX	POS
	EDGE X	1

9. At ***Delta t*** press ***Edge Find***. The Δt= reading, in the lower-right corner of the display, should be 0.00 ±1.00 ns. Record the reading.

10. Remove the cable from the CHAN 2 input and connect it to the CHAN 3 input.

11. Change the following parameters on the HP 54112D.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 2	Display	Off
Chan 3	Display	On
Delta V	MARKER 2 POSITION	Chan 3 0.00 V
	Preset Levels	50-50%

12. Press ***Delta t*** and ***Edge Find***. The Δt= reading should be 0.00 ±1.00 ns. Record the reading.

13. Remove the cable from the CHAN 3 input and connect it to the CHAN 4 input.

14. Change the following parameters on the HP 54112D.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 3	Display	Off
Chan 4	Display	On
Delta V	MARKER 2 POSITION	Chan 4 0.00 V
	Preset Levels	50-50%

15. Press ***Delta t*** and ***Edge Find***. The Δt= reading should be 0.00 ±1.00 ns. Record the reading.

LONG DELAY - TIMEBASE ACCURACY

16. Change the frequency of the signal generator to 1 MHz.

17. Change the HP 54112D with the following parameters.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 4	Display	Off
Delta V	V Markers	Off
Delta t	T Markers	Off
Timebase	TIME/DIV	200 ns/div

18. Press ***Trigger*** and ***Trigger Level***. Adjust the trigger so that the positive edge of the signal crosses exactly at center screen.

19. Press ***Timebase*** and ***Delay***. Enter 15 ms. The positive edge of the signal should cross within 1.5 divisions of center screen. Use the knob or cursors to set the positive edge at center screen. The delay should read between 14.9997 and 15.0003 ms (15 ms ± 304 ns). Record the reading.

3-16. TRIGGER SENSITIVITY

Description:

Channel and external trigger paths are checked for sensitivity vs. frequency. The displayed signal must remain triggered with a given input at the system bandwidth.

If these tests fail consult an HP Customer Service representative.

Specification:

Channels 1, 2, 3, 4: 0.1 of full scale, dc to 100 MHz
External: 100 mV p-p, dc to 50 MHz

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Signal Generator	50 MHz and 100 MHz sine wave 5 mV to 250 mV rms amplitude (-33 dBm to +9 dBm output)	HP 8656B
Power Meter/Sensor	50 MHz measure approximately 250 μW	HP 436A/8482A
Power splitter	Outputs differ by <0.15 dB	HP 11667A
Attenuator	10 ±0.6 dB 50 MHz	HP 8491B
Cable Adapter Adapters (2)	Type N(m) 24 inch N(f) to BNC(m) N(m) to BNC(f)	HP 11500B HP 1250-0077 HP 1250-0780
Cables (2) Termination	BNC(m) >24 inches BNC 50Ω feedthrough	HP 10503A HP 10100C

Procedure:

CHAN 1,2,3,4 TRIGGER TEST

1. Perform a one-key power up* to set instrument to default conditions.
   *Power to STBY. Press and hold one key Power to ON Release key when "Powerup Self Test Passed!" is displayed.
2. Set the signal generator frequency for 100 MHz and amplitude to 9 mV rms.
3. With the Type N cable and N(f)-to-BNC(m) adapter, connect the signal generator to the CHAN 1 input.

4. Press AUTOSCALE to establish the display, then set or ensure the following parameters. Press ***Chan 1***, 20 and mV, then ***Input Impedance*** to select 50Ω.

MENU SELECT	FUNCTION SELECT	SETTING
Display	NUMBER OF AVERAGES	8
Chan 1	VOLTS/DIV Input Impedance	20 mV 50Ω
Delta V	V Markers Preset Levels	On 0-100%

5. Press ***more, Trigger*** and ***Trigger Level***.

6. Reduce the output of the signal generator until ***Auto Triggering*** appears (top of display). Adjust ***Trigger Level*** as necessary to maintain triggering as long as possible. Slight movement of the waveform is due to sampling and averaging characteristics of the instrument. Increase output until stable triggering returns, indicated by no occurences of ***Auto Triggering*** in the display.

7. Press CLEAR DISPLAY. When ***#Avgs = 8***, press ***more, Delta V***, and ***Auto Level Set***. Read and record ***ΔV=***. It should be less than 16 mV (0.1 of full scale or 0.8 div.).

8. Repeat steps 3 through 7 for channels 2, 3, and 4, substituting channel references as appropriate.

EXTERNAL TRIGGER TEST

9. Connect the equipment as shown in the following diagram. Temporarily leave the BNC cable with 50Ω termination disconnected from the EXT. TRIGGER BNC connector on the rear panel.

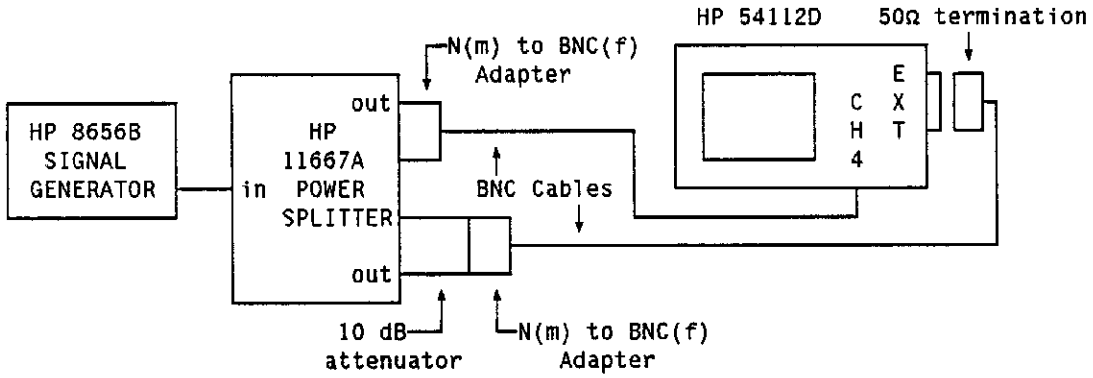


Figure 3-2. Trigger Sensitivity Test Connections.

10. Press ***Delta V*** and ***V Markers*** to shut them off and press ***more, Chan 4***, and ***VOLTS/DIV*** and ENTER 50 mV.

11. Zero and calibrate the power meter using the Power Reference on the meter and the REF Cal Factor on the power sensor.

12. Set the signal generator frequency to 50 MHz and output level to 250 mV rms.

13. Set the power meter Cal Factor % to the 50 MHz value from the chart on the probe.

14. Press ***Trigger*** and ***Trigger Src*** to select ***External***. Check that ***HF Reject*** is ***Off***.

15. Set ***TRIGGER LEVEL*** to 0.00 V. If any occurence of ***Running*** appears in the display (upper left corner) raise the trigger level until only occurences of ***Auto Triggering*** appear.

16. Connect the BNC cable with 50Ω termination to the EXT. TRIGGER INPUT on the rear panel. The waveform should be stably triggered.

17. Reduce the output of the signal generator until the waveform is no longer stably triggered. Slight movement of the waveform is due to the sampling and averaging characteristics of the instrument. Increase output until stable triggering returns.

18. Disconnect the 10 dB attenuator at the power splitter and connect the power meter to this port of the splitter.

19. Read the power reading. It should be less than 250.0 μW (100 mV p-p + 10 dB).

20. To convert the power reading to a peak-to-peak voltage value for recording, use the following formula:

$$V_{p\text{-}p} = 2.83\sqrt{\frac{P \times 50}{10}}$$

$$V_{p\text{-}p} = 6.32\sqrt{P}$$

$V_{p\text{-}p}$	EXT. TRIGGER input voltage
2.83	converts RMS to p-p
P	power reading on meter
50	ohms impedance
10	compensates for 10 dB atten.

NOTES

Table 3-2. Performance Test Record

HEWLETT-PACKARD
MODEL 54112D
DIGITAL OSCILLOSCOPE

SERIAL NO. _____

Recommended Cal Interval - 1 year/2000 hrs

Recommended Next Calibration _____

Tested by _____

Work Order No. _____

Date _____

Temperature _____

Humidity _____

TEST	LIMITS	RESULTS
3-9 Calibrator Amplitude	0.796 to 0.804 V	_____
3-10 Input Resistance	LIMITS: 49.5Ω to 50.5Ω	CHAN 1 _____ CHAN 2 _____ CHAN 3 _____ CHAN 4 _____
3-11 Voltage Measurement Accuracy	RANGE / LIMITS	CHAN 1 CHAN 2 CHAN 3 CHAN 4
	50 mV: 338 mV to 362 mV	_____ _____ _____ _____
	100 mV: 676 mV to 724 mV	_____ _____ _____ _____
	200 mV: 1.35 V to 1.45 V	_____ _____ _____ _____
	500 mV: 3.38 V to 3.62 V	_____ _____ _____ _____
	1 V: 6.76 V to 7.24 V	_____ _____ _____ _____
	2 V: 13.5 V to 14.5 V	_____ _____ _____ _____
	5 V: 33.8 V to 36.2 V	_____ _____ _____ _____
	10 V: 67.6 V to 72.4 V	_____ _____ _____ _____
	20 V: 135 V to 145 V	_____ _____ _____ _____
3-12 Vertical Offset Accuracy	SUPPLY VOLTAGE / LIMITS	CHAN 1 CHAN 2 CHAN 3 CHAN
	0 mV: -24 mV to 24 mV	_____ _____ _____ _____
	+300 mV: 272 mV to 328 mV	_____ _____ _____ _____
	-300 mV: -272 mV to -328 mV	_____ _____ _____ _____
	-9.50 V: -9.33 V to -9.67 V	_____ _____ _____ _____
	+9.50 V: 9.33 V to 9.67 V	_____ _____ _____ _____

Table 3-2. Performance Test Record (con't.)

TEST	LIMITS	RESULTS
3-12 Vertical Offset Accuracy (cont.)	RANGE 50 mV ±0.4 div or ±22 mV 200 mV ±0.2 div or ±47 mV 500 mV ±0.2 div or ±120 mV 1 V ±0.2 div or ±240 mV 2 V ±0.2 div or ±470 mV 5 V ±0.2 div or ±1.2 V 10 V ±0.2 div or ±2.4 V 20 V ±0.2 div or ±4.7 V	CHAN 1 CHAN 2 CHAN 3 CHAN 4 _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____
3-13 Bandwidth	Down from reference Repetitive 100 MHz <2.85 dB	CHAN 1 CHAN 2 CHAN 3 CHAN 4 _____ _____ _____ _____
3-14 Time Measurement Accuracy	Short Delay - Timebase Acc. 20 ns ±0.1 div or ±501 ps 40 ns ±0.1 div or ±501 ps 60 ns ±0.1 div or ±502 ps 80 ns ±0.1 div or ±502 ps 100 ns ±0.1 div or ±502 ps 1.0 µs ±0.1 div or ±520 ps 15.0 µs ±0.16 div or ±800 ps Channel-to-Channel Accuracy Chan 1 to Chan 2 Δt = 0.00 ±1.0 ns Chan 1 to Chan 3 Δt = 0.00 ±1.0 ns Chan 1 to Chan 4 Δt = 0.00 ±1.0 ns Long Delay - Timebase Acc. 15.0 ms ±304 ns - 14.9997 to 15.0003 ms	_____ _____ _____ _____ _____ _____ _____ _____ _____ _____ _____
3-15 Trigger Sensitivity	Triggers on less than: 0.8 div/16 mV p-p, 100 MHz Triggers on less than: 100 mV p-p, 50 MHz	CHAN 1 CHAN 2 CHAN 3 CHAN 4 _____ _____ _____ _____ EXTERNAL _____

SECTION 4
ADJUSTMENTS

4-1. INTRODUCTION

This section describes the adjustments required to make the instrument meet published specifications. Included are adjustments to the power supplies, acquisition system and color display.

4-2. ADJUSTMENT REQUIREMENTS

Adjustments should be performed as warranted by the Calibration Procedure (see section 3), by requirements after repair or requirements due to failure of a performance test (see section 3). Except for the Calibrator Amplitude Adjustment, which should be checked before every calibration cycle, adjustments should not be performed only on the basis of an elapsed period of time.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures. The apparatus should be disconnected from all voltage sources before it is opened for any adjustment, replacement, maintenance, or repair.

4-3. ADJUSTMENTS REQUIRED AFTER REPLACEMENTS

Some adjustments may be necessary after replacement of an assembly, though it may not be necessary to make all adjustments. Table 4-1 (next page) gives the adjustments necessary after replacement of a major assembly.

4-4. TEST EQUIPMENT REQUIRED

Required test equipment is listed in Table 1-4, Recommended Test Equipment.

4-5. ACCESS TO ADJUSTMENTS

Most adjustments can be accessed by removing the instrument covers (see section 6A, Instrument Disassembly).

Power supply adjustments (not done during routine calibration) require the additional removal of the power supply cover (under the top cover).

Adjustment of the attenuators requires partial removal of the front panel and attenuators. For this reason, and because misadjustment is unlikely, attenuator adjustment is not recommended during routine calibration.

Most adjustments of the Color CRT Module are under the clear plastic covers and are accessable from the sides or bottom of the instrument. However, several are at the rear of the module and require removal of the module from the instrument and operation of the module while outside the instrument. They also require a special tool as noted in the procedure. These adjustments are also not recommended during routine calibration.

4-6. ONE-KEY POWER UP

A one-key power up is a procedure where any one key is held depressed when the power is turned on. The key is held depressed until the power up cycle completes; "Powerup Self Test Passed!" (or Failed) is displayed. This is done to preset or reset the instrument to default conditions and prevent previous setups from interfering with the next test. It also simplifies the instrument setup procedure.

The one-key power up is a part of many procedures and should be performed like any other procedural step.

Table 4-1. Adjustments Required After Assembly Replacement.

ADJUSTMENT / ASSEMBLY	Power Supplies	V_{B1}	Calibrator Amplitude	Flatness	Complete* Software Calibration	Attenuator
Acquisition				RCO	X	
Timebase/Trig		X	X		X	
Attenuator				RCO	X	Adjusted at factory
Microprocessor					X	
Input/Output					X	
Power Supplies	Adjust supply replaced					

NOTE: The **Color Display** assembly and **Color CRT Module** do not require any adjustment after replacement.

KEY: RCO Replaced Channel Only. Perform this adjustment only on the channel in which the assembly was replaced.

X This adjustment must be performed.

* Software calibration includes: Vertical Cal, Probe Tip Cal, Offset Cal, Trigger Cal, and Timebase Cal (Channel Skew). See the appropriate procedures in this section.

4-7. POWER SUPPLY ADJUSTMENTS

Description:

This procedure is provided to adjust the power supply voltages in cases where a power supply has been inadvertently mis-adjusted or repairs have been made.

No performance tests are required after power supply adjustments.

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Voltmeter	Better than 0.05% accuracy	HP 3468A

Analog Power Supply Procedure:

NOTE

First, check for the presence of adjustment A12R61, located at the top front corner of the Analog Supply assembly. If there is no potentiometer there, the analog supply is a later version and no adjustment is required. Continue with the Digital Supply procedure.

This procedure adjusts the supply voltage to the fans. The locations of the test points are marked on the power supply cover as well as the PC board.

NOTE

*The instrument **MUST** be stabilized at ambient temperature with power off (front panel power switch to STBY) before this adjustment is made. This voltage will rise as internal temperature increases.*

1. Connect positive voltmeter lead to the FAN test point.
2. Connect negative voltmeter lead to the -18 V test point.
3. Turn on instrument power (from STBY to ON).
4. Before instrument warms up, adjust A12R61 (the only adjustment on Analog Supply) for a voltmeter reading of 9.5 Vdc ±0.1 V.

Digital Power Supply Procedure:

The locations of test points are marked on the power supply cover as well as the assemblies. First, the voltage is measured to be sure that it requires adjustment.

1. Allow the instrument to stabilize (power on) for one to two minutes.
2. Connect positive voltmeter lead to the +5 V test point (actual voltage = +5.1 V).
3. Connect negative voltmeter lead to the −5 V test point (actual voltage = −5.3 V).
4. The voltmeter should read 10.4 Vdc ±0.01 V. If the measurement is within specifications stop here. If not, then continue.
5. Disconnect power cord and remove voltmeter leads.

WARNING

Hazardous voltages capable of causing injury or death are present on the power supply assemblies when power is applied and for a period of time after power is removed. To avoid this hazard, DO NOT remove the top power supply shield until the LED on the Primary Power Supply (A11) is extinguished. This LED is visible through an inspection hole in the cover labeled "+300 V WHEN LAMP IS ON".

6. When the +300 V LED is extinguished, remove the top power supply cover.
7. Reconnect voltmeter leads per steps 2 and 3 above.
8. Reconnect power cord and allow instrument to stabilize for 1 to 2 minutes.
9. Adjust A13R56 (only adjustment on Digital Supply) for a voltmeter reading of 10.4 Vdc ± 0.01 V.
10. Disconnect power cord and wait until the +300 V LED is extinguished before re-installing power supply shield.

4-8. TIMEBASE VB1 ADJUSTMENT

Description:

This procedure adjusts the V_{B1} voltage level on the sync mux hybrid U4. V_{B1} represents a current level and may cause apparent failures if badly misadjusted.

No performance test is necessary after this adjustment.

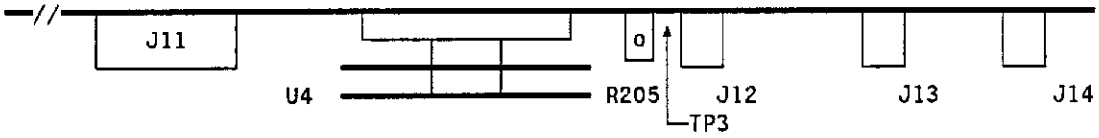
Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Digital Voltmeter	Better than 0.3% accuracy	HP 3468A

Procedure:

Refer to the drawing for the location of components.

Top view of rear of Timebase/trigger assembly (A8).



1. Turn off instrument power.
2. Connect the positive lead of the DVM to TP3 on the Timebase/trigger assembly A8. TP3 is a pad on the PC board and is marked "TP3."
3. Connect the negative lead to ground on the Timebase/trigger assembly. The shield of J12 is a good place.
4. Turn on instrument power.
5. Adjust R205 for a reading of −4.50 ±0.045 V (-4.455 V to -4.545 V).

4-9. CALIBRATOR AMPLITUDE ADJUSTMENT

Description:

This procedure adjusts the amplitude of the front panel CAL signal. This signal is used to run calibration routines in the instrument.

The adjustment is done by forcing this signal high and adjusting it while measuring it with an accurate voltmeter. Forcing the signal high is done from the front panel through one of the Extended Tests.

The specification for this adjustment is tighter than that required to perform an accurate calibration using the signal. The specification for CAL signal use is ±4 mV (as displayed on screen when the test is started). The signal is adjusted as close as possible, and not greater than ±2 mV, which will assure an accurate signal throughout the next calibration cycle.

Since the adjustment specification is tighter than the performance test specification, no performance test is necessary after this adjustment.

Equipment Required:

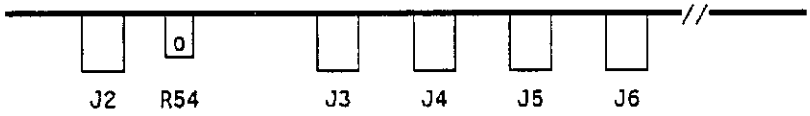
EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Voltmeter	Better than 0.05% accuracy	HP 3468A

Procedure:

1. Connect the DC voltmeter + input to the front panel calibrator signal and – input to ground at the CHAN 1 input BNC.

2. In order, press ***more***, ***Utility***, ***Test Menu***, and ***Extended Tests***, press 21 and ENTER, then ***Start Test***.

Top view of front of Timebase/Trigger assembly (A7).



4. Adjust R54 so that the CAL voltage is as close as possible to +0.8000 V. It must be within ±0.002 Vdc.

5. Press ***Stop Test*** then ***Exit Test Menu***.

4-10. FLATNESS ADJUSTMENT

Description:

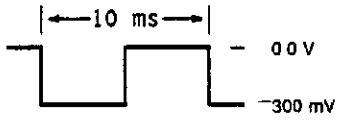
This adjustment equalizes low and high frequency gains. If adjustment is a result of assembly replacement (table 4-1), see table 3-1 for required performance tests. Otherwise, for any channel that has been adjusted, perform the Measurement Accuracy and Offset Accuracy tests in section 3.

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse Generator	≤±1% perturbations after 10 ns 0.0 to -300 mV output	Tek PG 506
Cable	BNC (m)	HP 10503A

Procedure:

1. Set the following parameters on the signal generator:
   Fast Rise output
   Period: 10 ms -- vernier to minimum
   Pulse amplitude: midrange (≈300 mV)



2. Connect the FAST RISE OUTPUT center BNC of the pulse generator to the CHAN 1 input.

1. Perform a one-key power up* to set the instrument to default conditions.
   *Power to STBY. Press and hold one key. Power to ON. Release key when "Powerup Self Test Passed!" is displayed.

3. Press ***Chan 1*** and set ***Input Impedance*** to 50Ω.

4. Press AUTOSCALE to establish the signal on the display.

5. Set the pulse generator amplitude to 300 mV p-p and period to 100 ms, then set the following parameters on the HP 54112D.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1,2,3,4	Display VOLTS/DIV OFFSET Input Impedance	Chan 1 On/Chan 2,3,4 Off 15.0 mV/div 0.00 V 50Ω
Timebase	TIME/DIV DELAY Auto/Trgd Sweep	7.00 ms/div 28.0000 ms Trgd
Trigger Ch 1,2,3,4	Trigger Mode TRIGGER LEVEL	Edge -150 mV
Display	NUMBER OF AVERAGES Graticule	8 Grid

6. You should have a display somewhat like that in the following figure. The figure shows the signal when adjusted and mis-adjusted.

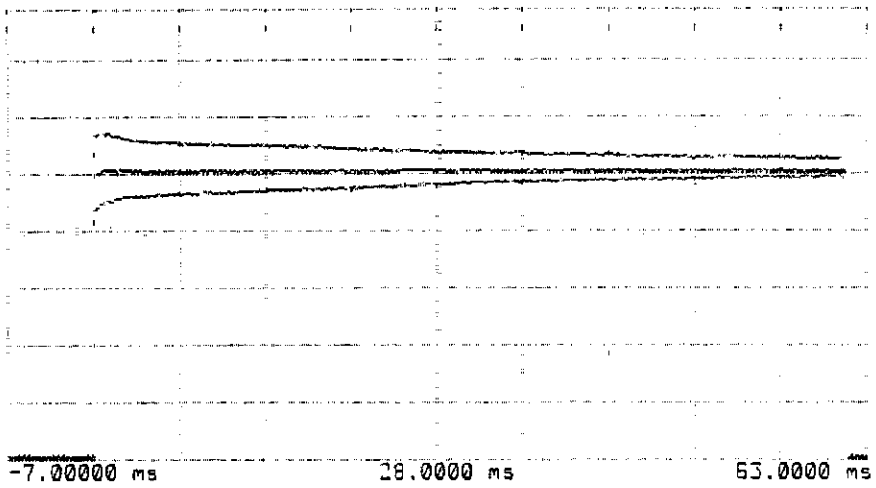


Figure 4-1. Flatness adjustment waveforms.

The following drawing shows a top view of the front of an ADC assembly. There are four of these assemblies, A4 - A7, one for each channel. Card cage assemblies are designated A1 to A9, from left to right starting near the Color CRT Module. A3 and A9 are not used.

Top view of front of ADC assemblies (A4 - A7).

7. Adjust R88 on the channel 1 ADC assembly for a level pulse top. Press ***Chan 1*** and ***Offset*** and use the offset to keep the waveform close to the grid line. This helps in judging the flatness of the pulse.

8. Press ***Display (Off)***, ***Trigger***, ***Trg Src***, ***Chan 2***, and ***Display (On)*** to set up channel 2.

9. Connect the cable from the pulse generator to the CHAN 2 input. Ensure that the ***Input Impedance*** is 50Ω.

10. Adjust R88 on the channel 2 ADC assembly for a level pulse top. Use the offset to keep the waveform close to the grid line.

11. Repeat steps 8, 9, and 10 for channels 3 and 4. Substitute appropriate channel references when necessary.

4-11. SOFTWARE CALIBRATION

Software calibration procedures calibrate circuitry with internal routines and adjustments. If doing a complete adjustment procedure, follow software calibration completely and in order.

No performance tests are necessary after software calibration.

4-12. Vertical Calibration

Description:

Vertical calibration calibrates vertical sensitivity.

Procedure:

1. Disconnect all inputs to channels.
2. Press the ***more***, ***Utility***, ***Cal Menu***, ***Vertical Cal*** and ***Continue***. Follow the instructions on the display. When calibration is complete the instrument will return to the Cal Menu.

4-13. Probe Tip Calibration

Description:

Probe Tip Cal calibrates the vertical channel from the probe tip through the A/D converters.

NOTE

This procedure is usually done for any channel that has had the probe changed. A channel's vertical specifications are met only when it's used with the probe it was calibrated with.

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Divider Probe	10:1 1 MΩ	HP 10431A/033A/017A

Procedure:

NOTE

You may use the same probe for all channels unless you need to calibrate each input to a specific probe (see note above).

1. Press ***Probe Tip Cal*** and ***Calibrate Probe Tip CHAN 1***. Follow the instructions on the display.
2. When the calibration for CHAN 1 is done, calibrate CHAN 2, 3, and 4.
3. Press ***Exit*** then continue with the next procedure.

4-14. Offset Calibration

Description:

The Offset Cal adjusts the channel offset values for various vertical sensitivities.

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC Power Supply	10 ±0.01 Vdc	HP 6115A
Oscilloscope Probe	10:1 1 MΩ	HP 10431A/033A/017A

Procedure:

1. Set the power supply to 10.0 ±0.01 V.
2. Connect the 10 V level through the 10:1 probe to the CHAN 1 input.
3. Press ***more, Utility, Cal Menu, Offset Cal*** and ***Calibrate Offset Channel 1***. Follow the instructions on the display.
4. When the calibration for CHAN 1 is done, calibrate CHAN 2, 3, and 4.
5. Press ***Exit*** then continue with the next procedure.

4-15. Trigger Calibration

Description:

Trigger Cal calibrates trigger levels and trigger sensitivity (hysteresis). This procedure does not require operator interaction but takes about 10 minutes.

Procedure:

1. Press ***Trigger Cal*** and follow the instructions on the display. The arrow will move across the display, showing the calibration is proceeding.
2. When calibration of the triggers is complete, the instrument will return to the Cal Menu.

4-16. Channel Skew Alignment

Description:

Channel Skew time-aligns the signal that is input to the channels and external trigger.

Alignment occurs at the intersection of the input signal's rising edge and the HP 54112D's center horizontal graticule. For each input, this point becomes time-aligned with the zero-delay point.

Alignment includes time delays both internal and external to the HP 54112D, including BNC cable length.

The reason for doing Channel Skew Alignment in the adjustment procedures is to set references for the Time Measurement Accuracy tests in the Performance Tests.

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Cables (2)	BNC to BNC (equal length and three feet long or longer)	HP 10503A
Adapter	BNC Tee (m)(f)(f)	HP 1250-0781
Termination	BNC 50Ω feedthrough	HP 10100C

Procedure:

1. Using the BNC tee, connect both cables to the rear panel TIMEBASE CAL output.
2. Press ***more, Utility, Cal Menu, Timebase Cal***, and ***Ch1 and Ch1-Ch2 Skew***.
3. Follow the instructions on the display.
4. When channnels 1 and 2 calibration is complete, perform the Ch1-Ch3, Ch1-Ch4, and Ch1-Ext skew calibrations. Press the appropriate softkey and follow the instructions on the display.

4-17. ATTENUATOR ADJUSTMENT

Description:

The channel attenuator assemblies have two compensation adjustments, X10 and X100. These are set at the factory and normally do not require further adjustment.

Perform Measurement Accuracy, Offset Accuracy, and Bandwidth tests (section 3) on any channel which has had the attenuator adjusted.

NOTE

DO NOT PERFORM THESE ADJUSTMENTS DURING ROUTINE CALIBRATIONS. *It is necessary to partially disassemble the instrument for these adjustments.* ***DO NOT*** *perform these adjustments unless the Flatness Adjustments have been made and it is desirable to optimize flatness from 50 mV/div to 5 V/div.*

Equipment Required:

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse Generator	≤1% perturbation	Tektronix PG 506
Cable	BNC (m)	HP 10503A
Adjustment tool	----------	HP 8710-1515

Procedure:

1. Without disconnecting any cabling, perform the Front Panel Removal procedure in Section 6A of this service manual. Set the front panel about 10 cm in front of its normal position.

2. Some attenuators do not need further removal to reach adjustments. Skip this step if the adjustments can be reached on the attenuator needing adjustment.

   The adjustments are about 1 cm from the front edge. The X100 adjustment is toward the front and the X10 directly behind it.

   With instrument in its normal operating position, remove the screw that fastens the rear of the attenuator to be adjusted. It can be reached from the top. *This screw is not captive.* ***DO NOT*** *allow it to fall into the instrument because it will be difficult to retrieve.*

3. Set the instrument on its left side. Without disconnecting any cabling, slide foreward to expose adjustments any attenuator loosened in step 2.

4. Set up the pulse generator with the following parameters.
   ```
   Output select   - Fast rise
   Period          - 0.1 ms
   Pulse Amplitude - 500 mV
   ```

5. Connect the FAST RISE OUTPUT left-hand BNC of the pulse generator to the input of the attenuator to be adjusted.

6. Press ***Chan X*** (whichever is appropriate) and ensure the ***Input Impedance*** is ***50Ω***. Press AUTOSCALE to establish the signal. Continue setup of the HP 54112D by setting or verifying the following parameters.

MENU SELECT	FUNCTION SELECT	SETTING
Chan 1 - 4	VOLTS/DIV	50 mvolts/div
	OFFSET	100 mV
Timebase	TIME/DIV	5 us/div
	DELAY	20 us
	Delay Ref at	Center
Display	Disp Mode	Repetitive
	Averaging	ON
	NUMBER OF AVERAGES	8
	Screen	Single
	Graticule	Grid

7. Press ***Chan X*** (whichever is appropriate) and ***OFFSET*** and set the the offset to put the top of the pulse 3 divisions above center screen. If it is slightly above or below a grid line, flatness deviations will be more readily apparent.

8. Adjust X10 adjustment (rear capacitor) for best flatness.

9. Set VOLTS/DIV to 500 mV/div.

10. Set pulse generator amplitude to MAX or 5 V, whichever occurs first.

    NOTE: *If you are using a PG 506 the maximum output is about 1 V, so the pulse amplitude will be about 2 divisions. Do not set the HP 54112D for a lower range since 500 mV/div is the lowest that this adjustment covers.*

11. Press ***Chan X*** (whichever is appropriate) and ***OFFSET*** and set the the offset to put the top of the pulse 3 divisions above center screen. If it is slightly above or below a grid line, flatness deviations will be more readily apparent.

12. Adjust X100 adjustment (front capacitor) for best flatness.

13. If other channels are being adjusted, repeat steps 2 through 12 for them.

14. After adjustments are complete, reassemble instrument following procedures in section 6A.

CAUTION

Before installing front panel, be sure the three-wire cables at front of the attenuators do not become pinched and ensure that all probe sense rings around the input BNCs are inserted into their recesses properly.

4-18. COLOR CRT MODULE ADJUSTMENTS

NOTES

DO NOT PERFORM THESE ADJUSTMENTS DURING ROUTINE CALIBRATIONS. *The following procedures are provided only for the few extreme cases where either the earth's magnetic field or the user's environment has caused an unusable display due to mis-convergence that cannot be corrected by degaussing the entire CRT screen.*

It is recommended that these adjustments be performed only by qualified personnel who are familiar with color CRT convergence procedures.

Before starting adjustments, mark the position where potentiometers are set. This helps in returning adjustments to their original positions if it becomes necessary to restart the procedure.

Description:

The Color CRT Module is adjusted to compensate for magnetic influences causing mis-convergence.

NOTE

DO NOT *continue this procedure before first degaussing the CRT screen using the rear panel degaussing switch. In extreme cases of magnetism, it may be necessary to degauss the CRT using a conventional external television-type degaussing coil.* ***During any of the following adjustments, the CRT module must face west.***

Equipment Required:

Non-metallic Adjustment Tool ..... HP Part Number 8710-1355

Procedure:

NOTE

The following adjustments are broken down into adjustment groups. The adjustment group sequence must be followed in order because of interaction and dependency. The adjustment group sequence is shown in the adjustment flow diagram on the next page. There will be cases where it will not be necessary to perform all adjustment group procedures. For example, if the Geometry Adjustment Group corrects the problem, this will be the only group that should be performed.

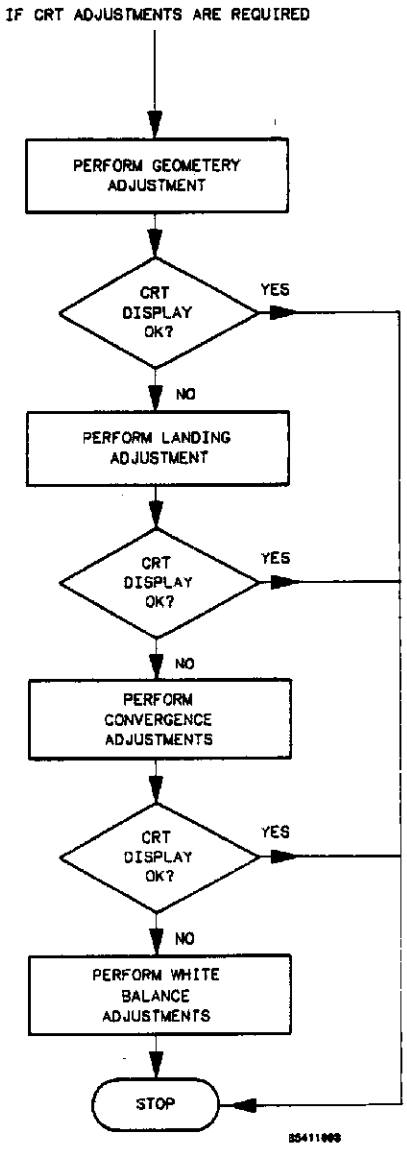


Figure 4-2. CRT Module Adjustment Flow Diagram.

Geometry Adjustments

1. Press ***Utility***, ***CRT Setup Menu***, then ***Pattern*** key as required until the white cross-hatch is displayed on CRT.
2. Preset front panel BACKGROUND control to mechanical center.
3. Preset front panel BRIGHTNESS control maximum clockwise.
4. Preset H.SUB SHIFT (RV006) and V.SUB SHIFT (RV008) located on the bottom PC board to mechanical center.
5. Using a flexible ruler, adjust H.SIZE (RV504) AND V.HEIGHT (RV502) located on the left hand side PC board so that the border of the cross-hatch pattern displayed on the CRT is 120.5 mm (4.74 in.) vertically and 161 mm (6.34 in.) horizontally.
6. Adjust V.CENT (RV510) AND H.CENT (RV503) located on the left hand side PC board to center pattern.
7. Adjust PIN AMP (RV506) located on the left hand side PC board to eliminate pincushion distortion in the vertical lines of the cross-hatch pattern as shown in the next figure.

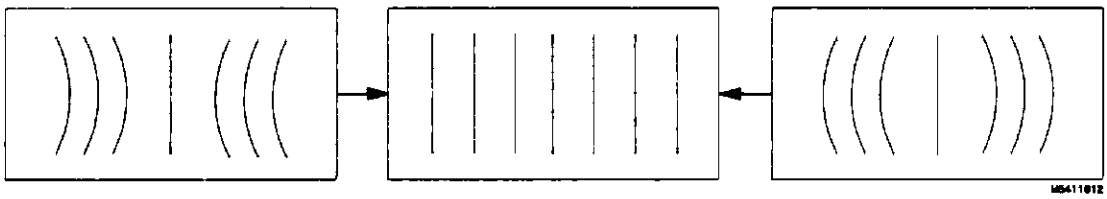


Figure 4-3. PIN AMP Adjustment.

8. Adjust PIN PHASE (RV505) located on the left side PC board to eliminate pin phase distortion in the vertical lines of the cross-hatch pattern as shown in the next figure.

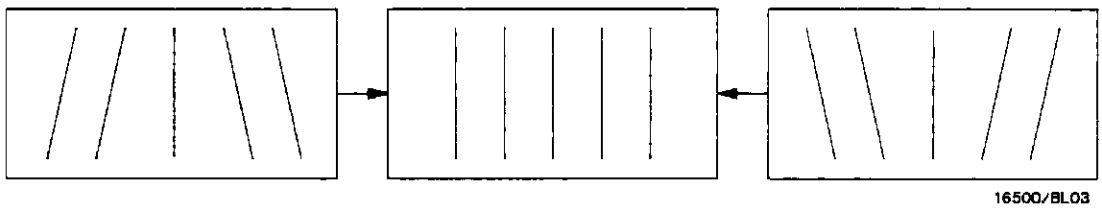


Figure 4-4. PIN PHASE Adjustment.

9. Adjust TOP PIN (RV511) located on the left hand side PC board so that top horizontal line is parallel with the center horizontal line.
10. Adjust BOTTOM PIN (RV512) located on the left hand side PC board so that bottom horizontal line is parallel with the center horizontal line.

Focus, Landing, and Convergence Adjustment Preparation Procedures

NOTE

Note the original routing of all cabling for proper routing when module is re-installed in instrument. Then, re-route the cables from inside the module to the outside (left side) of module for reconnection to the power supply for adjustments.

1. Remove Color CRT Module from the instrument (see section 6A of this service manual).
2. Reconnect instrument front panel and re-install front panel and CRT bezel (use two screws to temporarily hold front panel in place).
3. Loosen deflection yoke clamp screw.
4. With Color CRT Module placed to the left of mainframe, reconnect module.
5. Remove deflection yoke spacers by moving deflection yoke backward and removing spacers.

NOTE

The deflection yoke spacers are tapered rubber blocks located between front of yoke and rear of CRT funnel.

6. Apply power and allow the instrument to thermally re-stabilize for 20 minutes.

Focus Adjustment

NOTE

Geometry adjustments must be performed before making focus adjustment.

1. In ***Utility*** menu, press ***CRT Setup Menu***, then press ***Pattern*** key as required until the white cross-hatch is displayed on CRT.
2. Adjust FOCUS (RV701) located on the rear PC board for best overall focus.

Landing Adjustment

1. In ***Utility*** menu, press ***CRT Setup Menu***, then press ***Color Purity*** key (fourth key from top) as required until a white raster is displayed on CRT.

2. Turn front panel BRIGHTNESS control fully clockwise.

3. Degauss entire CRT screen by pressing momentary DEGAUSSING switch located on the instrument rear panel.

NOTE

In cases where the user's environment or shipping environment has caused high levels of magnetization to take place, it may be necessary to externally degauss the CRT using a conventional television type degaussing coil to completely degauss the CRT.

4. Set purity magnet tabs to mechanical center (see next figure).

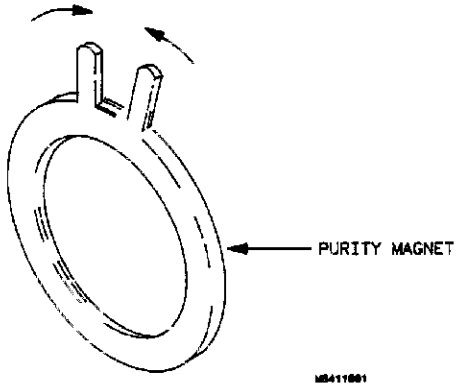


Figure 4-5. Purity Magnet Centering.

5. Press ***Color Purity*** key as required until a green raster is displayed on CRT.

6. Move deflection yoke rearward until left edge of raster turns red and right side of raster turns blue (see figure below).

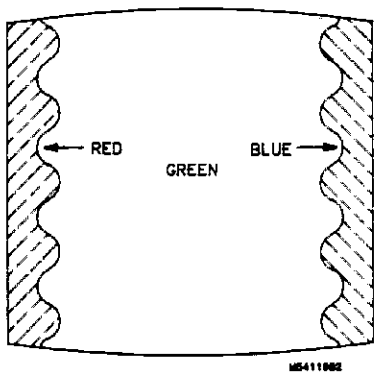


Figure 4-6. Purity Magnet Adjustment Raster.

7. Adjust purity magnets until green is in center of raster with red and blue bands evenly distributed on the sides (see above figure).

8. Move deflection yoke forward until entire raster is green.

NOTE

Landing adjustment is easier if yoke is moved all the way forward and then moved back until raster is completely green.

9. Using ***Color Purity*** key, replace green raster with red and then blue raster each time checking for proper landing adjustment (color purity of each).

10. If landing is not correct in step 9, repeat steps 6 through 9 for best compromise (see next figure).

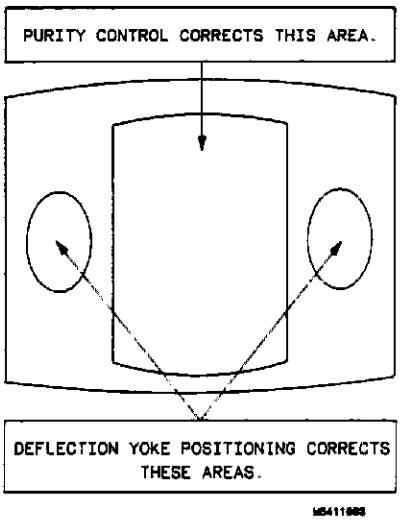


Figure 4-7. Landing and Purity Adjustment Guide.

11. If landing is not correct in step 10, readjust purity magnets for best landing of each color.

12. When landing adjustment is complete, tighten deflection yoke clamp screw just enough to keep yoke from moving. **DO NOT over tighten.**

NOTE

While moving deflection yoke forward and backward, rotate yoke as necessary to make vertical edges of raster parallel to the sides of the instrument frame.

Static Convergence

1. Preset front panel BACKGROUND control to mechanical center.
2. Preset front panel BRIGHTNESS control maximum clockwise.
3. Temporarily disconnect power from instrument and remove PC board shield cover from rear of Color CRT Module by prying evenly on all four sides.
4. Re-apply power. Press ***more***, ***Utility***, and ***CRT Setup Menu*** keys. Press ***Pattern*** key as necessary to obtain the white cross-hatch pattern.
5. Check the four dots which are located around the center intersection of the cross-hatch pattern for coincidence of the blue, red and green dots. If the dots are not coincident, adjust H.STAT (RV703) located on the rear PC board to obtain horizontal coincidence and V.STAT (RV803) located on the bottom PC board to obtain vertical coincidence (see figure below).

NOTE

Due to interaction, BEAM LANDING will need to be re-adjusted if either H.STAT or V.STAT adjustments are made. Once BEAM LANDING is re-adjusted, repeat step 5 above if necessary to obtain center screen coincidence of the dots.

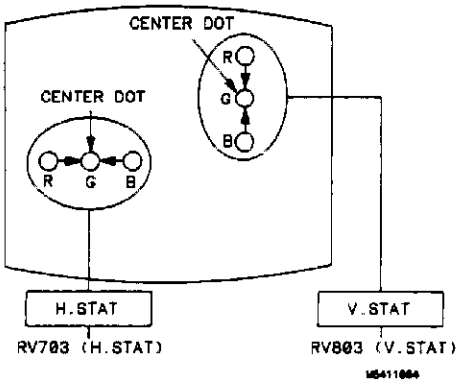


Figure 4-8. Static Convergence.

Dynamic Convergence

1. In ***Utility***, press ***CRT Setup Menu***, then press ***Pattern*** key (second key from top) as necessary to obtain the white cross-hatch pattern.

2. Adjust Y BOW (RV805) located on the bottom PC board to eliminate red, green and blue bowing at the top and bottom of the center vertical line (see next figure).

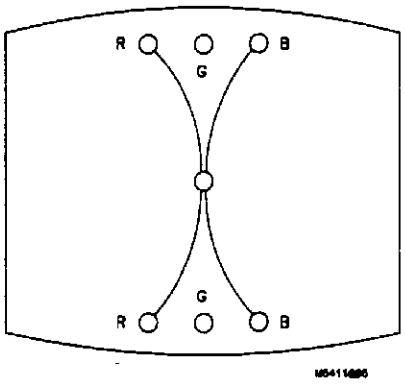


Figure 4-9. Y BOW Adjustment.

3. Adjust Y BOW CROSS (RV804) located on the bottom PC board to eliminate red green and blue orthogonal mis-alignment at the top and bottom of the center vertical line (see next figure).

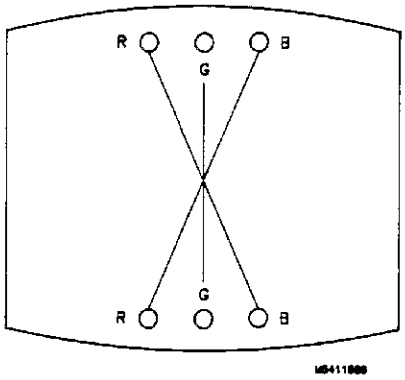


Figure 4-10. Y BOW CROSS Adjustment.

4. Adjust V.STAT TOP (RV801) and V.STAT BOTTOM (RV802) located on the bottom PC board to obtain coincidence of the red, blue and green at the intersection of the top and bottom horizontal lines with the center vertical line (see next two figures).

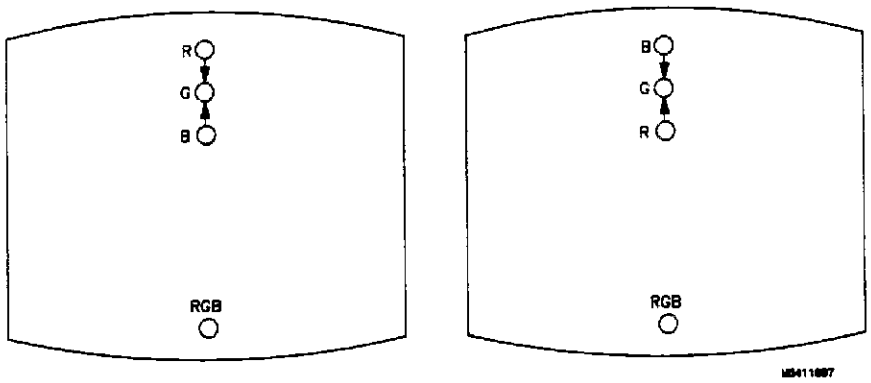


Figure 4-11. V.STAT TOP Adjustment.

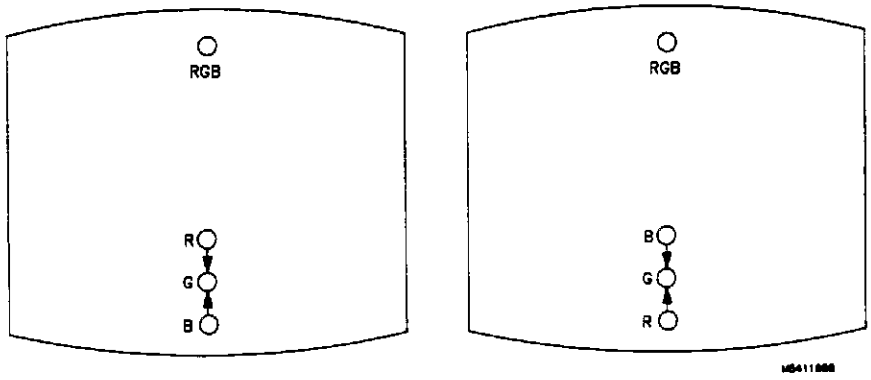


Figure 4-12. V.STAT BOTTOM Adjustment.

5. *Adjust H.AMP (RV807) located on the bottom PC board for equal amounts of mis-convergence at right and left sides of screen (see next figure).*

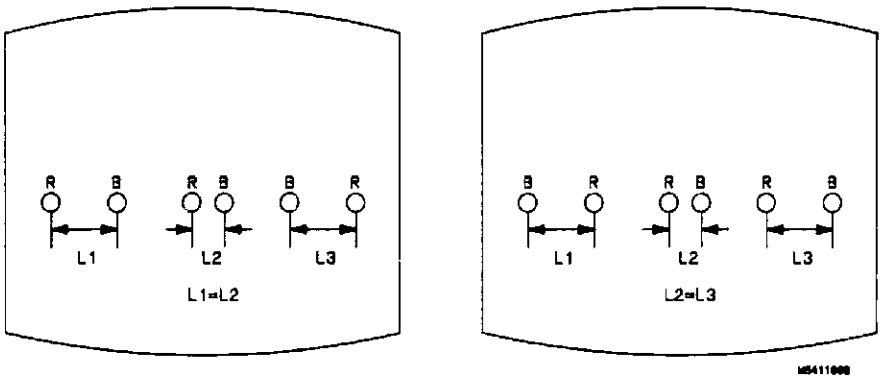


Figure 4-13. H.AMP Adjustment.

6. Adjust H.TILT (RV806) located on the bottom PC board for coincidence of red, green and blue at right and left sides of screen (see next figure).

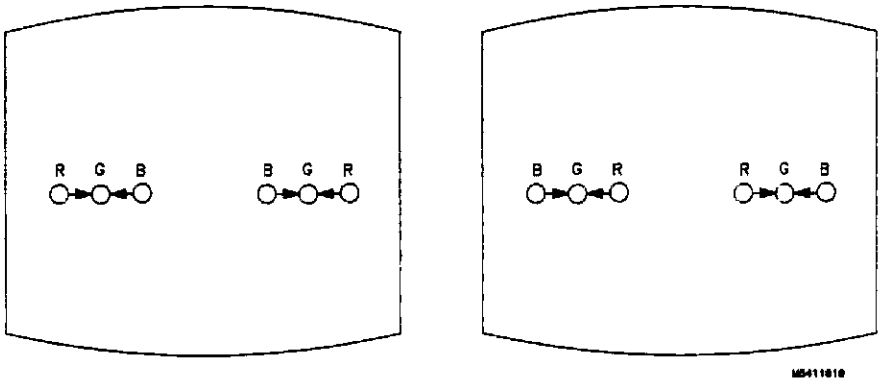


Figure 4-14. H.TILT Adjustment.

White Balance

1. In ***Utility***, press ***CRT Setup Menu***, then press ***Light Output*** key (third key from top) as necessary to obtain a blanked raster.

NOTE

The completely blanked raster will contain the text for the function keys on the right side of the display, however, this will not affect the adjustment.

2. Set front panel BACKGROUND and SUB BRT (RV901) located on the bottom PC board to mechanical center.
3. Set front panel BRIGHTNESS and SUB CONT (RV902) located on the bottom PC board to mechanical center.
4. Set G. DRIVE (RV921), B. DRIVE (RV931) and R. DRIVE (RV911) located on the bottom PC board to mechanical center.
5. Set G. BKG (RV721), B. BKG (RV731) and R. BKG (RV711) located on the rear PC board fully counterclockwise (CCW).
6. Adjust the SCREEN (RV702) located on the rear PC board until either red, green or blue raster just starts to become visible. Note which color becomes visible first and do not adjust the background control (BKG) for that color in the next step.
7. Adjust the other two background controls for best white balance.
8. Press ***Color Purity*** key as necessary to obtain the white raster.
9. Set front panel BRIGHTNESS control at maximum.
10. Observe the screen and adjust the DRIVE controls (RV921, RV931 and RV911) located on the bottom PC board for best white balance.

NOTE

White balance is checked in two ways. First, using an average piece of white photocopy paper, compare the white on the CRT to the paper. Second, in the CONFIDENCE TEST function, the gray scale blocks are checked to make sure the block at the far left of the CRT is visible.

11. Repeat steps 1-3 and 6-10 until satisfied with white balance.

SECTION 5
REPLACEABLE PARTS

5-1. INTRODUCTION

This section contains information for ordering parts. Table 5-1 lists the abbreviations used in the parts list and throughout this manual. Figure 5-1, which covers several pages, shows the locations of mainframe parts. Table 5-2 lists replaceable mainframe parts for the HP 54112D. Table 5-3 contains the names and addresses that correspond to the manufacturers' code numbers. Replaceable parts for individual assemblies are included in the HP 54112D Service Data Supplement which provides parts lists and schematics for applicable assemblies.

5-2. ABBREVIATIONS

Table 5-1 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

5-3. PARTS LIST

Table 5-2, the list of replaceable mainframe parts, is organized as follows:

a. Exchange assemblies. These assemblies can be ordered at reduced cost when the inoperative assembly is returned to Hewlett-Packard.

b. External parts. These parts are associated with the outside of the instrument and might be replaced during routine maintenance due to loss or damage.

c. Internal parts. These parts would be encountered only if the instrument was disassembled for repair. It includes assemblies, cables, mechanical parts, hardware, and other parts.

The information given for each part consists of the following:

a. Hewlett-Packard part number and the check digit (for HP internal use).

b. Total quantity (Qty) in the instrument, given only once, at the first appearance of the part number in the list.

c. Description of the part.

d. A typical manufacturer of a given part in a five digit code. Refer to table 5-3 for a code to manufacturer cross reference.

e. The manufacturers' number for the part.

5-4. EXCHANGE ASSEMBLIES

Some of the parts used in this instrument have been set up on the Blue-stripe exchange program. This allows the customer to exchange his faulty assembly with one that has been repaired, calibrated, and performance-verified by the factory. The cost is significantly less than that of a new part.

Exchangeable parts are listed in a separate section in the replaceable parts table. They have a part number in the form XXXXX-695XX (where the new part would be XXXXX-665XX).

Before ordering a Blue-stripe assembly, check with you're local parts or repair organization for the procedures associated with the Blue-stripe program.

5-5. ORDERING INFORMATION

To order a part listed in the replaceable parts list, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the replaceable parts table, include the instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

5-6. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

a. Direct ordering and shipment from the HP Parts Center.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

Mail-order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

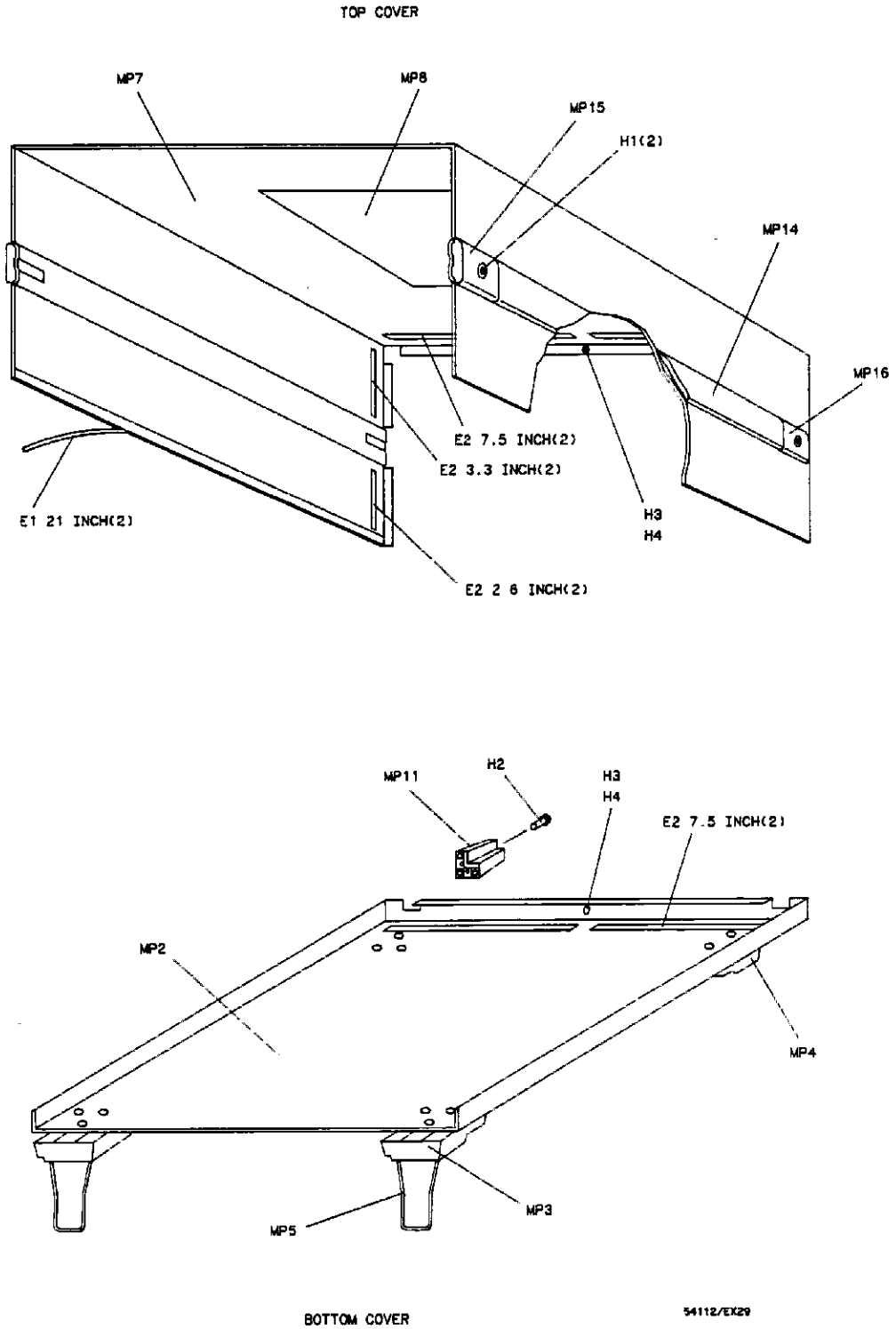
Table 5-1. Reference Designators and Abbreviations.

REFERENCE DESIGNATORS

A	=assembly	F	=fuse	Q	=transistor,SCR; triode thyristor	U	=integrated circuit; microcircuit
B	=fan;motor	FL	=filter	R	=resistor	V	=electron tube, glow lamp
BT	=battery	H	=hardware	RT	=thermistor	VR	=voltage regulator; breakdown diode
C	=capacitor	J	=electrical connector (stationary portion);jack	S	=switch;jumper	W	=cable
CR	=diode;diode thyristor; varactor	L	=coil;inductor	T	=transformer	X	=socket
DL	=delay line	MP	=misc mechanical part	TB	=terminal board	Y	=crystal unit(piezo-electric or quartz)
DS	=annunciator;lamp;LED	P	=electrical connector (moveable portion);plug	TP	=test point		
E	=misc electrical part						

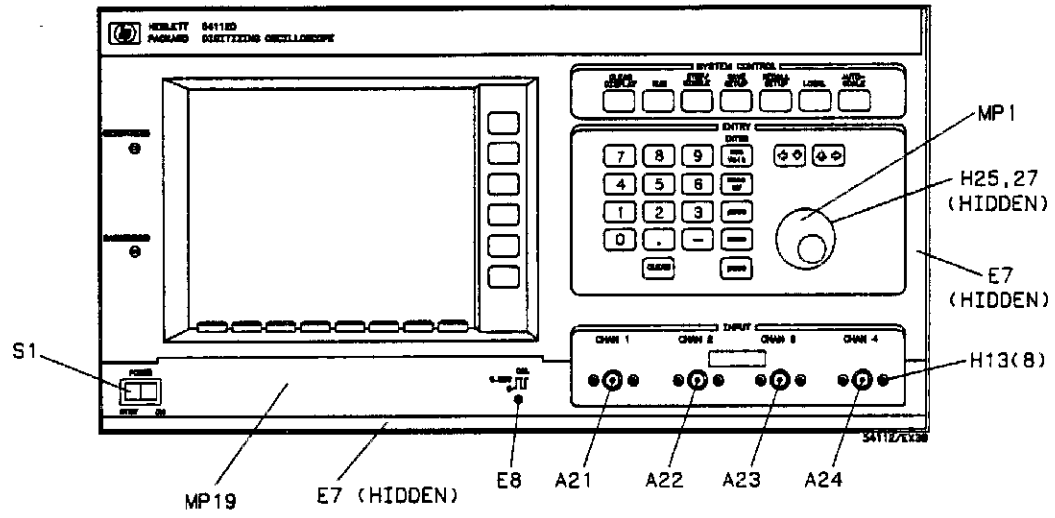
ABBREVIATIONS

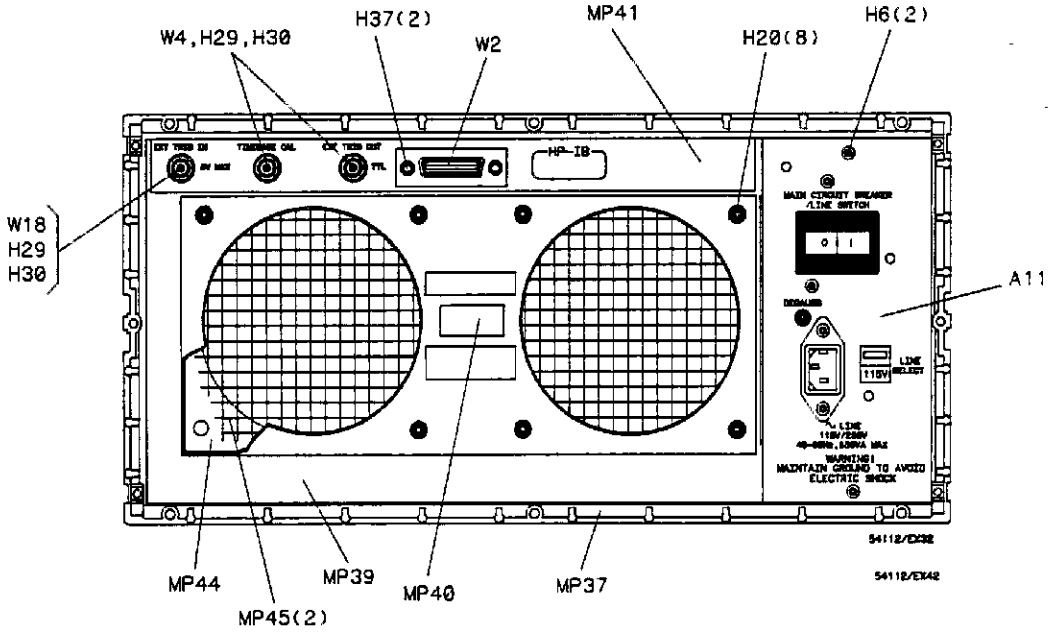
A	=amperes	DWL	=dowel	MFR	=manufacturer	RND	=round
A/D	=analog-to-digital	ECL	=emitter coupled logic	MICPROC	=microprocessor	ROM	=read-only memory
AC	=alternating current	ELAS	=elastomeric	MINTR	=miniature	RPG	=rotary pulse generator
ADJ	=adjust(ment)	EXT	=external	MISC	=miscellaneous	RX	=receiver
AL	=aluminum	F	=farads;metal film (resistor)	MLD	=molded	S	=Schottky-clamped, seconds(time)
AMPL	=amplifier	FC	=carbon film/ composition	MM	=millimeter	SCR	=screw;silicon controlled rectifier
ANLG	=analog	FD	=feed	MO	=metal oxide	SEC	=second(time);secondary
ANSI	=American National Standards Institute	FEM	=female	MTG	=mounting	SEG	=segment
ASSY	=assembly	FF	=flip-flop	MTLC	=metallic	SEL	=selector
ASTIG	=astigmatism	FL	=flat	MUX	=multiplexer	SGL	=single
ASYNCHRO	=asynchronous	FM	=foam;from	MW	=milliwatt	SHF	=shift
ATTEN	=attenuator	FR	=front	N	=nano(10^{-9})	SI	=silicon
AWG	=American wire gauge	FT	=gain bandwidth product	NC	=no connection	SIP	=single in-line package
BAL	=balance	FW	=full wave	NMOS	=n-channel metal-oxide-semiconductor	SKT	=skirt
BCD	=binary-code decimal	FXD	=fixed	NPN	=negative-positive-negative	SL	=slide
BD	=board	GEN	=generator	NPRN	=neoprene	SLDR	=solder
BFR	=buffer	GND	=ground(ed)	NRFR	=not recommended for field replacement	SLT	=slotted)
BIN	=binary	GP	=general purpose	NSR	=not separately replaceable	SOLD	=solenoid
BRDG	=bridge	GRAT	=graticule	NUM	=numeric	SPCL	=special
BSHG	=bushing	GRV	=groove	OBD	=order by description	SQ	=square
BW	=bandwidth	H	=hennies;high	OCTL	=octal	SREG	=shift register
C	=ceramic;cermet (resistor)	HD	=hardware	OD	=outside diameter	SRQ	=service request
CAL	=calibrate;calibration	HDND	=hardened	OP AMP	=operational amplifier	STAT	=static
CC	=carbon composition	HG	=mercury	OSC	=oscillator	STD	=standard
CCW	=counterclockwise	HGT	=height	P	=plastic	SYNCHRO	=synchronous
CER	=ceramic	HLCL	=helical	P/O	=part of	TA	=tantalum
CFM	=cubic feet/minute	HORIZ	=horizontal	PC	=printed circuit	TBAX	=tubeaxial
CH	=choke	HP	=Hewlett-Packard	PCB	=printed circuit board	TC	=temperature coefficient
CHAM	=chamfered	HP-IB	=Hewlett-Packard Interface Bus	PD	=power dissipation	TD	=time delay
CHAN	=channel	HR	=hour(s)	PF	=picofards	THD	=thread(ed)
CHAR	=character	HV	=high voltage	PI	=plug in	THK	=thick
CM	=centimeter	HZ	=Hertz	PL	=plate(d)	THRU	=through
CMOS	=complementary metal-oxide-semiconductor	I/O	=input/output	PLA	=programmable logic array	TP	=test point
CMR	=common mode rejection	IC	=integrated circuit	PLST	=plastic	TPG	=tapping
CNDCT	=conductor	ID	=inside diameter	PNP	=positive-negative-positive	TPL	=triple
CNTR	=counter	IN	=inch	POLYE	=polyester	TRANS	=transformer
CON	=connector	INCL	=includes)	POS	=positive;position	TRIG	=trigger(ed)
CONT	=contact	INCAND	=incandescent	POT	=potentiometer	TRMR	=trimmer
CRT	=cathode-ray tube	INP	=input	POZI	=pozidrive	TRN	=turn(s)
CW	=clockwise	INTEN	=intensity	PP	=peak-to-peak	TTL	=transistor-transistor
D	=diameter	INTL	=internal	PPM	=parts per million	TX	=transmitter
D/A	=digital-to-analog	INV	=inverter	PRCN	=precision	U	=micro(10^{-6})
DAC	=digital-to-analog converter	JFET	=junction field-effect transistor	PREAMP	=preamplifier	UL	=Underwriters Laboratory
DARL	=darlington	JKT	=jacket	PRGMBL	=programmable	UNREG	=unregulated
DAT	=data	K	=kilo(10^{3})	PRL	=parallel	VA	=voltampere
DBL	=double	L	=low	PROG	=programmable	VAC	=volt,ac
DBM	=decibel referenced to 1mW	LB	=pound	PSTN	=position	VAR	=variable
DC	=direct current	LCH	=latch	PT	=point	VCO	=voltage-controlled oscillator
DCDR	=decoder	LCL	=local	PW	=potted wirewound	VDC	=volt,dc
DEG	=degree	LED	=light-emitting diode	PWR	=power	VERT	=vertical
DEMUX	=demultiplexer	LG	=long	R-S	=reset-set	VF	=voltage,filtered
DET	=detector	LI	=lithium	RAM	=random-access memory	VS	=versus
DIA	=diameter	LK	=lock	RECT	=rectifier	W	=watts
DIP	=dual in-line package	LKWR	=lockwasher	RET	=retainer	W/	=with
DIV	=division	LS	=low power Schottky	RF	=radio frequency	W/O	=without
DMA	=direct memory access	LV	=low voltage	RGLTR	=regulator	WW	=wirewound
DPDT	=double-pole, double-throw	M	=mega(10^{6});megohms, meter(distance)	RGTR	=register	XSTR	=transistor
DRC	=DAC refresh controller	MACH	=machine	RK	=rack	ZNR	=zener
DRVR	=driver	MAX	=maximum	RMS	=root-mean-square	°C	=degree Celsius (Centigrade)
						°F	=degree Fahrenheit
						°K	=degree Kelvin



COVER PARTS

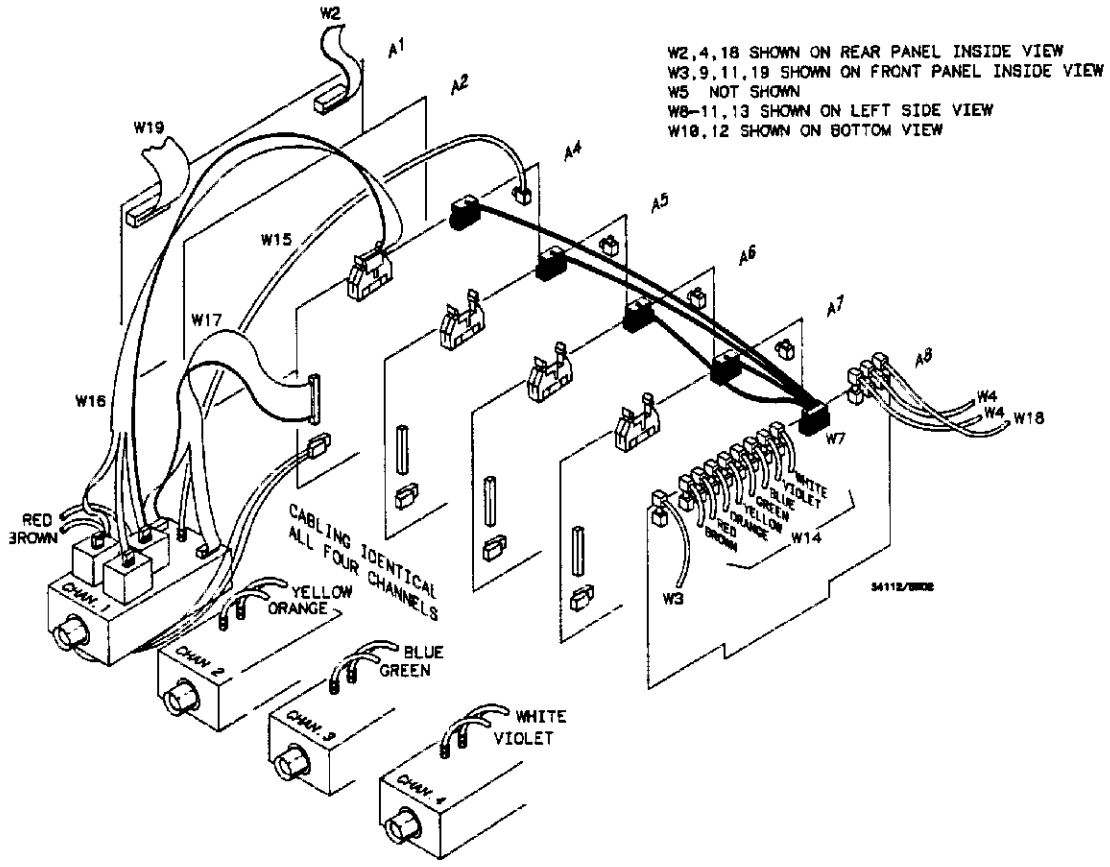
Figure 5-1. Mainframe Parts Locations (sheet 1 of 7)





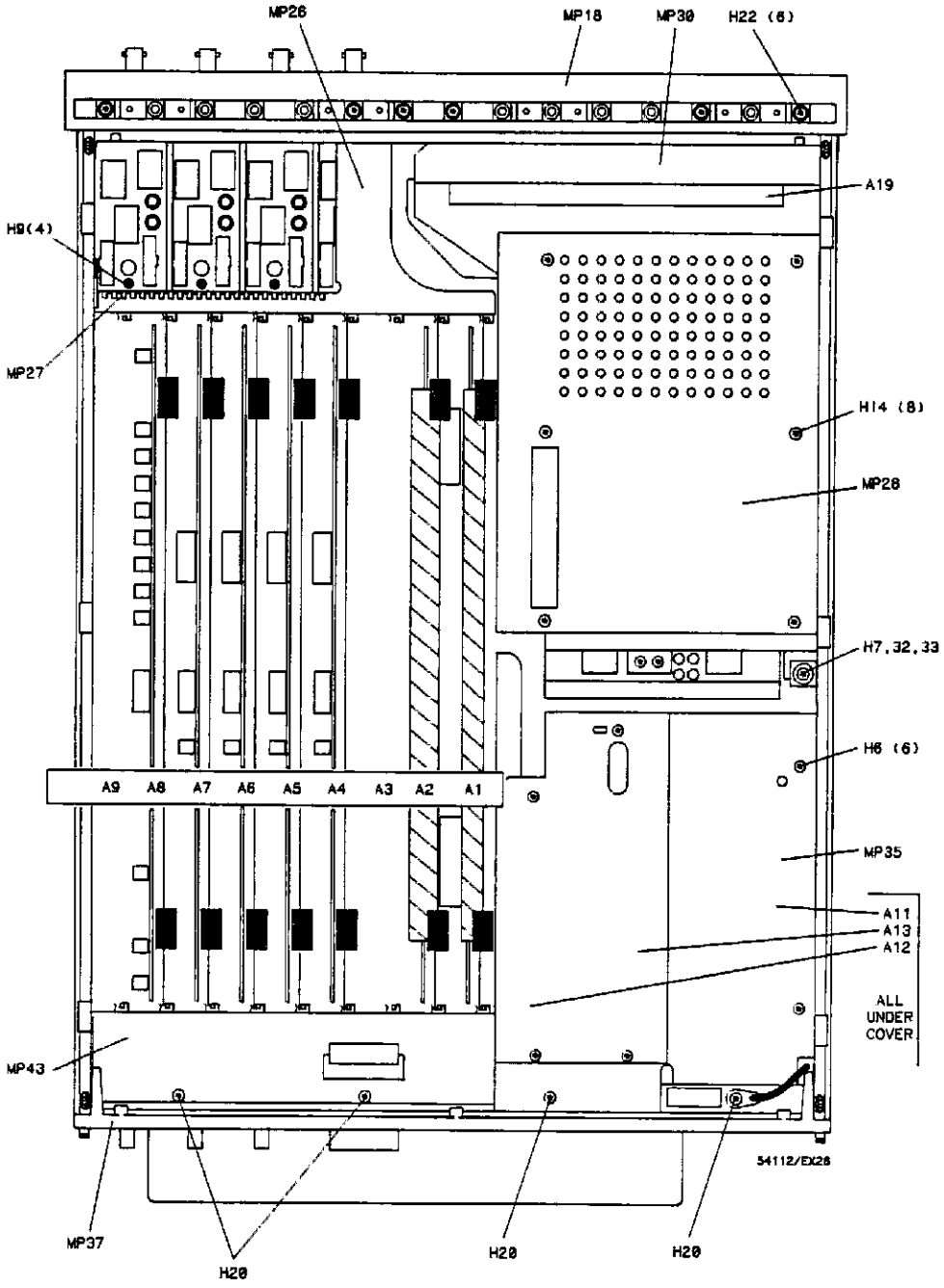
FRONT AND REAR PANEL VIEWS

Figure 5-1. Mainframe Parts Locations (sheet 2 of 7)



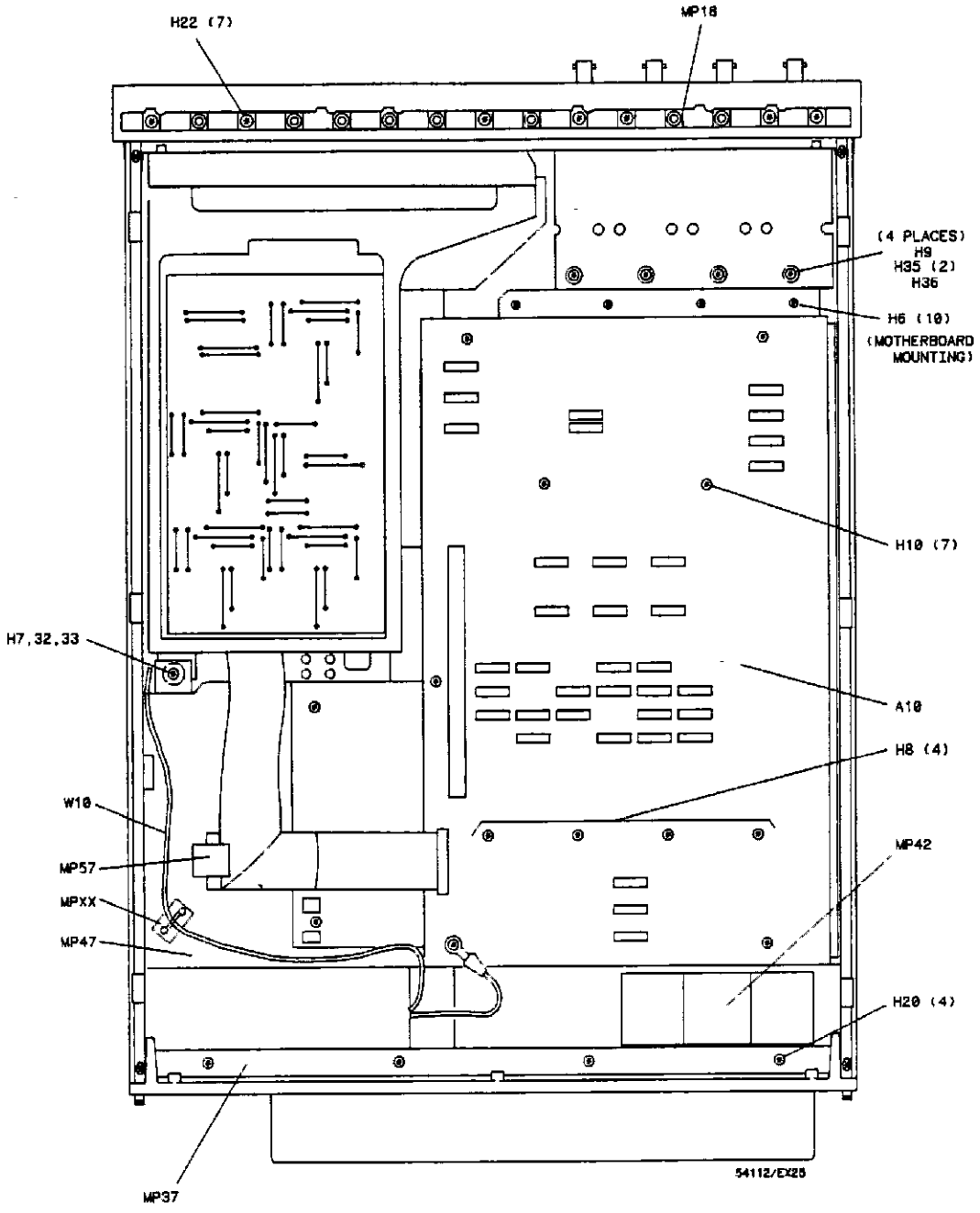
CABLING

Figure 5-1. Mainframe Parts Locations (sheet 3 of 7)



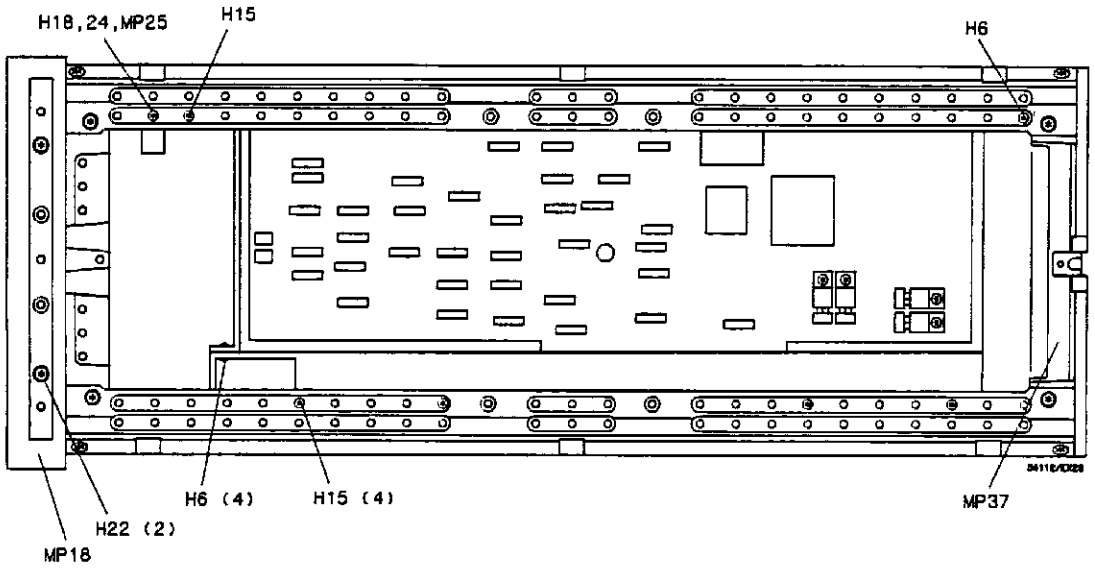
INSIDE, TOP VIEW

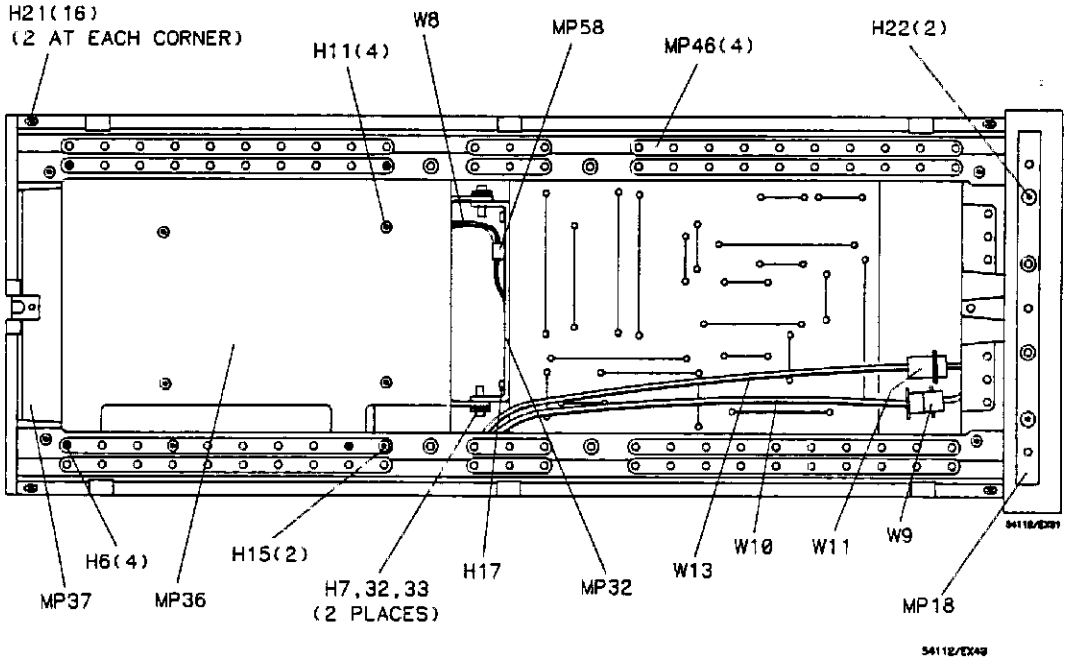
Figure 5-1. Mainframe Parts Locations (sheet 4 of 7)



INSIDE, BOTTOM VIEW

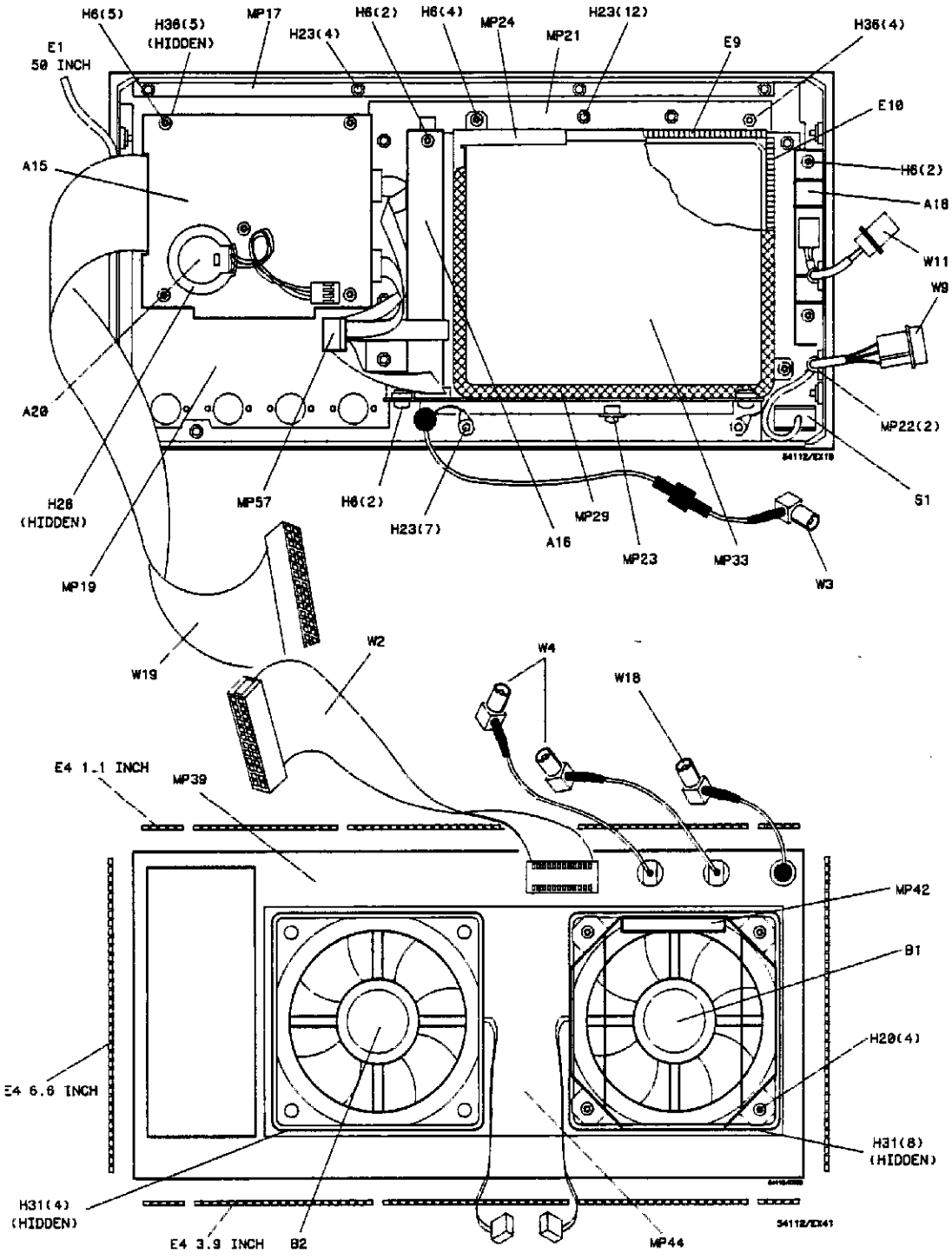
Figure 5-1. Mainframe Parts Locations (sheet 5 of 7)





INSIDE, SIDE VIEWS

Figure 5-1. Mainframe Parts Locations (sheet 6 of 7)



FRONT AND REAR PANELS, INSIDE VIEW

Figure 5-1. Mainframe Parts Locations (sheet 7 of 7)

Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				CURRENT PARTS LIST FOR HP 54112D		
				MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIX 2735A		
EXCHANGE ASSEMBLIES				(See paragraph 5-4 for exchange assembly ordering information)		
A1	54111-69506	8	1	INPUT/OUTPUT ASSEMBLY	28480	54111-69506
A2	54111-69511	5	1	MICROPROCESSOR ASSEMBLY	28480	54111-69511
A3				NOT ASSIGNED		
A4	54112-69503	8	4	ADC ASSEMBLY CHANNEL 1	28480	54112-69503
A5	54112-69503	6		ADC ASSEMBLY CHANNEL 2	28480	54112-69503
A6	54112-69503	6		ADC ASSEMBLY CHANNEL 3	28480	54112-69503
A7	54112-69503	8		ADC ASSEMBLY CHANNEL 4	28480	54112-69503
A8	54112-69502	5	1	TIMEBASE/TRIGGER ASSEMBLY	28480	54112-69502
A9				NOT ASSIGNED		
A10	54110-69512	5	1	BD ASSY COLOR DISPLAY	28480	54110-69512
A11	54110-69504	5	1	BD ASSY PRIMARY POWER SUPPLY	28480	54110-69504
A12	54110-69510	3	1	BD ASSY ANALOG POWER SUPPLY	28480	54110-69510
A13	54110-69508	1	1	BD ASSY DIGITAL POWER SUPPLY	28480	54110-69508
EXTERNAL PARTS						
E1	8160-0577	4	8ft	GASKET - RFI - BRAIDED WIRE - 0.1 IN	28480	8160-0577
E2	0363-0125	0	2	CONTACT STRIP - FINGERS - 24 IN LENGTH	28480	0363-0125
E3				NOT ASSIGNED		
H1	0515-1384	8	4	SCREW-MACH M5 10MM-LG FLAT-HEAD T25	00000	ORDER BY DESCRIPTION
H2	0515-1444	1	4	SCREW-MACH M3.5 25 4MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H3	0515-1245	0	2	SCREW-MACH M3.5 12MM-LG COVER MOUNTING	28480	0515-1245
H4	0510-1253	0	2	RETAINING RING FOR COVER MOUNTING SCREW	28480	0510-1253
H5				NOT ASSIGNED		
MP1	01650-47401	7	1	KNOB - RPG	28480	01650-47401
MP2	5061-9448	3	1	COVER - BOTTOM	28480	5061-9448
MP3	5040-7201	8	2	FOOT - BOTTOM - FRONT	28480	5040-7201
MP4	5040-7222	3	2	FOOT - BOTTOM REAR - NON SKID	28480	5040-7222
MP5	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP6				NOT ASSIGNED		
MP7	54112-04104	7	1	CVR - TOP	28480	54112-04104
MP8	54112-94302	6	1	CABLE ROUTING DIAGRAM	28480	54112-94302
MP9	5001-0441	2	2	TRIM STRIP - SIDE - SELF STICK	28480	5001-0441
MP10	5040-7202	9	1	TRIM STRIP - TOP - PLASTIC	28480	5040-7202
MP11	54110-40502	3	4	FOOT - REAR PANEL	28480	54110-40502
MP12				NOT ASSIGNED		
MP13				NOT ASSIGNED		
MP14	5060-9805	4	2	STRAP - HANDLE	28480	5060-9805
MP15	5041-6819	4	2	CAP - STRAP HANDLE (FRONT)	28480	5041-6819
MP16	5041-6820	7	2	CAP - STRAP HANDLE (REAR)	28480	5041-6820
W1	8120-1521	8	1	POWER CORD 125V USA/CANADA	28480	8120-1521
	8120-1703	6		POWER CORD OPTION 900 UNITED KINGDOM	28480	8120-1703
	8120-0698	4		POWER CORD OPTION 901 AUST/NEW ZEALAND	28480	8120-0698
	8120-1692	2		POWER CORD OPTION 902 EUROPEAN CONTINENT	28480	8120-1692
	8120-0698	6		POWER CORD OPTION 904 250V USA/CANADA	28480	8120-0698
	8120-2296	4		POWER CORD OPTION 906 SWITZERLAND	28480	8120-2296
	8120-2957	4		POWER CORD OPTION 912 DENMARK	28480	8120-2957
	8120-4211	7		POWER CORD OPTION 917 SOUTH AFRICA	28480	8120-4211
	8120-4754	3		POWER CORD OPTION 918 JAPAN	28480	8120-4754
PROBES	10033A	8	4	DIVIDER PROBE - 10:1	28480	10033A
RACK MOUNT KIT	5061-9679	2		RACK MOUNT KIT - OPTION 908	28480	5061-9679

See Introduction to this section for ordering information

Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
INTERNAL PARTS						
A1	54111-66508	2	1	INPUT/OUTPUT ASSEMBLY	28480	54111-66508
A2	54111-66511	9	1	MICROPROCESSOR ASSEMBLY	28480	54111-66511
A3				NOT ASSIGNED		
A4	54112-66503	0	4	ADC ASSEMBLY CHANNEL 1	28480	54112-66503
A5	54112-66503	0		ADC ASSEMBLY CHANNEL 2	28480	54112-66503
A6	54112-66503	0		ADC ASSEMBLY CHANNEL 3	28480	54112-66503
A7	54112-66503	0		ADC ASSEMBLY CHANNEL 4	28480	54112-66503
A8	54112-66502	9	1	TIMEBASE/TRIGGER ASSEMBLY	28480	54112-66502
A9				NOT ASSIGNED		
A10	54110-66512	9	1	COLOR DISPLAY ASSEMBLY	28480	54110-66512
A11	54110-66513	0	1	BD ASSY PRIMARY POWER SUPPLY	28480	54110-66513
A12	54110-66510	7	1	BD ASSY ANALOG POWER SUPPLY	28480	54110-66510
A13	54110-66506	1	1	BD ASSY DIGITAL POWER SUPPLY	28480	54110-66506
A14	54110-66511	8	1	BD ASSY MOTHER	28480	54110-66511
A15	54100-66505	8	1	BD ASSY CONTROL KEYBOARD	28480	54100-66505
A16	54110-66502	7	1	BD ASSY FUNCTION KEYBOARD	28480	54110-66502
A17	54100-66520	7	1	BD ASSY MENU KEYBOARD	28480	54100-66520
A18	54111-66514	2	1	BD ASSY DISPLAY CONTROL	28480	54111-66514
A19	2090-0092	3	1	MODULE - COLOR CRT * *Also order 8 ea M14 3 mm tapping screws	28480	2090-0092
A20	01980-61062	5	1	ASSY - RPG	28480	01980-61062
A21	1NC1-0003	9	4	ATTENUATOR ASSEMBLY CHANNEL 1	28480	1NC1-0003
A22	1NC1-0003	9		ATTENUATOR ASSEMBLY CHANNEL 2	28480	1NC1-0003
A23	1NC1-0003	9		ATTENUATOR ASSEMBLY CHANNEL 3	28480	1NC1-0003
A24	1NC1-0003	9		ATTENUATOR ASSEMBLY CHANNEL 4	28480	1NC1-0003
B1	3160-0521	3	2	FAN - TUBEAXIAL	28480	3160-0521
B2	3160-0521	3		FAN - TUBEAXIAL	28480	3160-0521
E4	8160-0590	8	3	RFI STRIP - FINGERS - 18 INCH LENGTH	28480	8160-0590
E5				NOT ASSIGNED		
E6				NOT ASSIGNED		
E7	4320-0418	8	1	GASKET - RFI - BRAIDED WIRE - 0.2 IN	28480	4320-0418
E8	0360-1848	8	1	TEST POINT - FRONT PANEL CAL SIGNAL	28480	0360-1848
E9	54112-07101	0	2	RFI STRIP - FINGERS - CRT BEZEL - LONG	28480	54112-07101
E10	54112-07102	1	2	RFI STRIP - FINGERS - CRT BEZEL - SHORT	28480	54112-07102
H6	0515-0372	2	48	SCREW-MACH M3 8MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H7	0515-0684	5	2	SCREW-MACH M3 12MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H8	0515-0430	3	4	SCREW-MACH M3 6MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H9	0515-0665	6	8	SCREW-MACH M3 14MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H10	0515-1410	1	7	SCREW-MACH M3 20MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H11	0515-1025	8	4	SCREW-MACH M3 26MM-LG PAN-HD T10	00000	ORDER BY DESCRIPTION
H12				NOT ASSIGNED		
H13	0515-1035	4	8	SCREW-MACH M3 8MM-LG FLAT-HEAD T10	00000	ORDER BY DESCRIPTION
H14	0515-1271	2	8	SCREW-MACH M3 6MM-LG THREAD ROLLING	00000	ORDER BY DESCRIPTION
H15	0515-0433	6	8	SCREW-MACH M4 8MM-LG PAN-HD T15	00000	ORDER BY DESCRIPTION
H16				NOT ASSIGNED		
H17	0515-0841	8	2	SCREW-MACH M4 10MM-LG THREAD ROLLING	00000	ORDER BY DESCRIPTION
H18	0515-0435	8	13	SCREW-MACH M4 14MM-LG PAN-HD T15	00000	ORDER BY DESCRIPTION
H19				NOT ASSIGNED		
H20	0515-0380	3	12	SCREW-MACH M4 10MM-LG PAN-HD T15	00000	ORDER BY DESCRIPTION
H21	0515-1403	2	16	SCREW-MACH M4 6MM-LG FLAT-HEAD T15	00000	ORDER BY DESCRIPTION
H22	0515-1269	9	17	SCREW-MACH M4 10MM-LG FLAT-HEAD T15	00000	ORDER BY DESCRIPTION
H23	0535-0031	2	23	NUT-HEX M3 W/LOCK WASHER	00000	ORDER BY DESCRIPTION
H24	0535-0043	6	1	NUT-HEX M4 W/LOCK WASHER	00000	ORDER BY DESCRIPTION
H25	2950-0043	6	1	NUT-HEX 3/8-32	00000	ORDER BY DESCRIPTION
H26	3050-1176	3	1	WASHER-FLAT NYLON 3/8	28480	3050-1176
H27	2190-0018	3	1	WASHER-INTERNAL LOCK 3/8	00000	ORDER BY DESCRIPTION
H28				NOT ASSIGNED		
H29	2950-0035	4	3	NUT-HEX 15/32-32	00000	ORDER BY DESCRIPTION
H30	2190-0068	5	3	WASHER-INTERNAL LOCK 1/2	00000	ORDER BY DESCRIPTION
H31	5061-6138	2	12	NUT-INSERT M4	28480	5061-6138
H32	2190-0763	1	2	WASHER-FLAT METAL 0.14ID 0.50D	28480	2190-0763
H33	3050-1238	8	2	WASHER-FLAT NEOPRENE 0.149ID 0.478OD	28480	3050-1238
H34				NOT ASSIGNED		
H35	3050-0005	5	8	WASHER-SHOULDER 0.14ID 0.375OD	28480	3050-0005
H36	0380-1902	9	13	STANDOFF-HEX M3	28480	0380-1902
H37	0380-1686	6	2	STANDOFF-HEX HP-IB	28480	0380-1686
MP17	54112-01206	4	1	UPPER BRACKET - FRONT PANEL	28480	54112-01206
MP18	5021-5807	6	1	FRAME - FRONT	28480	5021-5807
MP19	54112-00201	7	1	PANEL - FRONT	28480	54112-00201
MP20	54112-01205	3	1	LOWER BRACKET - FRONT PANEL	28480	54112-01205

See introduction to this section for ordering information

Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP21	54112-02201	1	1	BEZEL - CRT	28480	54112-02201
MP22	1400-1122	0	2	CLAMP - CABLE - STICK-ON	28480	1400-1122
MP23	0403-0092	6	1	RUBBER BUMPER (MENU KEYBOARD SUPPORT)	28480	0403-0092
MP24	54112-01204	2	1	RETAINER - GLASS FILTER * * Also order 1 ea MP29 CRT dust barrier	28480	54112-01204
MP25	1400-0025	0	1	CLAMP - CABLE - TRIG CABLE SUPPORT	28480	1400-0025
MP26	54111-01203	0	1	BKT - CARD CAGE FRONT	28480	54111-01203
MP27	0400-0018	0	.4ft	CHANNEL GROMMET - NYLON	28480	0400-0018
MP28	54112-00808	5	1	SHIELD - COLOR CRT MODULE	28480	54112-00808
MP29	54100-42701	6	1	CRT DUST BARRIER - FOAM	28480	54100-42701
MP30	54112-01203	1	1	BRACKET - COLOR CRT MOD - FRONT TOP	28480	54112-01203
MP31	54112-01202	0	1	BRACKET - COLOR CRT MOD - FRONT BOTTOM	28480	54112-01202
MP32	54110-04702	9	1	BRACKET - COLOR CRT MOD - REAR	28480	54110-04702
MP33	54112-22701	8	1	GLASS FILTER * * Also order 1 ea MP29 CRT dust barrier	28480	54112-22701
MP34				NOT ASSIGNED		
MP35	54112-04103	8	1	COVER - POWER SUPPLY (TOP)	28480	54112-04103
MP36	54112-04101	4	1	COVER - POWER SUPPLY (SIDE)	28480	54112-04101
MP37	5021-5808	7	1	FRAME - REAR	28480	5021-5808
MP38	54110-94303	5	1	LABEL - GROUND CONNECTION WARNING	28480	54110-94303
MP39	54112-60201	3	1	PANEL - REAR	28480	54112-60201
MP40	5958-5582	9	1	LABEL - X-RAY	28480	5958-5582
MP41	54112-94301	5	1	LABEL - REAR PANEL CONNECTORS	28480	54112-94301
MP42	54112-85201	3	1	AIR DIFFUSER ASSEMBLY	28480	54112-85201
MP43	54112-05201	7	1	BRACKET - CARD CAGE - REAR	28480	54112-05201
MP44	54112-04701	0	1	SPACER - FAN	28480	54112-04701
MP45	18500-00803	3	2	SCREEN - FAN	28480	18500-00803
MP46	5021-5838	3	4	STRUT - SIDE	28480	5021-5838
MP47	54111-00101	5	1	DECK - MAIN	28480	54111-00101
MP48				NOT ASSIGNED		
MP49	5041-1480	5	2	WIRE MARKER - BROWN	28480	5041-1480
MP50	5041-1481	6	2	WIRE MARKER - WHITE	28480	5041-1481
MP51	5041-1482	7	2	WIRE MARKER - VIOLET	28480	5041-1482
MP52	5041-1483	8	2	WIRE MARKER - BLUE	28480	5041-1483
MP53	5041-1484	9	2	WIRE MARKER - GREEN	28480	5041-1484
MP54	5041-1485	0	2	WIRE MARKER - YELLOW	28480	5041-1485
MP55	5041-1486	1	2	WIRE MARKER - ORANGE	28480	5041-1486
MP56	5041-1487	2	2	WIRE MARKER - RED	28480	5041-1487
MP57	1400-0611	0	2	CLAMP - RIBBON CABLE	28480	1400-0611
MP58	1400-0679	0	1	CLAMP - CABLE	28480	1400-0679
MP59	1400-1362	0	1	CLAMP - CABLE - TWIST TYPE	28480	1400-1362
S1	3101-2911	5	1	SWITCH - ROCKER (Standby)	28480	3101-2911
W2	54111-61612	1	1	CABLE - HPIB	28480	54111-61612
W3	54112-61610	0	1	CABLE - COAX - FRONT PANEL CAL SIGNAL	28480	54112-61610
W4	54100-61610	6	2	CABLE - COAX - TRIG OUT - TIMEBASE CAL	28480	54100-61610
W5	54100-61612	8	2	CABLE - 3-WIRE - 300VDC PRIMARY POWER	28480	54100-61612
W6				NOT ASSIGNED		
W7	54112-61604	2	1	CABLE - ACQUISITION CLOCK	28480	54112-61604
W8	54110-61601	5	1	CABLE - 3-WIRE - COLOR CRT MOD POWER	28480	54110-61601
W9	54112-61606	4	1	CABLE - SHIELDED - STBY SWITCH - FRONT	28480	54110-61610
W10	54111-61610	9	1	CABLE - SHIELDED - STBY SWITCH - REAR	28480	54111-61610
W11	54112-61611	9	1	CABLE - DISPLAY CONTROL - FRONT	28480	54112-61611
W12	54110-61607	3	1	CABLE - RIBBON - DISP ASSY TO COLOR MOD	28480	54110-61607
W13	54112-61612	1	1	CABLE - DISPLAY CONTROL - REAR	28480	54112-61612
W14	54111-61602	9	8	CABLE - COAX - TCLOCK/LTCLOCK	28480	54111-61602
W15	54112-61608	6	4	CABLE - VERTICAL SIGNAL	28480	54112-61608
W16	54111-61604	1	4	CABLE - ATTENUATOR SOLENOID CABLE	28480	54111-61604
W17	54111-61605	2	4	CABLE - RIBBON - ATTENUATOR POWER	28480	54111-61605
W18	54112-61602	0	1	CABLE - COAX - EXTERNAL TRIGGER INPUT	28480	54112-61602
W19	54100-61601	3	1	CABLE - RIBBON - I/O TO FRONT PANEL	28480	54100-61601

See introduction to this section for ordering information

Table 5-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
C0633	RIFA	BROMMA	SE	
S0167	FUJITSU LTD	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01281	TRW INC SEMICONDUCTOR DIV	LAWNDALE	CA	90260
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
06665	PRECISION MONOLITHICS INC	SANTA CLARA	CA	95050
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
18546	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
15454	AMETEK/RODAN DIV	ANAHEIM	CA	92808
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25403	N.V. PHILIPS-ELCOMA DEPARTMENT	EINDHOVEN	HL	02878
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
52763	STETTNER ELECTRONICS INC	CHATTANOOGA	TN	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72138	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
73138	BECKMAN INSTRUMENTS INC HELIPOT DIV	FULLERTON	CA	92634
75915	LITTELFUSE INC	DES PLAINES	IL	80018

SECTION 6A
MAINFRAME DISASSEMBLY

6A-1. INTRODUCTION

This section contains removal and replacement procedures for mainframe assemblies. It includes a diagram showing assembly locations and a diagram showing cabling.

6A-2. SAFETY CONSIDERATIONS

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

WARNING

The standby switch on the front panel of this instrument DOES NOT de-energize all power supplies. To avoid shock hazards capable of causing injury or death, de-energize the instrument with the main power switch on the rear panel or by disconnecting the power cable.

WARNING

These procedures are used while repairing an instrument without protective covers and which may have been recently powered. Only trained service personnel who are aware of the hazards involved (for example, fire and electrical shock) should perform this maintenance. Read the Safety Summary in the front of this manual.

CAUTION

Do not remove or replace any circuit board assemblies in this instrument while power is applied. The assemblies contain components which may be damaged if the assembly is removed or replaced while instrument is powered.

6A-3. TOOLS REQUIRED

Most hardware requires TORX® type tools in size #10, #15, #20, or #25. Also needed might be wrenches size 4.5 mm, 5.5 mm (7/32 inch), 9/32 inch (also fits 7 mm), 8 mm, 7/16 inch, and 15/32 inch.

A 6 mm open end wrench is needed when replacing an Attenuator assembly. This wrench is provided in the HP 54100 Family Support Kit.

6A-4. COVERS

There are two outside covers on the HP 54112D – a top cover (which also covers the sides) and a bottom cover. For most procedures it is not necessary to remove the bottom cover. However, for easier removal of the top cover, remove the bottom cover first.

While removing covers, note where shielding braid is located. If it separates from the covers, reinstall it when replacing covers or the instrument may not meet EMI specifications.

COVER REMOVAL

1. Remove rear feet. Their screws are accessible through the holes in the end.

2. Remove side strap handles. Note that the handles have smoother curves on the side closest to instrument. Reinstall with the same side toward the instrument.

3. Remove bottom cover. The screw at the rear center of the cover is captive and it will pull the cover back as it is removed.

   If the shielding braid pulls out of the channel at the edges of the top cover, be sure to reinstall it before replacing the cover.

4. Remove top cover. The screw at the rear center of this cover is also captive and will pull the cover back as it is removed.

   Later covers have two threaded inserts, identifiable by two holes either side of the cover screw and near the sides. Install a 3 mm screw about 25 mm long into each insert. When screwed in they will contact the frame and help force the cover off.

   Use the effective force of these screws while removing the cover with the center screw. Notice that the removal effect is with counter-clockwise rotation of the center screw and clockwise rotation of the side screws.

COVER INSTALLATION

Cover replacement is the reverse of removal.

CAUTION

Be sure all shielding components are installed when reinstalling covers. Incomplete shielding may result in the instrument not meeting EMI specifications. Refer to the drawings in the parts list for locations of shielding parts.

6A-5. MAJOR ASSEMBLY REMOVAL PROCEDURES

The following procedures should be followed when disassembling the instrument. Particular care should be taken with the cabling connecting card cage assemblies and attenuators.

6A-6. Card Cage PC Assemblies

REMOVAL

1. Disconnect power cable.
2. Remove covers (see previous procedure).
3. Disconnect any cables from assembly to be removed. Be very careful to pull coaxial connectors straight off. Do not bend the connectors. Some assemblies have cables along the front edge. These must be removed before the assembly is pulled up.
4. Refer to the illustration on top the power supply. Release PC assembly by pulling the flexible plastic extractors away from the assembly shield, then up.
5. Pull the assembly from the connector by pulling up on the extractors. As the assembly is removed, check for cables connected to the center of the assembly and remove them.

CAUTION

Removing the Microprocessor or Input/Output assemblies (A1 or A2) results in loss of calibration.

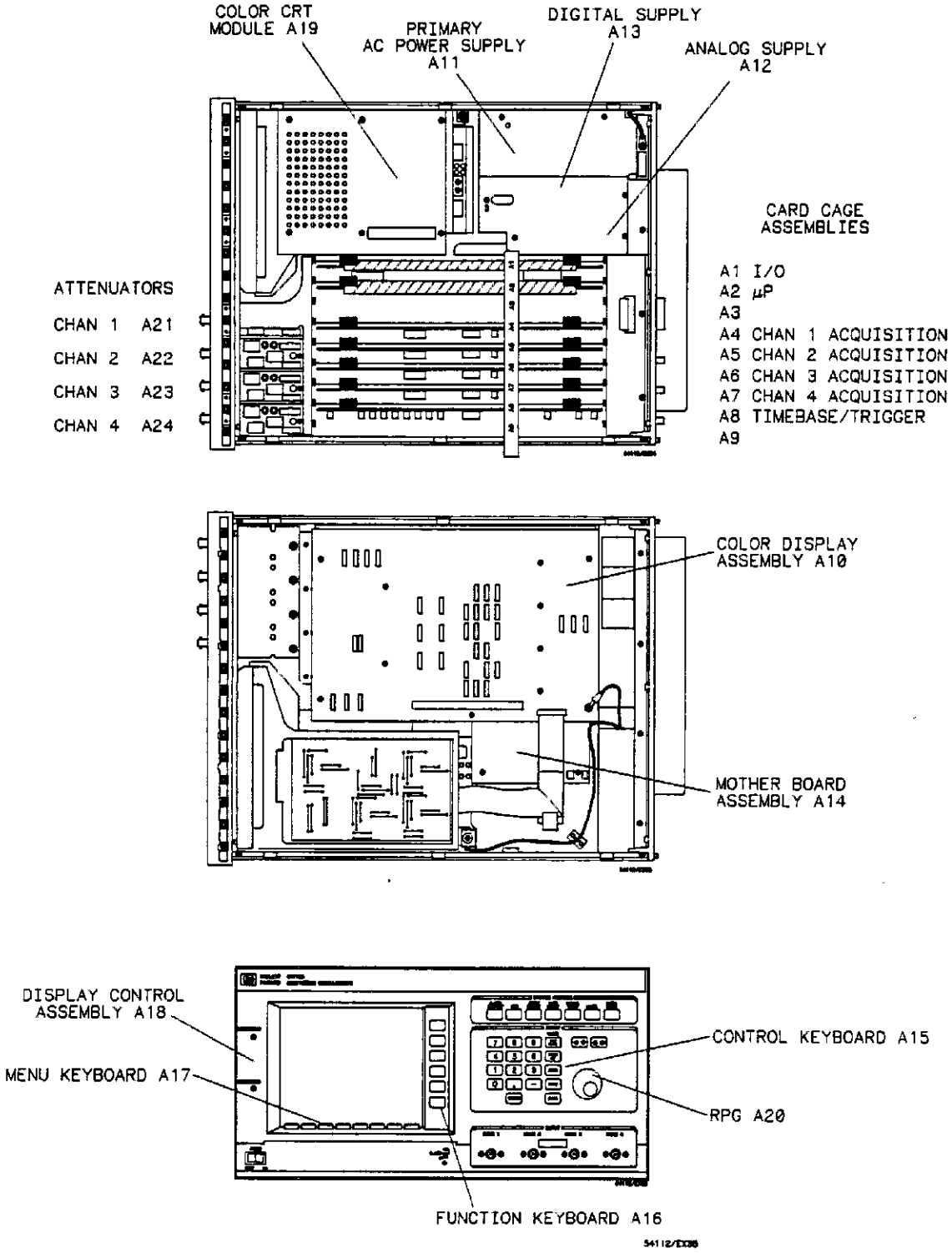


Figure 6A-1. Major Assembly Locations.

REPLACEMENT

1. Insert PC assembly shield edges in proper guides.
2. Keep the extractors up while sliding the assembly in.
3. If the assembly has cabling to its center area, it must be connected as the board is being inserted.
4. If the assembly has cabling to its front edge, it will be easier to connect the cables as soon as the connector is below the top edge of the card cage frame. Refer to the cabling diagram on the instrument top cover or the diagram at the end of this section.
5. While keeping assembly properly aligned in guides, push it in. When the top edge of the assembly is nearly level with the top of the card cage, the connector will start to engage. Keep assembly level and apply even pressure until connector is seated.

CAUTION

Do not use the extractors to lever the assembly into the connector. *Using the extractors makes it too easy to apply excessive force that might bend misaligned connector pins. If the connector will not seat with moderate pressure, remove the assembly and check for bent pins.*

Avoid pinching cabling between the assembly and the mainframe. Coaxial cables are particularly vulnerable to damage by pinching.

6. Reconnect all remaining cabling. Refer to the diagram on the instrument cover or the diagram at the end of this section.

6A-7. Power Supplies

This procedure should be used to remove all supplies: Primary, Digital, and Analog. Follow the procedure as far as necessary to remove the desired supply.

PRIMARY SUPPLY REMOVAL

1. Disconnect power cable.
2. Remove covers (see cover removal procedure).

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard be sure the AC power cable is disconnected before continuing with this procedure.

3. Through the hole in the top power supply shield, observe the red LED located on the Primary Power Supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding.
4. Remove top power supply shield (six small screws, and one large screw at rear frame).
5. Remove the screw that attaches the ground wire (green/yellow) to top corner of rear frame.
6. Remove the three cables at the top front of the Primary Power Supply PC board.
7. Remove four screws from power supply side cover (figure 6A-2).
8. Remove two screws which attach power supply assembly to rear panel (figure 6A-2).
9. Turn instrument onto its left side. Pull the power supply assembly rearward until the STBY switch cable at the rear bottom of power supply board can be disconnected. Disconnect the cable.
10. Pull supply rearward until it clears the instrument.
11. Continue with step 12 to remove the Digital and/or Analog supplies.

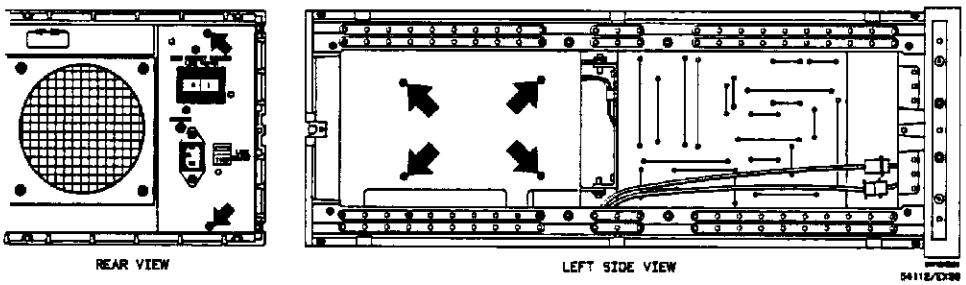


Figure 6A-2. Primary Power Supply Mounting Screws.

PRIMARY SUPPLY REPLACEMENT

Reverse removal procedure to install supply.

WARNING

Power supply safety grounding will be defeated if ground wire removed in step 5 above is not reconnected. To avoid a defeated ground, make sure this green/yellow wire is re-attached to top rear corner of the rear frame.

DIGITAL SUPPLY REMOVAL

12. After removing the Primary supply, steps 1 through 10, use a flat-blade screwdriver to loosen the captive screw at the bottom front of the Digital supply.

13. Release power supply board connector by pulling board straight up and off the guide posts.

14. Slide the rear end of the supply toward the left side of the instrument so that it is diagonal in the power supply area. It can then be lifted out of the instrument.

15. Continue with step 16 to remove the Analog supply.

DIGITAL SUPPLY REPLACEMENT

Reverse the procedure to install the Digital and Primary supplies.

WARNING

Power supply safety grounding will be defeated if ground wire removed in step 5 above is not reconnected. To avoid a defeated ground, make sure this green/yellow wire is re-attached to top rear corner of the rear frame.

ANALOG SUPPLY REMOVAL

16. After removing the Primary and Digital supplies, steps 1 through 14, remove the six additional 4 mm screws that secure the rear panel in the rear frame. There are two on the top (two have already been removed) and four on the bottom.

17. Slide the left side of the rear panel (power supply end) out 1 to 2 inches. It shouldn't be necessary to disconnect any of the cabling to the rear panel but it may be necessary to guide cable slack through the rear card cage frame.

18. Use a flat-blade screwdriver to loosen the captive screw at the bottom front of the Analog supply, under the rear edge of the Color CRT Module.

19. Release power supply board connector by pulling board straight up and off the guide posts.

20. Slide the rear end of the supply toward the left side of the instrument so that it is diagonal in the power supply area. Remove it from the instrument by lifting the front end first.

ANALOG SUPPLY REPLACEMENT

Reverse the entire power supply removal procedure to install all supplies.

WARNING

Power supply safety grounding will be defeated if ground wire removed in step 5 above is not reconnected. To avoid a defeated ground, make sure this green/yellow wire is re-attached to top rear corner of the rear frame.

6A-8. Front Panel Assemblies

This procedure covers removal of the front panel, keyboards, CRT Control board, and CRT bezel. Front panel removal is also a step preliminary to removal of Attenuator assemblies and Color CRT Module.

These procedures are necessarily different than those for similar models such as the HP 54110D and 54111D and should be followed without regard to those two instruments. The front frame must be removed along with the front panel and associated assemblies.

FRONT PANEL ASSEMBLY REMOVAL

1. Disconnect main power cable.
2. Remove covers. (See cover removal procedure.)
3. Remove top trim strip. There are two slots (visible from the rear) to aid in removal.
4. Remove the two screws on either side of each of the input BNC connectors.
5. Remove the front panel screws marked in the following figure.

CAUTION

The Instrument will be hard to handle once the connection between the front frame and struts is removed. When the front frame is removed the only support for the Color CRT Module is at the rear bracket. Handle the instrument carefully and with consideration for the structural instability.

6. At each corner of the front frame, remove two screws that attach the struts (long pieces from front to back) to the front frame.

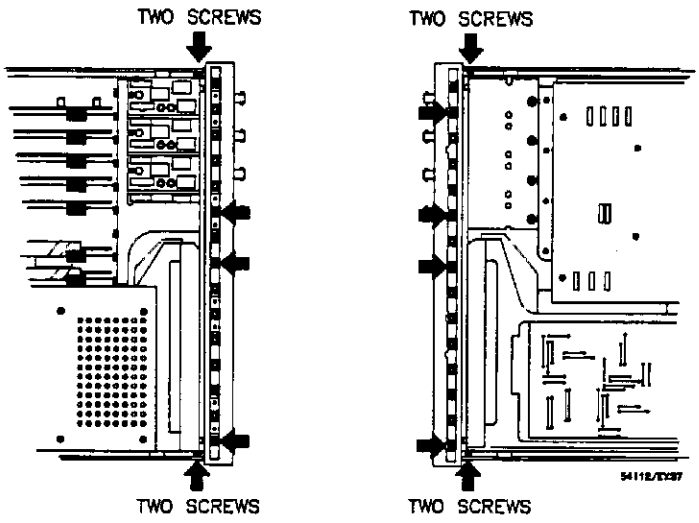


Figure 6A-3. Front Panel Assembly Mounting Screws.

7. Set instrument in its normal operating position.

8. Note the routing of the calibrator signal coax at the front connector on the Timebase/trigger assembly (A8, right-most card cage assembly) and disconnect it at the Timebase/trigger and slide it out through the slot in the card cage frame.

9. Disconnect the STBY switch and Display Control cables by separating the connectors at the front of the left side of the instrument. If you have an older instrument there may be only one connection, see step 10.

10. If you have an older instrument with only one cable connection in step 9, disconnect the one, then pull the front panel just far enough to gain access to the cable connector on the CRT Control board (left side of front panel) and disconnect the cable. Open the cable clamp that holds this cable and remove the cable.

11. Disconnect the large ribbon cable from the Control Keyboard and separate the front panel from the instrument.

NOTE

At the front of the attenuators is a plastic bushing containing the Probe ID sensing ring. Note the orientation of this bushing and ring. The tabs of the bushing should be horizontal and fit into the recess on the front of the attenuator. Be sure the bushings for all attenuators are properly aligned before replacing the front panel.

GLASS FILTER REMOVAL

The glass filter is designed to limit EMI as well as reflected light. It is secured by a metal retainer which has a screw at each corner. In early instruments the glass filter is fastened to the bezel with conductive glue. In later instruments, four sections of metal fingers contact the perimeter of the glass for electrical conduction.

When replacing a glass filter that has been glued to the bezel, contact an HP Service Center

The foam dust barrier is not part of the metal retainer and may be destroyed when the retainer is removed.

DISPLAY CONTROL REMOVAL

Remove two screws attaching the Display Control assembly.

CONTROL KEYBOARD REMOVAL

1. Disconnect the RPG cable at the Control Keyboard and if necessary the cables from the Function and Menu Keyboards.

   The Function Keyboard (side of display) cable goes to the top connector and the Menu Keyboard (bottom of display) cable goes to the bottom connector on the Control Keyboard.

2. Remove five screws and remove keyboard.

3. Pass RPG cable through hole in Control Keyboard.

MENU KEYBOARD REMOVAL

To remove the Menu Keyboard (along the side of the display) remove two screws attaching the Keyboard and disconnect the cable at the Control Keyboard.

FUNCTION KEYBOARD REMOVAL

1. The screws for the Function Keyboard (across the bottom of the display) cannot be reached with the front panel in the frame. To remove the front panel, remove the remaining screws around the outside of the front frame casting. There are two at each side, three across the top, and three across the bottom.

2. Remove the front panel from the front frame. There is a section of RFI braid along the left side and bottom (as viewed from the back) between the panel and the frame. Be sure to reinstall it during reassembly or EMI specifications may be compromised.

3. The screws to the Function Keyboard can now be reached and removed.

4. Remove the rubber bumper below the keyboard.

5. Remove the keyboard and disconnect the cable at the Control Keyboard.

ASSEMBLY REPLACEMENT

1. Replace minor assemblies, keyboards, CRT Control board, etc. in reverse of their removal procedures.

2. Check that all front panel cabling is dressed properly. Dress the small ribbon cables so they will clear the channel 1 Attenuator assembly and insert them into the clamp.

3. Set the instrument vertical, so that it rests on the fan housing with the front up.

4. Check that each sense ring around an Attenuator assembly BNC is aligned with the recess in the front of the assembly.

5. Set the front panel lightly in place over the Color CRT Module and Attenuator assemblies.

   Check the CAL cable and wide ribbon cable so they are not caught in the hardware and can be dressed later.

   Check that corner struts are outside the front frame.

   Allow the BNC connectors and sense rings to center in the holes in the front panel.

   The front panel assembly should fit into place without forcing. If not check for pinched cables and other obstructions. It may however, be held up slightly by the foam dust shield between the CRT and bezel.

6. Fasten the struts to all four corners of the front frame using two screws on each corner. Be sure to use the same screws removed.

7. Set instrument down in its normal operating position.

8. Fasten the Color CRT Module top bracket and the card cage brace using three screws through the top of the frame (see figure 6A-3).

   If the Color CRT Module does not align well, temporarily loosen the screws securing the module at the rear bracket, install the screws at the top front bracket, and retighted the screws at the rear bracket.

9. Turn instrument onto its left side and fasten the Color CRT Module bottom bracket and the main deck using four screws through the bottom of the frame (see figure 6A-3).

10. Set the instrument in the normal operating position.

11. Loosen the screw at the back of each Attenuator assembly.

12. Use eight screws to fasten the front of the Attenuator assemblies to the front panel.

13. Tighten the screw at the rear of each Attenuator assembly.

14. Pass the wide ribbon cable through an opening in the front of the card cage and connect to the front connector of the Input/output assembly.

15. Pass the front panel CAL cable through an opening in the front of the card cage and connect to the front connector of the Timebase/trigger assembly.

6A-9. Attenuator Assemblies

CAUTION

Protect against static discharge while working with attenuators. Input FET of preamplifier is sensitive to static discharge.

REMOVAL

1. Remove covers and front panel (refer to front panel removal procedure). Set instrument in its normal operating position.

2. Remove the screw at the rear of the attenuator assembly to be removed. This screw is not captive. Don't let it fall into the interior of the instrument because it will be hard to retrieve.

3. Remove the connector for the three-wire cable that connects to the front of the attenuator assembly. The connection is made at the front edge of one of the card cage boards.

3. Remove the three connectors from the attenuator solenoids.

4. Remove the cable connectors at the back of the Attenuator assembly. Note the orientation of these connectors.

5. Remove the three coaxial cables. Of the two trigger cables, remove the rear one first. The HP 54100 Family Support Kit provides a 6 mm open-end wrench for removing these cables. The Attenuator assembly should now be free of the instrument.

REPLACEMENT

1. Use the following table while connecting the coaxial cables to an attenuator.

NOTE

The two cables on the side are the trigger connections. The cable at the rear is the vertical signal connection. The trigger cables have a colored marker at each end. Connect the cables to the attenuator using the following chart.

ATTENUATOR	FRONT CONNECTOR	REAR CONNECTOR
CHAN 1	Brown	Red
CHAN 2	Orange	Yellow
CHAN 3	Green	Blue
CHAN 4	Violet	White

In the event that the cables were inadvertently removed at the Trigger/timebase assembly, they should be re-installed in order of color, front to back, following the standard color code. You can also use the diagram on the cover of the instrument or at the back of this section.

CAUTION

To avoid damage to the ceramic substrate of the preamplifier, push connectors onto the Attenuator Assembly gently.

2. Connect the rear ribbon cables to the Attenuator assembly. The connectors are keyed.

3. Carefully connect the cables to the solenoids. The connectors are keyed but the keying can be defeated by excessive force. Use the cabling diagram on the inside of the instrument top cover or the figure at the end of this section.

4. Connect the three-wire cable to the front of the appropriate card cage assembly. Use the cabling diagram for reference. Route the cable along the right side of the Attenuator assembly.

5. Insert the rear mounting screw into the hole at the rear of the Attenuator assembly. Slide the Attenuator assembly into place and rest the mounting screw on the standoff. Temporarily tighten the screw.

6. Recheck the routing of all cables, especially the three-wire cable. It can become pinched when the front panel is installed.

7. Check the alignment of the probe sensing ring on the BNC connector of all attenuator assemblies. It should fit into the recess at the front of the attenuator.

8. Install the front panel per the front panel procedures and reassemble the rest of the instrument. Use the appropriate procedures in this section.

6A-10. Color CRT Module

The Color CRT Module is replaceable only as a complete unit.

REMOVAL

1. Remove covers and front panel (refer to the appropriate procedures).
2. Disconnect the wide ribbon cable from the Color Display Assembly and remove cable from clip.
3. At rear of module, remove two screws attaching module mounting bracket to the mounting bracket on the mainframe. Each screw uses a metal washer and a rubber washer.
4. Slowly pull module forward until the power cable (small three-wire) can be disconnected at the Primary Power Supply board.
5. Continue pulling module forward until it clears the instrument.

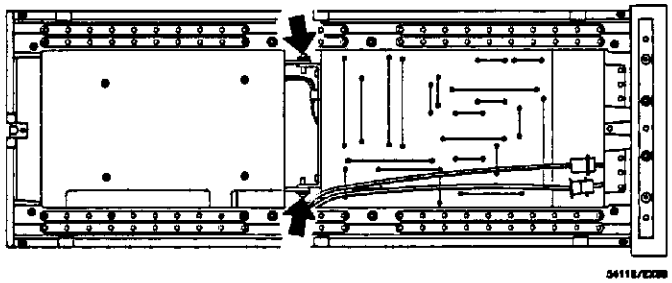


Figure 6A-4. Color CRT Module, Rear Mounting Screws

REPLACEMENT

It is necessary to remove several items from the inoperative Color CRT Module and install them on the new one. Use the following procedures to do that and install the new module.

TRANSFER PARTS TO NEW MODULE

1. Remove the eight small screws that hold the shield to the top and side of the inoperative module.

CAUTION

These screws are special self-tapping screws, different from others the same size. Do not use them anywhere else in the instrument.

It is best if you throw the old screws away and use new ones when installing a new module. Used ones may not be good enough to tap the holes in the new module.

2. Use an 8 mm wrench to remove the four nuts on the front of the inoperative module and remove the shield.

3. Remove the front mounting brackets and put the 8 mm nuts back on the module.

4. Remove the large nuts from the new module, do not remove any other hardware, and install the front mounting brackets.

5. Install the shield on the new module. Place it over the two front mounting screws and front mounting brackets.

6. Install the four large nuts but leave them loose so the shield can move.

7. Use the special self-tapping screws (step 1) to fasten the top and side of the shield. They will be hard to start while they are tapping the holes.

CAUTION

Be careful that excessive tightening does not strip the self-tapped holes. It is best to use new screws. If you use screws from the old module they may be ruined while trying to tap the holes on the new module.

8. Tighten the large nuts at the front of the module.

9. Remove the two screws that hold the rear bracket to the inoperative module.

   THESE SCREWS ARE SPECIAL self-tapping screws that must be used for mounting the bracket assembly on the new module. Do not use them for any other purpose.

10. Mount the rear bracket to the new module. The screws will be hard to start because they must self-tap the mounting holes. Be careful that excessive tightening does not strip the self-tapped holes.

11. Note the routing of the power cable and CRT Control cable and one at a time, remove them and install them on the new module.

12. Remove the wide ribbon cable from the old module and install it on the new one.

INSTALL NEW MODULE

13. Install the new module most of the way into the instrument. Avoid pinching cables as module is being installed.

14. Connect the power cable to the appropriate connector at the top front corner of the Primary Power Supply and slide module the rest of the way in.

15. Install the two rear mounting screws (see figure 6A-4). These may be loosened later to align the module while installing the front panel.

16. Install the front panel using the installation procedure in the front panel procedures.

6A-11. Fans

REMOVAL

1. Remove the Primary Power Supply following the procedure in this section.
2. Remove remaining six 4 mm screws that fasten the rear panel to the rear frame. (Two were removed when the Primary Power Supply was removed.)
3. Disconnect fan power cables from rear corner of Mother board.
4. Disconnect HP-IB cable at the Input/Output assembly.
5. Disconnect three coaxial cables at the rear of the Timebase/trigger assembly.
6. While noting cable routing, carefully remove rear panel from instrument.

CAUTION

The fan on the instrument's right side (card cage side) has an air deflector mounted to it. Note the orientation of the deflector in the instrument and the orientation to the fan. The opening in the side of the deflector should be toward the bottom of the instrument when the rear panel is installed.

7. If replacing the right-side fan, remove the air deflector.

NOTE

Before removing fan, note the orientation of the fan in the housing. The side of each fan where the cable exits is toward the center of the housing.

8. Remove the four screws holding the defective fan in the rear panel.

REPLACEMENT

TRANSFER PARTS TO NEW FAN

The screws securing the fans in the housing and the air deflector to the right-side fan are held by nuts pressed into the mounting holes from the back side of the flanges. Remove these press-in nuts and use a plier to press them into the mounting holes of the new fan. The right-side fan uses eight nuts and the other fan four.

INSTALL FAN AND DEFLECTOR

Reverse removal procedure to install fan. If only one fan is removed, the fan spacer and screens should stay in place. If both fans were removed and parts have shifted, the screens go into the housing first, then the fan spacer, then the fans. Check the orientation of fans and air deflector during installation.

6A-12. Color Display Assembly

REMOVAL

1. Disconnect power cable.
2. Remove bottom rear feet and bottom cover.
3. Disconnect wide ribbon cable from Color Display assembly.
4. Remove assembly mounting screws as shown in the figure below.
5. Carefully lift board straight up to disengage Mother board connector.

NOTE

The connector between the Display assembly and Mother board exhibits resistance while the board is being removed. The major lifting force should be exerted along the edge of the Color Display assembly at the connector.

REPLACEMENT

Reverse removal procedure to install assembly. Use additional care when inserting the connector pins into connector on Mother board.

NOTE

Color Display assembly power comes from the Mother board via the four short mounting screws marked +5 or GD on the board. Install and tighten these screws before expecting proper operation of the instrument.

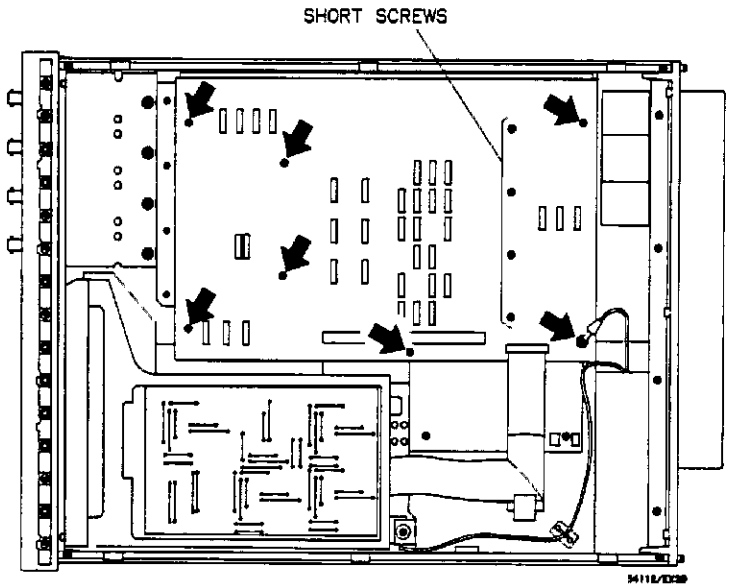


Figure 6A-5. Color Display Assembly Mounting Screws.

6A-13. Mother Board

REMOVAL

1. Disconnect power cable.
2. Remove covers (refer to appropriate paragraph).
3. Remove all card cage PC boards (refer to appropriate paragraph).
4. Remove Power Supplies (refer to appropriate paragraph).
5. Remove Color Display Assembly (refer to appropriate paragraph).
6. Disconnect fan power cables at corner of Mother board.
7. Remove the remaining mounting screws and remove board (see figure below).

REPLACEMENT

Reverse removal procedure to install board.

NOTE

The Mother board and Color Display assembly share some of the same mounting screws. When installing the Mother board install only the screws removed in step 7 above (see figure below).

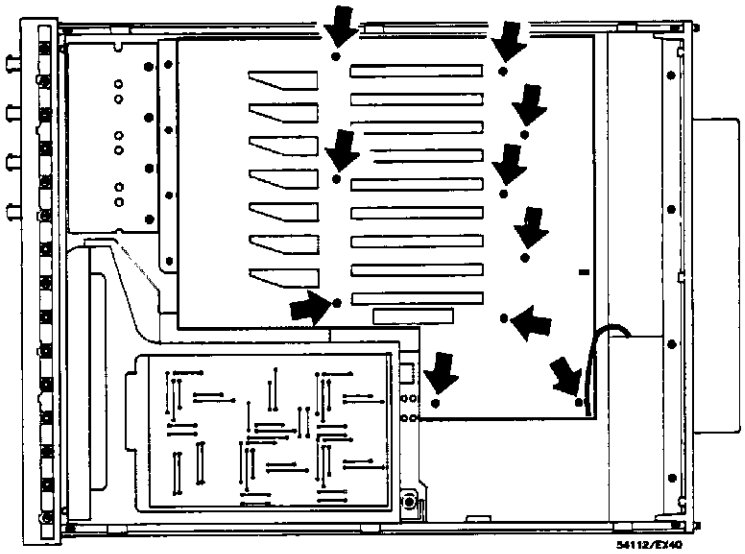


Figure 6A-6. Mother Board Mounting Screws.

6A-14. CABLING DIAGRAM

The following cabling diagram should be used when removing and replacing boards and assemblies.

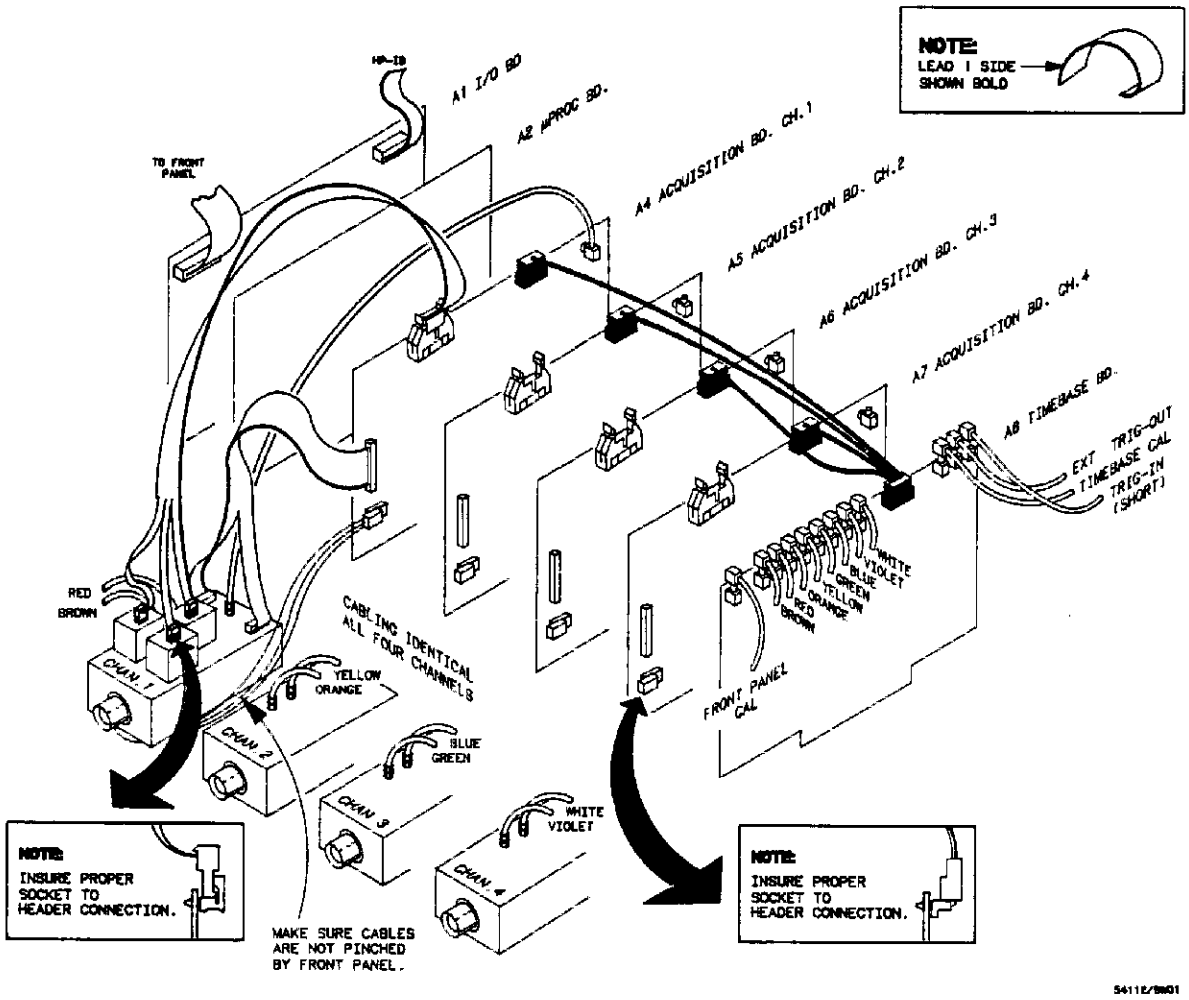


Figure 6A-7. Cabling Diagram.

SECTION 6B
THEORY OF OPERATION

6B-1. INTRODUCTION

The HP 54112D is a digitizing oscilloscope with up to 400 MS/s sampling rate and 100 MHz bandwidth. It has four input channels, which are simultaneously digitized and provide internal trigger. There is an additional external trigger input.

There are two sections of theory. The instrument theory, consisting of Acquisition System and Mainframe, covers a general view of the instrument from a major assembly perspective. The functional theory, Acquisition Theory and Timebase/trigger Theory, covers general operation of Attenuator Functions, Acquisition Functions, Trigger Functions, and Timebase Functions.

Following the theory is a brief description of the operating cycle during a real-time acquisition.

6B-2. INSTRUMENT THEORY

The mainframe consists of Power Supplies, Color CRT Module, and Display assembly. The Microprocessor and Input/Output assemblies, which for instrument theory are part of the mainframe, are located in the card cage. The card cage also holds the acquisition system (except Attenuator assemblies).

The acquisition system consists of four Attenuator assemblies, four Acquisition assemblies, and the Timebase/trigger assembly. The Attenuator assemblies are located between the card cage and the front panel.

Refer to the adjacent block diagrams for the following discussion.

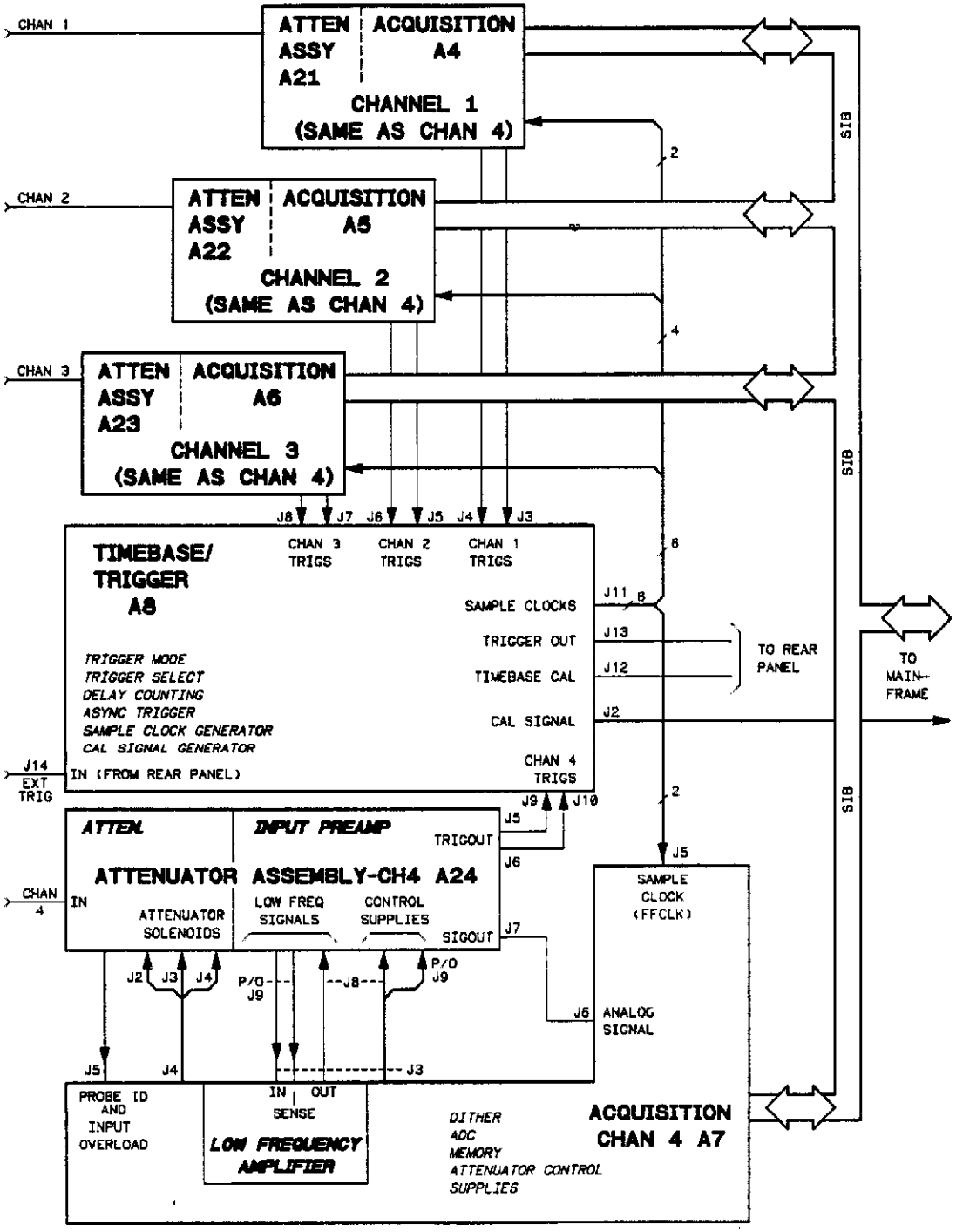


Figure 6B-1. Instrument Block Diagram, Acquisition System

6B-3. Acquisition System

All four acquisition channels are identical.

ATTENUATORS. Attenuator assemblies provide signal conditioning between the front panel channel input and the Acquisition assembly. At full scale, the outputs are a ±0.64 V single-ended signal, representative of the input signal, and two complementary trigger signals whose edges represent the desired trigger point for the channel. The Acquisition assembly provides power supplies, control signals, and the low frequency amplifier, and it receives the probe ID and input overload signals in addition to the channel signal. The trigger signals go to the Timebase/trigger assembly.

ACQUISITION. The Acquisition assembly digitizes and stores the channel input signals. It receives sample clocks from the Timebase/trigger assembly. The output from memory is read onto the system interface bus (SIB). The Acquisition assembly also provides the low frequency amplifier, supplies, and control for the Attenuator assembly.

TIMEBASE/TRIGGER. The Timebase/trigger sets up the trigger modes and generates the sample clocks for the Acquisition assembly.

The channel and external trigger signals are processed and provide the acquisition trigger to the timebase. A 400 MHz oscillator,part of the timebase, provides the base sample rate. Frequency dividers provide sample rates down to 50 Hz.

The acquisition trigger is provided at the rear-panel Trigger Out BNC.

The Timebase/trigger provides a vertical calibration signal to the CAL connector on the front panel.

The Timebase/trigger provides either of two signals to the rear panel Timebase Cal BNC. When the instrument is running in the acquisition modes, the signal is approximately 32 KHz and asynchronous with other signals. In a test mode (Extended Test 21) it is 10 MHz and derived from acquisition clock.

6B-4. Mainframe

MICROPROCESSOR. The Microprocessor uses a 68000 16-bit processor to handle all processing on the system interface bus (SIB). The assembly includes 512K bytes of ROM and 32K bytes of non-volitile CMOS RAM. Bus buffers, interrupt logic, and a time-out counter are part of the Microprocessor assembly.

INPUT/OUTPUT. The Input/Output (I/O) assembly combines several functions on one PC board. The dynamic RAM on this assembly is used for basic operation of the instrument and to store waveforms.

The keyboard control provides scanning and reading of the three keyboards and RPG (rotary pulse generator).

The HP-IB interface couples the SIB to the HP-IB port on the rear panel.

An oscillator and divider circuit provides 16, 8, 4, and 2 MHz clocks for the system. The battery back-up provides power to non-volitile RAM on the microprocessor assembly.

The Power Test circuitry monitors the supplies on the SIB. The output of the circuit is a status bit that the microprocessor can read. If all supplies are greater than 50% it will register as passing.

The Power-On Reset provides a glitch-free reset pulse to the SIB for use by any circuitry on the bus.

FRONT PANEL ASSEMBLIES. Front panel assemblies include three keyboards, an RPG (rotary pulse generator), and the Display Control. The Control Keyboard allows direct entry of values into the field selected on the CRT. The Function and Menu keyboards, to the right of and below the CRT respectively, give control of functions noted on the display. The RPG provides the digital equivalent of a potentiometer for functions such as OFFSET or TRIGGER LEVEL as well as sequential stepping through functions such as V/div and Sweep Speed. The Display Control provides analog brightness and background control of the display.

COLOR DISPLAY ASSEMBLY. The Color Display Assembly provides interface between the SIB and the Color CRT Module. It includes graphics RAM, character generation, and RGB generation. Horizontal and vertical sync also drive the Color CRT Module.

COLOR CRT MODULE. The Color CRT Module includes the color CRT and its associated driving circuitry. It uses H and V sync and red, green, and blue video from the Color Display assembly. It gets 120V dc power from a switching supply on the Primary Power Supply.

6B-5. Power Supplies

PRIMARY SUPPLY. The Primary supply provides an unregulated 300Vdc primary voltage to the switching supplies. It can be set for 115 or 230 V line input (-25%, +15%). A circuit breaker provides rear panel switching of the line input. The STBY (standby) switch on the front panel controls a 120 Vdc switching regulator which supplies the Color CRT Module as well as an on/off control voltage to the Analog and Digital supplies.

DIGITAL SUPPLY. The Digital Supply switching regulator provides +5 V and -5.2 V to most of the digital circuitry. It uses 300 Vdc from the Primary Supply and is controlled (on/off) by an output from the 120 V Supply. These supplies are designated +5 and -5 on the SIB and are referenced to DGND of the SIB.

ANALOG SUPPLY. The Analog Supply switching regulator provides ±8.5 Vdc and ±18.5 Vdc to much of the analog circuitry. It uses 300 Vdc from the Primary Supply and is controlled (on/off) by an output from the 120 V Supply. Many assemblies in the instrument use local regulation of these supplies to provide decoupling from system noise. These supplies are designated ±8 and ±18 on the SIB and are referenced to AGND of the SIB.

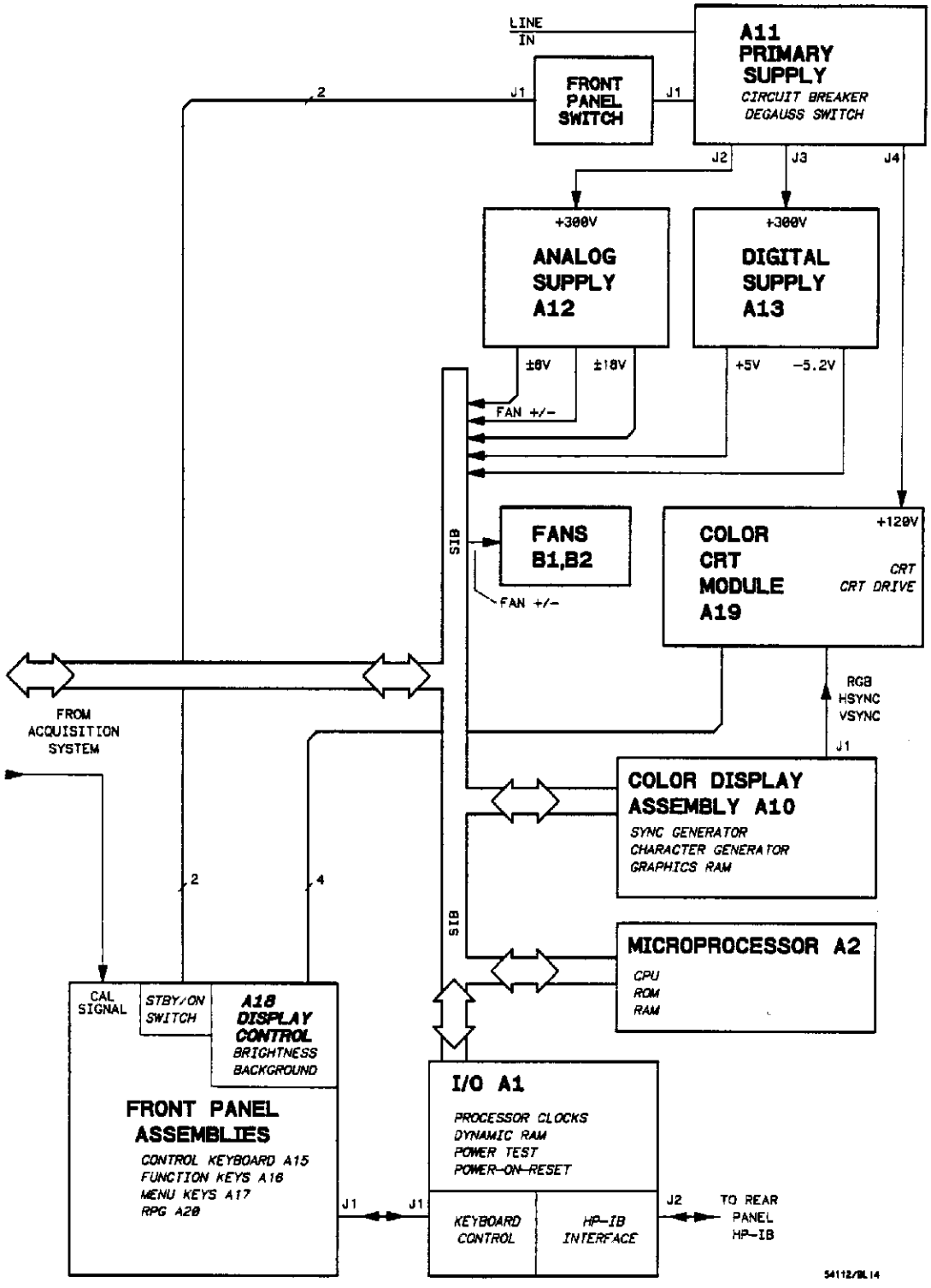


Figure 6B-2. Instrument Block Diagram, Mainframe

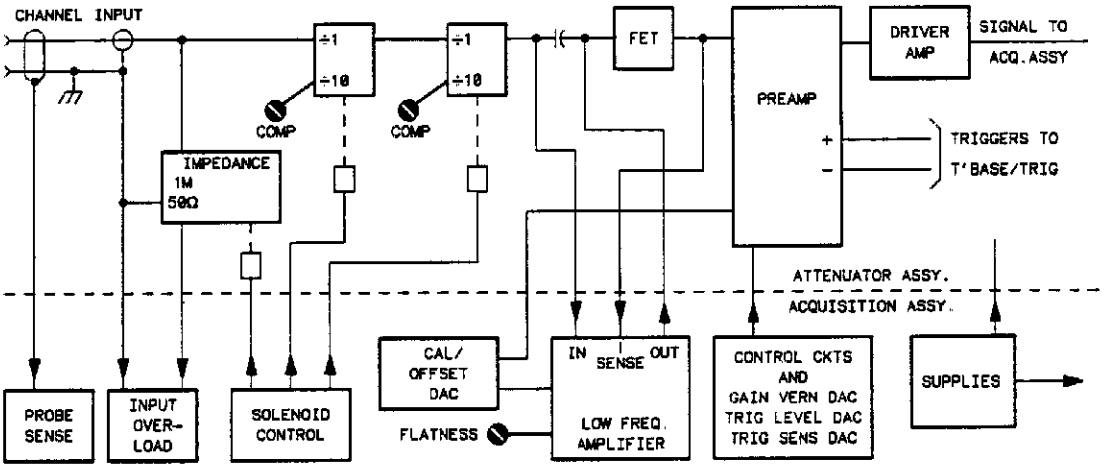


Figure 6B-3. Attenuator and Preamp Functions Block Diagram

6B-6. ACQUISITION THEORY

6B-7. Attenuator Functions

The Attenuator assembly consists of two main sections, the attenuator and the preamplifier. It gets power and control from the Acquisition assembly for its respective channel.

INPUT ATTENUATOR. The input attenuator section provides 50Ω or 1MΩ impedance switching and two ÷10 sections which can be cascaded for ÷100. Magnetically latching solenoids control the switching. A ring on the input BNC connector provides means for identifying properly equipped high impedance 10:1 voltage divider probes. A sample of the input signal from a tap on the 50Ω input termination is used to control an overload protection circuit. The microprocessor will remove the 50Ω termination under certain overload conditions.

PREAMPLIFIER. The preamplifier hybrid consists of several sections, a high-pass filter and FET and associated circuitry, the main preamplifier with trigger circuitry, and the driver amplifier.

At the input to the preamp, the low frequency component of the input signal is sent to the low frequency amplifier on the Acquisition assembly. AC/DC coupling and offset are incorporated in the low frequency amplifier.

Upon return to the attenuator assembly, the low frequency and high frequency signals are summed at the input FET of the preamplifier. The preamplifier incorporates the gain changing and the trigger conditioning. Three incremental gain ranges, ÷1, ÷2, and ÷4 affect the signal before trigger pick-off. Vernier gain affects the signal after trigger pick-off.

The output of the preamplifier is fed to the driver and the output of the driver is fed by a coaxial cable to the Acquisition assembly and analog-to-digital converter hybrid.

The trigger signals are complementary, with edges representing the selected trigger point on the input signal. Two coaxial cables conduct them to the Timebase/trigger assembly.

6B-8. Acquisition Functions

The Acquisition assembly samples one channel input signal and stores it in memory. It also provides interface to the system interface bus (SIB) and attenuator supplies and control.

LOW-PASS FILTER. The input signal is the output of the Attenuator assembly. A low-pass passive filter, with a 3 dB rolloff of about 115 MHz, attenuates signals above 200 MHz to eliminate aliasing by the analog-to-digital convertor (ADC).

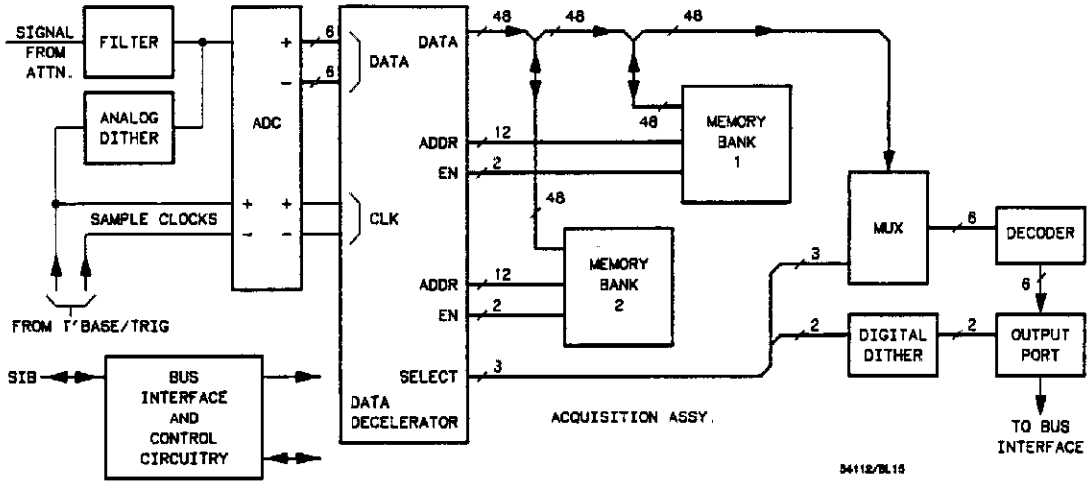


Figure 6B-4. Waveform Sampling and Storage Block Diagram

ANALOG DITHER. Analog dither, part of the dithering circuitry, acts directly on the analog signal. Two flip-flops form a divide-by-four counter clocked by the sample clock. They repeatedly subtract the equivalent of 1/4, 1/2, 3/4, or 0 LSB (least significant bit) from the signal for four successive samples. Together with digital dithering, when several dithered acquisitions are averaged the result is improved resolution over a single undithered acquisition.

SAMPLE CLOCKS. The complementary sample clocks (FFCLK+/-) come from the Timebase/trigger assembly.

ADC. The ADC hybrid is a six bit silicon flash converter. The rising edge of the sample clock samples the input signal and the falling edge clocks a counter that provides the clock signal for the data decelerator. The six-bit data is in grey-code.

DATA DECELERATOR. The data decelerator slows data from six-bit samples at a 400 MHz (max) sample rate, to a pair of 48-bit words at one sixteenth the sample rate. Eight six-bit data samples are accumulated in the decelerator. While the eight samples, one 48-bit word, are being stored in one memory bank eight more samples are being accumulated to store in the other memory bank.

The decelerator provides separate addresses and enables for the memory banks. Data lines are common. The decelerator also addresses memory for reading data onto the SIB (system interface bus) for processing. When instructed by the microprocessor through the data bus, it also provides data patterns for testing the memory banks.

MEMORY BANKS. The memory consists of of twenty-four 4K x 4 static RAMs organized in two banks of 4K x 48. It can store a total of 64K six-bit samples. The decelerator writes to alternate memory banks because the 48 bit word is updated faster than it can be stored.

MULTIPLEXER. Waveform data is read from memory into the multiplexer which, now at a rate compatible with the microprocessor, feeds data through a grey-to-binary converter and port onto the SIB. The 48-bit data word is demultiplexed by the select lines, actually the three LSBs of the address counters.

DIGITAL DITHER. Digital dither works in synchronism with analog dither. It appends two lesser bits to the six bits representing the signal sample. These two bits, an addition, are proportional to the subtraction of the analog dither. As was stated before, several dithered and averaged acquisitions result in improved resolution.

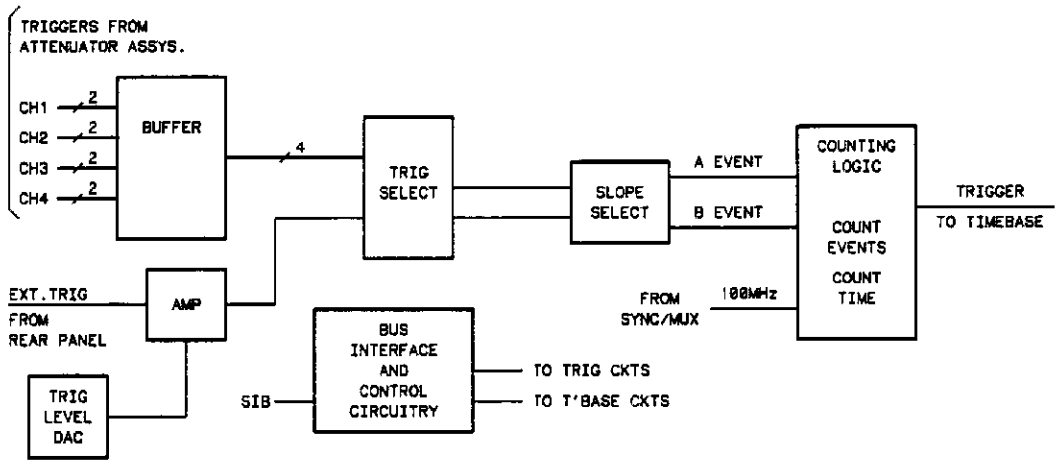


Figure 6B-5. Triggering Block Diagram

6B-9. TIMEBASE/TRIGGER THEORY

The Timebase/trigger assembly provides trigger logic, sample clocks, external trigger amplifier, front panel CAL, and rear panel timebase cal and trigger output.

6B-10. Triggering Functions

CHANNEL TRIGGERS. Channel triggers are converted from complementary to single-ended signals in buffer circuitry.

EXTERNAL TRIGGER. The external trigger amplifier conditions the signal from the rear panel. The 200 KΩ input impedance at the rear panel BNC is fixed. A front panel menu selection can limit the frequency response to approximately 4 KHz. Trigger level and slope are selected in this circuitry.

TRIGGER SELECT. Trigger select circuitry provides two trigger events, either of which can be a combination of the channel or external triggers. Trigger combinations are set up by the requirements of the front panel trigger mode selections: edges, patterns, or a combination thereof.

SLOPE SELECT. The polarity of the two trigger events can be changed to accomodate the further requirements of front panel trigger modes.

COUNTING LOGIC. The two trigger events are fed into the counting logic. The counting logic can count one of the events to qualify the other or use the 100 MHz input as a time reference to qualify one event after the other.

BUS INTERFACE AND CONTROL. The bus interface provides level shifting, gating, and other functions necessary to couple trigger and timebase circuitry to the system interface bus (SIB).

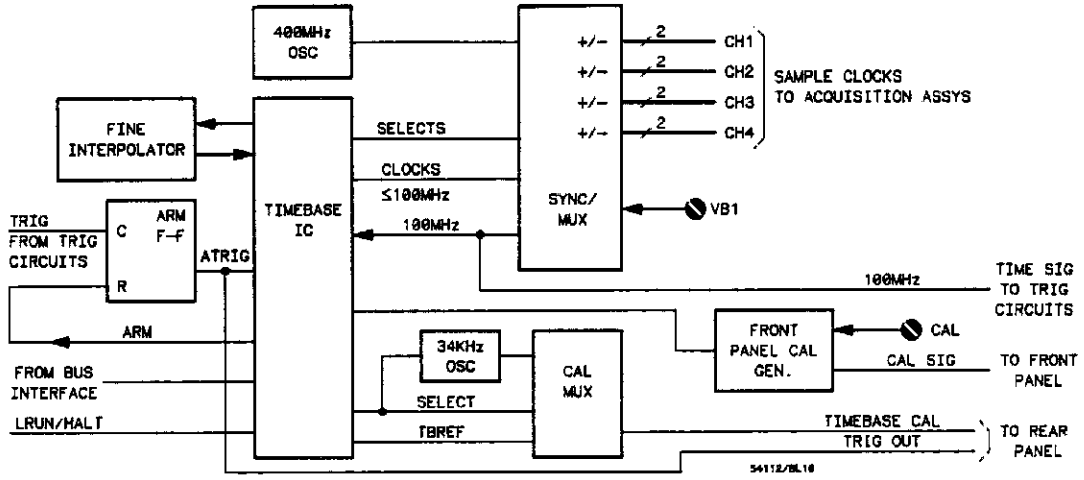


Figure 6B-6. Timebase Block Diagram

6B-11. Timebase Functions

Timebase circuitry develops the acquisition sample clock in reference to the trigger. It also does the trigger interpolation and several other functions.

400 MHZ OSCILLATOR. The 400 MHZ oscillator is a packaged circuit that generates the basic acquisition sample clock.

MUX/SYNCHRO. The multiplexer/synchronizer IC provides the high frequency division ratios for the acquisition sample clock. It develops the 400, 200, and 100 MHz sample rates. A 100 MHz output goes to the timebase IC for further division. It provides fan-out of the sample clocks to the four Acquisition assemblies.

TIMEBASE IC. The timebase IC is a multifunction IC. It provides the majority of the sample clock rates, from 100 MHz down to 50 Hz. It divides the 100 MHz output of the multiplexer/synchronizer IC in a 1, 2, 4, 10 sequence. It feeds the divided rate back into the mux/synchro for output to the Acquisition assemblies. It also provides counters and gating for coarse and fine interpolators and the pre- and post-trigger counting.

ARM FLIP-FLOP. The arm flip-flop receives qualified triggers from the triggering circuitry. Once the flip-flop has been reset by the ARM signal from the timebase IC, the next valid trigger will clock the flip-flop and assert the ATRIG line. ATRIG is also an output to the rear panel as the trigger out signal.

FINE INTERPOLATOR. During sampling, acquired data must be correlated to the trigger point. Each acquisition cycle has a different relationship to the trigger. Correlation is done by the trigger interpolator. It makes a high precision time interval measurement which is used to position the acquired data. The coarse interpolator is part of the timebase IC. The fine interpolator uses a dual slope technique to increase the accuracy of the time interval measurement. It is gated by the timebase IC and its output controls a counter in the timebase IC.

FRONT PANEL CAL GENERATOR. This 2 KHz oscillator provides a square-wave signal to the front panel CAL output. It can be latched by using a cal menu so that it can be measured and/or adjusted.

6B-12. OPERATING CYCLE

The following discussion gives a general description of a real time acquisition cycle. Numbers given are only general and vary in actual operation. The memory size is a 64K sample loop for all acquisitions; the record length can be less, and is 8K samples for this discussion. The size of the display is 501 points. Use the drawings on the right for the following description. The "T" represents the trigger point.

6B-13. General Description

The instrument fills the entire record length during each acquisition. Where the Delay Reference is set — Center, Right, or Left — determines several things. It sets the trigger point reference for the display, at the center or the right or left edges of the graticule respectively. It also positions the trigger point within the acquisition record. It therefore influences the minimum number of samples that must be taken before the trigger. For example, with the Delay Reference at center at least half the record, 4K samples, must be taken before trigger. The pre-trigger counter is set to 4K and the post-trigger counter is set to the remainder, 4K.

With the Delay Reference on the right, nearly the entire 8K record is pre-trigger. The pre-trigger counter counts almost 8K samples. Enough post-trigger samples are taken to view the trigger time and a short period thereafter.

With the Delay Reference at left, very few samples must be taken before the trigger; enough to allow seeing a short time before the trigger. The balance, for the post-trigger counter, is nearly the full record, 8K samples.

Though the pre-trigger count is set so that enough of the record fills with signal data before the trigger is armed, the post trigger count is what really determines what part of the acquired signal comprises the record. The period between trigger arming and the trigger is not known, so the acquisition will continue and could fill the entire 64K memory more than once before a trigger.

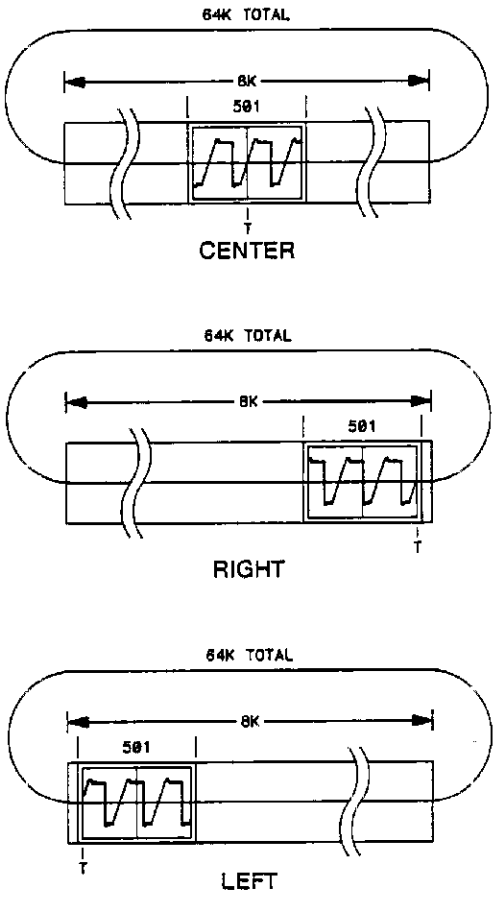


Figure 6B-7. Acquisition Cycle Diagrams

Once trigger occurs the post-trigger counter will start. When the post-trigger counter stops, the microprocessor will calculate how far back in the memory loop an 8K record would start and that is the beginning of the actual record. The rest of the memory is skipped by counting through it at high speed to the beginning of the record.

The reason for a choice between 64K or 8K record length is processing time and therefore update time. Display update is much faster with the 8K record because the system needs to process one eighth the amount of data.

6B-14. In Brief

Use the figure at right in conjunction with those on the previous page for the following description, in brief, of the real-time operating cycle.

1. Microprocessor loads pre-and post-trigger counters.

2. Microprocessor asserts low LRUN/HALT to timebase IC and pre-trigger acquisition begins.

3. Pre-trigger count ends and timebase IC enables triggering by resetting Arm F-F with ARM signal.

4. Next qualified trigger clocks Arm F-F and the result, ATRIG (asynchronous trigger), initiates trigger interpolators and post- trigger counter.

5. At the third sample clock after ATRIG, STRIG (synchronous trigger) marks the sample the trigger interpolators measure to.

6. Post-trigger count ends.

7. The microprocessor, through the timebase IC, provides the correct number of clocks at 100 MHz to move the memory address to the beginning of the record. Meanwhile, it also reads the trigger interpolators.

8. Clock rate is lowered and memory is read onto the SIB.

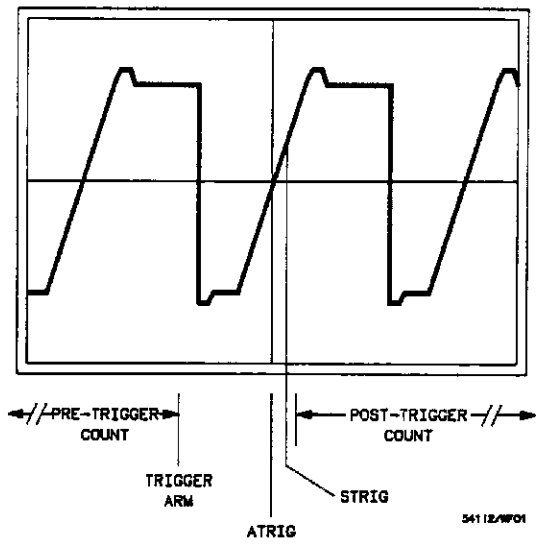


Figure 6B-8. Operating Cycle Trigger Diagram

SECTION 6C
SERVICE MENUS/KEYS

6C-1. INTRODUCTION

This section describes the service menus and keys that are available for calibration, troubleshooting and CRT display alignment. A basic understanding of these will be helpful in troubleshooting failures, however, Self-Test and Troubleshooting is covered specifically in Section 6D.

6C-2. SERVICE MENUS

The service menus are part of the Utility menu, in the second level of the menu softkeys. Once Utility is pressed, six function keys will be displayed: Probe Menu, HP-IB Menu, Cal Menu, Test Menu, Color Menu, and CRT Setup Menu.

PROBE MENU. The Probe Menu is used to set the attenuation factor before the input of the instrument. This sets the instrument scaling factors for a special probe or other device. This is not a service menu though the functions may be used during service procedures. Further use of this menu is covered in the Operating and Programming and other user manuals.

HPIB MENU. The HPIB Menu provides keys that are used to set the HPIB attributes. These attributes are address number, Talk/Listen, and EOI. This menu is discussed in detail in the Operating and Programming and other user manuals.

CAL MENU. The Cal Menu is used to calibrate the instrument. The calibration factors are stored in non-volitle memory. Use of this menu is covered in the *HP 54112D Operating and Programming Manual*. Basic functions of the Cal menus are covered in this section.

TEST MENU. The Test Menu provides several functions used to set up and run internal diagnostics test and view the results. Use of these functions is covered briefly in following paragraphs and comprehensively in the Self-Tests/Troubleshooting, section 6D.

COLOR MENU. The Color Menu provides functions used to set the characteristics of the colors displayed. These characteristics include hue, saturation, and luminosity. This menu is covered in detail in the Operating and Programming and other user manuals.

CRT SETUP MENU. The CRT Setup Menu provides several functions that provide confidence testing as well as test patterns for adjusting the Color CRT Module. These functions are discussed in following paragraphs.

6C-3. ONE-KEY POWER UP

A one-key power up is often performed to return the instrument setup to default conditions. This is done as follows:

1. Set the front panel POWER switch to STBY,
2. Press and hold one front panel key,
3. Turn front panel POWER switch to ON.
4. Release key when display shows "Powerup Self Test Passed!" or Failed.

6C-4. TWO-KEY POWER UP

CAUTION

Using the two-key power up will leave the instrument uncalibrated. Effort needed for recalibration should be considered before using this mode to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.

A two-key power up is a basic reset of the entire operating system of the HP 54112D. All volatile and non-volatile RAM is cleared. As a

result, all calibration factors are purged and the instrument must be recalibrated.

All calibration except Offset Cal can be done with just the front panel CAL signal or the rear panel Timebase Cal signal and the software cal menus. Offset Cal requires a 10 Vdc power supply. The two-key power up is performed in much the same way as the one-key power up.

1. Set the front panel POWER switch to STBY.
2. Press and hold the top and bottom keys in the group at the right edge of the display.
3. Turn front panel POWER switch to ON.
4. Release keys when display shows "Powerup Self Test Passed!" or Failed.

6C-5. CAL MENU

When the Cal Menu key is pressed the following calibration keys are displayed.

6C-6. Vertical Cal

Vertical Cal sets software gain coefficients for vernier control of various gain settings. Cal is run by pressing the appropriate menu and function keys. No front panel inputs are needed. All front panel inputs and rear panel trigger input should be removed to avoid extraneous noise. An internal signal is supplied to the attenuator preamplifier from the Acquisition assembly. This cal sets gain from the attenuator assembly preamp through the ADC hybrid.

6C-7. Probe Tip Cal

The Probe Tip Cal uses a triggering technique to measure where the CAL signal from the front panel triggers the system. The front panel CAL signal is calibrated independently from the operating system. The software stores the cal factors and uses them to manipulate acquired data.

The vertical specifications of the HP 54112D are based on calibration of the vertical system through the probe. Changing the probe at an input nullifies the calibration of that channel or trigger. Restoring calibration at that input requires a Probe Tip Cal of that input.

Use of Probe Tip Cal in service procedures is accompanied by instructions appropriate to the procedure. Other information about Probe Tip Cal can be found in the Utility Menu chapter of the *HP 54112D Operating and Programming Manual*.

6C-8. Offset Cal

The Offset Cal sets the offset coefficients at various vertical sensitivities. An external +10 Vdc source is required for this cal. The accuracy of the source must be ±0.1% or the accuracy of the instrument will be compromised and the instrument may not pass the performance tests. See the Adjustments section of this service manual or the appropriate chapter of the operators manuals for the Offset Cal procedure.

6C-9. Trigger Cal

Trigger Cal is a trigger level and sensitivity calibration. There are no input signals used for this calibration and the user needs only to follow the prompts on the screen to remove any signals before the routine is run.

The software sets the trigger level and hysteresis (sensitivity).

6C-10. Timebase Cal

Channel Skew, in the Timebase Cal menu, compensates for time differences between the channel displays and triggers. A signal from the rear panel is applied to the CHAN 1 input and another input, CHAN 2, CHAN 3, CHAN 4, and the external trigger in turn. A measure routine finds the edges of the signals, and the time difference between them is stored and used to time-align displayed signals and triggers.

For the channels, the reference points are the offset voltage (vertical center screen) for the displayed signals and the trigger levels for the triggers.

For the external trigger, the reference is the trigger level.

The procedure for this calibration is covered in the Adjustment procedures, the *HP 54112D Operating and Programming manual*, or you can follow the prompts on the display in the Channel Skew menu.

6C-11. TEST MENU

Five sub-menus are available when the Test Menu is selected. The menus allow the user to access and run internal diagnostics and view the results. In addition, the position of printed circuit assemblies located in the card cage can be displayed.

Use of the test menus is covered in depth in section 6D, Troubleshooting.

6C-12. Repeat Loop/Run From Loop

The top key toggles between REPEAT LOOP and RUN FROM LOOP. These keys in conjunction with Loop # = [0-68], # Repetitions = [1-1000 or Infinite], and Start/Stop Test key will execute internal self-test diagnostic routines. All input signals must be disconnected from the instrument for these tests.

REPEAT LOOP. Selecting this mode will continuously execute the Loop # entered at RUN FROM LOOP. Pressing ***Start Test*** will start execution and the loop will continuously run until the ***Stop Test*** key is pressed. Pressing ***Display Errors*** will show the number of executions and number of failures of the loop.

Entering a value in # Repetitions will cause the software to run the designated loop that many times and stop. Start the test at REPEAT LOOP.

There are a number of loops that will blank or over-write the Stop Test key display on the CRT. The test can still be terminated by pressing the third function key from the top.

RUN FROM LOOP. Selecting this mode will start execution from the loop entered and will proceed to execute all higher numbered loops. After the last test, the cycle will be repeated.

Starting tests at RUN FROM LOOP ignores the number of repetitions (entered at REPEAT LOOP) and defaults to infinite.

If any test should fail, the instrument will change from RUN FROM LOOP to REPEAT LOOP and will repeatedly execute the loop that failed and appear to be stuck.

By starting the self-test at Loop 1 and letting it run for a bit, then stopping the test, it's easy to determine which loop the self-test stopped at. This loop should have more than one execution. To check the rest of the self test loops, ENTER the next highest loop number at RUN FROM LOOP and restart the test. The test will continue until the next loop fails. By continuing this, all loops will be forced to be tested.

When the instrument is powered up all loops will be tested except those purposely skipped due to specific failed tests. Four loops, 47, 51, 55, and 59 (one test on each of the four channels), will not cause a "Powerup Self Test Failed" message if they fail. This is because of possible noise during power up, if a signal is at the input of the instrument for example. The loops will be reported as failed in the Display Errors menu however. For more information see the Data Acquisition Subsystem Diagnostic Routines table in section 6D.

6C-13. Extended Tests

When this key is chosen there are 22 internal instrument tests that may be selected by entering the test number with the entry devices. The tests are numbered 0 through 21. All input signals must be disconnected from the instrument for these tests.

Many of the extended tests are useful only at the factory. Those that are of use to field service personnel are covered in the troubleshooting in section 6D.

6C-14. Start/Stop Test

This key is used to initiate any test where a test number is entered by one of the entry devices. Once the test number is entered, pressing ***Start Test*** initiates the test and the key toggles to ***Stop Test***. Pressing ***Stop Test*** stops the test in progress and the key toggles back to ***Start Test***.

There a number of tests that will blank or overwrite the ***Stop Test*** key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

6C-15. Display Errors

Pressing this key will display the number of any loops which failed while one of the following tests was run:

- Powerup self test
- INTERFACE tests
- REPEAT and RUN FROM LOOP tests
- HP-IB commanded self test

The display shows the current loop or last loop executed, the number of times the loop was executed, and the number of times that it failed. The bottom of the display shows all loops that failed starting with the first failure.

Error indications are accumulated since the last occurence of any of the following: Power up, I/O Assembly reset pushed, or Extended Test 12 run. An occurence of one of these conditions resets the error list.

The four STATUS x = xxxxx lines in the Display Errors field are primarily for factory use. Any field usable information in this part of the display is covered in section 6D.

To return to the Test Menu, press ***Exit Display***.

6C-16. Display Configuration

Most of the assemblies used in the HP 54112D have circuitry that allows interrogation directly by the microprocessor, the exception being the Microprocessor assembly itself. The HP 54112D card cage has 9 slots. When ***Display Configuration*** is pressed, the resulting display shows the firmware date and location of the card cage assemblies, except the microprocessor.

To return to the Test Menu, press ***Exit Display***.

6C-17. CRT SETUP MENU

When CRT Setup Menu is selected, four keys are displayed that allow access to CRT setup displays. The keys available are, from top to bottom, Confidence Test, Pattern Off, Light Output Off, Color Purity Off, and at the bottom, Exit CRT Setup Menu.

Even though some of the patterns overwrite the key display, the functions can be selected. The bottom key can be pressed at any time to exit the CRT Setup Menu.

6C-18. Confidence Test

This function displays the confidence test pattern. The pattern consists of three parts. At the top is a complete character set, in the center is a group of seven color blocks, and at the bottom a seven block grey-scale.

The top four lines of the character set display include the complete character set. The bottom line displays three sets of numerals. The first set is displayed in inverse video, the second set flashes between normal and inverse video and the third set is normal video and underlined.

The seven color blocks displayed at the center are, from left to right; beige, grey, red, yellow, green, amber, and cyan.

NOTE

Since color perception is subjective, any slight variation in colors from what is described here should be disregarded.

At the bottom of the CRT a seven block grey-scale is displayed, with increasing luminosity from left to right. This grey-scale display is used if Color CRT Module adjustments are necessary.

6C-19. Pattern

These patterns are used when Color CRT Module adjustments are necessary. When CRT Setup Menu is selected, this key is initially ***Pattern Off***.

Pressing ***Pattern Off*** once will display a white cross-hatch pattern over the entire CRT and the Pattern Off key changes to Pattern White. Inside the cross-hatch pattern there are dots at the center, corners, and at the 12, 3, 6 and 9 o'clock positions. Additionally, there are test matrices in the center and corners.

Pressing ***Pattern White*** key changes the pattern color to red and the key lable changes to "Pattern Red". Successive pressings of this key will change the color of the pattern to green then blue, the name of the Pattern key is the color displayed.

Pressing ***Pattern Blue*** key changes the display to the white cross- hatch pattern on the top half of the CRT and white with a dark cross-hatch on the bottom. The key then changes to Pattern HV Reg. This test is used primarily by the factory, however it may indicate the need for service if there are severe high voltage problems.

Pressing ***Pattern HV Reg*** changes the display to a solid white screen with dark cross hatch lines. The key changes to Pattern I White. Successive pressing of this key changes the color to red, green and then blue, the name of the Pattern key is again the color of the display.

Pressing ***Pattern I Blue*** changes the display to a white cross- hatch pattern with the inside flashing between solid white and cross- hatch. The key changes to Pattern Bounce. This test is primarily used by the factory, however, it may indicate the need for service if there are severe high voltage problems.

Pressing ***Pattern Bounce*** exits this set of tests and returns the CRT Setup Menu.

6C-20. Light Output

These displays are used by the factory.

Pressing ***Light Output White*** displays a horizontal band of white half the height of the display. The key display is not overwritten. Successive pressing of this key will change the color of this band to red, green, blue and then a grey-scale. Each time the key is pressed it also changes to the appropriate description.

Pressing ***Light Output Grey-Scale*** exits this set of tests and returns the CRT Setup Menu.

6C-21. Color Purity

Pressing ***Color Purity Off*** displays a full white raster. Successive pressing of this key changes the color of the raster to red, green and then blue. At each color display the name of the key changes to the appropriate description. These displays are used when Color CRT Module adjustments are necessary.

Pressing ***Color Purity Blue*** exits this set of tests and returns the CRT Setup Menu.

SECTION 6D
SELF-TESTS/TROUBLESHOOTING

6D-1. INTRODUCTION

This section describes the self-tests and troubleshooting routines that service personnel can use to locate failures to the assembly level. A basic understanding of the service menus and keys will be helpful in troubleshooting failures and is covered specifically in Section 6C.

The material presented in this section is in only a general order of importance, or use. Depending on the problem encountered, troubleshooting may progress back and fourth within the section but should start with the Main Troubleshooting Procedure.

Following are the troubleshooting sections in order of appearance:

- Main Troubleshooting
- "No Display" Troubleshooting
- Power Supply Troubleshooting
- Color CRT Module Failure Isolation
- Software Troubleshooting
- Core Subsystem Troubleshooting
- Data Acquisition Troubleshooting
- Front End Troubleshooting
- Hints, Tricks, and Arcana

6D-2. FAILURE INDICATIONS

The majority of failures in the HP 54112D are initially indicated in one of several ways: improper display (blank, distorted, or random) on the CRT after power-up, the keyboard is locked after power up, or "Powerup Self Test Failed!" is displayed on the CRT.

Other failures may be apparent during normal operation, but most problems are caught by the internal self-test routines and will result in one of the indications mentioned.

Loop failures may occur occasionally due to system or environmental noise. This may result in intermittent power-up failure messages. Loops must fail a certain percentage of the time to be considered a true failure and must be specially tested if random failures are occuring. See Main Troubleshooting for further information and procedures.

NOTE

In addition to the front panel power switch (STBY), there is a main breaker power switch located on the rear panel. Before troubleshooting a "no display" failure, make sure the rear panel switch has not been inadvertently turned off.

6D-3. TEST EQUIPMENT REQUIRED

The HP 54100 Family Product Support Kit consists of assembly and cable extenders and other tools. Some of the parts in this kit are necessary for certain assembly level diagnostic procedures. These procedures aid in troubleshooting, but are not necessary for troubleshooting most failures.

In addition, other than the equipment required for performance tests and adjustments, all that is needed is a general purpose 300 MHz oscilloscope such as the HP 54201A.

6D-4. ONE-KEY POWER UP

A one-key power up is often performed to return the instrument setup to default conditions. This is done as follows:

1. Set the front panel POWER switch to STBY,
2. Press and hold one front panel key,
3. Turn front panel POWER switch to ON.
4. Release key when display shows "Powerup Self Test Passed!" or Failed.

6C-5. TWO-KEY POWER UP

CAUTION

Using the two-key power up will leave the instrument uncalibrated. Effort needed for recalibration should be considered before using this method to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.

A two-key power up is a basic reset of the entire operating system of the HP 54112D. All volatile and non-volatile RAM is cleared. As a result, all calibration factors are purged and the instrument must be recalibrated.

All calibration except Offset Cal can be done with just the front panel CAL signal or the rear panel Timebase Cal signal and the software cal menus. Offset Cal requires a 10 Vdc power supply. The two-key power up is performed in much the same way as the one-key power up.

1. Set the front panel POWER switch to STBY.
2. Press and hold the top and bottom keys in the group at the right edge of the display.
3. Turn front panel POWER switch to ON.
4. Release keys when display shows "Powerup Self Test Passed!" or Failed.

6D-6. MAIN TROUBLESHOOTING

Figure 1, Main Troubleshooting Flow Diagram, should be used as the initial and primary troubleshooting procedure.

6D-7. Connectors

Most instruments are sensitive to connectors and assemblies that are not completely seated. So, one of the initial steps needs to be to make a mechanical check of all the connectors and assemblies to make sure that everything is properly seated before you start the trouble shooting procedure.

Check the coaxial connectors, ensure that the ribbon connectors are completely snapped in place, and press down gently on each of the card cage assemblies to ensure that they are properly seated.

6D-8. System Lock-up

After running the power-up self tests the instrument may be locked up by a system error, it will not respond to the keyboard. This can be a random failure or a hard failure. An error message such as one of the following,

```
SYSTEM  ERROR! Zero Divide XXXXXXH
SYSTEM  ERROR! Bus Error XXXXXXH
SYSTEM  ERROR! Address Error XXXXXXH
```

will be displayed on screen, followed by

```
To clear, cycle power with one front-panel key
pressed. If the error condition remains please
consult the service manual.
```

Note the hex number (XXXXXXH) after the error message. This may be useful if help from an HP Service Center is needed later.

Follow the instructions to see if the one key power-up is sufficient to reset the instrument. If the instrument is failing after a one key power-up and calibration traceability need not be maintained, try to reset the instrument with a two key power-up.

CAUTION

Using the two-key power up will, at least temporarily, leave the instrument in an uncalibrated state. Effort needed for recalibration should be considered before using this mode to reset the instrument. Calibration traceability will be lost if a two-key powerup is used.

If the instrument is still failing, to obtain information about the failure mode it will be necessary to "break in" to the power-up routine before the system becomes locked. Go to the Software Troubleshooting procedure for further information.

6D-9. Input Overload

If an Input Overload message is displayed on screen immediately after power-up the cause is usually an input sense cable that has become disconnected or mis-connected. This failure also results in lock-up of the instrument; there will be no response to the keyboard.

CAUTION

Do not perform a two-key powerup. The instrument will be harder to return to proper operation.

Use the following procedure to check for this problem.

1. Turn the POWER to STBY.
2. Remove the covers (see section 6A).
3. Ensure that all of the input sense cables are properly connected. (See the diagram on the cover of the instrument or at the end of section 6A.)
4. If the instrument still fails to power up properly, continue with troubleshooting based on known symptoms.

If a two-key powerup was performed, it may be necessary to clear the non-volitile RAM manually.

1. Turn POWER to STBY.
2. Pull the Microprocessor assembly clear of the mother board. This separates the RAM from its battery supply on the I/O assembly. Leave separated for several seconds.
3. Re-insert Microprocessor assembly and apply power. Instrument should power up and display a message that calibration is needed.

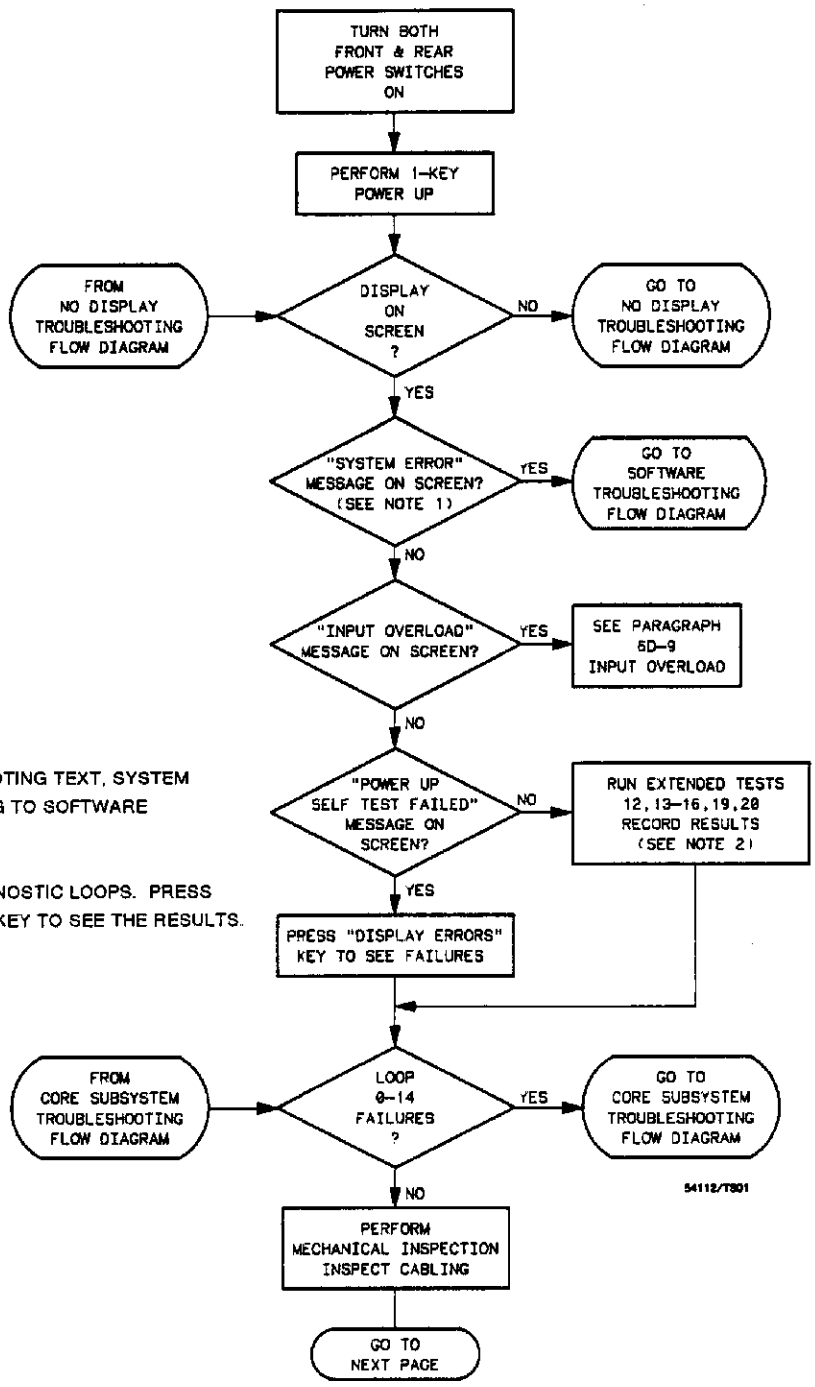
6D-10. Intermittent Failures

Loop failures that are intermittent may not be true failures. A loop must fail more than one percent of the time to be considered a true failure. If a loop seems to be intermittent it should be run in the REPEAT LOOP mode to determine the failure percentage.

Use the following procedure to check the failure percentage of a given loop.

1. Press ***more***, ***Utility***, and ***Test menu***.
2. Press the top softkey to get ***RUN FROM LOOP*** and ENTER the Loop # with the ENTRY keys.
3. Press ***RUN FROM LOOP*** to get ***REPEAT LOOP*** and ENTER the # Repetitions with the ENTRY keys. The number of repetitions must be high enough to get a proper sampling. Checking for one percent of errors will need several hundred repetitions for a good sample.
4. Press ***Start Test***.

   Several hundred samples may take a few minutes to complete. You can press ***Stop Test*** then ***Display Errors*** to check on the progress of the test but starting the test again will start it at the beginning.
5. When the display returns to the test menu press ***Display Errors*** to check the error rate. If ***Failures*** = is greater than one percent of ***Executions*** = the loop has a true failure.



NOTES

1 SEE MAIN TROUBLESHOOTING TEXT, SYSTEM LOCK-UP, BEFORE GOING TO SOFTWARE TROUBLESHOOTING

2 TEST 12 RUNS THE DIAGNOSTIC LOOPS. PRESS THE "DISPLAY ERRORS" KEY TO SEE THE RESULTS.

Figure 6D-1. Main Troubleshooting Flow Diagram

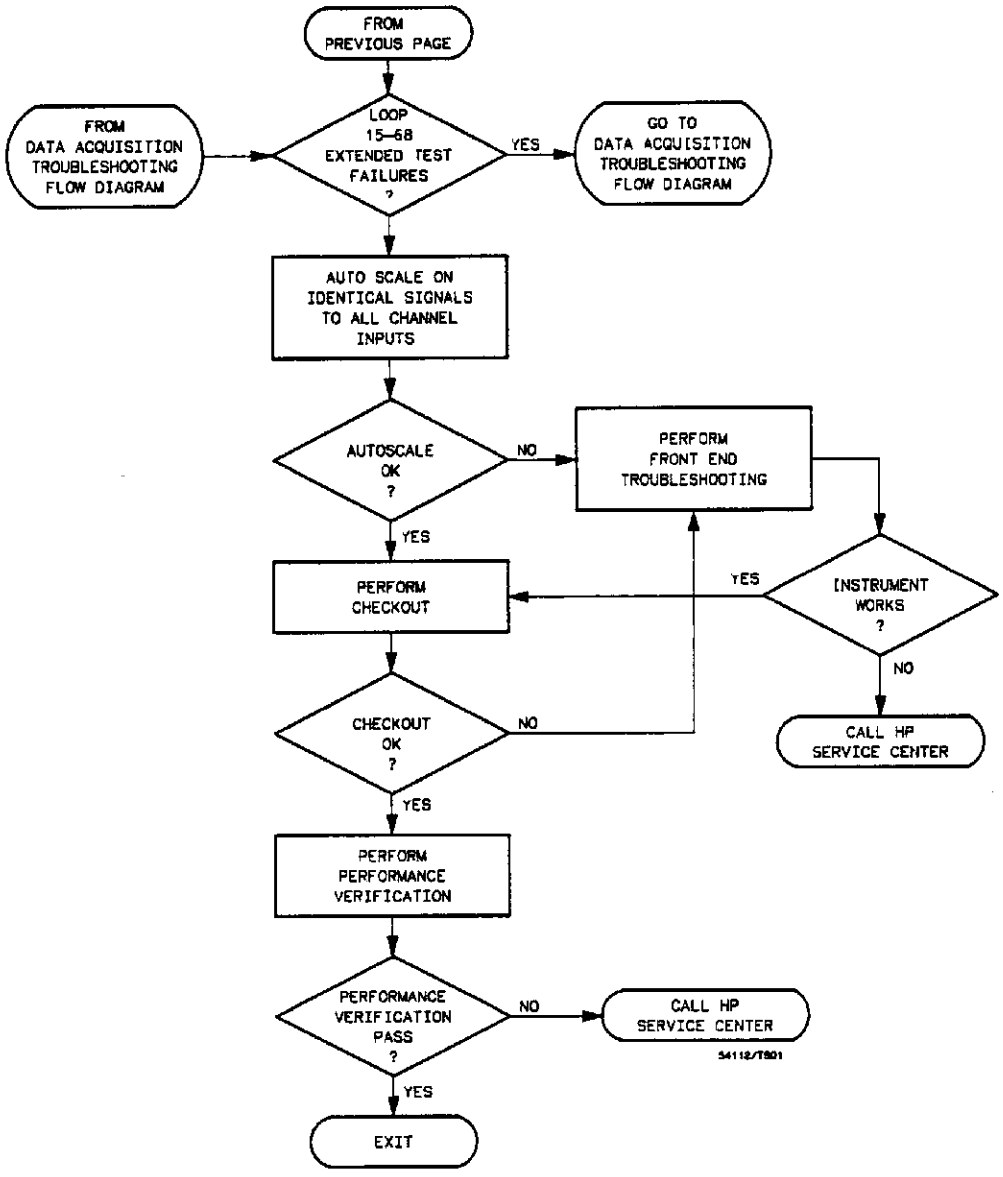


Figure 6D-1. Main Troubleshooting Flow Diagram (con't.)

6D-11. NO-DISPLAY TROUBLE-SHOOTING

Check to see whether the power supply is functioning correctly by checking the four LEDs that indicate supply function. One is located on the I/O assembly (A3), and the others are located on the primary, digital, and analog power supply boards. If any of these LEDs is not lit, proceed directly with the Power Supply Troubleshooting procedures.

Use a voltmeter to check the voltages at the test points on the power supply. If voltages are not correct (see Power Supply Troubleshooting) proceed with the Power Supply Troubleshooting procedure.

If the supplies are correct and there is still no display, cycle the power with the front panel switch. If the display produces a normal flash at powerup and powerdown, the Color CRT Monitor is probably working. If it does not light at all, check if the 120 V LED at the front of the Primary Supply is lit. If it is, outrig a working Color CRT Module (see Color CRT Module Outrigging). Replace Color CRT Module if outrigged module works. If outrigged module does not work, see Power Supply Troubleshooting procedure.

If the display lights, determine whether the problem is in the Color Display assembly or in the Color CRT Module, as follows:

1. Check the voltage on the 120 Volt pin on the Color CRT Module; also check the Red, Blue, and Green Video signals. If these signals are correct (see Color CRT Module Failure Isolation) then outrig a new Color CRT Module and test it. If it works, replace the module.

2. If they are not correct, the display assembly is suspect. Check the +/- 5 Volts on the display assembly and the Vertical and Horizontal Sync signals coming from the display assembly. If these are not present, the Color Display assembly is suspect. Remove boards not in the core system and proceed with verifying its operation (see Core Subsystem Troubleshooting).

If you have not been able to find the problem using these techniques, call your HP Service Center.

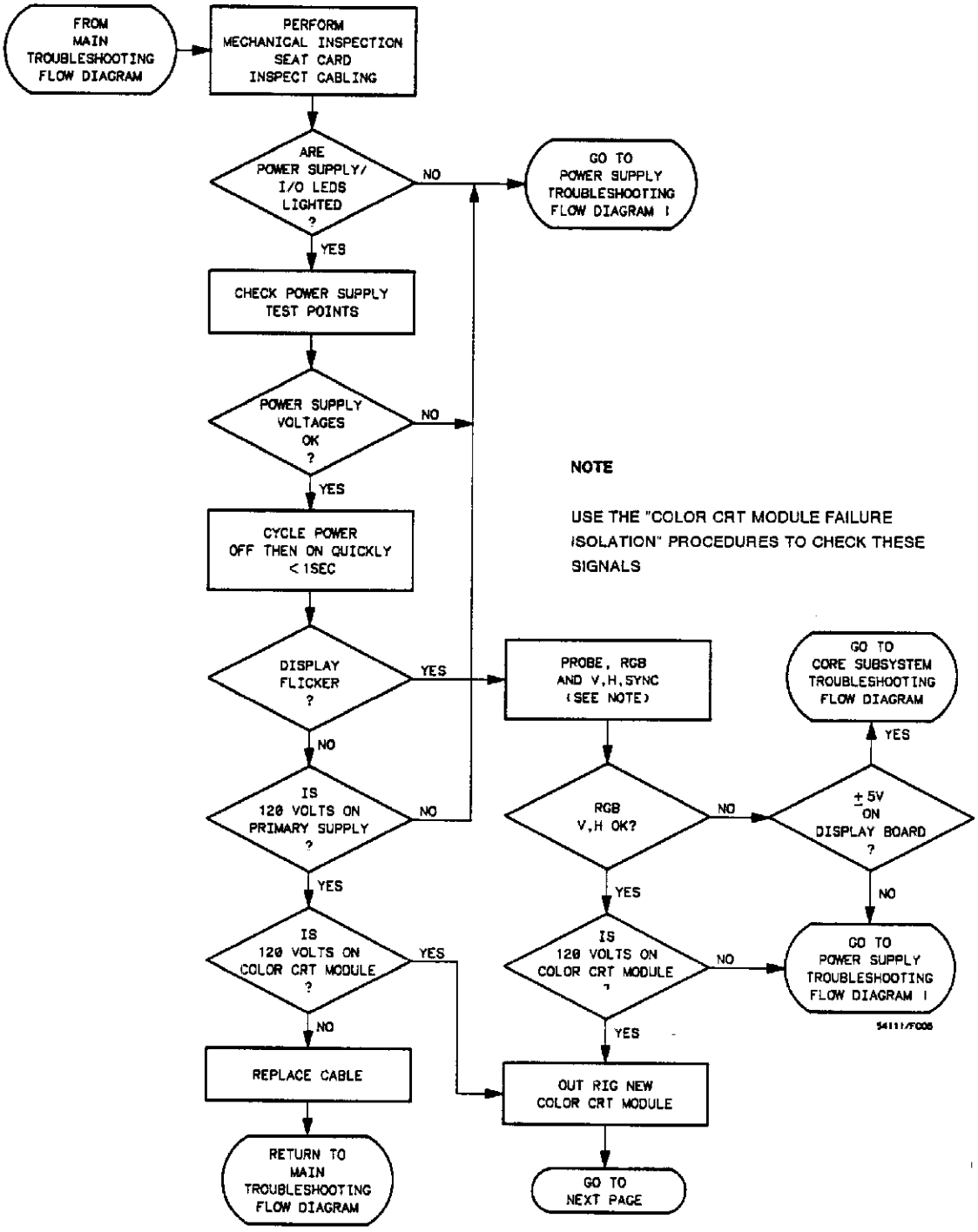


Figure 6D-2. No Display Troubleshooting Flow Diagram

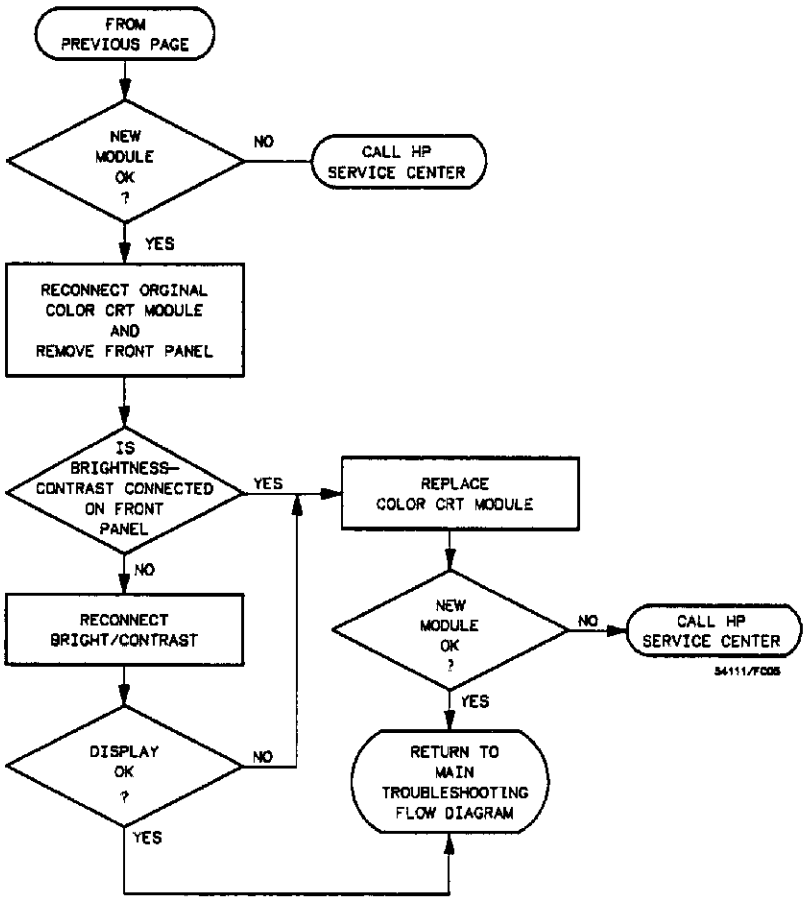


Figure 6D-2. No Display Troubleshooting Flow Diagram (con't.)

6D-12. POWER SUPPLY TROUBLE-SHOOTING

When a power supply problem is suspected, it is first important to make sure that no unusual load is keeping the supply in a current limited condition. The table below shows which supplies are used on each assembly.

1. If the 300V LED on the Primary Supply is not lit go directly to the Power Supply Troubleshooting Flow Diagram, next page.

2. If the 300V LED is lit, find the LEDs on the Analog and Digital supplies and I/O assembly. They are near the top-front of each assembly, so if you cannot see them they are probably not lit.

3. If the LEDs are lit and you still suspect a supply problem, go to the Power Supply Troubleshooting Flow Diagram, next page.

4. If the LEDs are not lit continue with this procedure before going to the Power Supply Troubleshooting Flow Diagram, next page.

5. Pull up the Timebase/trigger assembly (right side of card cage) until it clears the motherboard connector, about one half inch.

6. Check to see if the LEDs are lit. If the LEDs are lit troubleshoot the Trigger Qualifier for excessive loading. If they are not lit, leave the assembly up and go to the next step.

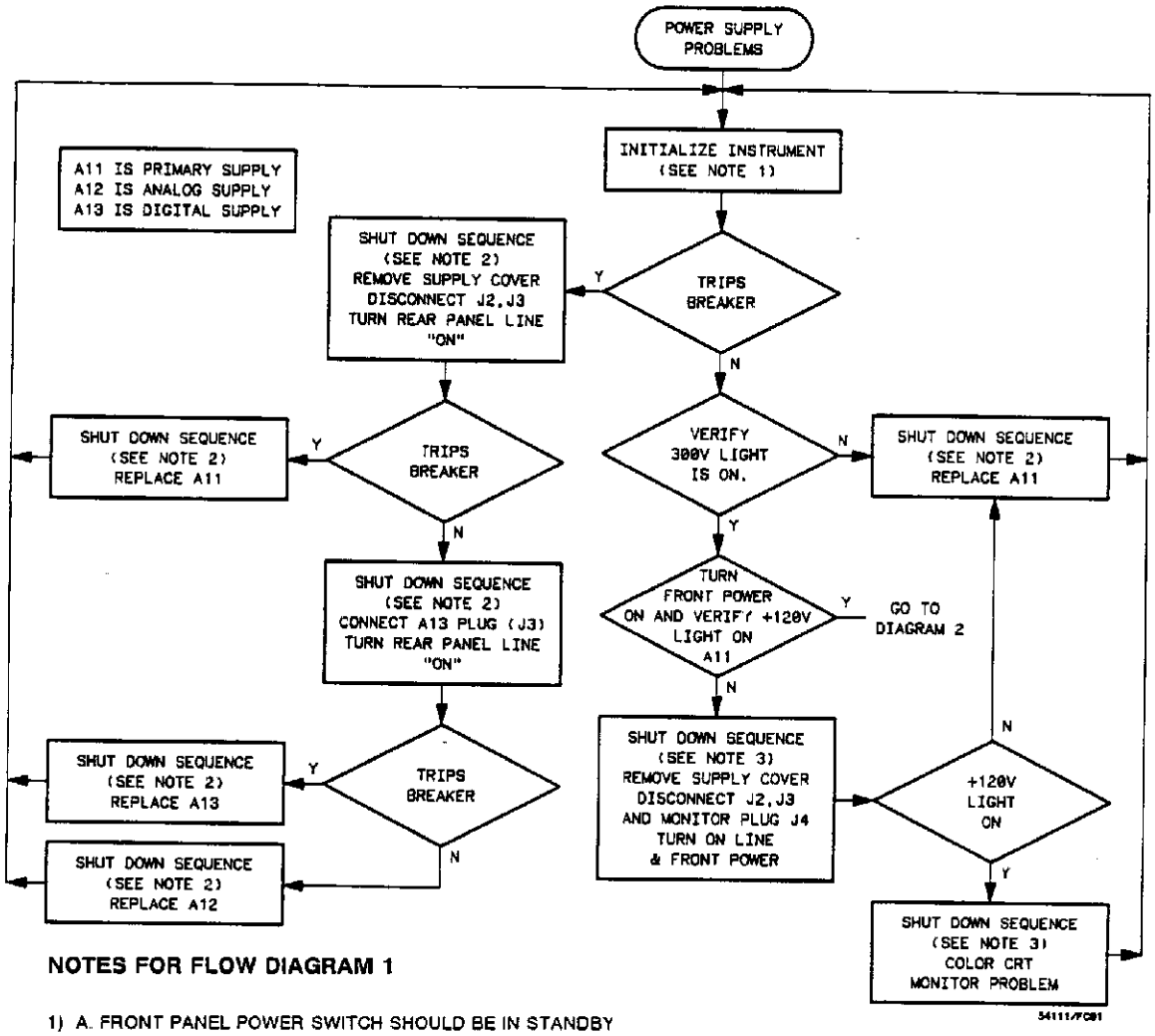
7. Working from right to left, pull up each card cage assembly while watching for the LEDs to light. If they light, troubleshoot for excessive loading, the last assembly pulled up.

8. After the I/O assembly is pulled up, watch only for the supply LEDs. If all nine card cage assemblies are up, and the supply LEDs are not lit, go to the following Power Supply Troubleshooting Flow Diagram.

Table 6D-1. Power Supply Distribution

	+5V	-5V	+18V	+8V	-8V	-18V	+120V
MICROPROCESSOR	*						
INPUT/OUTPUT †	*	*	*	*	*	*	
ACQUISITION	*	*	*	*	*	*	
TIMEBASE/TRIG			*	*	*	*	
COLOR DISPLAY	*						
COLOR CRT MOD.							*

†ONLY THE +5V IS USED FOR POWER. THE OTHER SUPPLIES CONNECT FOR POWER TEST ONLY AND ARE HIGH IMPEDANCE POINTS. LIKELYHOOD OF LOADING THESE SUPPLIES IS LOW.



NOTES FOR FLOW DIAGRAM 1

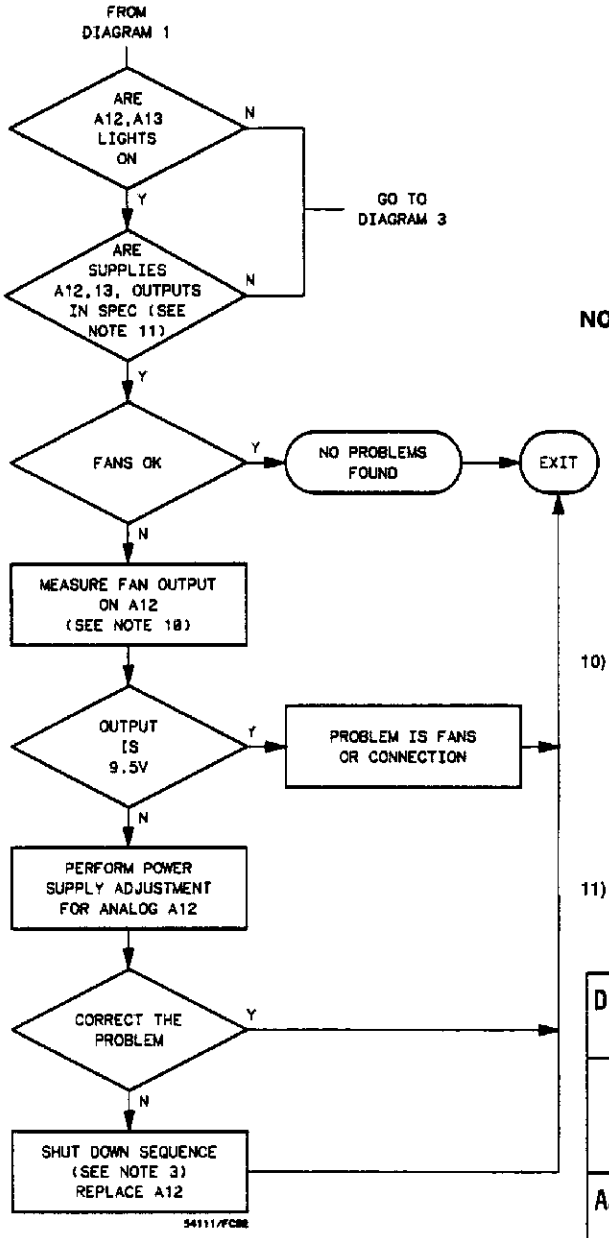
1) A. FRONT PANEL POWER SWITCH SHOULD BE IN STANDBY
   B. REAR PANEL LINE SWITCH SHOULD BE OFF "0"
   C. CONNECT AC POWER SOURCE
   D. TURN REAR PANEL LINE SWITCH TO ON "1"

2) A. TURN REAR PANEL LINE SWITCH TO OFF "0"
   B. ALWAYS UNPLUG AC POWER SOURCE
   C. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

WARNING
EXTREME CAUTION MUST BE TAKEN WHEN REMOVING POWER SUPPLY COVER.

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

Figure 6D-3. Power Supply Troubleshooting Flow Diagram (part 1)



A11 IS PRIMARY SUPPLY
A12 IS ANALOG SUPPLY
A13 IS DIGITAL SUPPLY

NOTES FOR FLOW DIAGRAM 2

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

10) CONNECT THE VOLTMETER (+) LEAD TO THE "FAN" TEST POINT AND THE (-) LEAD TO THE -18V TEST POINT. THE READING SHOULD BE 9.5V. THIS VOLTAGE WILL INCREASE WITH INCREASING AMBIENT TEMPERATURE. SEE THE POWER SUPPLY ADJUSTMENT PROCEDURE FOR THE ANALOG SUPPLY.

11) FOR POWER SUPPLY TEST POINTS AND SPECIFICATIONS SEE TABLE BELOW.

DIGITAL SUPPLY TST PTS (+) LEAD	(-) LEAD	VOLTAGE
+5V	GND	+5.10 ±0.1V
-5V	GND	-5.30 ±0.1V
+14B	GND	>+5V
ANALOG SUPPLY TST PTS (+) LEAD	**(-) LEAD**	**VOLTAGE**
+18V	GND	+18.5 ±0.3V
+8V	GND	+8.9 ±1V
-8V	GND	-8.5 ±1V
-18V	GND	-18.5 ±0.3V
FAN	-18V	+9.5 ±0.3V
+26B	GND	>+5V

Figure 6D-3. Power Supply Troubleshooting Flow Diagram (part 2)

NOTES FOR FLOW DIAGRAM 3

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

4) THE NOMINAL OUTPUT FOR +14B IS 21V. HOWEVER, WHEN THE SUPPLY IS OPERATING IN THE CURRENT LIMIT MODE, IT CAN BE AS LOW AS +5V. THE NOMINAL OUTPUT FOR +26B IS 26V. IT TOO CAN BE AS LOW AS +5V WHEN IN CURRENT LIMIT.

5) MEASURE OUTPUTS +5V AND -5V ON THE DIGITAL POWER SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES. IF OUTPUTS ARE GREATER THAN HALF THE ANSWER IS NO

6) WHEN THE SUPPLIE(S) ARE RUNNING IN THE CURRENT MODE THIS MEANS THAT AN EXTERNAL LOAD IS PULLING DOWN THE SUPPLY OUTPUT(S). AN EXTERNAL LOAD COULD BE A BOARD IN THE CARD CAGE OR THE COLOR DISPLAY ASSEMBLY (NOT THE COLOR CRT MODULE). THE ONLY WAY TO ISOLATE THE COLOR DISPLAY ASSEMBLY IS TO COMPLETELY REMOVE IT FROM THE MAINFRAME. THE FANS CAN ALSO PUT THE ANALOG BOARD INTO THE CURRENT MODE. YOU CAN DISCONNECT THE FANS BY REMOVING THE BOTTOM COVER AND DISCONNECTING THE FAN CABLE

   TO ISOLATE A CURRENT PROBLEM, REMOVE ONE LOAD AT A TIME UNTIL THE PROBLEM IS FOUND. PROBLEMS COULD INCLUDE BENT PINS ON THE MOTHER BOARD OR A BAD COMPONENT ON A PC ASSEMBLY. SEE THE TABLE BELOW FOR POWER DISTRIBUTION TO THE VARIOUS ASSEMBLIES.

7) MEASURE OUTPUTS ±18V AND ±8V ON THE ANALOG SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES. IF OUTPUTS ARE GREATER THAN HALF THE ANSWER IS NO.

8) THE TEST POINTS TO MEASURE +14.6V ARE AT THE BACK OF THE BOARD CLOSE TO THE TOP. CONNECT THE VOLTMETER COMMON LEAD TO THE COM TEST POINT ON THE BOARD. **CAUTION!!!** ***USE CAUTION WHEN MEASURING THIS VOLTAGE. IT IS NOT ISOLATED FROM THE LINE (MAINS) INPUT AND THE PRIMARY SUPPLY IS EXPOSED WITH THE POWER SUPPLY COVER REMOVED.***

9) BY REMOVING THE CONNECTORS AT J2 AND J3 YOU ARE CHECKING IF EITHER THE ANALOG OR DIGITAL SUPPLY IS LOADING VCNTL.

   EXTREME CAUTION MUST BE TAKEN WHEN MEASURING VCNTL ON THE PRIMARY SUPPLY. THE TOP PIN ON CONNECTORS J2 AND J3 IS VBULK WHICH IS +300V. THE PINS BELOW ARE VCNTL, THEN GROUND.

   TO MEASURE VCNTL, TURN THE POWER OFF AND MAKE SURE THE +300V LAMP (NEAR TOP OF BOARD) IS OFF. CONNECT THE VOLTMETER (+) LEAD TO VCNTL (SECOND PIN FROM TOP) AND THE (-) LEAD TO GROUND (BOTTOM PIN). APPLY POWER AND OBSERVE THE METER READING. WITH ONE SUPPLY CONNECTED THE READING SHOULD BE ABOUT +25V AND WITH NEITHER CONNECTED ABOUT +42V. TURN OFF POWER (+300V LAMP IS OFF) BEFORE REMOVING THE VOLTMETER LEADS

	+5V	-5V	+18V	+8V	-8V	-18V	+120V
MICROPROCESSOR	*						
INPUT/OUTPUT †	*	*	*	*	*	*	
ACQUISITION	*	*	*	*	*	*	
TIMEBASE/TRIG			*	*	*	*	
COLOR DISPLAY	*						
COLOR CRT MOD.							*

NOTE:

†ONLY THE +5V IS USED FOR POWER. THE OTHER SUPPLIES CONNECT FOR POWER TEST ONLY AND ARE HIGH IMPEDANCE POINTS. LIKELYHOOD OF LOADING THESE SUPPLIES IS LOW.

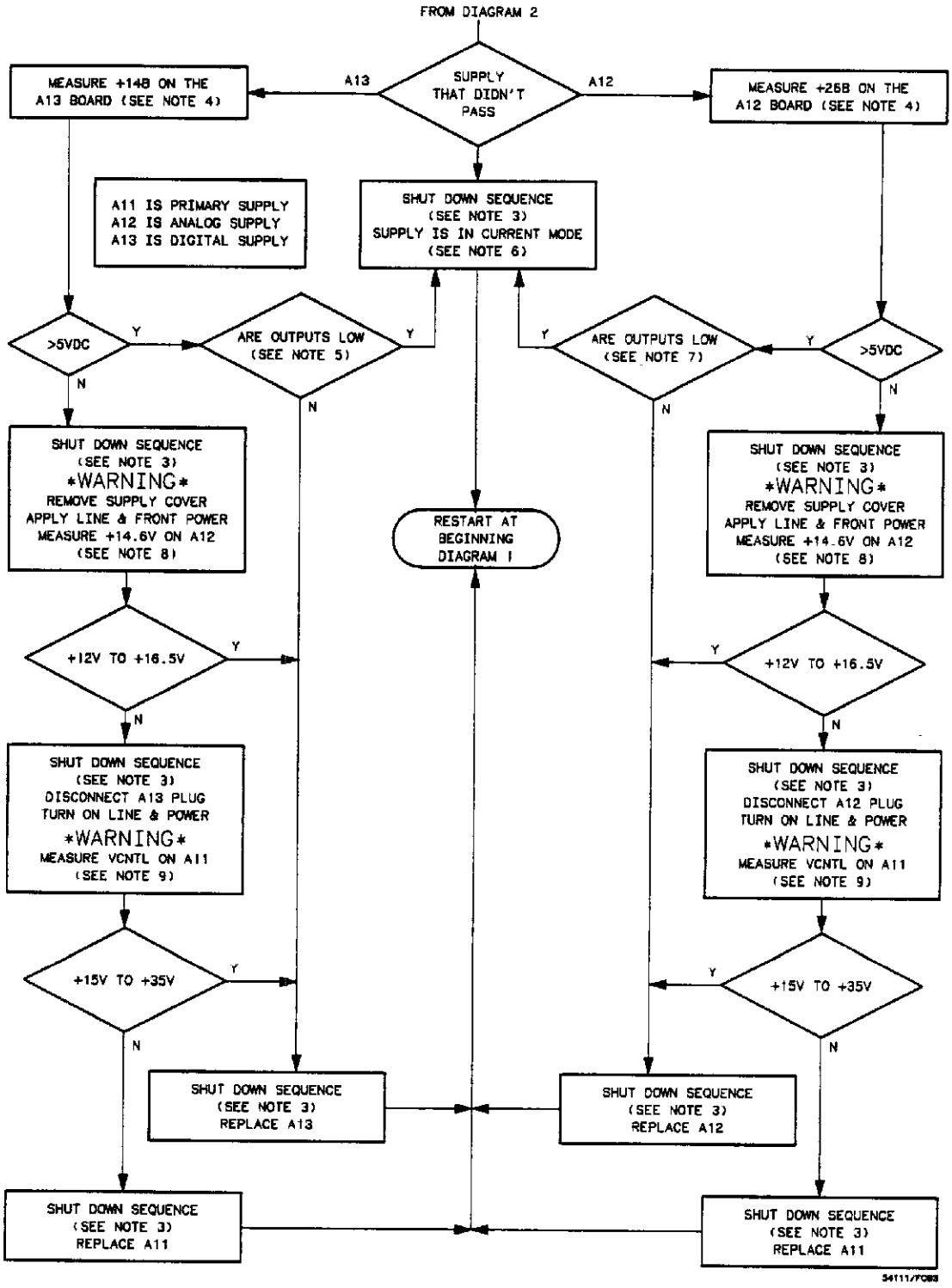


Figure 6D-3. Power Supply Troubleshooting Flow Diagram (part 3)

6D-13. COLOR CRT MODULE FAILURE ISOLATION

The following procedure causes the processor to write a known pattern of video to the module. The video waveforms, the vertical and horizontal sync signals, and the +120V primary module power are checked at the module inputs. If the inputs are present and correct, use the Color CRT Module Outrigging procedure to ensure that replacement of the module will correct the problem.

6D-14. Troubleshooting Procedure

1. Turn instrument to STBY using the front panel power switch.

2. Remove covers (see Instrument Disassembly, section 6A).

3. Turn power on and check the +120 V module power at the module power input connector (see next figure). The correct voltage will be between +118 and +122 volts. If the +120 V supply voltage is incorrect, see the power supply troubleshooting procedures.

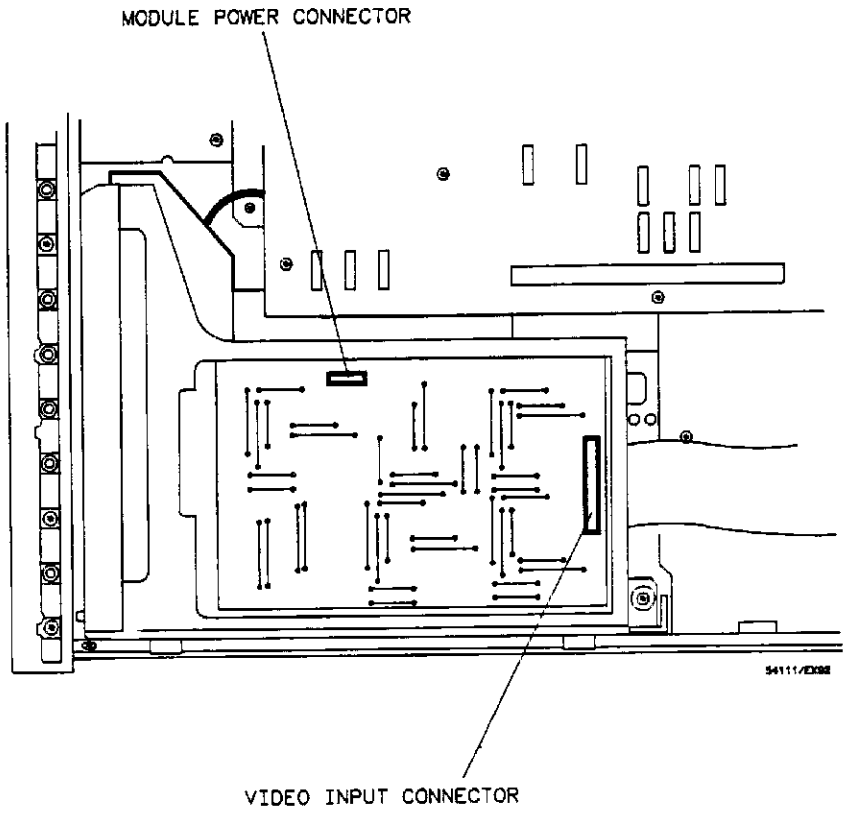


Figure 6D-4. Color CRT Module Input Connections

4. Move clear plastic board shield on bottom of Color CRT Module by pushing rearward until it clears front frame and hinge it away from the board.

5. With 10:1 divider probes, connect channel 1 of the monitor oscilloscope to vertical sync test point VD (located on module video input connector, pin 3) and channel 2 of the monitor oscilloscope to horizontal sync test point HD (located on module video input connector, pin 7). These test points are located on the Color CRT Module (A19). The vertical and horizontal sync signals are TTL levels and should resemble the waveforms in the following figure. The vertical sync is on the top and the horizontal sync on the bottom.

6. To see if the Color CRT Module is loading the signals, disconnect the wide ribbon cable at the Color Display assembly and check the signals at the two labled test points (VSYNC, HSYNC near U119) on the Color Display assembly.

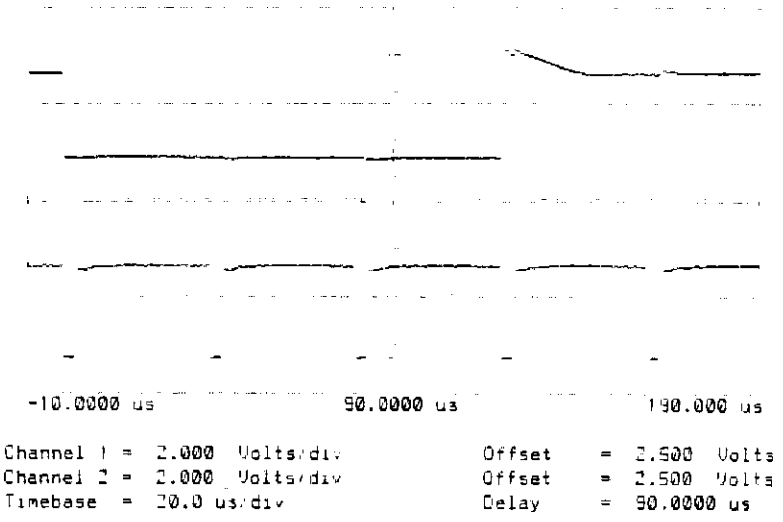


Figure 6D-5. Vertical and Horizontal Sync Waveforms

7. It is helpful to try to get a known display before checking the video waveforms. If the display is operating, press ***more, Utility, CRT Setup Menu***, and ***Color Purity***. This will give a white raster so all video signals will be at maximum.

   If there is no display, try to get the same signals using the following procedure.

   a. Turn instrument off, then on, then press the following softkeys, in order given.

   b. In bottom row press:
      Key at extreme right
      Key second from right
   c. In vertical column press:
      Key at bottom
      Key third from bottom

8. Check the red, green, and blue video signals at the module video input connector at pins 21, 29, and 37 respectively (see Color CRT Module Input Connections drawing).

   The video signals have a 0 V baseline and will vary in amplitude from 0 V to approximately +600 mV, depending on the characteristics of the colors displayed.

9. Video signals can be adversely loaded by input circuit failures within the Color CRT Display Module. Therefore, before assuming Color Dispaly assembly failures, repeat this test with the video cable disconnected from the Color CRT Module and the measurements taken at the pins of U145 on the Color Display assembly. The red, green, and blue signals are on U145 pins 14, 18, and 22 respectively.

6D-15. Incorrect Display Color

Using the CRT Setup Menu, then pressing the ***Color Purity*** key it is easy to locate a potentially defective CRT write gun or associated electronics. By pressing the ***Color Purity*** key several times the primary colors will be displayed. The colors displayed on the measurement screens are user definable, while the color purity check displays fixed primary colors.

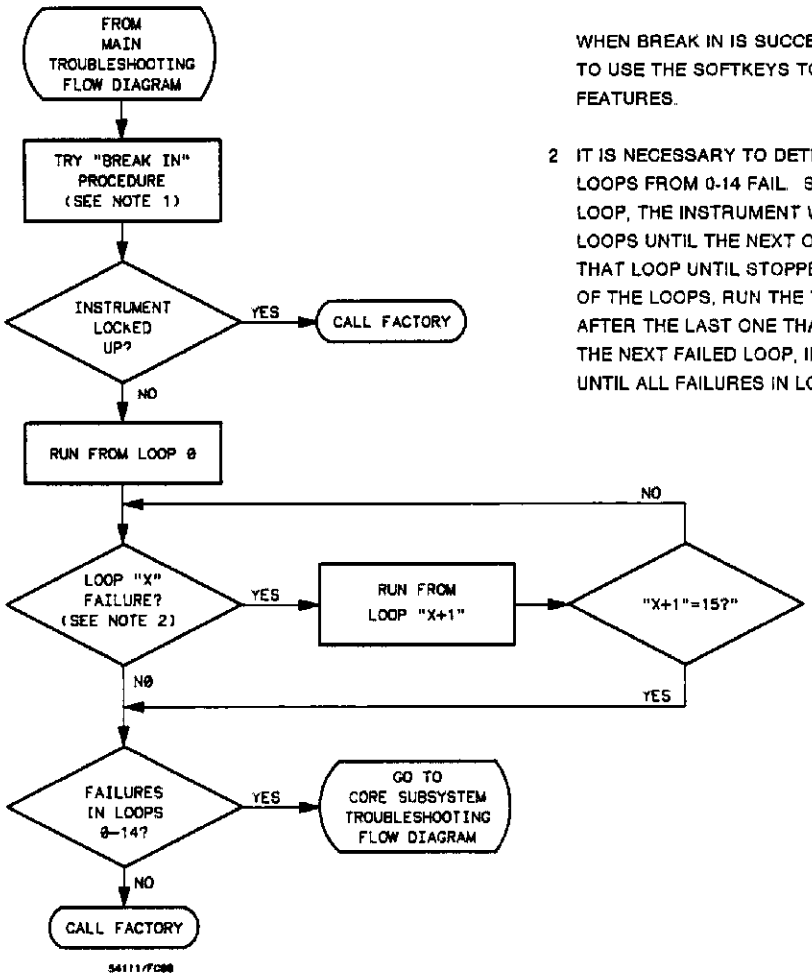
6D-16. Module Outrigging Procedure

Due to the amount of work and time involved in changing the Color CRT Module it is prudent to verify the defective module diagnosis by outrigging a good module. Required parts which are part of the 54100 Family Support Kit are: Color CRT Module power cable, Display Control assembly, and Display Control Cable. Also necessary is a working Color CRT Module which is not part of the service kit.

1. Turn power off and remove instrument power cable.
2. Remove covers (see Instrument Disassembly, section 6A).
3. Disconnect Color CRT Module power cable at the primary power supply.
4. Connect the Color CRT Module power cable from the support kit to the primary power supply.
5. On the bottom of the instrument, disconnect the wide ribbon cable from the the suspect Color CRT Module and extend it as far as possible from the instrument when it is in a normal operating position.
6. Set the working Color CRT Module next to the instrument.
7. Connect the wide ribbon cable to working module.
8. Connect the module power cable to the mating connector towards the front of the CRT Module. This connection can be verified by noting that the connector is labled B-4 on the bottom of the PC board at the connector.
9. Connect the Display Control Cable from the support kit to the mating connector which is toward the rear of the module. This connector is labled B-2 on the bottom of the PC board.
10. Connect the CRT Brightness Control from the support kit to the other end of the Display Control Cable.
11. Re-connect the power cord and turn instrument on.
12. Verify display operation.

6D-17. SOFTWARE TROUBLE-SHOOTING

Software troubleshooting is used to evaluate a software problem that prevents the instrument from displaying self-test information by locking up the keyboard. This routine is entered from the Main Troubleshooting Flow Diagram.



NOTES

1 THIS PROCEDURE ALLOWS YOU TO "BREAK IN" TO AN INSTRUMENT THAT IS LOCKING UP DURING THE POWERUP CYCLE. IT IS NECESSARY TO INTERRUPT THE POWERUP CYCLE BEFORE IT LOCKS UP THE INSTRUMENT.

IF THE INSTRUMENT IS LOCKING UP, CYCLE THE POWER WITH THE STBY SWITCH. JUST AS THE GRATICULE IS BEING DISPLAYED DURING THE POWERUP ROUTINE, PRESS THE STOP/SINGLE KEY TIMING IS IMPORTANT HERE AND IT MAY TAKE SEVERAL TRIES TO "BREAK IN".

WHEN BREAK IN IS SUCCESSFUL, YOU WILL BE ABLE TO USE THE SOFTKEYS TO ACCESS THE SELF TEST FEATURES.

2 IT IS NECESSARY TO DETERMINE WHICH OF THE LOOPS FROM 0-14 FAIL. STARTING AT A SELECTED LOOP, THE INSTRUMENT WILL RUN THROUGH THE LOOPS UNTIL THE NEXT ONE FAILS, THEN REPEAT THAT LOOP UNTIL STOPPED. TO CHECK THE REST OF THE LOOPS, RUN THE TEST FROM THE LOOP AFTER THE LAST ONE THAT FAILED AND CHECK FOR THE NEXT FAILED LOOP, IF ANY. REPEAT THIS UNTIL ALL FAILURES IN LOOPS 0-14 ARE FOUND.

Figure 6D-6. Software Troubleshooting Flow Diagram

6D-18. CORE SUBSYSTEM TROUBLE-SHOOTING

GENERAL

It is best to attempt to get the HP 54112D to pass all the Core Tests before going on to fix more complex loops. Occasionally, bent motherboard pins or defects in other system elements will cause these loops to fail. By making a system of the Microprocessor assembly, I/O assembly and one other assembly, it is possible to determine which socket or assembly may be causing an interaction that causes one of the core loops to fail. Using this technique, seat each assembly into the motherboard one at a time. Be sure to turn the power off before raising or seating an assembly into the motherboard.

If only the Microprocessor and I/O assemblies are seated, the system will go into a repeating multicolored routine with about a two second cycle. This is useful in certain troubleshooting situations but no loop error information will be available.

LOOP 11

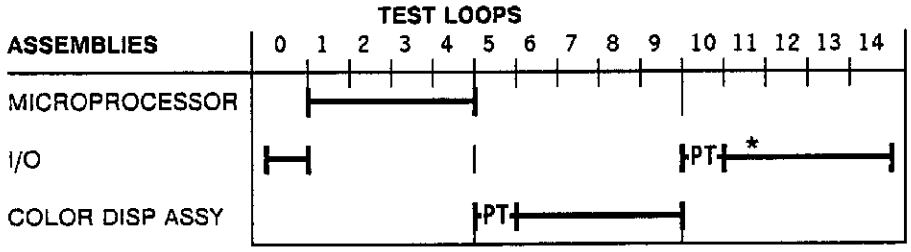
Loop 11, which can test every addressable location in the DRAM on the I/O assembly, is a special case. Using RUN FROM LOOP does not completely execute this test because that would take about 18 minutes to complete. Instead, RUN FROM LOOP tests a random block of this memory.

The REPEAT LOOP mode will run the complete Loop 11 test, but only once due to its length. A complete test of DRAM should be done only if the I/O assembly is suspected of failing and there is not enough proof, or if loop 11 has an intermittent failure. This test takes about 18 minutes to run.

Table 6D-2. Core Subsystem Diagnostic Routines.

NOTE

For the Core Subsystem tests to be available and meaningful, the power supplies, Color CRT Module, and Color Display assembly must be working, and the Microprocessor, I/O, and one other assembly must be present.

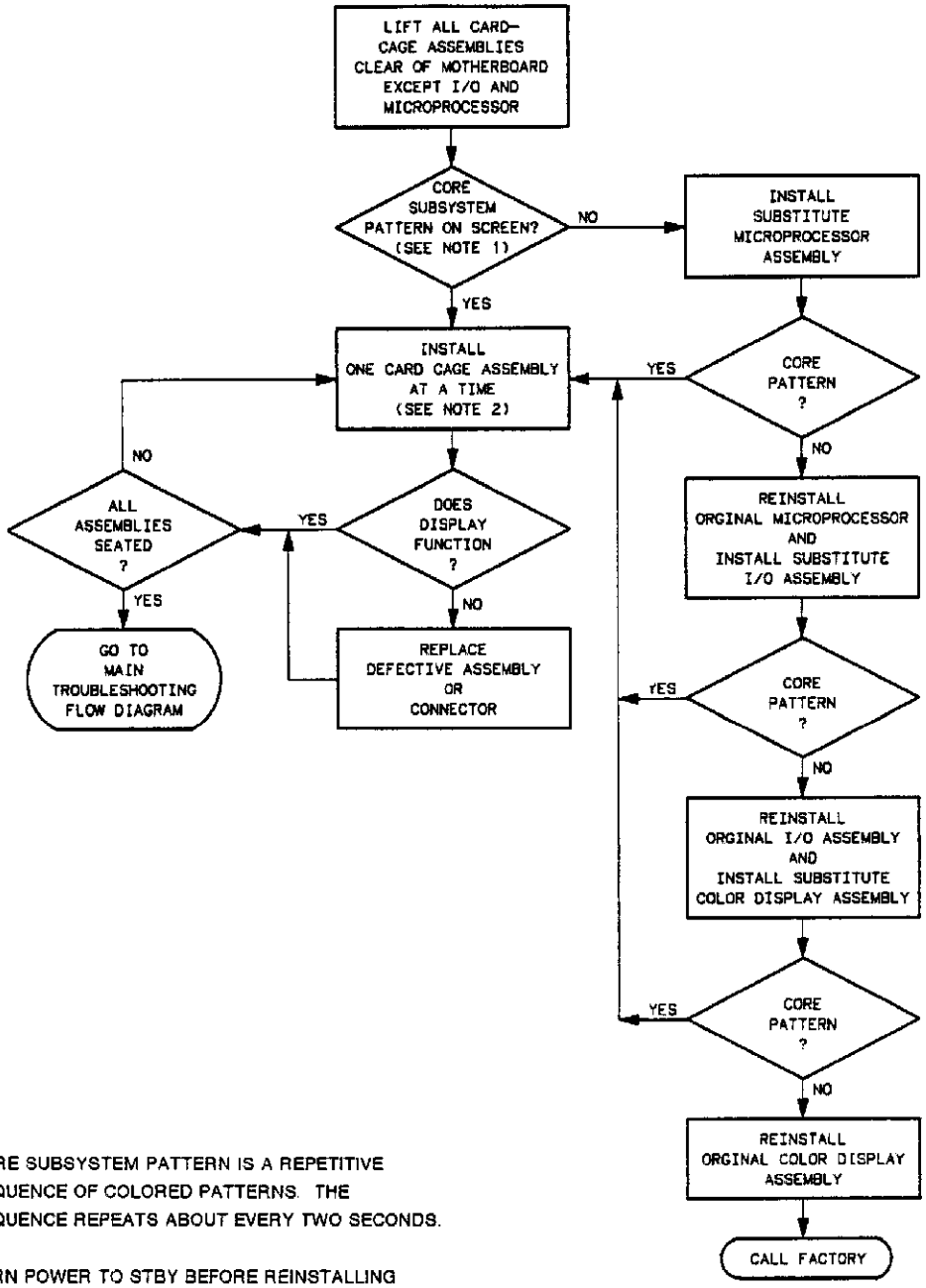


KEY:

PT — Presence test. If the diagnostic software fails to find the assembly, this loop fails and all other self tests that include this assembly are skipped.

This assembly must work for the test to be successful. The test will be skipped and will not show a failure if the assembly is not present.

* See Loop 11 text above



NOTES

1 CORE SUBSYSTEM PATTERN IS A REPETITIVE SEQUENCE OF COLORED PATTERNS. THE SEQUENCE REPEATS ABOUT EVERY TWO SECONDS.

2 TURN POWER TO STBY BEFORE REINSTALLING EACH ASSEMBLY, THEN TURN POWER TO ON TO CHECK DISPLAY

Figure 6D-7. Core Subsystem Troubleshooting Flow Diagram

6D-19. DATA ACQUISITION SUBSYSTEM TROUBLESHOOTING PROCEDURE

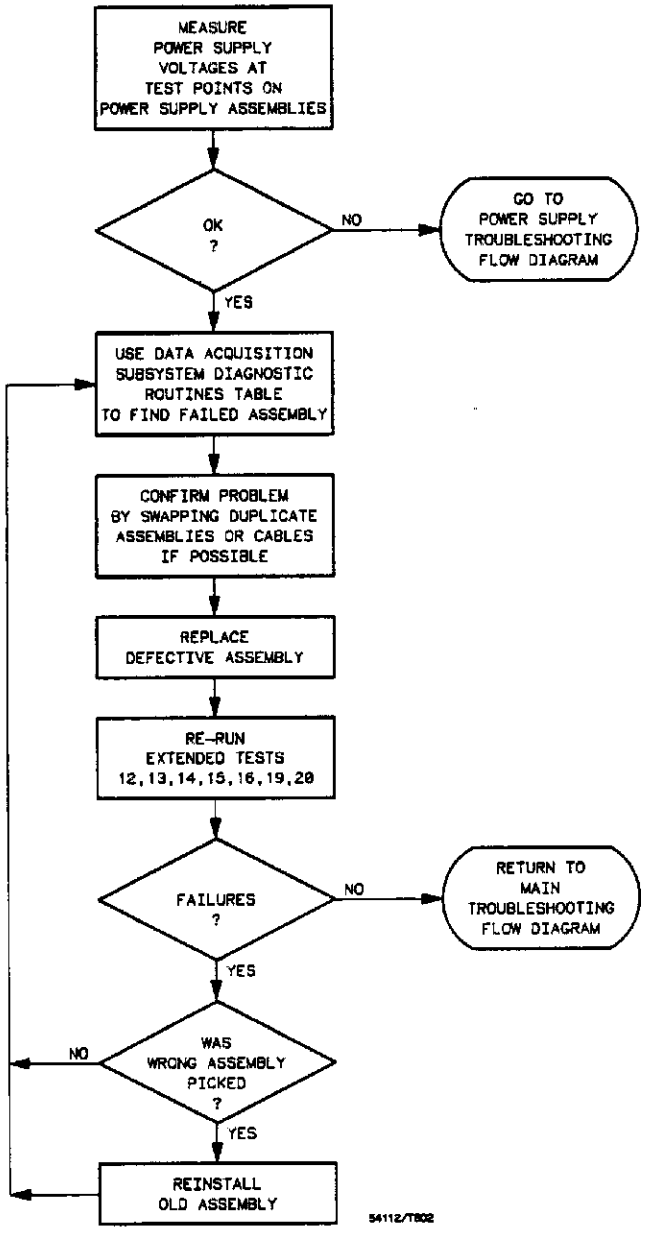


Figure 6D-8. Data Acquisition Subsystem Troubleshooting Flow Diagram

6D-20. Data Acquisition Subsystem Diagnostic Routines

The Data Acqusition Diagnostics consists of several tests:

- Timebase Tests
- Acquisition Control Tests
- Acquisition Memory Tests
- Acquisition System Tests
- Trigger Tests
- State Trigger Tests
- Extended Tests

The tests are arranged in a meaningful order. The more complex and complete tests are located at the end of the group. The software executes the tests in numerical order.

Troubleshooting the Data Acquisition Subsystem is based on the Data Acquisition Subsystem Diagnostic Routines table, table 6D-3. The areas tested are shown across the top of the table. Various letters indicate a function of the card in a particular test. If a particular card is not present, its presence test fails, and the tests for that assembly are skipped. Test loop numbers are shown at the top and bottom of the table.

Information about instrument loop errors is accessed by pressing ***Utility***, ***Test Menu***, and ***Display Errors***. The display shows only the numbers of failed loop tests. Once an error appears on the Display Errors screen the error will stay until the power is cycled or until extended test 12 is run, even if the fault has been corrected.

NOTE

It is best to disconnect all front panel inputs from the instrument while using the self-test loops for troubleshooting. Some of the loops can be affected by a signal at a front panel BNC.

6D-21. How To Use The Diagnostic Routines Table

The table on the next pages correlates diagnostic loop test and extended test results to replaceable assemblies. It provides a technique for rapidly and correctly identifying an assembly to replace when loop failures occur. Most true hardware failures result from the failure of a single circuit element on a single assembly, though they can cause several loops to fail. The correct use of this table allows the technician to confidently determine the most probable cause of the observed loop failures.

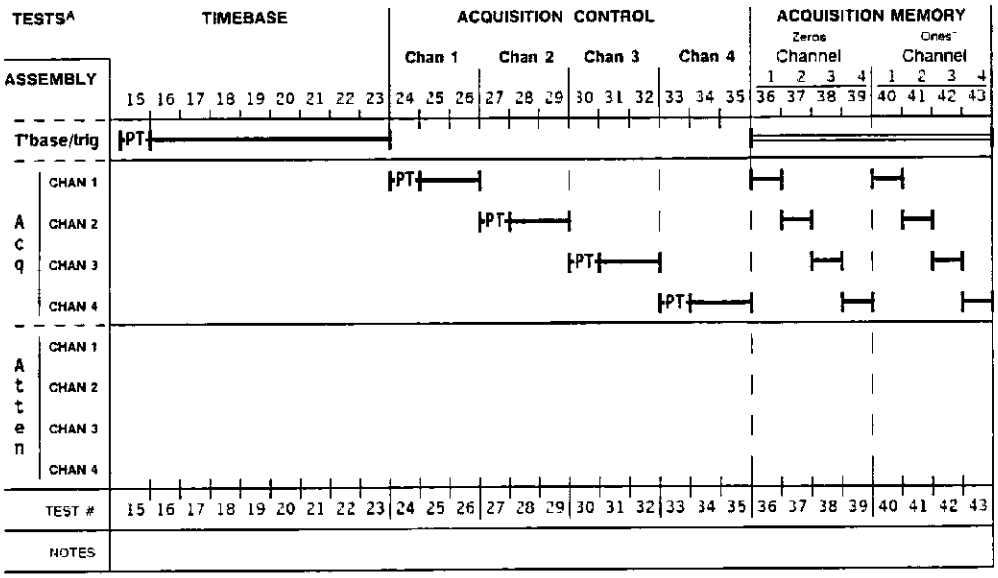
After running the powerup self-tests (or extended test 12) and extended tests 13, 14, 15, 16, 19, and 20, you will have a set of test results, consisting of a "pass" or "fail" for each loop. It is important to emphasize that passing a loop test is valuable information, even though only failures are displayed. If a loop is not listed in the "Loop failures" list on the DISPLAY ERRORS screen, it has passed its most recent test.

Comparing these test results to the information in the table often yields an immediate, clear indication of the most probable cause of failure. For example, when loops 25, 26, 36, 40, and 44-47 have failed, and all other loops and extended tests have passed, the most probable cause is a failure of the channel 1 acquisition assembly. This can be verified by swapping the channel 1 and channel 2 acquisition assemblies and running the tests again. Now loops 28, 29, 37, 41, and 48-51 should fail.

In some cases, several assemblies appear to be suspect from looking at the list of loop failures. In such cases, noting which loops have successfully completed before the first failure often allows you to conclude that at least part of one of the suspect assemblies is working. For example, when only loops 44 and 46 fail, the Timebase/trigger, channel 1 Acquisition, and channel 1 Attenuator assemblies are suspect. However, loops 15-23, 36-43, 45, and 47-68 which test the timebase/trigger have passed. This means initial attention should be directed away from the Timebase/trigger and toward the Attenuator and Acquisition assemblies.

Extended test 20 can help verify the cabling connecting the Attenuator assembly to the channel 1 Acquisition assembly.

Table 6D-3. Data Acquisition Subsystem Diagnostic Routines



KEY:

|PT| Presence test. If the diagnostic software fails to find the assembly, this loop fails and all other self tests that include this assembly are skipped.

This assembly must work for the test to be successful. The test will be skipped and will not show a failure if the assembly is not present.

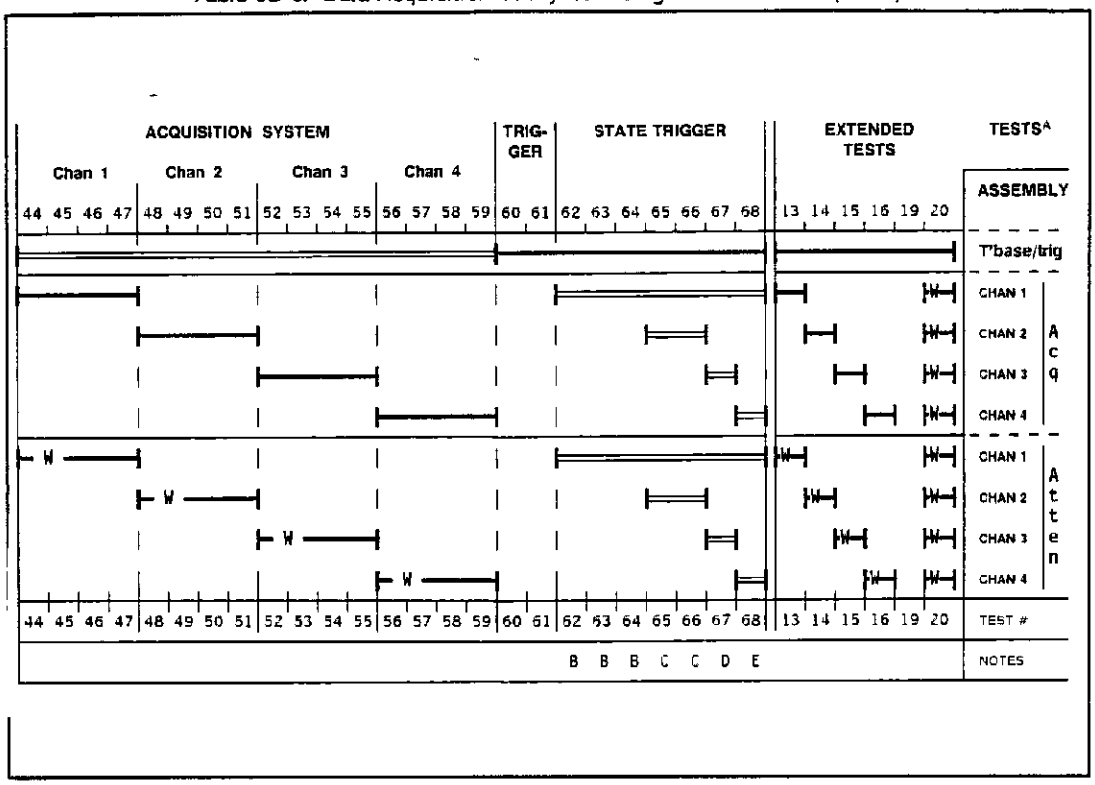
This assembly is involved in the test and must be working, but it is not likely the source of a problem if it has passed earlier tests.

|W| This assembly must work for the test to be successful. However, in this test there is no presence test for this assembly; the software assumes that it is there. If the assembly is not present, then the loop will fail just as if the assembly functions failed.

NOTES:

A. The Microprocessor, I/O, and Color Display assemblies must work for these tests to be valid.
B. This test will not run if loops 45 or 61 fail.
C. This test will not run if loops 45 or 49 fail.
D. This test will not run if loops 45 or 53 fail.
E. This test will not run if loops 45 or 57 fail.

Table 6D-3. Data Acquisition Subsystem Diagnostic Routines (con't.)



Extended tests 13 and 19 may help isolate between a channel or Timebase/trigger failure.

It may then help to swap the channel 1 and channel 2 Acquisition or Attenuator assemblies. If loops 48 and 50 fail (channel 2 loops), the failure has been further isolated.

If unexpected failures, or no changes result from swapping two assemblies, the cause is probably elsewhere. Factory experience has shown that careful rechecking of the interconnections of the swapped assemblies, or restoring the orginal setup and swapping related assemblies (the ones not swapped in the example immediately preceeding), are the most effective courses in this situation.

Sometimes the loop failures will not make any sense at all. Try The Core System Plus One (following) to isolate individual assemblies into a "suspect bad" or "known good" status.

If the failure still cannot be isolated, more information is available from the status fields for each loop, and can be analyzed by the factory. If you can not resolve your loop test results, we encourage you to call your nearest HP Service Center. They will help you or obtain information from the factory to resolve the problem.

6D-22. The Core System Plus One

Occasionally, the indications from the loop errors, the extended tests and the display can be so confusing that it is difficult to determine where to start the trouble shooting process. When this happens, it's sometimes best to start with the Core System plus one other assembly. This means that all assemblies are pulled up except the I/O assembly, microprocessor assembly and one other assembly, usually the Timebase/trigger.

Always turn power OFF when pulling or seating assemblies, and be sure to use proper ESD precautions.

Once you get this system working with no loop errors associated with the Timebase/trigger assembly, then one Acquisition assembly can be reinserted. Again, check for associated loop errors with these particular assemblies.

Once a small system is successful the other Acquisition assemblies can be put down one at a time. Always rerun extended test 12 to write the current loop failures into display memory.

Another useful technique is to put the core system in place, plus one assembly, and check it. If it functions correctly, then remove that assembly and reinsert another assembly and check it. Using the diagnostic table you should be able to quickly draw some good conclusions about the status of all the assemblies in the system.

Note that if an assembly is not present, after it fails its presence test none of the remaining tests that include that assembly are run.

6D-23. Timebase Tests

Self Test Loops 15 - 23

These loops test the timebase functions of the Timebase/trigger assembly. They are very independent loops, so if any are failing this assembly is most certainly the cause.

If the Timebase/trigger assembly presence test fails none of these tests will be run. Additionally, no other test loops that require use of the Timebase/trigger assembly will be run.

LOOP	TEST
15	Timebase/trigger Presence
16	Pre-Trigger Delay Clock on the Timebase IC
17	Pre-Trigger Delay Time in the Timebase IC
18	Clear Coarse and Fine Interpolators
19	Fine Interpolator at 100 MHZ
20	Fine Interpolator at 200 MHZ
21	Coarse Interpolator on the Timebase IC
22	Post Trigger Delay Time
23	Event Delay

6D-24. Acquisition Control Tests — Self Test Loops 24 - 35

In this group there are four sets of three tests each, one set for each channel.

TEST / CHANNEL	Assembly Presence	Preamp Control Register	Solenoid Register
Chan 1	24	25	26
Chan 2	27	28	29
Chan 3	30	31	32
Chan 4	33	34	35

ASSEMBLY PRESENCE TEST

Tests for the presence of the Acquisition assembly. If an assembly is not present or does not respond to a poll, the test fails. If the presence test fails, the rest of the loops that require that assembly to be present are not run.

PREAMP CONTROL REGISTER TEST

These loops check the ability of the preamp control registers to accept the values the CPU programs into them. This is done by toggling each bit in the control string and reading the status register on the Acquisition assembly to see if it changed. The test checks only that the register latched the data, not that it is actually being received by the Attenuator assembly.

SOLENOID REGISTER TEST

These loops are identical to the preamp control register tests except that the solenoid control registers are checked.

6D-25. Acquisition Memory Tests — Self Test Loops 36 - 43

There are two sets of tests in this group of loops. The first set tests that "0"s (zeros or low state) can be stored in all acquisition memories. The second set tests for "1"s (ones or high state). Acquisition memory is located on each of the Acquisition assemblies.

Four loops, 36 through 39, test for the ability of the memories of channels 1 through 4 respectively to store all "0"s. Data is written directly into memory through special circuitry.

Loops 40 through 43 test channels 1 through 4 respectively for ability to store "1"s. The tests are performed in the same way as the test for "0"s.

"0"s (low state) Test		"1"s (high state) Test	
LOOP	**CHANNEL**	**LOOP**	**CHANNEL**
36	1	40	1
37	2	41	2
38	3	42	3
39	4	43	4

6D-26. Acquisition System Tests — Self Test Loops 44 - 59

Four sets of four test loops check several functions of the acquisition system. There is one set for each channel. The sets are identical except for the channel tested. The table shows a cross-reference between tests, channels, and loop numbers.

TEST / CHANNEL	Cal/Offset DAC	Trig Lvl/Sens DAC	Gain Vern DAC	Analog Dither Flip-Flop
Chan 1	44	45	46	47
Chan 2	48	49	50	51
Chan 3	52	53	54	55
Chan 4	56	57	58	59

GENERAL

Use of these loops requires that an acquisition be taken. This means that the Timebase/trigger assembly must have working timebase functions. Loops 16 through 23 test those timebase functions so if they pass, the timebase functions of the timebase/trigger should be working well enough for loops 44 through 59 to run.

CAL/OFFSET DAC TEST

The Cal/offset DAC is a dual purpose DAC used to perform firmware calibration or provide dc offset, depending on the instrument mode.

These test loops test the data acquisition path from the Attenuator assembly preamp through to the acquisition memory.

First the test disables the dither circuitry. It starts an acquisition cycle and during the acquisition ramps the Cal/offset DAC from 0 (zero) up to its maximum output voltage. When the DAC reaches maximum, the acquisition memory is read. The test looks for the minimum and maximum voltages and checks for a linear ramp.

Troubleshooting these loops would involve first swapping the Acquisition assembly with that of a working channel, then the attenuator if necessary.

TRIGGER LEVEL DAC AND TRIGGER SENSITIVITY DAC TESTS

The trigger level DAC sets the nominal trigger level. The trigger sensitivity DAC sets gain in the trigger circuitry on the Attenuator assembly preamp hybrid.

These loops tests the trigger sensitivity of the channels. The test checks a signal path from the Attenuator assembly preamp through the trigger circuitry on the Timebase/trigger assembly.

The test compares trigger sensitivities for two different trigger gains. The sensitivity for high gain should be greater than that for a lower gain.

To determine the sensitivity for high gain, the loop sets the trigger level DAC to a median value and the trigger sensitivity DAC to the maximum value. The Cal/offset DAC is then ramped up from 0 V

until a trigger occurs and the offset level is recorded. The offset DAC is then set to maximum and ramped down until another trigger occurs and the offset level is again recorded. The difference between the two levels is the sensitivity for high gain.

To determine the sensitivity for low gain, the trigger sensitivity DAC is set to a median value (gain) and the process is repeated. The sensitivity at high gain should be a smaller value than that at low gain.

The DAC's are separate for each channel and trigger paths are separate until they reach the Timebase/trigger assembly. Trigger paths are combined on the Timebase/trigger so a failure of one trigger path may be a failure in an attenuator preamp or a failure of trigger functions on the Timebase/trigger assembly. A failure on the Timebase/trigger is less likely so the channel path should be checked first when only one channel is failing this test.

GAIN VERNIER DAC TEST

The gain vernier DAC sets the channel gain on the Attenuator assembly preamp hybrid.

These loops test function of the gain vernier DAC. With a given instrument setup, an acquisition taken with the vernier DAC at maximum should give a higher output from the ADC than an acquisition taken with the DAC at a middle value.

The trigger level is at zero, the trigger sensitivity is maximum, and the cal/offset DAC is at a high value. Since no triggers are present, acquisitions are initiated by auto-triggering.

ANALOG DITHER FLIP-FLOP TEST

There are two dither functions in the HP 54112D, analog dither and digital dither. Analog dither influences the analog signal before digitizing.

This test checks the analog dither function.

The dither circuitry is turned off and the cal/offset DAC is adjusted until a level is found that produces a 50-50 distribution between two q-levels in the digital output of the ADC. The dither is turned on. The ADC output is read and should show a change in the q-level distribution caused by the dither.

This test is susceptible to noise and can fail if a connection is on any of the front panel inputs or if the instrument is in a noisy environment. Failures during power-up do not result in a "Powerup Self Test Failed" message because of the noise susceptibility. If there was a failure during powerup however, the failed loop will be listed in the Loop Failures section of the Display Errors menu. It may be necessary to run a manual test of the loop to confirm the failure.

6D-27. Trigger Tests — Self Test Loops 60, 61

These two loops test trigger functions of the Timebase/trigger assembly.

LOOP 60 TIME DELAY TEST

Loop 60 disables the all trigger inputs and sets delay to a long value. False trigger events are created and a software clock times the delay between trigger events.

This test is nearly identical to loop 23.

LOOP 61 EXTERNAL TRIGGER TEST

Loop 61 checks the function of the rear panel external trigger input. It slews the external trigger level DAC and checks for the simulated trigger transitions.

6D-28. State Trigger Tests — Self-Test Loops 62 - 68

These loops test the Timebase/trigger assemblies' ability to recognize various state trigger patterns. These loops are highly dependent on the trigger outputs of the Attenuator assemblies; therefore, if loops 45, 49, 53, or 57 (trigger level/sensitivity DAC) fail or loop 61 (external trigger level DAC) fails, some of these tests may not be executed.

LOOP	TEST
62	Trigger on Pos edge of CHAN 1 when -XXXH pattern is present.
63	Trigger on Pos edge of CHAN 1 when -XXXL pattern is present.
64	Trigger on Pos edge of CHAN 1 when -XXXL pattern is not present.
65	Trigger on Pos edge of CHAN 1 when -HXXX pattern is present.
66	Trigger on Pos edge of CHAN 2 when H-XXX pattern is present.
67	Trigger on Pos edge of CHAN 1 when -XHXX pattern is present.
68	Trigger on Pos edge of CHAN 1 when -XXHX pattern is present.

6D-29. Extended Tests

Not all Extended Tests are of use to field service personnel. Tests 11 and 12 can be used for service. Tests 13-16, 19, and 20 are part of the table and they have the most use for field service.

The extended tests must be individually executed by the service person. The Extended Tests are part of the Test Menu. To select a test, press ***Extended Test***, ENTER the test number, and press ***Start Test***. The results of the test appear in a few seconds. To exit the test, press ***Stop Test***. Errors or problems appear in red on the screen after the test.

TESTS 0 - 9. These tests have factory use only.

TEST 10. Test 10 repeats loops 6-9 continually. It is similar to the test that runs when all of the acquisition boards are removed. This is an alternative to removing the boards; however it is usually better to remove the boards while troubleshooting the core system because the CPU interface to the data acquisition system is eliminated.

TEST 11. Extended Test 11 is not covered in the table. It is used to verify that all front panel keys and RPG are working. When the test is entered and initiated a keyboard mockup is displayed on the CRT. The mockup consists of boxes corresponding to each key on the front panel. A box lights when it's key is pressed. The RPG mockup consists of a set of radial lines representing a circle. When the RPG is rotated, an O cursor rotates around the circle.

To exit this test at any time the third key from the top, along the right edge of the display, must be pressed twice.

TEST 12. Test 12 is not part of the diagnostic table. Test 12 resets the system and initiates the powerup self test. If the advisory message "Powerup Self Test Failed" should appear on the display, the failing loops may be found by pressing ***Utility***, ***Test Menu***, then ***Display Errors*** keys.

TESTS 13 - 16. These are missing codes tests for the channel acquisition memory. They check for stuck bits in the acquisition circuitry. The offset DAC is incremented slowly and the output of the ADC is checked for proper progression of codes, from 000000 to 111111. Tests 13, 14, 15, and 16 test channels 1, 2, 3, and 4 respectively.

TEST 17. Has factory use only.

TEST 18. This test is for factory use. It slews all of the DAC outputs so that they can be checked for smooth outputs. Checking DAC outputs is only usefull for component level troubleshooting which is not supported on this instrument.

TEST 19. Test 19 evaluates the internal clock rates of the Timebase IC.

TEST 20. Test 20 uses the state trigger path to determine if the pre-amps are cabled properly. This test also checks the FET input. If a problem exists in the signal path in front of the FET, test 20 will not show a defective input.

TEST 21. This test serves two functions. First, it latches the front panel CAL signal in its high state, +800 mV dc. The cal signal can then be be measured for a performance test or measured and adjusted as in the adjustment procedures.

Test 21 also outputs a derivative of the acquisition sample rate to the Timebase Cal output on the rear panel. The menu describes steps to take to measure this signal but this part of test 21 has no use at this time.

6D-30. FRONT END TROUBLE-SHOOTING

Once all loop errors and extended test failures have been eliminated, some symptoms may persist. Most of the remaining problems will be found in the front-end subsystem, the attenuators. Below are identified some common symptoms and their causes, and procedures to ensure that the front end subsystem is functioning properly.

6D-31. Remaining Symptoms

PROBE OR OVERLOAD SENSE FAILURE

Probe and overload sense is conducted to the Acquisition assembly through a three-wire cable. The cable can get pinched between the frame and attenuator assembly and become grounded. If the overload wire is grounded the 50Ω input resistance will be out of specification and overload sense will not work.

If the probe sense wire is grounded the instrument will operate as if that channel has a 10:1 probe attached to it. The vertical scaling may be wrong or the menus will not allow access to the 50 ohm termination (the softkey selecting 50 ohms will not be displayed).

The cable is part of the attenuator. If a wire is pinched, repairing it with tape will be less expensive than replacing the attenuator.

INSTRUMENT WON'T TRIGGER AFTER TRIGGER CAL, OR TRIGGER CAL WON'T COMPLETE (Trigger Cal takes about 10 minutes).

Most probable cause: trigger output failure from an attenuator assembly. The trigger signal may be good enough to pass self tests but not good enough for operation.

To verify, apply a signal to the suspect attenuator and view the TCLOCK+ output on another oscilloscope. With a square wave input, such as the front panel CAL signal, the trigger signal out of the attenuator should be a square wave with approximately 50% duty cycle. You can use cables and adapters from the HP 54100 Family Support Kit to connect the trigger to the oscilloscope. If problems persist, replace the failed attenuator assembly.

6D-32. Checkout Procedure

If an attenuator assembly has been replaced, or if other front-end problems are suspected, use this check-out procedure to verify operation of the front end subsystem. Normally, it is not needed unless the front-end is suspected of failure and loop failures do not isolate the problem.

SIGNAL TESTS

1. Do a one-key power up.
2. Do the software calibrations. Perform Vertical Cal, Probe Tip Cal, Offset Cal, and Trigger Cal. Troubleshoot any cal failures before proceeding.
3. Connect a known signal to the channel inputs to be tested. If only one channel is suspected of failure, connect the signal to a functioning channel also, to provide a basis for comparison.
4. Press AUTOSCALE. All channels having signal inputs should be displayed. The result should be similar traces of the signal. Compare sensitivities, offset values and other parameters for clues about failures. Check for proper probe attenuation factor.
5. If the instrument does not autoscale properly, the most probable cause is an unrecognized failure of trigger calibration. Check for improper cabling as a potential cause of this failure, particularly the solenoid control cables. Try the "Click Tests" that follow this procedure.
6. If there is still a problem, the most probable cause of failure is an unrecognized probe-tip calibration failure, unless other loops have begun to fail. Check for other loop failures and if any are found, refer to the Data Acquisition System Troubleshooting Procedures. If none are found, perform a Probe Tip Cal. If this fails to solve the problem, contact HP Customer Support.

CLICK TESTS

1. Check to see that the 50 ohm/1Mohm switches work. Remove probes from front panel, and switch between 50 and 1M ohm at each channel menu. A click should come from the attenuator assembly as impedance is switched.

2. If there is no click, check the attenuator cabling for loose, miscabled, or detached connectors, and for debris such as loose screws or other conductive material on top of the attenuators.

3. Check the operation of the vertical sensitivity solenoids on the channel attenuators by varying the vertical sensitivity on each channel, as follows:

   Be sure the probes are disconnected and attenuation factors are 1:1. With a single display, and when using the increment/decrement (arrow) keys, clicks will occur on the channel attenuator assemblies when switching between vertical sensitivities of 20 and 50 mV/div and between 200 and 500 mV/div.

   Normally a click is heard when switching both ways through these transitions. Different circuitry is used when switching up than when switching down. However, if one switching direction is faulty the solenoid will stay in the first direction it switches to and no clicks will be heard at that range transition. If any clicks are not present, check cabling and look for debris in the solenoids.

   It is usually not be necessary to remove attenuators while determining if the attenuator, cable, or control is causing a failed click test. Use swapping techniques to isolate the fault. Swap one end of the solenoid cables (connected at the top of the Acquisition assembly) and try to control the suspect attenuator with a different channel menu; or swap the entire cable.

6D-33. Attenuator Outrigging

It is possible to quickly check the effect of replacing an attenuator by using the following procedure to outrig a substitute. The additional required cables are in the 54100 Family Support Kit.

NOTE

Use the cabling diagram on the top cover of the instrument or the end of section 6A to recable the instrument during or after this procedure.

1. Turn off power and remove covers.

2. Connect three Coaxial Cables to the good attenuator assembly.

3. Remove the Attenuator Power Cable from suspect assembly at the attenuator and Acquisition assemblies.

4. Extend the Power Cable using the extender cable from the support kit.

5. Connect the extended power cable between the good attenuator and the Acquisition assembly.

6. Disconnect the Solenoid Cable at the suspect attenuator and connect to the good attenuator.

7. The probe sense and input overload cable is difficult to remove and connect at the Acquisition assembly. It may not be necessary to connect the cable from the substitute attenuator, depending on the symptoms and methods being used to determine the failure. If necessary, disconnect the cable from the suspect attenuator and connect the one from the substitute.

8. Connect the signal and trigger coaxial cables to the proper locations on the Acquisition and Timebase/trigger assemblies.

9. Verify proper operation.

6D-34. HINTS, TRICKS, AND ARCANA

6D-35. Multiplicity of Function

Many parts of the HP 54112D are duplicated. This allows part swapping to troubleshoot for a defective assembly. There are four Attenuator assemblies and four Acquisition assemblies. Multiple inputs and outputs on these assemblies allow part swapping or recabling to be effective troubleshooting tools.

CLOCK SIGNALS

Four pairs of acquisition clock signals (FFCLKs) originate at the Timebase/trigger assembly. If the Timebase/trigger assembly is suspected as a probable cause for a defect and only one channel is affected, try to switch the clock outputs to the Acquisition assemblies, and see whether the symptoms change. If the symptoms change to a different channel the problem would be in the cable or on the Timebase/trigger assembly. The 54100 Family Support Kit includes a long clock cable that can be used as a substitute for troubleshooting.

The converse is also true, if the problem stays with the same channel, then the Acquisition assembly is the most suspect.

CONNECTORS AND CABLES

The many identical cables on the HP 54112D can be interchanged to test suspected defective cables.

6D-36. System Interface Bus

All the slots in the mother board are identical and have identical voltages or signals associated with each pin. This means that defective motherboard slots can be found by rearranging the assemblies in the card cage. The assemblies have been arranged in the order that gives the lowest system noise, but any of the assemblies can work in any of the slots.

Rearranging the assemblies is of course limited by the cabling, which may not accomodate some arrangements.

HEWLETT PACKARD

SERVICE MANUAL

HP 54120T
DIGITIZING OSCILLOSCOPE

SERIAL NUMBERS

This manual applies directly to instruments
prefixed with serial number:

HP 54120A=2734A
HP 54121A=2802A

For additional information about serial numbers see
INSTRUMENTS COVERED BY THIS MANUAL
in Section I.

Manual Part No. 54120-90902
Microfiche Part No. 54120-90802

Printed in U.S.A. November 1987
Update 1 January 1988
Update 2 May 1988

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CWA584

X-RAY RADIATION NOTICE

ACHTUNG Model **54111D/54112D/54120A** **WARNING**

Während des Betriebs erzeugt dieses Gerät Röntgenstrahlung. Das Gerät ist so abgeschirmt, daß die Dosisleistung weniger als 36 pA/kg (0,5 mR/h) in 5cm Abstand von der Oberfläche der Katodenstrahlröhre beträgt. Somit sind die Sicherheitsbestimmungen verschiedener Länder, u.A. der deutschen Röntgenverordnung eingehalten.

Die Stärke der Röntgenstrahlung hängt im Wesentlichen von der Bauart der Katodenstrahlröhre ab sowie von den Spannungen, welche an dieser anliegen. Um einen sicheren Betrieb zu gewährleisten, dürfen die Einstellungen des Niederspannungs— und Hochspannungsnetzteils nur nach der Anleitung in Kapitel Einstellvorschriften des Service Handbuches vorgenommen werden.

Die Kathodenstrahlröhre darf nur durch die gleiche Type ersetzt werden. (Siehe Kapitel Ersatzteile für HP-Teilenummern.)

Das Gerä ist in Deutschland zugelassen unter

der Nummer **BW/218/86/ROE**

When operating, this instrument emits x-rays; however, it is well shielded and meets safety and health requirements of various countries, such as the X-ray Radiation Act of Germany.

Radiation emitted by this instrument is less than 0.5 mR/hr at a distance of five (5) centimeters from the surface of the cathode-ray tube. The x-ray radiation primarily depends on the characteristics of the cathode-ray tube and its associated low-voltage and high-voltage circuitry. To ensure safe operation of the instrument, adjust both the low-voltage and high-voltage power supplies as outlined in the Adjustments Section of the Service Manual.

Replace the cathode-ray tube with an identical CRT only Refer to the Replacement Parts Section for proper HP part number.

Number of German License: **BW/218/86/ROE**

GEWERBEAUFSICHTSAMT STUTTGART

- Zentrale Stelle für Sicherheitstechnik und Vorschriftenwesen in Baden-Württemberg -

Gewerbeaufsichtsamt Hegerstr. 22 Postfach 703 7000 Stuttgart 1

Hewlett-Packard GmbH
Herrenberger Straße 110

7030 Böblingen

Stuttgart, den 02.06.1986
Fernsprecher
(0711) 205 01 (Behördenzentrum)
Durchwahl 2050 - 4798
Aktenzeichen: Z 5108/Hewlett-Packard/Ws/Vg
(Bitte bei Antwort angeben)

Betr.: Durchführung der Röntgenverordnung (RöV)
hier: Bauartzulassung gem. § 7 Abs. 2 RöV

Bezug: Ihr Antrag vom 22.05.1986; PSD US-ab

Nachtrag 1

zum Zulassungsschein Nr. BW/218/86/Rö

Aufgrund des § 7 Abs. 2 der Röntgenverordnung vom 1.3.1973 (BGBl. I S. 173) wird die der Firma Hewlett-Packard GmbH, Herrenberger Straße 110, 7030 Böblingen, erteilte Zulassung Nr. BW/218/86/Rö vom 16.01.1986 wie folgt erweitert:

Gegenstand:	Digital-Oszilloskop
Firmenbezeichnung:	HP Typ 54 111 D HP Typ 54 112 D HP Typ 54 120 A
Bauartunterlagen:	Service Manuals Nr. 54 111 - 90 902 vom 21.94.86 Nr. 54 112 - 90 902 vom 24.04.86 Nr. 54 120 - 90 902 vom 26.04.86

Die für den Strahlenschutz wesentlichen Merkmale entsprechen der bereits zugelassenen Ausführung.

Typenbezeichnung der Bildröhre, Auflagen, Hinweise und Befristung ergeben sich aus dem Zulassungsschein Nr. BW/218/86/Rö vom 16.01.1986.

Dieser Nachtrag gilt nur im Zusammenhang mit dem vollständigen Text des o.g. Zulassungsscheins.

Reutter

GEWERBEAUFSICHTSAMT STUTTGART

Dieses Gerät wurde nach den Auflagen der Zulassungsbehörde einer Stückprüfung unterzogen und entspricht in den für den Strahlenschutz wesentlichen Merkmalen der Bauartzulassung. Die Beschleunigungsspannung betragt maximal 22,3 kV.

Hewlett-Packard
1900 Garden of the Gods Road
Colorado Springs
Colorado 80907, USA

GEWERBEAUFSICHTSAMT STUTTGART

- Zentrale Stelle für Sicherheitstechnik und Vorschriftenwesen in Baden-Württemberg -

Gewerbeaufsichtsamt · Jägerstr. 22 · Postfach 703 · 7000 Stuttgart 1

Stuttgart, den 16.01.1986

Fernsprecher
(0711) 20501 (Behördenzentrum)
Durchwahl 2050 - 4798

Aktenzeichen: Z 5108/HP/Ws/Hh
(Bitte bei Antwort angeben)

Firma
Hewlett Packard GmbH
Herrenberger Str. 110/130

7030 Böblingen

Zulassungsschein Nr. BW/218/86/Rö

Gemäß § 9 der Röntgenverordnung vom 01.03.1973 (BGBl. I S. 173) wird die Zulassung der Bauart durch den Bauartzulassungsbescheid vom 16.01.1986 mit Aktenzeichen Z 5108/HP/Ws/Hh für den nachfolgend aufgeführten Störstrahler bescheinigt:

Gegenstand	:	Digital-Oszilloskop
Firmenbezeichnung	:	HP Typ 54110D
Bildröhre	:	Sony Typ M23 JHU 15X
Hersteller	:	Hewlett-Packard 1900 Garden of the Gods Road Colorado Springs Colorado 80907, USA
Betriebsbedingungen	:	Hochspannung: max. 22,3 kV Strahlstrom: max. 0,4 mA
Zulassungskennzeichen	:	BW/218/86/Rö

Die Bauartzulassung ist befristet bis 16.01.1996.

Für den Strahlenschutz wesentliche Merkmale

1. Die Art und Qualität der Bildröhre,
2. die der Hochspannungserzeugung und -stabilisierung dienenden Bauelemente.

Auflagen:

1. Die Geräte sind bezüglich der für den Strahlenschutz wesentlichen Merkmale entsprechend den vorgestellten und geprüften Mustern und Antragsunterlagen herzustellen.

2. Die Geräte sind einer Stückprüfung daraufhin zu unterziehen, ob sie bezüglich der für den Strahlenschutz wesentlichen Merkmale der Bauartzulassung entsprechen.

   Die Prüfung muß umfassen:

   a) Kontrolle der Hochspannung an jedem einzelnen Gerät,

   b) Messung und Dosisleistung nach Festlegung im Bauartzulassungsbescheid.

3. Die Herstellung und die Stückprüfung sind durch den von der Zulassungsbehörde bestimmten Sachverständigen überwachen zu lassen.

4. Die Geräte sind deutlich sichtbar und dauerhaft mit dem Kennzeichen

   BW/218/86/Rö

   zu versehen sowie mit einem Hinweis folgenden Mindestinhalts:

   "Die in diesem Gerät entstehende Röntgenstrahlung ist ausreichend abgeschirmt.
   Beschleunigungsspannung maximal 22,3 kV."

Hinweis für den Benutzer des Geräts:

Unsachgemäße Eingriffe, insbesondere Verändern der Hochspannung oder Auswechseln der Bildröhre können dazu führen, daß Röntgenstrahlung in erheblicher Stärke auftritt. Ein so verändertes Gerät entspricht nicht mehr dieser Zulassung und darf infolgedessen nicht mehr betrieben werden.

Reutter

GEWERBEAUFSICHTSAMT STUTTGART

Dieses Gerät wurde nach den Auflagen der Zulassungsbehörde einer Stückprüfung unterzogen und entspricht in den für den Strahlenschutz wesentlichen Merkmalen der Bauartzulassung. Die Beschleunigungsspannung beträgt maximal 22,3 kV.

Hewlett-Packard
1900 Garden of the Gods Road
Colorado Springs
Colorado 80907, USA

SAFETY CONSIDERATIONS

GENERAL - This is a Safety Class I instrument (provided with terminal for protective earthing)

OPERATION - BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings) In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNING

- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord The mains plug shall only be inserted in a socket outlet provided with a protective earth contact The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply

SAFETY SYMBOLS

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates hazardous voltages

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

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GENERAL INFORMATION

SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION

This service manual contains information necessary to test, adjust and service the Hewlett-Packard 54120T Digitizing Oscilloscope. The HP 54120T is comprised of two major components. These are the HP 54120A Digitizing Oscilloscope Mainframe and the HP 54121A Four Channel Test Set. Throughout this manual when HP 54120T is used, it includes the HP 54120A and the HP 54121A. The mainframe will be referred to as the HP 54120A Mainframe. The test set will be referred to as the HP 54121A Four Channel Test Set.

This manual is divided into 10 sections as follows:

1 - General Information

2 - Installation

3 - Performance Tests

4 - Adjustments

5 - Replaceable Parts

6A - Disassembly

6B - Theory

6C - Service Menu Keys

6D - Troubleshooting

Information on operating, programming, and interfacing the HP 54120T is contained in the HP 54120T Operating and Programming Manual supplied with each instrument.

The "General Information" Section includes a description of the HP 54120T Digitizing Oscilloscope, its specifications, operating characteristics, general characteristics, safety considerations, instruments covered by this manual, options, accessories supplied, recommended test equipment, and X-ray license forms.

Also listed on the title page of this manual is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of this manual. Each microfiche contains up to 96 photo-duplicates of manual pages. The microfiche package also includes the latest Manual Changes supplement as well as pertinent Service Notes.

1-2. DESCRIPTION

The HP 54120T is a fully programmable 20 GHz, four channel, digitizing oscilloscope with a nine inch color display. The HP 54120T is capable of automated measurements, digital storage, and TDR measurements.

The color display of the HP 54120T provides many colors which are mapped to provide specific colors for specific display functions. For example, channel 1 is displayed in yellow, channel 2 in green, and error messages are displayed in red.

The HP 54120T contains extensive self-tests to ensure proper functioning of the oscilloscope. These self-tests are in addition to internal diagnostics that help locate faults efficiently and identify repairs, if a failure does occur.

1-3. SPECIFICATIONS

Table 1-2 lists the specifications for the HP 54120T. These specifications include the performance standards against which the oscilloscope is tested.

1-4. INSTRUMENT OPERATING CHARACTERISTICS

Table 1-3 lists the operating characteristics for the HP 54120T. These characteristics are not specifications but are typical characteristics included as additional information only.

1-5. GENERAL CHARACTERISTICS

Table 1-4 lists general characteristics, not specifications, but typical characteristics included as additional information only.

1-6. SAFETY CONSIDERATIONS

The appropriate sections contain safety information relevant to the service procedure it describes. Both the HP 54120T and this manual should be reviewed for safety markings and instructions before work is begun. Refer to the pages following the title page. They include a safety summary and safety considerations.

1-7. INSTRUMENTS COVERED BY THIS MANUAL.

The oscilloscope's serial number is on the rear panel. Hewlett-Packard uses a two-part serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter (0000A00000). The prefix is the same for all identical oscilloscopes and changes only when a modification is made that affects parts compatibility. The suffix differs for each oscilloscope. This manual applies directly to oscilloscopes with the serial prefix shown on the tiltle page.

For previous prefix numbers refer to appendix B. Appendix B contains instrument backdating information on what was changed for previous prefix numbers. **Do Not** use Appendix B as a reference for ordering replaceable parts. Backdated parts are usually obsoleted and directly replaced by new part numbers. Refer to the Replaceable Parts, Section 5, for which part numbers to use for ordering purposes.

1-8. OPTIONS

The following options are available for the HP 54120T:

Option 908 - Rack mount kit
Option 910 - Additional copies of operating manuals
Power cord options (see table 2-1)

1-9. ACCESSORIES SUPPLIED

The following accessories are supplied with the HP 54120T.

1 - Service manual
1 - *Getting Started Guide*
1 - Operating manual
1 - Programming manual
1 - Antistatic mat with wrist strap
1 - RF Accessory kit HP part number 54121-68701
5 - Connectors savers HP part number 5061-5311
5 - Coaxial shorts HP part number 0960-0055

Table 1-5 lists the RF Accessories.

1-10. ACCESSORIES AVAILABLE

The following accessories are available for the HP 54120T:

Accessory kit HP Model 54007A
6 GHz Probe kit HP Model 54006A

1-11. RECOMMENDED TEST EQUIPMENT

The test equipment recommended for maintaining the HP 54120T is listed in table 1-1 The three sections requiring test equipment are

- Performance Tests (section 3)
- Adjustments (section 4)
- Troubleshooting (section 6D)

1-12. SYSTEMIZING

At the factory the HP 54120A Digitizing Oscilloscope Mainframe and the HP 54121A Four Channel Test Set are calibrated together as a system called the HP 54120T. This system will meet all published specifications when shipped from the factory.

If the system is split up, (a different HP 54121A Four Channel Test Set is used with the HP 54120A Mainframe), the system will meet all specifications except for the dc accuracy specifications for single voltage and dual voltage markers. The single voltage marker specification will change

from ±0.4% of full scale ±2 mV
to ±1.0% of full scale ±2 mV.

The dual voltage marker specification will change

from ±0.8% of full scale
to ±2% of full scale.

To obtain the original factory specifications, perform the vertical adjustments in section 4, paragraphs 4-13 and 4-14, of this manual.

Table 1-1. Recommended Test Equipment.

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL	USE*
Synthesized ** sweeper	20 GHz, +12 dBm, -6 dBm, stability .25 ppm/yr, <-25 dBc harmonics	HP 8341	P,A
Power splitter	APC 3.5 connectors	HP 11667B	P,A
DMM	5 1/2 digits	HP 3478A	P,A
Power meter	20 GHz	HP 436A	P
Power sensor	20 GHz	HP 8485A	P
50 ohm load	APC 3.5 (m)	HP 909D	P,A
50 ohm load	APC 3.5 (f)	HP 909D/011	P
Calculator	Log base 10 function	HP 11C	P
6 dB pad	APC 3.5 connections	HP 33340C/006	P
10 dB pad	APC 3.5 connections	HP 33340C/010	P
20 dB pad	APC 3.5 connections	HP 33340C/020	P,A,T
RF amplifier	Gain 20 dB at 10 MHz flatness ±.7 dB, noise < 6 dB harmonic distortion -32 dB for 0 dB output	HP 8447A	P
Frequency synthesizer	100 KHz to 10 MHz frequency Stability .05 ppm/yr 200 mV output level sine and square wave outputs dc mode 1/2 volt output 100 μV resolution	HP 3325A/001	P,A,T
Oscilloscope	300 MHz general purpose	HP 54100A	T

* P=Performance Tests A=Adjustments T=Troubleshooting
** For adjustments and systemizing, only 250 MHz, +12 dBm, synthesized sine wave generator is required

Table 1-1. Recommended Test Equipment (continued).

ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER	USE*
Adapter BNC (m-m)		1250-0216	A
Adapter BNC (f) to SMA (m)	Quantity needed - 2	1250-1200	P,A
Adapter APC 3.5 (m-m)		1250-1864	P
Adapter APC 3.5 (f-f)	Neither end precise **	1250-1865	A
Adapter APC 3.5 (f-f)	26.5 GHz Both ends precise	1250-1865	P
Adapter APC 3.5 (m-f)	26.5 GHz Both ends precise	1250-1866	P,A
Adapter APC 3.5 (m-f)	26.5 GHz, Male end precise Quantity needed - 6	1250-1866	P,A
Adapter APC 3.5 (m-f)	26.5 GHz, Female end precise Quantity needed - 1	1250-1866	A
Adapter N (m) to APC 3.5 (m)		1250-1743	P
Adapter N (m) to APC 3.5 (f)	26.5 GHz	1250-1744	P,A
BNC Tee	1 male end 2 female ends	1250-0781	P,A,T
Coaxial cable APC 3.5 (m-f)	26.5 GHz	8120-4942	P,A
Coaxial cable APC 3.5 (m-m)	18 GHz Quantity needed - 3	8120-4948	P,A,T
Coaxial Cable BNC	Length - 48 inches Quantity needed - 2	10503A	P,A,T

* P=Performance Tests A=Adjustments T=Troubleshooting
** A precise connector is an APC 3.5 connector which has never been connected to an SMA connector or received any other physical damage

Table 1-1. Recommended Test Equipment (continued).

ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER	USE*
Coaxial short	APC 3.5 (f) short	1250-2127	P
Coaxial short	APC 3.5 (m)	1250-2128	P
Adapter banana to BNC (f)		1250-2277	P,A
Semi-rigid U cable	No substitute	54121-61601	P,A
Semi-rigid S cable	No substitute	54121-61602	P,A
20 ns delay line	APC 3.5 connectors both ends precise	Call HP service center for No.	P
Clip lead	Alligator to alligator	N/A	A
Jewelers screwdriver	.01 inches thick .04 inches long	N/A	A
Alignment tool	Non-metallic	8710-1355	A
Torque wrench	5 in/lb	8710-1582	P,A,T
Torque wrench	8 in/lb	8710-1765	P,A,T
* P=Performance Tests A=Adjustments T=Troubleshooting			

Table 1-2. Specifications

Channels (Vertical)

20 GHz Bandwidth available in average display mode only.
-3 dB dc to 20 GHz channels 2-4 (channel 1 is -3.5 dB at 20 GHz)
dc to 18 GHz channel 1

12.4 GHz Bandwidth available in either average or persistence display modes.
-3 dB dc to 12.4 GHz channels 1-4

20 GHz Transition Time available in average display mode only. (Calculated)
≤17.5 ps channels 2-4
≤19.4 ps channel 1

12.4 GHz Transition Time available in average or persistence display modes. (Calculated)
≤28.2 ps channels 1-4

12.4 GHz Maximum Noise (rms) persistence display mode.
≤1 mV channels 1-4

Scale Factor (full scale is 8 divisions)
Minimum 1 mV/div
Maximum 80 mV/div

dc Accuracy single voltage marker
Average mode ±0.4% of which is greater (full-scale or marker reading) ±2 mV
Persistence mode ±0.4% of full-scale ± 2 mv ±3.0% of (reading - channel offset)

dc Difference Voltage Accuracy with two voltage markers on same channel.
Average mode ±0.8% of which is greater (full-scale or Delta V reading)
Persistence mode ±0.8% of full-scale ±3.0% of reading

Programmable dc Offset
±500 mV channels 1-4

Inputs

Number	Four
Dynamic Range	±320 mV relative to channel offset
Maximum Input V	±2 V dc + ac peak (16 dBm)
Nominal Impedance	50 Ω
Percent Reflection	≤5% for 30 ps risetime
Connectors	3.5 mm (m)

Table 1-2. Specifications (continued)

TDR System

Risetime combined oscilloscope and TDR performance
≤45 ps (measured at 12.4 GHz bandwidth in average mode)

Flatness combined oscilloscope and TDR performance
≤±1% after 1 ns from edge
≤+5%,-2% to 1 ns from edge (measured at 12.4 GHz bandwidth in average mode)

Levels combined oscilloscope and TDR performance
Low 0 V ±2 mV
High 200 mV ±2 mV

Timebase (Horizontal)

Scale Factor full-scale is 10 divisions
Minimum 10 ps/div
Maximum 1 s/div

Delay time offset relative to trigger
Minimum 16 ns
Maximum 1000 screen diameters or 10 seconds, whichever is smaller

Time Interval Accuracy dual marker measurement
≤10 ps ±0.1% of reading

Time Interval Resolution
0.25 ps or .02 divisions, whichever is larger

Table 1-2. Specifications (continued)

Trigger-External Input Only

Sensitivity

dc to 100 MHz	40 mV peak-to-peak
100 MHz to 500 MHz	100 mV peak-to-peak

Pulse Width

1 ns ≥80 mV

Trigger Level Range

±1 V

Jitter trigger and timebase combined (one standard deviation)

≤5 ps + 5E-5 x delay setting

Trigger Input

Maximum Input V	±2 V dc + ac peak (16 dBm)
Nominal Impedance	50 Ω
Percent Reflection	≤10% for 100 ps risetime
Connector	3.5 mm (m)

Table 1-3. Operating Characteristics

Channels (Vertical)

Scale Factors: Adjustable from 1 mV/div to 80 mV/div in a 1-2-5-10-20-50-80 sequence from the RPG control or the increment decrement keys. Also adjustable over the range in 1 mV increments from the numeric keypad.

Attenuation Factors: Factors may be entered to scale the oscilloscope for external attenuators connected to the channel inputs.

Noise: Averaging reduces noise by $1+\sqrt{n}$ where n is the number of averages, until a system limitation of approximately 35 μV is reached.

Typical noise

Display Mode	Noise (RMS)
20 GHz bandwidth, Avg = 1	1.2 mV
20 GHz bandwidth, Avg = 256	80 μV
12.4 GHz bandwidth, Avg = 1	500 μV
12.4 GHz bandwidth, Avg = 256	35 μV
12.4 GHz bandwidth, persistence	400 μV

Channel-to-channel Isolation: 80 dB at 20 GHz

Timebase (Horizontal)

Delay Between Channels: The difference (up to 100 ns) in delay between channels can be nulled out in 1 ps increments to compensate for differences in input cables or probe length.

Reference Location: The reference point can be located at the left edge or center of the display. The reference point is that point where the time is offset from the trigger by the delay time.

Triggered Mode: Causes the scope to trigger synchronously to the trigger input signal.

Free Run Mode: Causes the scope to generate its own triggers at a user specified rate (between 15.3 Hz and 500 kHz). Used with the Channel 1 step generator for TDR and transmission measurements. The channel 1 step may also be used to trigger a device under test for viewing information prior to the trigger.

Table 1-3. Operating Characteristics (continued)

Trigger

Attenuation Factors: Factors may be entered to scale the oscilloscope for external attenuators connected to the trigger input.

Edge Trigger: Triggers on the positive or negative edge of the trigger source.

Display

Data Display Resolution: 501 points horizontally X 256 points vertically.

DATA DISPLAY FORMATS

Full screen: All channel displays are superimposed and are eight divisions high.

Split screen: With four graphs, channels are displayed separately and are two divisions high; or with two graphs, channels 1 and 3 are superimposed and channels 2 and 4 are superimposed and are four divisions high.

DISPLAY MODES

Persistence: The time that each data point is retained on the display can be varied from 300 ms to 10 seconds, or it can be displayed infinitely.

Averaging: The number of averages can be specified as powers of 2, up to 2048. On each acquisition, 1/n times the new data is added to (n-1) ÷ n of the previous value at each time coordinate. Averaging operates continuously, except over HP-IB where it terminates at the specified number of averages.

Graticules: The user may choose full grid, axes with tic marks, frame with tic marks, or no graticule.

Bandwidth: When in the average display mode, the user may select between a 20 GHz bandwidth and a 12.4 GHz bandwidth. The 12.4 GHz bandwidth reduces noise. The 20 GHz bandwidth is not available in the persistence display mode. See channel characteristics for bandwidths and noise levels.

Display Colors: Users may choose default colors or select their own colors from the front panel or over HP-IB. Different colors are used for display background, channels, functions, background text, highlighted text, advisories, markers, overlapping waveforms, and memories.

Table 1-3. Operating Characteristics (continued)

Programmability

Instrument settings and operating modes, including automatic measurements, may be remotely programmed by HP-IB (IEEE-488). HP-IB programming complies with IEEE 488.2 standards. The HP 54120T can be programmed to take data only at specified time points, or to return only measurement results, (i.e., tr, tf, frequency, etc.,) to speed up data acquisition.

Data Output Transfer Rate: 115 kbytes/s

Typical Measurement Times: 200-700 ms

Data Record Lengths:

Timebase Setting/Histogram Type	Number of points/record
10 ps/div ≤ time/div < 20 ps/div	100, or 400
20 ps/div ≤ time/div < 50 ps/div	100, 400, or 800
50 ps/div ≤ time/div < 200 ps/div	100, 500, or 1000
200 ps/div ≤ time/div ≤ 1 s/div	128, 256, 500, 512, or 1024
Voltage Histogram	256
Time Histogram	501

Histograms

Time and voltage histograms may be taken with a user-specified number of samples (between 100 and 655,000,000) within a user-specified voltage window (time histogram) or time window (voltage histogram). To accelerate throughput when taking voltage histograms, take samples only in the user-specified time window.

Distribution markers: Two markers, labeled Upper and Lower Distribution Limits, indicate the cumulative occurrences of samples from the edge of the display to a given time (time histogram) or voltage (voltage histogram).

Mean and Standard Deviation: Calculates the mean and standard deviation of a distribution on screen, or between the distribution limits, assuming a Gaussian distribution.

Table 1-3. Operating Characteristics (continued)

Measurement Aids

Markers: Dual voltage or time markers can be used for a variety of time and voltage measurements. Voltage markers can be assigned to channels, memories, or functions.

Automatic Level Set: Voltage markers may be preset to 10%-90%, 20%-80%, 50%-50%, or to user specified levels.

Automatic Edge Find: The time markers can be assigned automatically to any displayed edge of either polarity on any channel. The voltage markers establish the reference, on the edge, for the time markers in this mode.

Automatic Pulse Parameter Measurements: The HP 54120T automatically takes ten pulse parameter measurements, (as defined by IEEE standard 194-1977, "IEEE Standard Pulse Terms and Definitions"). The standard measurement thresholds are 10%, 50%, and 90%. The measurement modes are frequency, period, positive pulse width, negative pulse width, duty cycle, risetime, falltime, preshoot, overshoot, and RMS voltage, peak-to-peak voltage.

Waveform Math: Any two of seven waveform math operations may be assigned to two displayable math functions. The available operations are Plus, Minus, Invert, Versus, Max, Min, and Only. Max and Min, which define an envelope about the waveform, are only available in the persistence mode. The vertical channels, or any of the waveform memories can be used as operands for the waveform math. Function sensitivity and offset may be adjusted independently of the channel display settings.

Waveform Save: Four waveforms may be stored and displayed in four non-volatile waveform memories. Waveform memories are typically used in the average display mode. Screen displays may be stored in two volatile pixel memories. Pixel memories are typically used in the persistence display mode.

TDR System - normalized characteristics

Risetime: adjustable, allowable values based on timebase setting.
Minimum - 10 ps or .08 X time/div, whichever is greater
maximum - 5 X time/div

Flatness: ≤±.1%

Levels:
Low - 0 V ± 2 mV
High - 200 mV ±2 mV

Table 1-3. Operating Characteristics (continued)

Networks

REFLECTION MEASUREMENTS

Source: Measurements are made using the Channel 1 step source or a user-supplied external source.

Calibration: A reference plane is defined by calibrating the reflection channel with a short placed at the point where the device under test will be connected. The short calibration is followed with a 50 Ω calibration. These calibrations are used to derive the normalization filter.

Cursor: Reads out the percent reflection, impedance, time, and distance from the reference plane to the cursor. See note 1.

Percent Reflection: Automatically calculates the maximum and minimum percent reflection of the waveform shown on screen.

Normalization Filter: Applies a firmware digital filter to the measured data and stores the resulting waveform in memory 1. The risetime of the filter may be varied to allow the user to simulate the edge speeds which would be seen by the device under actual operation. Normalization also removes errors caused by discontinuities prior to the reference plane.

Note 1: Percent reflection measurements should be used to quantify reactive peaks and valleys of the TDR display. Impedance measurements are valid only for resistive, horizontal flat line TDR displays. Because the accuracy depends on the measurement being made, percent reflection and impedance accuracies are not specified. Percent reflection and impedance measurements are ratios of voltage measurements whose accuracies are specified.

Percent Reflection (Rho) = (Vcursor - Vtop)÷(Vtop - Vbase)

Impedance (Z) = 50 Ω X (1 + Rho)÷(1-Rho)

Vcursor = voltage at the cursor
Vtop = high level of calibration reflected step and is determined during the reflection calibration.
Vbase = low level of calibration reflected step and is determined during the reflection calibration.

Distance measurements are subject to the accuracy of the velocity factor or dielectric constant entered by the user. Since the HP 54120T has no control over the accuracy of these numbers, distance accuracy is not specified. Distance is derived from time interval measurements whose accuracies are specified.

Distance (d) = one half times the quantity (delta t divided by the velocity constant)

Where delta t = time from the reference plane to the cursor.

Dielectric Constant = $(3 \times 10^{8} m/s)^{2}$ (Velocity Constant)^{2}

Table 1-3. Operating characteristics (continued)

Where the user enters either a relative Dielectric Constant or a velocity constant. The TDR's ability to resolve the distance between two discontinuities is limited to 1/2 the system risetime. Without normalization, this is approximately 1/2 of 45 ps or 7 mm in air. For the distance resolution in your media, divide 7 mm by the the square root of the effective dielectric constant of your media. With normalization, the system risetime can be 10 ps yielding 1.5 mm of resolution in air. The maximum length the TDR can measure is subject to media loss. For a lossless vacuum, and with a 15.3 Hz TDR repetition rate, the HP 54120T can measure 4,900 km. Actual maximum lengths will generally be limited by the losses of the media under test.

TRANSMISSION MEASUREMENTS

Source: Measurements are made using the channel 1 step source or a user-supplied external source.

Calibration: A calibration with a straight-through path or through a user's standard device determines reference amplitude levels, reference time, and distances of the signal path. These reference levels are used for gain and propagation delay measurements.

Cursor: Reads out time referenced to the calibration edge and gain referenced to the transmission calibration results. (See Note 2.)

Propagation Delay and Gain: Automatically calculates the difference in time and distance between the calibration signal path and the test signal path. Also calculates the ratio of the test signal amplitude to the calibration signal amplitude. (See Note 2.)

Normalization Filter: Applies a firmware digital filter to the measured data and puts the resulting waveform in memory 2. The risetime of the filter may be varied to allow the user to simulate the edge speeds which would be seen by the device under actual operation. See TDR output specifications for allowable risetime values.

Note 2:

Delta t = Time of the cursor - Time of reference edge (50%)

Gain = (Vtop - Vbase) signal ÷ (Vtop - Vbase) reference

Prop Dly = Time of test edge (50%) - Time of reference edge (50%)

Distance (d) = Prop Dly × Velocity Constant

Vtop = High level of waveform

Vbase = Low level of waveform

Table 1-3. Operating Characteristics (continued)

Setup Aids

Auto-Scale: Pressing the Auto-Scale key automatically adjusts the vertical and horizontal scale factors and the trigger level for a display appropriate to the signals applied to the inputs. Auto-Scale requires a signal with a duty cycle greater than 2%, a frequency greater than 50 Hz, and an input level of 5 mV for low bandwidth mode or 20 mV for high bandwidth mode. Auto-Scale is operative for relatively stable input signals, and the signal applied to the external trigger input must meet the minimum trigger specifications.

Save/Recall: Up to ten front-panel setups may be saved in non-volatile memory.

Preset Reflection Channel: Sets up the instrument for making TDR measurements.

Documentation Aids

Waveforms, scaling information, and measurement results can be transferred directly to HP-GL compatible digital plotters and HP-IB raster graphics printers, including the HP 2225A ThinkJet printer and the HP 3630A printer.

Digitizer

Converter: 12-bit successive approximation A/D converter.

Resolution: The useable full-scale range of the A/D is 640 mV. One LSB of the A/D converter equals 250 μV. This gives one part in 2560, or slightly more than 11 bits of resolution. Averaging can extend the resolution to 32 μV. This increased resolution of around 14 bits can be seen at more sensitive ranges or over the HP-IB.

Digitizing Rate: The signal is sampled and digitized at a rate dictated by the trigger rate, repetition rate, timebase range, display mode, and number of channels turned on. If data acquisition is not limited by trigger rate, the actual sampling and digitizing rate will vary within the following range:

a. Maximum of 10k samples per second at 10 ns/div or faster with one channel on while the HP 54120T is in infinite persistence display mode.

b. Minimum of 1k samples per second at timebase ranges of 46 μs/div or slower, regardless of number of channels turned on or the display mode.

A typical sample rate is 4500 samples per second.

Table 1-4. General Characteristics

Environmental Conditions

Temperature Operating: +15° C to +35° C (+59° F to +95° F).

Temperature Non-operating: -40° C to +70° C (-40°F to +158° F).

Humidity Operating: Up to 90% relative humidity at +35° C (95° F).

Humidity Non-operating: Up to 95% relative humidity at +65° C (+149° F).

Altitude Operating: Up to 4600 metres (15,000 ft).

Altitude Non-operating: Up to 15,300 metres (50,000 ft).

Vibration Operating: Random vibrations 5-500 Hz, 10 minutes per axis, –0.3 g (rms).

Vibration Non-operating: Random vibration 5-500 Hz, 10 minutes per axis, =2.41 g (rms); and swept sine resonant search, 5-500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Power Requirements

Power requirements listed are for the combined HP 54120T system. The HP 54121A Four Channel Test Set obtains its power over the provided interface cable from the HP 54120A Digitizing Oscilloscope Mainframe.

Voltage: 115/230 Vac, -25% to + 15%, 48-66 Hz.

Power: 200 watts, 400 VA maximum.

Weight

HP 54120A Net: Approximately 20.5 kg (45 lb).

HP 54121A Net: Approximately 3.2 kg (7 lb).

Combined Shipping Weight: Approximately 28.2 kg (62 lb).

Dimemsions

Dimensions are for general information only. If dimensions are required for building a special enclosure, contact your local HP sales office. Dimensions are in millimetres and (inches). Refer to figure 1-1.

Table 1-5. RF Accessory Kit HP Part Number 54121-68701.

Qty	Description of Part	HP Part Number
5	APC 3.5 (f-m) 20 dB attenuators	33340C/020
1	50 ohm load SMA (f)	1250-2151
1	Coaxial short SMA (f)	1250-2152
1	50 ohm load SMA (m)	1250-2153
2	SMA (m) to BNC (f) adapters	1250-1200
3	SMA (m-m) 36-inch coaxial cables	8120-4948

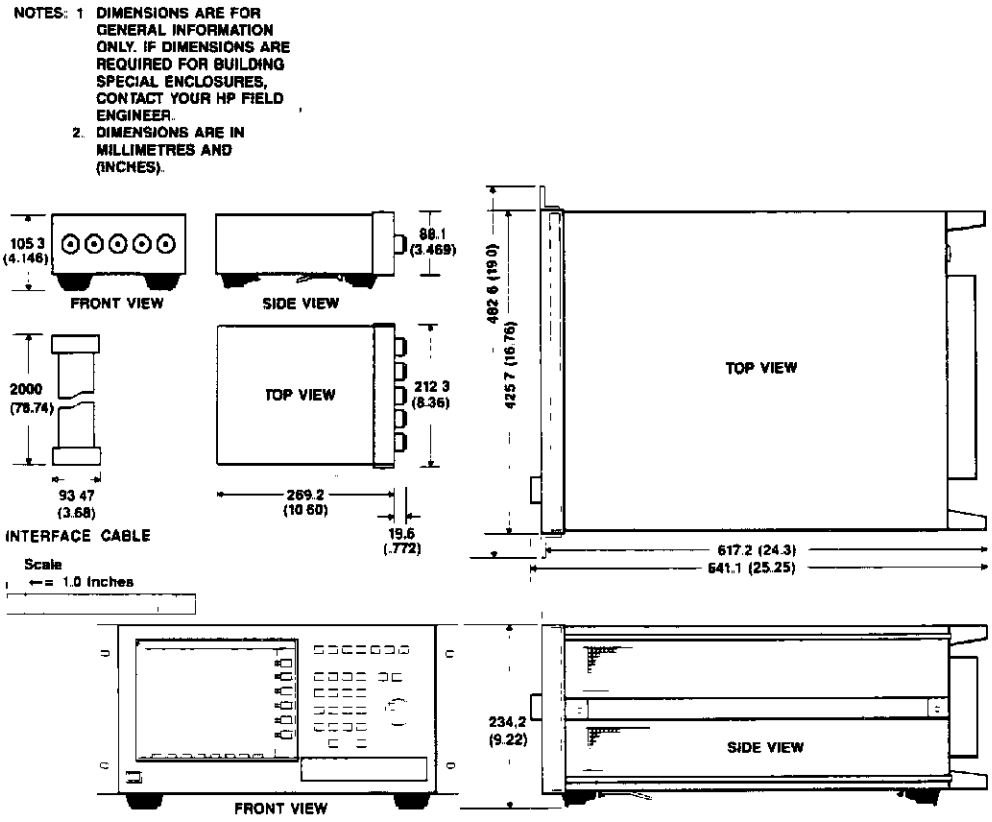

Figure 1-1. HP 54120A and HP 54121A Dimensions

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INSTALLATION

SECTION 2

INSTALLATION

2-1. INTRODUCTION

This section contains installation instructions, information about operating environments, cleaning the HP 54120T, and storage and shipment.

2-2. PREPARATION FOR USE

CAUTION

To prevent damage to the instrument, make sure the line voltage selector switch is in the correct setting for your AC voltage source.

2-3. Power Requirements

The HP 54120T requires a power source of 115 or 230 Vac +15/-25 percent; 48 to 66 Hz single phase. Power consumption is 200 watts or 400 VA maximum.

2-4. Line Voltage Selection

A blade-type screwdriver may be used to change the position of the line select switch. Figure 2-1 is a drawing of the line select switch in the 115 V position. Correctly setting the line switch sets the correct circuit breaker trip current. For 100 volt line operation, the line switch must be in the 115 V position.

2-5. Power Cables

WARNING

To protect operating personnel from possible injury or death, the chassis must be properly grounded. The proper power cord must be used and the power cord ground must ***NOT*** *be defeated. Refer to table 2-1 for power cable description and application.*

This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See Table 2-1 for option numbers of available power cables and plug configurations.

2-6. FOUR CHANNEL TEST SET CONNECTION

The HP 54120A Digitizing Oscilloscope Mainframe is connected to the HP 54121A Four Channel Test Set by cable HP Part Number 54120-61601. Reference designator is W3, and description is Umbilical Cable. Connect the Umbilical Cable to the Interface Cable Ports on the Mainframe and Four Channel Test Set. See figure 2-1. The Mainframe supplies all power for the Four Channel Test Set over the Umbilical Cable.

2-7. OPERATING ENVIRONMENT

The operating environment is noted in section 1, table 1-2. Note the non-condensing humidity limitation. Because condensation within the instrument can cause poor operation or malfunction, protection should be provided against it.

The HP 54120T will operate to all specifications with the temperature and humidity range given in section 1, table 1-2.

2-8. CLEANING

When cleaning the HP 54120T, CAUTION must be exercised about which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE DAMAGED.

CAUTION

BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuit if it seeps under the keys.

2-9. STORAGE AND SHIPMENT

The instrument may be stored or shipped in environments with the following limits:

Temperature:	-40°C to +70°C (-40° to +158°F)
Humidity:	Up to 95% at +65°C (+149°F)
Altitude:	Up to 15,300 metres (50,000 feet)

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause malfunction if the instrument is operated under these conditions.

If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of servicing required, the return address, model number, and full serial number. In any correspondence refer to the instrument by model number and full serial number.

2-10. PACKAGING

Original packaging i.e., containers and material identical to those used in factory packaging are available from Hewlett-Packard. If other packaging is to be used the following general instructions for repackaging with commercially available materials should be followed:

a. Wrap the oscilloscope in heavy paper or plastic. Install shorts on the HP 54121A Four Channel Test Set's inputs.

b. Use a strong shipping container. A double wall carton made of 2.4 MPa (350 psi) test material is adequate.

c. Use a layer of shock absorbing material 75 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect the control panel with cardboard.

d. Seal the shipping container securely

e. Mark the shipping container FRAGILE to ensure careful handling.

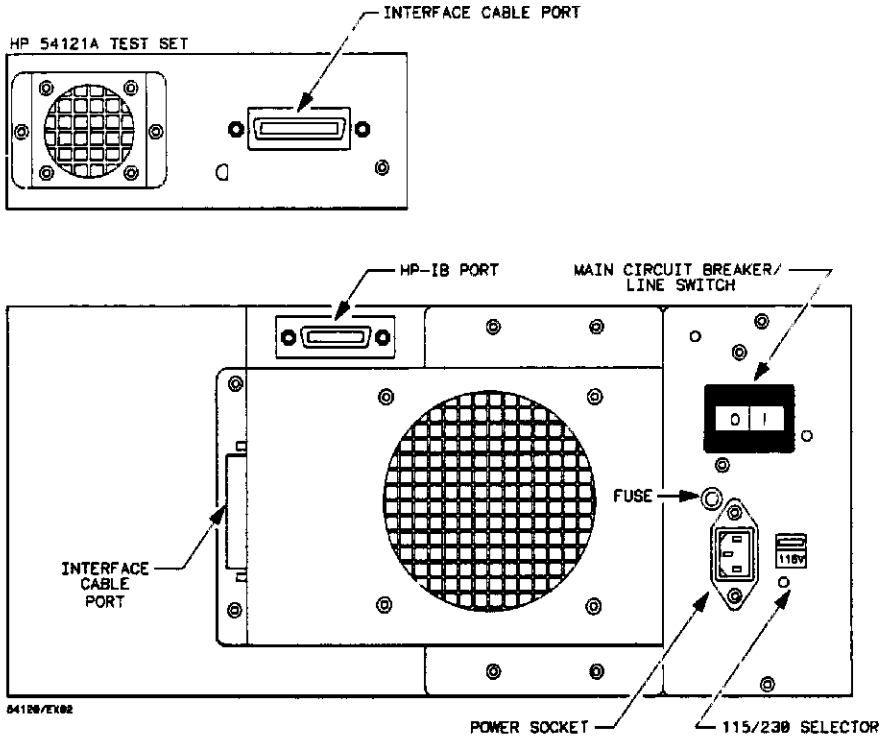
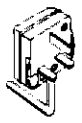
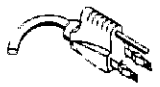


Figure 2-1. Line Voltage Selection and Umbilical Cable Connections

Table 2-1. Power Cord Configurations

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 250V 900 	8120-1351 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore
OPT 250V 901 	8120-1369 8120-0696	Straight *NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray	Australia, New Zealand
OPT 250V 902 	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So. Africa, India (Unpolarized in many nations)
OPT** 125V 903 	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical) UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Mexico, Philippines, Taiwan,
OPT** 250V 904 	8120-0698	Straight *NEMA6-15P	90/228	Black	United States, Canada
OPT 250V 905 	8120-1396 8120-1625	CEE22-V1 (System Cabinet Use) 250V	30/76 96/244	Jade Gray	For interconnecting system components and peripherals. United States and Canada only
OPT 250V 906 	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 220V 912 	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark
OPT 250V 917 	8120-4600 8120-4211	Straight SABS164 90°	79/200 79/200	Jade Gray	Republic of South Africa India
OPT 100V 918 	8120-4753 8120-4754	Straight Mitsumi 90°	90/230 90/230	Dark Gray	Japan

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug.
**These cords are included in the CSA certification approval of the equipment.
E = Earth Ground
L = Line
N = Neutral

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PERFORMANCE TESTS

SECTION 3

PERFORMANCE TESTS

3-1. INTRODUCTION

The procedures in this section test the instrument's electrical performance using the specifications in Section I as performance standards. All tests can be performed without access to the interior of the instrument.

3-2. RECOMMENDED EQUIPMENT FOR PERFORMANCE TESTS

Equipment recommended for performance tests is listed in table 1-1. Any equipment that satisfies the critical specifications stated in table 1-1 may be substituted.

3-3. TEST RECORD

Results of performance tests may be tabulated on the Performance Test Record (table 3-1) at the end of the procedures. The Test Record lists all of the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison during periodic maintenance, troubleshooting, and after repairs or adjustments.

3-4. PERFORMANCE TEST CYCLE

This instrument requires periodic verification of performance. The instrument should be checked using the following performance tests at least every twelve months or every 2000 hours of operation. Amount of use, environmental conditions, and the user's experience concerning need for performance checks will contribute in deciding the performance test cycle.

3-5. SPECIAL PROCEDURES

1. All connectors should be clean and undamaged to ensure accurate measurements. All APC 3.5 (f-f) adapters of the test set should be mechanically and visually checked before inserting any calibration test tool into them. Damaged connectors or loose connections may cause the performance verification tests to fail. See appendix A at the end of this manual.

2. The HP 54120T should be allowed to warm up for at least 15 minutes.

3. To avoid damage to the HP 54121A Four Channel Test Set connectors, use of the APC 3.5 (f-f) connector savers is encouraged. These connector savers are supplied with the HP 54120T. Refer to appendix A for information on what happens to APC 3.5 connectors when used with SMA connectors.

4. Avoid sharp bends in the two 17 inch coaxial cables, HP part numbers 8120-4941 and 8120-4942.

5. When mating APC 3.5 connectors to APC 3.5 connectors or devices, torque all connections to 8 in/lbs. When mating APC 3.5 to SMA or SMA to SMA, torque all connections to 5 in/lbs.

6. If possible, minimize connector swapping during the procedures. APC 3.5 and SMA connectors wear out with age. All test tool connectors should be inspected both visually and mechanically every few calibrations.

7. The performance test procedures outlined in this section make use of extra connectors. These are used to save expensive parts from repeated excessive wear caused by many reconnections. These parts are not necessary, but their use is highly advised.

8. Throughout the procedure identical connectors are used in different ways. One way is precision at both ends. This means that both ends of the APC 3.5 connector should be precise and should never have been connected to an SMA connector. The other way is precise at one end. This means that one of the APC 3.5 ends may be used with SMA connectors, but the other end should never have been connected to any SMA connectors. Unless otherwise stated, all APC 3.5 connectors should never be connected to SMA connectors.

3-6. PERFORMANCE TEST PROCEDURES

NOTE

Allow instrument to warm up for at least 15 minutes prior to beginning performance tests.

CAUTION

The Four Channel Test Set is very sensitive to static discharge. Failure to observe proper antistatic methods may result in damage to the gallium arsenide samplers. All maintenance or operation should be performed with the antistatic mat and wrist strap, which are supplied with the instrument.

3-7. BANDWIDTH TEST

Specifications:

20 GHz bandwidth with average display mode, bandwidth at -3 dB
channel 1 dc to 18 GHz (-3.5 dB at 20 GHz)
channels 2-4 dc to 20 GHz

12.4 GHz bandwidth mode with persistence display mode, bandwidth at -3 dB
channels 1-4 dc to 12.4 GHz

Description:

The following procedure calculates the HP 54120T's bandwidth. The sine wave output of a synthesized sweeper is leveled with a power meter. The sine wave's rms voltage is measured and converted to a power measurement to determine bandwidth. This is done on four frequencies on all four channels. This allows use of the HP 54120T's auto measurement modes to increase the measurement's accuracy.

The specification at 20 GHz is -3 dB, however the oscilloscope is tested at 19.98 GHz. The generator's vertical output is not synchronized with its 10 MHz reference output at 20.000 GHz. When the oscilloscope is tested at 19.98 GHz, the specification is -2.99 dB for channels 2 through 4 and -3.49 dB for channel 1.

If this performance test fails, perform the vertical system adjustments in the following order; 10 V reference, step recovery diode, sampler bias, offset gain, and feedthrough compensation adjustments.

Recommended Test Equipment:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Synthesized sweeper	20 GHz, +6 dBm <-25 dBc subharmonics	HP 8341
RF amplifier	Gain 20 dB at 10 MHz flatness ±.7 dB, noise < 6 dB harmonic distortion -32 dB for 0 dB output	HP 8447A
Power meter	20 GHz	HP 436A
Power sensor	20 GHz	HP 8485A
Calculator	Log base 10 function	HP 11C
20 dB pad	APC 3.5 connections	HP 33340C/020
ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
Adapter BNC (f) to SMA (m)	Quantity needed - 2	1250-1200
Adapter N (m) to APC 3.5 (m)		1250-1743
Adapter APC 3.5 (f-f)	26.5 GHz	1250-1865
Adapter APC 3.5 (m-f)	Precise male end	1250-1866
Adapter APC 3.5 (m-f)	Precise both ends	1250-1866
Coaxial cable APC 3.5 (m-f)	26.5 GHz	8120-4942
BNC cable	Length - 48 inches Quantity needed - 2	10503A

Procedure:

Characterizing the sweep oscillator's output.

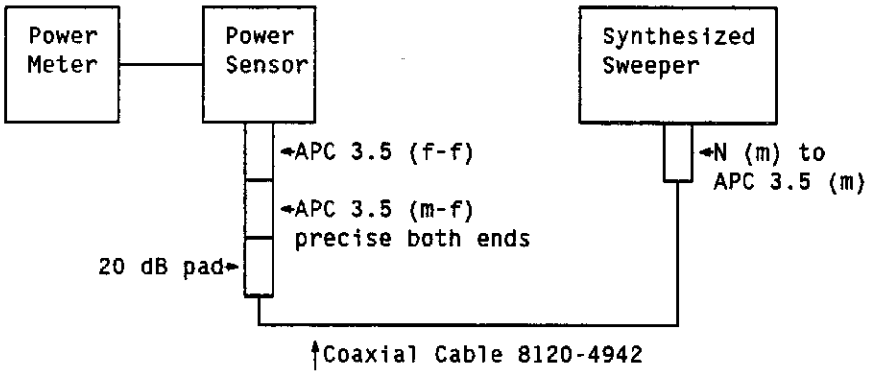
Note

The sweep oscillator's output will change slightly from one day to the next day. That makes this part of the calibration procedure difficult to repeat. Improperly torqued connectors or the usage of a different 20 dB pad is the most likely source of errors for regaining previously obtained numbers.

Type of Equipment	Model Number	Serial Number
Synthesized sweeper		
Power meter		
Power sensor		
20 dB pad		

1. Calibrate and zero power meter before connecting sensor to device under test. Use an N type (m) to APC 3.5 (f) adapter.

2. Connect equipment as shown below.



3. Set sweep oscillator's frequency to 50 MHz.

4. Set sweep oscillator's output power to +6 dBm.

5. Set power meter's cal factor to 100%. **DO NOT** change its setting during this procedure.

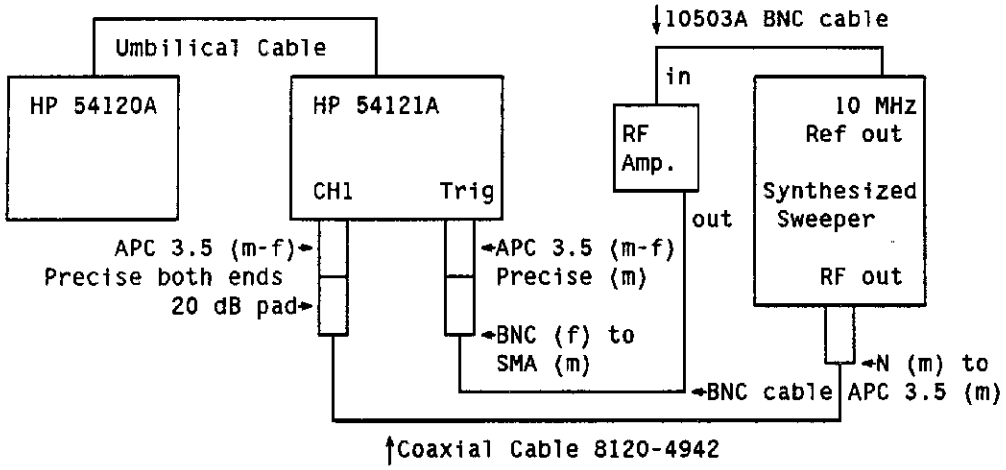
6. Record power meter's reading in μW in step 22 part 1.

7. Set sweep oscillator's frequency to 12.4 GHz, 18 GHz, 19.98 GHz and note power meter's readings in μW in step 22 part 1.

8. Record power sensor's cal factors (CF) in step 22 part 2 (assume 100% for 50 MHz).

Checking the oscilloscope's bandwidth

9. Connect the equipment as shown below.



10. Perform a one-key down power up on the HP 54120T. Hold down any key and cycle the oscilloscope's power off and on. Continue to hold the key down until graticules are displayed on screen.

11. Change the oscilloscope's display to 64 averages, bandwidth to 12.4 GHz, and screen to single. Turn channel 1 on and channels 2 through 4 off. Set vertical sensitivity to 20 mV/div on all four channels, and timebase sweep to 5 ns/div.

12. Set sweeper's frequency to 50 MHz.

13. Press ***Clear Display*** key and wait for 64 averages to accumulate at top left corner of screen.

14. Press ***More*** key, ***Measure*** key, ***Precision*** key until ***fine*** is highlighted, then ***RMS Voltage*** key.

15. Note the VRMS reading on bottom of screen and record the value in step 25 part 3.

16. Change oscilloscope's sweep speed to 15 ps/div.

17. Change sweeper's frequency to 12.4 GHz and repeat steps 13-15.

18. Change display bandwidth mode to 20 GHz.

19A. For channel 1 change sweep oscillator's frequency to 18 GHz and repeat steps 13 through 15.

19B. For channels 1-4 change sweep oscillator's frequency to 19.98 GHz and repeat steps 13 through 15.

20. Change display bandwidth to 12.4 GHz, timebase sweep speed to 5 ns/div.

21. Repeat steps 12 through 20 for channels 2-4.

22. Calculate oscilloscope's three bandwidth gains at 12.4 GHz, 18 GHz, and 19.98 GHz with the values and the formula listed below.
There is an example on the next page which uses the formula.

Part 1

Frequency	Synthesized sweeper output in μW
50 MHz	_____ μW
12.4 GHz	_____ μW
18 GHz	_____ μW
19.98 GHz	_____ μW

Part 2

Frequency	Power sensor cal. factor
50 MHz	_____ %
12.4 GHz	_____ %
18 GHz	_____ %
19.98 GHz	_____ %

Part 3

Frequency	HP 54120T measurement results in RMS volts			
	Ch. 1	Ch. 2	Ch. 3	Ch. 4
50 MHz	_____ mV	_____ mV	_____ mV	_____ mV
12.4 GHz	_____ mV	_____ mV	_____ mV	_____ mV
18 GHz	_____ mV	N/A	N/A	N/A
19.98 GHz	_____ mV	_____ mV	_____ mV	_____ mV

$$\text{Gain} = 10 \log_{10} \left[\left[\frac{\text{Power Meter reading 50 MHz}}{\text{Power Meter reading high freq}} \right] \left[\frac{\text{CF high freq}}{\text{CF 50 MHz}} \right] \left[\frac{V_{RMS} \text{ high freq}}{V_{RMS} \text{ 50 MHz}} \right]^2 \right]$$

Example:

Power Meter Reading at low frequency of 50 MHz = 38.8 μW
Power Meter Reading at high frequency of 20 GHz = 27.6 μW
VRMS of HP 54120A at low frequency of 50 MHz = 43.79 μV
VRMS of HP 54120A at high frequency of 20 GHz = 28.55 μV
CF of power meter at low frequency of 50 MHz = 100%
CF of power meter at high frequency of 20 GHz = 91.7%

$$-2.6\text{db} = 10 \log_{10} \left[\left[\frac{38.8\ \mu\text{w}}{27.6\ \mu\text{w}} \right] \left[\frac{91.7\%}{100\%} \right] \left[\frac{28.55\ \mu\text{v}}{43.79\ \mu\text{v}} \right]^2 \right]$$

3-8. DC VOLTAGE MEASUREMENT ACCURACY AND RMS NOISE TEST

Specifications:

DC voltage accuracy (50 Ω source)

Single voltage marker
Average mode ±.4% of which is greater (full-scale or marker reading) ±2 mV
Persistence mode ±.4% of full-scale ±2 mV ±3% of (reading - channel offset)

Dual voltage markers (on same channel)
Average mode ±.8% of which is greater (full-scale or Delta V reading)
Persistence mode ±.8% of full-scale ±3% of reading

RMS noise in persistence mode (1 sigma)
12.4 GHz bandwidth mode ≤1 mV RMS

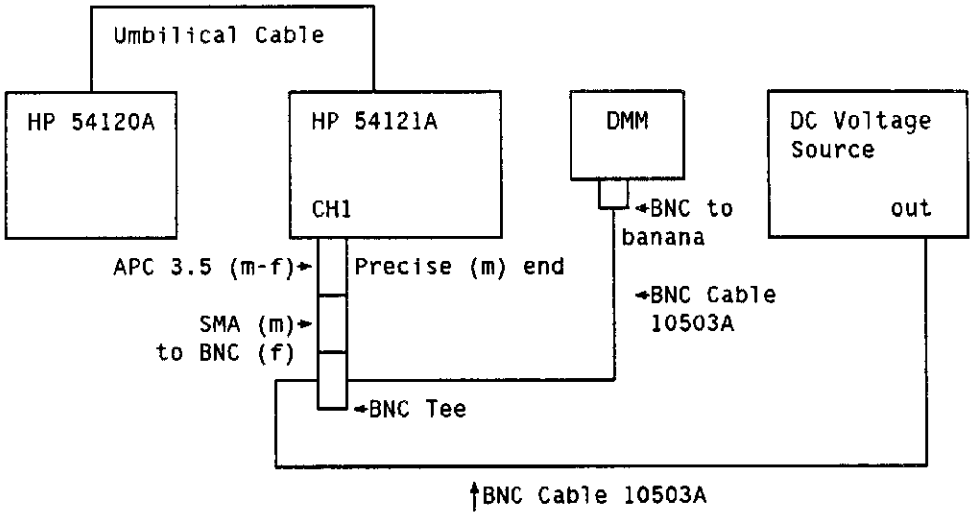
Description:

This test checks the offset accuracy, offset gain accuracy, sampler gain accuracy, and the 12.4 GHz RMS noise level of the HP 54120T. If this performance test fails, perform the vertical system adjustments in the following order; 10 V reference, step recovery diode, sampler bias, offset gain, and feedthrough compensation adjustments.

Recommended Test Equipment:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
dc voltage source	±1/2 volt, 100 μV resolution	HP 3325A
DMM	5 1/2 digits	HP 3478A
ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
BNC cable	Length - 48 inches Quantity needed - 2	10503A
BNC Tee		1250-0781
Adapter BNC (f) to SMA (m)		1250-1200
Adapter APC 3.5 (m-f)	Precise male end 26.5 GHz	1250-1866
Adapter BNC to banana		1250-2277

Equipment Connections:



Equipment Setup:

DC Voltage Source

Mode	dc
Offset	500 mV
Output	enabled

CAUTION

Exceeding 2V on the dc power supply may damage the oscilloscope's input

HP 54120T

Display

Display Mode	Averaged
No. of Averages	16
Screen	Single
Graticule	Frame
Bandwidth	12.4 GHz

Channels

Channels	1-4
Display	Off
Volts/Div	5 mV/div
Offset	0 V
Attenuation	1

Timebase

Time/Div	1 μs/div
Delay	200 ns
Delay Ref at	Left
Sweep	Freerun
Freerun Rate	10 KHz

Trigger

Trigger Level	0 V
Slope	Pos
HF Sense	Off
HF Reject	Off
Attenuation	1

Network

Reflect/Trans/CAL	Reflect
Step & Chan 1	Off

Procedure:

1. Press ***Save Setup*** key, then *1* key on oscilloscope.
   This saves the front panel setup in memory location 1.

2. Change the vertical sensitivity on channels 1-4 to 80 mV/div, and display mode to a persistence of 300 ms.
   Press ***Save Setup*** key, then *2* key on oscilloscope.

3. If BNC tee is connected to the four channel test set, remove the tee and leave it disconnected for now.

4. Press ***Recall Setup*** key, then *1* key.
   This recalls instrument setup from memory location 1.
   Turn channel 1 on.

5. Turn Delta V markers on and overlay both markers on channel 1.
   Press ***Preset Levels*** until ***50%-50%*** is highlighted.

6. Press ***Clear Display*** key and wait for 16 averages to accumulate on top left of screen.

7. Press ***Auto Level Set*** key and note the V1 value. It should be 0 V ±2.16 mV.

8. Press ***Display*** key and change bandwidth to 20 GHz.

9. Press ***Clear Display*** key and wait for 16 averages to accumulate.
   Press ***Delta V*** menu key, then ***Auto Level Set*** key.
   The V1 value should be 0 V ±2.16 mV.

10. Connect BNC tee to channel 1.

11. Change channel 1's offset to 500 mV. Change display bandwidth to 12.4 GHz.

12. Adjust dc source until DMM reads 500 mv ±100 μV.

13. Press ***Clear Display*** key and wait for 16 averages to accumulate.
    Turn Delta V markers on and overlay marker 2 on trace.
    The V2 value should be 500 mV ±4 mV.

14. Change channel 1 offset to -500 mV.

15. Adjust dc source until DMM reads -500 mV ±100 μV.

16. Press ***Clear Display*** key and wait for 16 averages to accumulate.
    Turn Delta V markers on and overlay marker 1 on trace.
    The V1 value should be -500 mV ±4 mV.
    The delta V value should be 1.0000 V ±8 mV.

17. Recall instrument setup from memory location 2.
    Turn channel 1 on.

18. Press ***More*** key, then press ***Wfm Math*** key.
    Press ***Function*** key until *1* is highlighted.
    Press ***Display*** key until ***On*** is highlighted.
    Change first ***Chan-Mem*** key until ***Chan 1*** is highlighted.
    Press ***Operation*** key until ***Only*** is highlighted.
    Press ***Display Scaling*** key until ***Volts/Div*** is highlighted.
    Adjust sensitivity to 5 mV/div.
    Press ***Display Scaling*** key until ***Offset*** is highlighted.
    Adjust offset to 250 mV.

19. Adjust dc source until DMM reads 250 mV ±100 μV.

20. Turn Delta V markers on and overlay both markers on function 1.
    Press ***preset levels*** until ***50%-50%*** is highlighted.
    Manually overlay delta V marker 1 to center of trace.
    The V1 value should be 250 mV ± 9.66 mV.

21. Press ***Wfm Math*** key.
    Press ***Display Scaling*** key until ***Offset*** is highlighted.
    Adjust offset to -250 mV.

22. Adjust dc source until DMM reads -250 mV ±100 μV.

23. Manually overlay delta V marker 2 to center of trace.
    The V2 value should be -250 mV ±9.66 mV.

RMS noise test

24. Press ***Recall 2*** key.

25. Disconnect all signals from channel 1 and place SMA shorts on all inputs.

26. Change display mode to infinite persistence, and timebase delay to 16 ns.

27. Turn function display off.
    Change channel 1 sensitivity to 2 mV/div and 0 V offset.

28. Press ***Histogram*** menu key and then press ***Window/Acquire/Results*** key until ***Window*** is highlighted.

29. Press ***Voltage/Time*** key until ***Voltage*** is highlighted.

30. Set windows to screen's left and right sides.

31. Press ***Window/Acquire/Results*** key until ***Acquire*** is highlighted.
    Select 10000 samples and press ***Start Acquiring*** key.
    Wait until oscilloscope finishes acquiring data.

32. Press ***Window/Acquire/Results*** key until ***Results*** is highlighted.
    Press ***Sigma*** key.
    The sigma value should be <1 mV.

33. Repeat steps 3-32 for channels 2-4.

3-9. TIME INTERVAL ACCURACY TEST

Specifications:

Time interval accuracy ≤10 ps ±.1% of reading

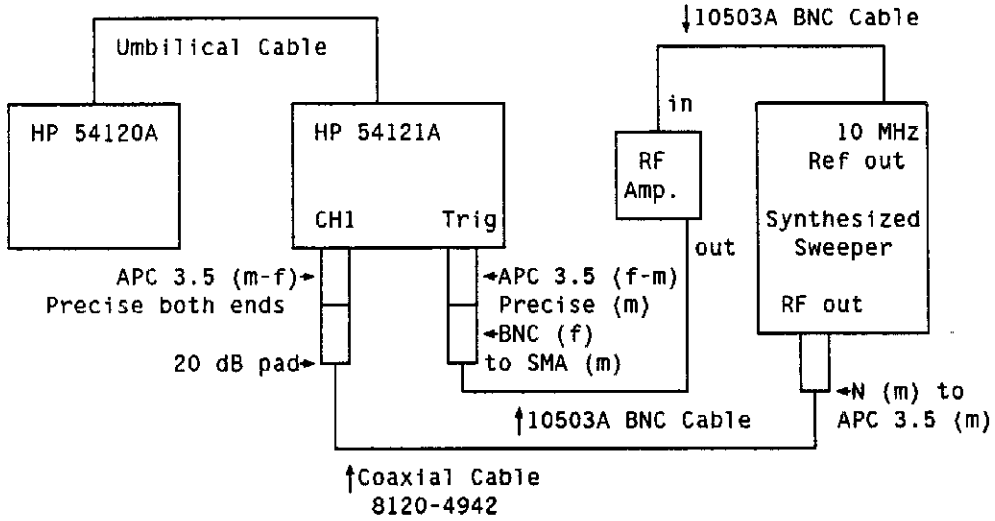
Description:

This tests the accuracy of all timebase delay counter modes. If this performance test fails, perform these adjustments in the following; delta current, range, frequency, end, and 4 ns cal adjustments.

Recommended Test Equipment:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Synthesized sweeper	20 GHz, -25 dBc harmonics, stability .25 ppm/yr, +6 dBm	HP 8341
20 dB pad	APC 3.5 connections	HP 33340C/020
RF amplifier	Gain 20 dB at 10 MHz flatness ±.7 dB, noise < 6 dB harmonic distortion -32 dB for 0 dB output	HP 8447A
Frequency synthesizer	10 MHz square wave 120 mV output stability .05 ppm/yr	HP 3325A/001
ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
Adapter BNC (f) to SMA (m)	Quantity needed - 2	1250-1200
Adapter N (m) to APC 3.5 (m)		1250-1743
Adapter APC 3.5 (m-f)	Precise both ends 26.5 GHz	1250-1866
Adapter APC 3.5 (m-f)	Male end precise 26.5 GHz Quantity needed - 2	1250-1866
Coaxial cable APC 3.5 (m-m)	26.5 GHz	8120-4942
BNC cable	Length - 48 inches Quantity needed - 2	10503A

Equipment Connections:



Equipment Setup:

Synthesized Sweeper

Mode	Sine wave
Frequency	19.98 GHz
Amplitude	+6 dBm

Frequency Synthesizer

Frequency	10 MHz
Amplitude	120 mV
Mode	Square wave

HP 54120T

Display

Display Mode	Averaged
No. of Averages	64
Screen	Single
Graticule	Frame
Bandwidth	20 GHz

Channels

Channels	1-4
Display	Off
Volts/Div	20 mV/div
Offset	0 V
Attenuation	1

Timebase

Time/Div	10 ps/div
Delay	16 ns
Delay Ref at	Left
Sweep	Trg'd

Trigger

Trigger Level	0 V
Slope	Pos
HF Sense	Off
HF Reject	Off
Attenuation	1

Network

Reflect/Trans/CAL	Reflect
Step & Chan 1	Off

Procedure:

Short Delta T

1. Press ***Save Setup*** key, then *3* key.
   Turn channel 1 on.

2 Press ***Clear Display*** key and wait until 64 averages accumulate.

3. Press ***Measure*** menu key.
   Press ***Precision*** key until fine is highlighted.
   Press ***Period*** key to measure period of 19.98 GHz sine wave.
   The period should be 50.1 ps ±10.1 ps.

4. Repeat steps 2 and 3 for timebase delay settings of 18 ns, 19.9 ns, 19.95, 23.95 ns, 27.95 ns, and 55.95 ns.

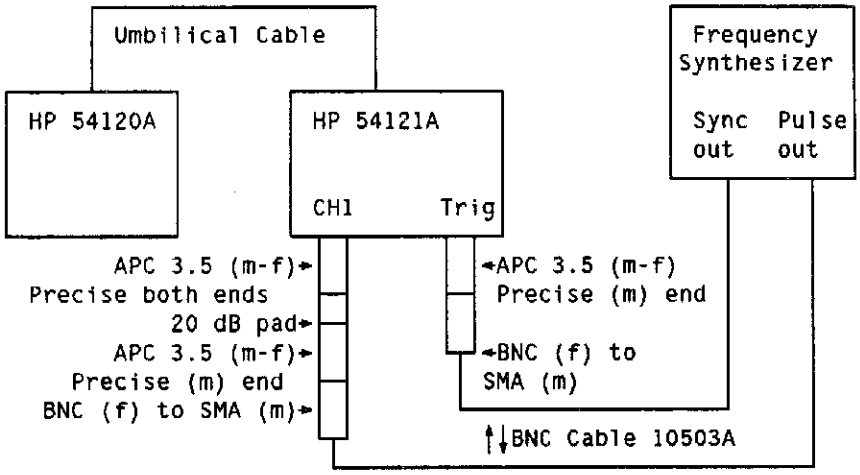
5. Change timebase delay to 16 ns and display bandwidth to 12.4 GHz.

6. Repeat step 2 and 3 for the following oscilloscope timebase settings and sweeper frequency settings, and ensure the measured results are within the allowable limits.

Timebase setting	Sweeper setting	Test limits
50 ps/div	10 GHz	100 ps ±10.1 ps
100 ps/div	5 GHz	200 ps ±10.2 ps
250 ps/div	2 GHz	500 ps ±10.5 ps
500 ps/div	1 GHz	1 ns ±11.0 ps
1 ns/div	500 MHz	2 ns ±12.0 ps
2.5 ns/div	200 MHz	5 ns ±15.0 ps
5 ns/div	100 MHz	10 ns ±20.0 ps
10 ns/div	50 MHz	20 ns ±30.0 ps
25 ns/div	20 MHz	50 ns ±60.0 ps

Long Delta T

7. Change the equipment setup as follows.



8. Press ***Recall 3.***

9. Change timebase sweep to 20 ns/div and trigger level to 500 mV.

10. Press ***Clear Display*** key and wait until 64 averages accumulate.

11. Press ***Measure*** menu key.
    Press ***Precision*** key until fine is highlighted.
    Press ***Period*** key and wait for oscilloscope to measure period of 10 MHz sine wave.
    The period should be 100 ns ±110.0 ps.

12. Repeat steps 10-11 for the following settings and ensure the measured values are within the allowable limits.

Timebase setting	Frequency Synthesizer	Test limits
100 ns	5 MHz	200 ns ±210.0 ps
250 ns	2 MHz	500 ns ±510.0 ps
500 ns	1 MHz	1 μs ±1.01.ns
1 μs	500 KHz	2 μs ±2.01 ns
2.5 μs	200 KHz	5 μs ±5.01 ns
5 μs	100 KHz	10 μs ±10.01 ns
10 μs	50 KHz	20 μs ±20.01 ns
25 μs	20 KHz	50 μs ±50.01 ns (.05001 μs)
50 μs	10 KHz	100 μs ±100.01 ns (.10001 μs)

3-10. TRIGGER SENSITIVITY TEST

Specification:

External trigger sensitivity

dc to 100 MHz	40 mV p-p
100 MHz to 500 MHz	100 mV p-p

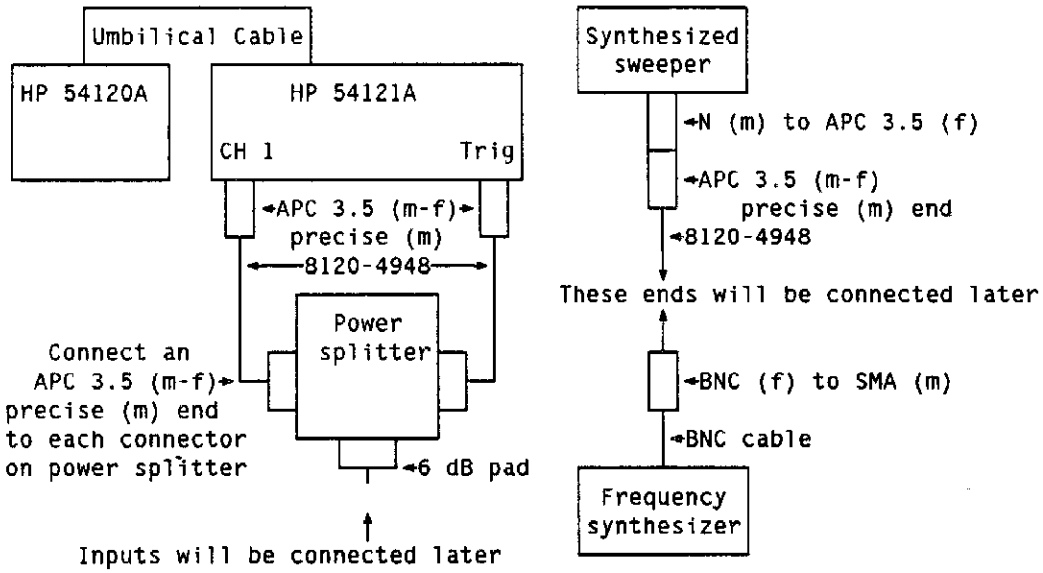
Description:

This tests the high and low frequency trigger sensitivities by applying a 500 MHz sine wave . If the oscilloscope triggers at 500 MHz, it will also trigger on a 1 ns pulse width at 80 mV.
If this performance test fails, adjust the trigger hysteresis and trigger offset adjustments in paragraph 4-17.

Equipment Recommended:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Synthesized sweeper	20 GHz -6 dBm	HP 8341/003
Power splitter	APC 3.5 connectors	HP 11667B
Frequency synthesizer	100 KHz sine wave 200 mV output	HP 3325A
ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
Adapter APC 3.5 (m-f)	Both ends precise 26.5 GHz Quantity needed - 6	1250-1866
Adapter N (m) to APC 3.5 (f)		1250-1744
Adapter SMA (m) to BNC (f)		1250-1200
Coaxial cable APC 3.5 (m-m)	18 GHz Quantity needed - 3	8120-4948
BNC cable	48 inches	10503A
6 dB pad	APC 3.5 connectors	33340C/006

Equipment Connections:



Equipment Setup:

Frequency Synthesizer

Frequency	100 KHz
Power output	200 mV
Mode	Sine wave

Synthesized Sweeper

Frequency	100 MHz
Power output	-6 dBm

HP 54120T

Display

Display Mode	Averaged
No. of Averages	64
Screen	Single
Graticule	Frame
Bandwidth	12.4 GHz

Channels

Channels	1-4
Display	Off
Volts/Div	20 mV/div
Offset	0 V
Attenuation	1

Timebase

Time/Div	1 ns/div
Delay	16 ns
Delay Ref at	Left
Sweep	Trg'd

Trigger

Trigger Level	0 V
Slope	Pos
HF Sense	Off
HF Reject	Off
Attenuation	1

Network

Reflect/Trans/CAL	Reflect
Step & Chan 1	Off

Procedure:

Low frequency trigger hysteresis sensitivity

1. Connect frequency synthesizer to power splitter.

2 Turn channel 1 on.

3. Adjust frequency synthesizer until signal on screen is exactly 100 mV p-p.

4. Slowly adjust trigger level greater than 0 V until oscilloscope just stops triggering. This is indicated on screen by pressing ***Clear Display*** key each time the trigger level is changed. If the oscilloscope is triggered, the waveform will be displayed on screen. Note the trigger level, this is V_{pos}.

5. Return trigger level to 0 V. Slowly adjust trigger level less than 0 V until oscilloscope just stops to trigger. This is V_{neg}.

6. Calculate hysteresis. $V_{hysteresis} = 100\ mV - (V_{pos} - V_{neg})$
The value should be ≤40 mV.

100 MHz/500 MHz trigger sensitivity

7. Change oscilloscope's timebase sweep speed to 2 ns/div.

8. Connect synthesized sweeper to power splitter.

9. Adjust sweeper's amplitude to exactly 150 mV amplitude as displayed on screen.

10. Slowly adjust trigger level greater than 0 V until oscilloscope just stops triggering. This is V_{pos}.

11. Return trigger level to 0 V. Slowly adjust trigger level less than 0 V until oscilloscope just stops to trigger. This is V_{neg}.

12. Calculate sensitivity. $V_{sense} = 150\ mV - (V_{pos} - V_{neg})$.
The value should be ≤40 mV.

13. Change oscilloscope's sweep speed to 500 ps/div and trigger level to 0 V.

14. Change the sweeper's frequency to 500 MHz.

15. Repeat steps 9 through 12.
The value should be ≤100 mV.

3-11. JITTER TEST

Specifications:

Jitter (one standard deviation) = ≤ 5 ps + (5E-5 X delay setting)
(trigger and timebase combined)

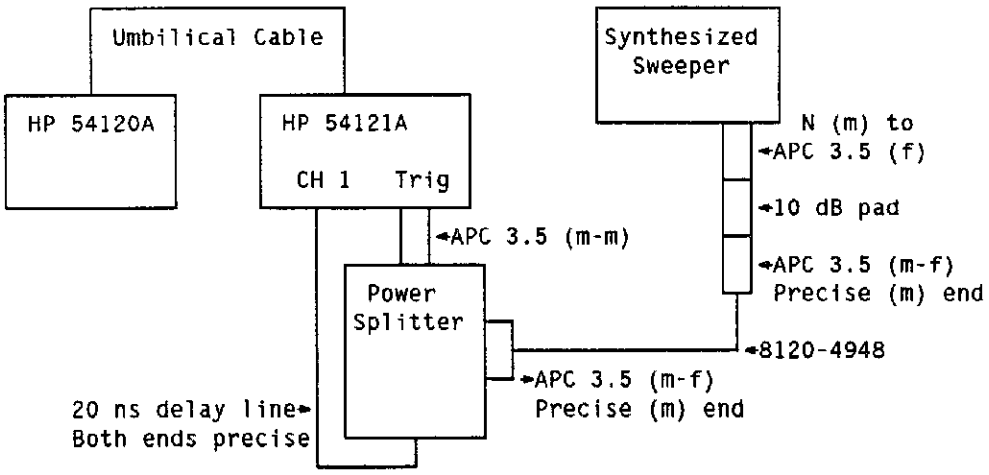
Description:

This test measures the oscilloscope's internal jitter with a 500 MHz sine wave. The instrument's jitter is less with fast rise input signals. If a generator is substituted, careful consideration of the generator's horizontal jitter and vertical noise is important.

Equipment recommended:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Synthesized sweeper	20 GHz +6 dBm	HP 8341
Power Splitter	APC 3.5 connectors	HP 11667B
10 dB pad	APC 3.5 connectors	HP 33340C/010
ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
Adapter APC 3.5 (m-f)	26.5 GHz (male end precise) Quantity needed - 2	1250-1866
Adapter N (m) to APC 3.5 (f)		1250-1744
Adapter APC 3.5 (m-m)	APC 3.5 connectors, both ends precise	1250-1864
Coaxial cable APC 3.5 (m-m)	18 GHz	8120-4948
20 ns delay line	APC 3.5 connectors, both ends precise	Call HP service center for No.

Equipment connections:



Equipment Setup:

Synthesized sweeper

Frequency	500 MHz
Power output	+12 dBm (do not exceed +12 dBm on the generator)
Mode	Sine wave

Procedure:

1. Perform a one-keydown power up. Hold down any key and cycle the oscilloscope's power off and on. Continue to hold the key down until graticules are displayed on screen.

2. Change the oscilloscope's display to single screen, turn channels 2-4 off, set channel 1 to 50 mV/div, change timebase sweep speed to 2 ns/div, and delay to value specified by delay line manufacturer.

3. Slightly vary the generator's frequency and observe the positive trigger slope on screen. If the positive trigger slope varies as the generator's frequency is varied, this positive trigger slope is not the actual trigger point. Choose different positive trigger slopes until the actual trigger point is obtained. Depending on delay line length, the oscilloscope's sweep speed and delay may need to be varied to help find the actual trigger point.

4. Turn Delta V markers on.
   Press ***Preset Levels*** key until *50%-50%* is highlighted.
   Press ***Auto Level Set*** key.

5. Turn Delta T markers on .
   Set start marker on 50% point of actual trigger point's positive slope.

6. Change the oscilloscope's sweep speed to 200 ps/div and delay to start marker's value.

7. Change generator's frequency to 500 MHz.

8. Adjust oscilloscope's delay to center waveform's positive edge on screen.

9. Slowly adjust generator's amplitude until signal just fills screen. If the delay line attenuates the signal too much, a 6 dB pad may be substituted for the 10 dB pad. Change oscilloscope's sweep speed to 100 ps/div.

10. Press ***Histogram*** menu key.

11. Press ***Window/Acquire/Results*** key until ***Window*** is highlighted.
    Press ***Time/Voltage*** histogram key until ***Time*** is highlighted.
    Set window marker 1 to 1 mV and window marker 2 to -1 mV.

12. Press ***Window/Acquire/Results*** key until ***Acquire*** is highlighted.
    Set number of samples to 1000.
    Press ***Start acquiring*** key.
    Wait until acquire cycle is 100% complete.

13. Press ***Window/Acquire/Results*** key until ***Results*** is highlighted.
    Press ***Sigma*** key.
    Sigma value should be ≤5.8 ps.

3-12. TDR SYSTEM TESTS

Specifications:

Combined oscilloscope and TDR risetime performance ≤45 ps
measured in 12.4 GHz bandwidth averaged mode

Combined oscilloscope and TDR flatness performance
measured in 12.4 GHz bandwidth average mode.
After 1 ns from edge - ≤±1%
≤+5%, -2% to 1 ns from edge

Combined oscilloscope and TDR levels performance
Low - 0 V ±2 mV
High - 200 mV ±2 mV

Description:

This test verifies correct operation of the TDR system by checking the specifications of both the TDR system and the oscilloscope. If this performance test fails, perform the TDR adjustments in paragraph 4-15.

Equipment Recommended:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
50 ohm load	APC 3.5 (m)	HP 909D

Equipment setup:

Perform a one-keydown power up. Hold down any key and cycle the oscilloscope's power off and on. Continue to hold the key down until graticules are displayed on screen.
Make the following changes to the oscilloscope's setup.

HP 54120T

Display

Display Mode	Averaged
No. of Averages	16
Screen	Single
Graticule	Grid
Bandwidth	12.4 GHz

Channels

Channel	1
Display	On
Volts/Div	5 mV/div
Offset	0 V
Channels	2-4
Display	Off

Timebase

Time/Div	50 ps/div
Delay	16 ns
Delay Ref at	Left
Sweep	Freerun
Rate	10 KHz

Network

Reflect/Trans/CAL	Reflect
Step & Chan 1	On

Procedure:

Note

If there is a rising edge on screen, the "TDR Step Adjustments" in section 4 must be performed before continuing with this procedure.

1. Select Delta V menu and press ***V Markers*** key until ***On*** is highlighted.
   Press ***Preset Levels*** key until ***50%-50%*** is highlighted.
   Press ***Auto Level Set*** key. V(1) should read 0 V ±2 mV.

2. Change oscilloscope's sweep speed to 1 ns/div, channel 1 vertical sensitivity to 80 mV/div, and offset to 200 mV.

3. Select Delta V menu and press ***Preset Levels*** key until ***50%-50%*** is highlighted.
   Press ***Auto Level Set*** key.

4. Select Delta T menu and press ***T Markers*** key until ***On*** is highlighted.
   Press ***Start On edge*** key until ***Pos 1*** is highlighted.
   Press ***Stop on Edge*** key until ***Pos 1*** is highlighted.
   Press ***Precise Edge Find*** key.

5. Change Stop marker's value to the Start marker's value plus 1 ns.

6. Change oscilloscope's sweep speed to 100 ns/div, delay to Stop marker's value, and channel 1 vertical sensitivity to 2 mV/div.

7. Select Delta V menu and overlay marker 1 on trace at right edge of screen. Marker 1 should read 200 mV ±2 mV. This is the final value which will be used for flatness measurements.

8. Allow 16 averages to accumulate.
   Adjust marker 2 to signal's lowest point on screen.

9. Select timebase menu and press ***Time/Div*** key.
   Press front panel ***increment*** key to select the next fastest sweep speed.
   If this point is lower than marker 2's previous position, adjust V marker 2 to the lowest point on screen.
   Repeat this step until a sweep speed of 1 ns is reached.

10. The absolute value of delta V divided by V(1), multiplied by 100% should be ≤1% (-1% at > 1 ns after edge).

11. Change timebase sweep speed to 100 ns/div. Adjust marker 2 to signal's highest point on screen. The absolute value of delta V divided by V(1), multiplied by 100% should be ≤1% (+1% at > 1 ns after edge).

12. Change timebase sweep speed to 100 ps/div. and change delay setting equal to Start marker's value.

13. Adjust marker 2 to the signal's lowest point on screen. **DO NOT** include the signal's rising edge. The absolute value of delta V divided by V(1), multiplied by 100% should be ≤2% (-2% at < 1 ns).

3-13. INPUT REFLECTION TEST

Specifications:

Percent Reflection

Channels 1-4	≤5% for 30 ps risetime
External Trigger	≤10% for 100 ps risetime

Description:

This test uses a calibrated four channel test set channel to measure the amount of reflection each channel reflects back to the test line when pulsed with a fast edge signal.

Recommended Test Equipment:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
50 ohm load	APC 3.5 (f)	HP 909D/011
ACCESSORIES	**CRITICAL SPECIFICATIONS**	**RECOMMENDED HP PART NUMBER**
Adapter APC 3.5 (m-m)	26.5 GHz	1250-1864
Adapter APC 3.5 (f-f)	26.5 GHz	1250-1865
Coaxial short	APC 3.5 female connector	1250-2127
Coaxial short	APC 3.5 male connector	1250-2128
Semi-rigid U	No substitute	54121-61601
Semi-rigid S	No substitute	54121-61602

Equipment Connections:

1. Do not tighten the following connections until step 5.
2. Connect short end of semi-rigid U cable to short end of semi-rigid S cable through an APC 3.5 (f-f) adapter.
3. Connect semi-rigid U cable's other end to channel 1.
4. Without bending or damaging the semi-rigid cables, bring the semi-rigid S cable's other end toward channel 2. The joint where the semi-rigid S and U cables join will flex upwards until the semi-rigid cable's other end is connected to channel 2.
5. Tighten all cable connections.

3-13. INPUT REFLECTION TEST

Specifications:

Perc ent Reflection

Channels 1-4	≤5% for 30 ps risetime
External Trigger	≤10% for 100 ps risetime

Description:

This test uses a calibrated four channel test set channel to measure the amount of reflection each channel reflects back to the test line when pulsed with a fast edge signal.

Recommended Test Equipment:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
50 ohm load	APC 3.5 (f)	HP 909D/011
ACCESSORIES	**CRITICAL SPECIFICATIONS**	**RECOMMENDED HP PART NUMBER**
Adapter APC 3.5 (m-m)	26.5 GHz	1250-1864
Adapter APC 3.5 (f-f)	26.5 GHz	1250-1865
Coaxial short	APC 3.5 female connector	1250-2127
Coaxial short	APC 3.5 male connector	1250-2128
Semi-rigid U	No substitute	54121-61601
Semi-rigid S	No substitute	54121-61602

Equipment Connections:

1. Do not tighten the following connections until step 5.
2. Connect short end of semi-rigid U cable to short end of semi-rigid S cable through an APC 3.5 (f-f) adapter.
3. Connect semi-rigid U cable's other end to channel 1.
4. Without bending or damaging the semi-rigid cables, bring the semi-rigid S cable's other end toward channel 2. You will be told to connect the semi-rigid cable to channel 2 later in the procedure.
5. Tighten all cable connections.

Equipment Setup:

Perform a one-keydown power up. Hold down any key and cycle the oscilloscope's power off and on. Continue to hold the key down until graticules are displayed on screen.
Change the following on the HP 54120T

Display	
Screen	Single
Mode	Averaged
No. of averages	16
Channels	
Channel 1	On
Channels 2-4	Off
Volts/Div	5 mV/div
Offset	200 mV
Timebase	
Time/Div	350 ps/div
Delay	23.5 ns
Network	
Reflect/Trans/CAL	Reflect
Step & Chan 1	On

Procedure:

1. Adjust delay so that the signal's second rising edge (representing an open circuit condition) is 4 divisions left of center screen.
   Press ***Network*** menu.
   Press ***Reflect/Trans/CAL*** key until CAL is highlighted.

2. Press ***Reflect Cal*** key.
   Connect a coaxial short with an APC 3.5 (f) connector to the semi-rigid cable.
   Press ***Reflect Cal*** key again.

3. Remove coaxial short from semi-rigid cable and connect a 50 Ω load APC 3.5 (f) to semi-rigid cable.
   Press ***Reflect Cal*** key again.

4. Remove 50 Ω load from semi-rigid cable and reconnect semi-rigid cable to channel 2.
   Press ***Clear Display*** key and wait for 16 averages to accumulate.

5. Press ***Network*** menu key.
   Press ***Reflect/Trans/Cal*** key until reflect is highlighted.

6. Set normalized risetime to 30 ps.
   Press ***Normalize to mem 1*** key.

7. Press ***Stop*** key.
   Press ***Clear Display*** key.

8. Press ***Cursor Chan 1*** until ***cursor memory 1*** is highlighted.

9. Press ***Min & Max Reflect*** key.
   The absolute value of Rho minimum and Rho maximum should be <5%.

13. Press ***Run*** key.

14. Loosen connection where semi-rigid S and U cables join together.
    Move semi-rigid cable from channel 2 to channel 3 and press ***Clear Display*** key.
    Retighten connection where semi-rigid S and U cables join together.

15. Repeat steps 6 through 13 for channel 3.

16. Loosen connection where semi-rigid S and U cables join together.
    Move semi-rigid from channel 3 to channel 4 and press ***Clear Display*** key.
    Retighten connection where semi-rigid S and U cables join together.

17. Repeat steps 6 through 13 for channel 4.

18. Loosen joint where semi-rigid S and U cables join together.
    Move semi-rigid cable from channel 4 to external trigger input and press ***Clear Display*** key.
    Retighten connection where semi-rigid S and U cables join together.

19. Repeat steps 6 through 13 for external trigger input except change normalize risetime from 30 ps to 100 ps and change the RHO limits from 5% to 10%.

20. Remove the semi-rigid S and U cables from the oscilloscope.
    Connect the precision short to channel 1's input APC 3.5 connector.

21. Change offset to 0 V.

22. Change sweep speed to 2 ns/div and delay to 35 ns.

23. Press ***Delta V*** key.

24. Press ***Marker 1 position*** and overlay this marker on the center of the trace.

25. Press ***Marker 2 position*** and overlay this marker on the highest portion of ringing which occurs near center screen and is greater than marker 1.

26. The delta V value should be < 10 mV.

27. Reposition marker 2 to the highest portion of ringing which occurs near center screen and is less than marker 1.

28. The absolute value of Delta V should be < 10 mV.

Table 3-1. Performance Test Record

Hewlett-Packard
Model 54120T
Digitizing Oscilloscope

Tested by _____

Work Order No. _____

Date Tested _____

HP 54120A Serial No. _____

HP 54121A Serial No. _____

Recommended Calibration

Interval ____ Months

Paragraph No	Test	Results	
3-7	Low bandwidth 12.4 GHz	Minimum	Maximum
	channel 1	_____	-2.99 dB
	channel 2	_____	-2.99 dB
	channel 3	_____	-2.99 dB
	channel 4	_____	-2.99 dB
	High bandwidth 18 GHz		
	channel 1	_____	-2.99 dB
	High bandwidth 20 GHz		
	channel 1	_____	-3.49 dB
	channel 2	_____	-2.99 dB
	channel 3	_____	-2.99 dB
	channel 4	_____	-2.99 dB

Table 3-1. Performance Test Record (continued)

Paragraph No	Test	Results		
3-8	Channel 1 dc Accuracy Test	Minimum	Actual	Maximum
	12.4 GHz BW mode 0 V offset	-2.16 mV	_____	2.16 mV
	20 GHz BW mode 0 V offset	-2.16 mV	_____	2.16 mV
	+ Offset Gain 500 mV offset	496 mV	_____	504 mV
	- Offset Gain -500 mV offset	-504 mV	_____	-496 mV
	Delta V Offset Gain	992 mV	_____	1.0080 V
	+ Sampler Gain 250 mV offset	240.34 mV	_____	259.66 mV
	- Sampler Gain -250 mV offset	-259.66 mV	_____	-240.34 mV
	RMS noise 0 V offset		_____	1 mV
	Channel 2 dc Accuracy Test			
	12.4 GHz BW mode 0 V offset	-2.16 mV	_____	2.16 mV
	20 GHz BW mode 0 V offset	-2.16 mV	_____	2.16 mV
	+ Offset Gain 500 mV offset	496 mV	_____	504 mV
	- Offset Gain -500 mV offset	-504 mV	_____	-496 mV
	Delta V Offset Gain	992 mV	_____	1.0080 V
	+ Sampler Gain 250 mV offset	240.34 mV	_____	259.66 mV
	- Sampler Gain -250 mV offset	-259.66 mV	_____	-240.34 mV
	RMS noise 0 V offset		_____	1 mV

Table 3-1. Performance Test Record (continued)

Paragraph No	Test	Results		
3-8	Channel 3 dc Accuracy Test	Minimum	Actual	Maximum
	12.4 GHz BW mode 0 V offset	-2.16 mV	_____	2.16 mV
	20 GHz BW mode 0 V offset	-2.16 mV	_____	2.16 mV
	+ Offset Gain 500 mV offset	496 mV	_____	504 mV
	- Offset Gain -500 mV offset	-504 mV	_____	-496 mV
	Delta V Offset Gain	992 mV	_____	1.0080 V
	+ Sampler Gain 250 mV offset	240.34 mV	_____	259.66 mV
	- Sampler Gain -250 mV offset	-259.66 mV	_____	-240.34 mV
	RMS noise 0 V offset		_____	1 mV
	Channel 4 dc Accuracy Test			
	12.4 GHz BW mode 0 V offset	-2.16 mV	_____	2.16 mV
	20 GHz BW mode 0 V offset	-2.16 mV	_____	2.16 mV
	+ Offset Gain 500 mV offset	496 mV	_____	504 mV
	- Offset Gain -500 mV offset	-504 mV	_____	-496 mV
	Delta V Offset Gain	992 mV	_____	1.0080 V
	+ Sampler Gain 250 mV offset	240.34 mV	_____	259.66 mV
	- Sampler Gain -250 mV offset	-259.66 mV	_____	-240.34 mV
	RMS noise 0 V offset		_____	1 mV

Table 3-1. Performance Test Record (continued)

Paragraph No	Test		Results		
3-9	Short Delta T		Minimum	Actual	Maximum
	Delay Setting	16 ns	40.0 ps	_____	60.2 ps
		18 ns	40.0 ps	_____	60.2 ps
		19.9 ns	40.0 ps	_____	60.2 ps
		19.95 ns	40.0 ps	_____	60.2 ps
		23.95 ns	40.0 ps	_____	60.2 ps
		27.95 ns	40.0 ps	_____	60.2 ps
		55.95 ns	40.0 ps	_____	60.2 ps
	Long Delta T Frequency	10 GHz	89.9 ps	_____	110.1 ps
		5 GHz	189.8 ps	_____	210.2 ps
		2 GHz	489.5 ps	_____	510.5 ps
		1 GHz	.9890 ns	_____	1.011 ns
		500 MHz	1.988 ns	_____	2.012 ns
		200 MHz	4.985 ns	_____	5.015 ns
		100 MHz	9.980 ns	_____	10.02 ns
		50 MHz	19.97 ns	_____	20.03 ns
		20 MHz	49.95 ns	_____	50.06 ns

Table 3-1. Performance Test Record (continued)

Paragraph No	Test		Results		
3-9	Frequency	10 MHz	99.89 ns	_____	100.11 ns
		5 MHz	199.79 ns	_____	200.21 ns
		2 MHz	499.49 ns	_____	500.51 ns
		1 MHz	.99899 us	_____	1.00101 us
		500 KHz	1.99799 us	_____	2.00201 us
		200 KHz	4.99499 us	_____	5.00501 us
		100 KHz	9.98999 us	_____	10.01001 us
		50 KHz	19.97999 us	_____	20.02001 us
		20 KHz	49.94999 us	_____	50.05001 us
		10 KHz	99.89999 us	_____	100.10001 us
3-10	Trigger Sensitivity Test		Minimum	Actual	Maximum
	Trigger hysteresis	Vpos		_____	
		Vneg		_____	
		Vhyst	40 mV	_____	
	100 MHz	Vpos		_____	
		Vneg		_____	
		Vsense	40 mV	_____	
	500 MHz	Vpos		_____	
		Vneg		_____	
		Vsense	100 mV		
3-11	Jitter Test		Minimum	Actual	Maximum
				_____	5.8 ps

Table 3-1. Performance Test Record (continued)

Paragraph No	Test	Results		
3-12	TDR system	Minimum	Actual	Maximum
	Low level	-2 mV	_____	+2 mV
	High level	198 mV	_____	202 mV
	Flatness >1 ns: -1%	-1%	_____	
	+1%		_____	+1%
	<1 ns: -2%	-2%	_____	
	+5%		_____	+5%
	Risetime		_____	45 ps
3-14	Input Reflection	Minimum	Actual	Maximum
	Channel 2 pos.		_____	5%
	neg.		_____	5%
	Channel 3 pos.		_____	5%
	neg.		_____	5%
	Channel 4 pos.		_____	5%
	neg.		_____	5%
	External trigger pos.		_____	10%
	neg.		_____	10%
	Channel 1 pos.		_____	5%
	neg.		_____	5%

TABLE OF CONTENTS

ADJUSTMENTS

SECTION 4

ADJUSTMENTS

4-1. INTRODUCTION

This section describes the adjustments for returning the instrument to peak operating capabilities after repairs have been made or during routine preventive maintenance. In this section the HP 54120A Digitizing Oscilloscope Mainframe will be referred to as the mainframe, and the HP 54121A Four Channel Test Set will be referred to as the the four channel test set.

WARNING

Read the "Safety Summary" at the front of this manual before performing adjustment procedures. The instrument should be disconnected from all voltage sources before it is opened for any adjustments, replacements, maintenance, or repairs.

CAUTION

The four channel test set is very sensitive to static discharge. Failure to observe proper antistatic procedures may result in damage to the gallium arsenide samplers. Perform all maintenance or operation while using the antistatic mat and wrist strap supplied with the instrument.

4-2. ADJUSTMENT INTERVAL

To maintain proper calibration, these adjustments should be made at approximately one year or after 2000 hours of operation, whichever is less. Some or all of these adjustments may need to be made after repairs have been completed. Amount of use, environmental conditions, and the user's experience concerning need for adjustment verification will contribute in deciding the adjustment interval.

4-3. RECOMMENDED TEST EQUIPMENT

Table 1-1 lists the recommended test equipment to use for the adjustment procedures. Any equipment that satisfies the critical specifications may be used.

4-4. RECOMMENDED ADJUSTMENT SEQUENCE

Table 4-1 lists the factory recommended sequence of adjustments.

Table 4-1. Recommended Adjustment Sequence

Power Supply Adjustments
Delta Current Adjustment
10.000 Reference Voltage Adjustment
Range Adjustment
Step Recovery Diode (SRD) Adjustments
Frequency and TB Fine Tune Adjustments
END and 4 ns CAL Adjustments
Sampler Bias Adjustments
Vertical Soft Cal
Offset Gain Adjustments
TDR Step Adjustments
Feedthrough Compensation Adjustments
Trigger Hysteresis and Offset Null Adjustments
Channel Skew Calibration

4-5. SPECIAL PROCEDURES

1. All connectors should be clean and undamaged to ensure accurate measurements. Check all test set APC 3.5 (f-f) connectors mechanically and visually before inserting any calibration test tool in them. Damaged connectors or loose connections may cause unreliable adjustment results. See Appendix A at the end of this manual.

2. The HP 54120T should be allowed to warm up for at least 15 minutes.

3. To avoid damage to the HP 54121A Four Channel Test Set connectors, use of the APC 3.5 (f-f) connector savers is encouraged. These connector savers are supplied with the HP 54120T. Refer to Appendix A for information on what happens to APC 3.5 connectors when they're used with SMA connectors.

4. Avoid sharp bends in the two 17-inch coaxial cables, HP part numbers 8120-4941 and 8120-4942.

5. When mating APC 3.5 connectors to APC 3.5 connectors or devices, torque all connections to 8 in/lbs. When mating APC 3.5 to SMA or SMA to SMA, torque all connections to 5 in/lbs.

6. Do as little connector swapping as possible during the procedures. APC 3.5 and SMA connectors wear out with age. All test tool connectors should be inspected both visually and mechanically every few calibrations.

7. The adjustment procedures outlined in this section make use of extra connectors. These are used to save expensive parts from repeated excessive wear caused by many reconnections. These parts are unnecessary, but their use is highly advised. They will not interfere with measurement capabilities.

8. Throughout the procedure identical connectors are used in different ways. One way is precision at both ends. This means that both ends of the APC 3.5 connector should be precise and should never be connected to an SMA connector. The other way is precise at one end. This means that one of the APC 3.5 ends may be used with SMA connectors, but the other end should never be connected to any SMA connectors. Unless otherwise stated, all APC 3.5 calibration test connectors should never be connected to SMA connectors.

4-6. POWER SUPPLY ADJUSTMENTS

Description:

This procedure is for adjusting the power supply voltages in cases when either the power supplies have been inadvertently mis-adjusted or when repairs have been made.

NOTE

The power supply voltages are factory set and rarely require re-adjustment.

Equipment Recommended:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DMM	Better than 0.3% accuracy	HP 3478A

Analog Power Supply Procedure:

This procedure adjusts the fan supply voltage.

The test point locations are marked on the power supply cover and on the Analog PC assembly (A12). A12R61 is the only adjustment on the Analog Power Supply assembly. This adjustment has been eliminated in recently manufactured instruments. Before continuing with this procedure, check to see if your instrument contains A12R61.

NOTE

The instrument ***MUST*** be stabilized at ambient temperature with front-panel power switch to STBY before this adjustment is made. The fan voltage will increase with the instrument's internal temperature. If the instrument is not allowed to cool down, the following voltage measurement and adjustment will be inaccurate.

1. Remove two top rear feet from mainframe.
2. Remove top cover from mainframe.
3. Connect positive voltmeter lead to FAN test point.
4. Connect negative voltmeter lead to -18 V test point.
5. Turn instrument's front-panel power switch to ON.
6. Before the instrument warms up, adjust A12R61 for a voltmeter reading of 9.5 V ±100 mV.

Digital Power Supply Procedure:

The test point locations are marked on the power supply cover and on the Digital PC assembly (A13). A13R56 is the only adjustment on the Digital Power Supply assembly. First, the voltage is measured to see if any adjustment is required.

1. Turn instrument on and allow it to warm up for approximately two minutes.
2. Connect positive voltmeter lead to +5 V test point (actual voltage = +5.1 V).
3. Connect negative voltmeter lead to -5 V test point (actual voltage = -5.3 V).
4. The voltmeter should read 10.4 Vdc ±10 mV. If the measurement is within specifications, stop here. If the measurement is out of specifications, then continue with steps 5-11.
5. Disconnect power cord and remove voltmeter leads.

WARNING

Hazardous voltages capable of causing injury or death are present on the AC Power Supply assembly (A11) when power is applied and for a period of time after power is removed from the instrument. To avoid this hazard, DO NOT remove the power supply shield until the LED on the AC Power Supply assembly (A11) is extinguished. This LED is visible through an inspection hole in the cover labeled "+300 V WHEN LAMP IS ON".

6. When the +300 V lamp is extinguished, remove the top power supply cover.
7. Reconnect positive voltmeter lead to +5 V test point.
8. Reconnect negative voltmeter lead to -5 V test point.
9. Reconnect power cord and turn instrument on. Allow instrument to warm up for approximately two minutes.
10. Adjust A13R56 for a voltmeter reading of 10.4 Vdc ±10 mV.
11. Disconnect power cord and wait until +300 V lamp is extinguished on the Primary Power Supply (A11) before re-installing power supply cover.

4-7. TIMEBASE DELTA CURRENT ADJUSTMENT

Description:

This is a timebase system adjustment. After this adjustment is made, any HP 54121A Four Channel Test Set may be used with this mainframe without degrading the timebase accuracy specifications.

To accomplish this, A3R29 (R29 on the Horizontal Control board) is adjusted so that the delta (change) in output current flow from the fine delay DAC on the Horizontal Control board to the four channel test set is 9.7632 mA, when delay is switched from 16.000 ns to 19.999 ns.

The procedure consists of three main parts.

1. Steps 1-6 measure the resistance of A3R46. This is the resistance value in the ohm's law formula I = E ÷ R used in step 12.

2. Steps 6-12 measure the voltage across A3R46 with the oscilloscope's timebase delay set to 16.000 ns. This is the voltage value in the ohm's law formula I = E ÷ R used in step 12.

3. Steps 13-21 calculate the desired delta current across A3R46 when the oscilloscope's timebase delay is changed from 16.000 ns to 19.999 ns. A3R29 is adjusted if the measured delta current does not equal the desired delta current.

Equipment Recommended:

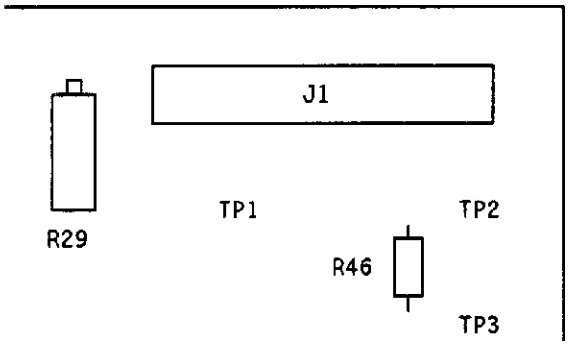
INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DMM	40 μV and 24 milliohm accuracy	HP 3478A
Clip lead	Alligator to alligator	N/A

Procedure:

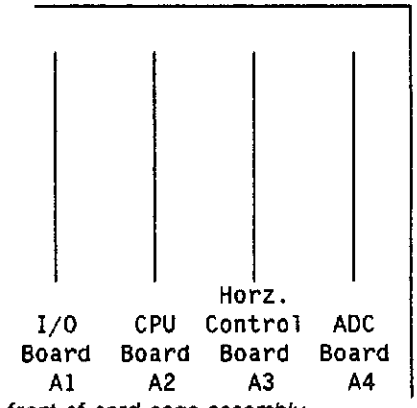
Part 1: Determining R in the ohm's law formula I = E ÷ R

1. Turn mainframe's front-panel power switch to STBY.
2. Place DMM in four-wire resistance measurement mode.
3. Connect one end of alligator clip lead to (A3) TP2.
4. Connect both positive DMM leads to other end of alligator clip lead.
5. Connect both negative DMM leads to ground point TP3.

Top-Rear Corner of Horizontal Control Assembly (A3)



Top View of Mainframe's Card Cage



front of card cage assembly

6. Record resistance reading in steps 12 and 14 (2 places after the decimal are required). An example might be 200.06 Ω.
   Leave DMM connected across A3R46.

Part 2: Determining E in the ohm's law formula I = E ÷ R

7. Disconnect the ribbon cables which attach to the rear of the horizontal control and ADC assemblies.
8. Change DMM to make voltage measurements.
9. Short Horizontal Control assembly (A3) test point TP1 to TP2.
10. Turn mainframe on, and set timebase delay to 16 ns.
11. Record DMM voltage reading in step 12 (5 places after the decimal are required.
    An example might be -1.00039.

12. Record DMM voltage reading from step 11 here _____ V Example -1.00039 V
    Record DMM resistance reading from step 6 here _____ Ω Example 200.06 Ω
    Divide voltage by resistance to obtain current _____ mA Example 5.0004 mA
    (four digits after the decimal are required, and drop the negative sign).

    The result of the calculation is the fine delay DAC output current at delay value of 16.000 ns. Record this value in step 13.

Part 3: Steps 13-21 calculate the value to which A3R29 should be set.

13. Subtract the current result in step 12 from desired delta current 9.7632 mA.
    9.7632 mA - (_____ mA) = _____ mA. Record this value in step 14.

    Example: 9.7632 mA - 5.0004 mA = 4.7628 mA

14. Convert calculated current from step 13 to a voltage value by multiplying it by the resistance value in step 6.

    Record calculated current from step 13 here _____ mA Example 4.7628 mA
    Record DMM resistance reading from step 5 here _____ Ω Example 200.06 Ω
    Multiply resistance by current to obtain a voltage _____ V Example .95284576 V

15. Round voltage value from step 14 to 5 decimal places _____

    Example: .95285 V

16. Change mainframe's timebase delay setting to 19.999 ns.

17. With DMM still connected across TP2 and TP3, check DMM voltage reading.
    If voltmeter reading is equal to calculated voltage in step 15, then go to step 18.
    Otherwise, adjust A3R29 for a DMM voltage reading as close as possible to the calculated value in step 15.

18. Turn mainframe's front-panel power switch to STBY.

19. Remove short from TP1 to TP2.

20. Disconnect DMM from mainframe.

21. Reconnect umbilical cable to mainframe and tighten attaching screws.

4-8. 10 VOLT REFERENCE ADJUSTMENT

Description:

This is a systemizing adjustment so any HP 54121A Four Channel Test Set may be used with this mainframe without degrading the vertical gain specifications.

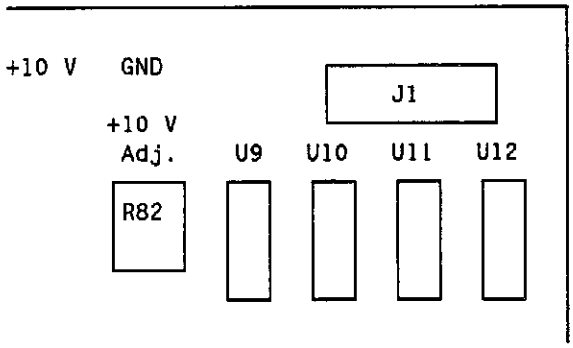
Equipment Recommended:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DMM	.01% accuracy	HP 3478A

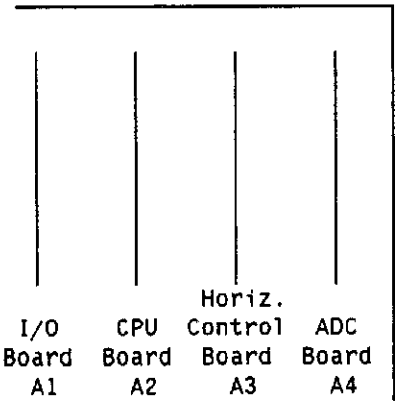
Procedure:

1. Turn mainframe's front-panel power switch to STBY.
2. Connect positive DMM lead to +10 V test point on ADC assembly (A4).
3. Connect negative DMM lead to ground test point next to +10 V test point.
4. Turn mainframe's front-panel power switch to ON.
5. Adjust +10 V ADJUST (R82) for 10 V ±1 mV.

Top-Rear Corner of ADC Assembly (A4)



Top View of Mainframe's Card Cage



6. Disconnect DMM leads from ADC assembly.
7. Re-install mainframe's top cover and two top rear feet.

4-9. RANGE ADJUSTMENT

Description:

This adjustment matches the linear input range of the timebase hybrid to the linear output range of operational amplifier U8 on the Horizontal assembly. Anytime this adjustment is performed, the following adjustments must also be performed; Frequency on paragraph 4-11, end and 4 ns cal on paragraph 4-12. If this adjustment fails, perform the delta current adjustment on paragraph 4-7.

Equipment Recommended:

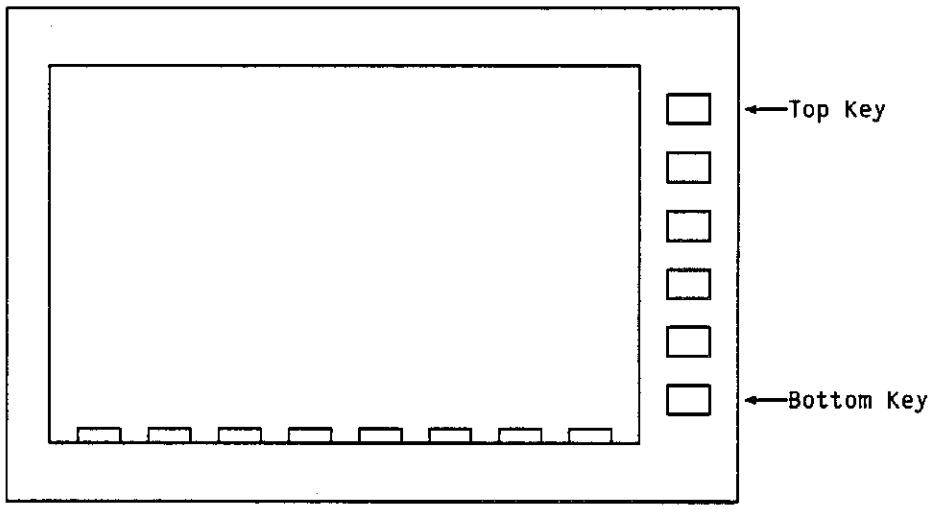
EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DMM	Better than 0.3% accuracy	HP 3478A

Procedure: The adjustment locations are shown on page 4-50.

1. Remove top and bottom covers from four channel test set.

2. Perform two key-down powerup. This must be performed to ensure the value on TP1 is correct, otherwise the adjustment may drift on the next trigger event. Turn oscilloscope's power switch to STBY. Hold down top and bottom function keys immediately to right of screen. Turn oscilloscope's power switch to ON. Continue holding function keys until graticule display is on screen. Ignore "Front Panel Cals Lost" warnings on top of screen; CALs will be performed later.

Keys to Hold Down for Two Key-Down PowerUp.



3. Change timebase delay to 18 ns, and sweep to Trg'd mode.

4. Connect positive DMM lead to Horizontal Board (A1) TP1. The horizontal assembly is on the test set's bottom side. Connect negative DMM lead to chassis ground near TP1.

5. Adjust RANGE (R52) for a reading of 5 V ±1 V on DMM.

4-10. STEP RECOVERY DIODE (SRD) ADJUSTMENTS

Description:

The sampler hybrids for each channel contain step recovery diodes. The bias on these diodes is adjusted for optimum performance. SRD BIAS adjusts the bias of the step recovery diode for a zero temperature coefficient. SRD DRIVE adjusts the output level of the sample pulse generator. SRD DRIVE affects the bandwidth of all four channels simultaneously. Anytime this adjustment is performed, SBIAS in paragraph 4-13 and offset gain in paragraph 4-14 must also be performed. If this adjustment fails, readjust the 10 V reference adjustment in paragraph 4-8.

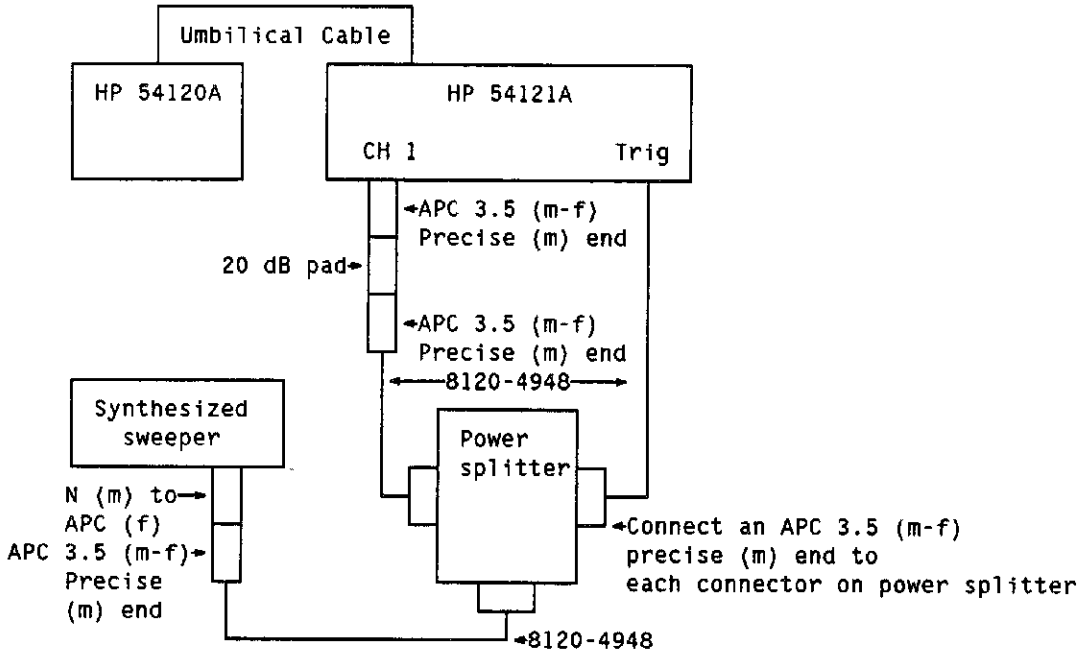
Equipment Recommended: This list is used in paragraphs 4-11, 12, 13, and 18.

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Synthesized sweep oscillator	20 GHz +12 dBm	HP 8341B/003
Power splitter	APC 3.5 connectors	HP 11667B
20 dB pad	APC 3.5 connections	HP 33340C/020
ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
Adapter APC 3.5 (m-f)	26.5 GHz (male end precise) Quantity needed - 6	1250-1866
Adapter N (m) to APC 3.5 (f)		1250-1744
Coaxial cable APC 3.5 (m-m)	18 GHz Quantity needed - 3	8120-4948

NOTE

If this adjustment is performed out of the normal adjustment sequence, (refer to table 4-2) a two key-down powerup must be performed first.

Equipment Connections: This setup is used in sections 4-11, 12, 13, and 18.



Equipment Setup:

Signal Source

Frequency	250 MHz
Amplitude	+12 dBm

HP 54120T

Display

Display Mode	Averaged
No. of Averages	4
Screen	Single
Graticule	Grid
Bandwidth	12.4 GHz

Channels

Channel 1	On
Volts/Div	20 mV/div
Offset	Center signal
Channels 2-4	Off
Attenuation	1.0

Timebase

Time/Div	500 ps/div
Delay	16 ns
Delay Ref. at	Left
Sweep	Trg'd

Trigger

Trigger Level	0 V
Slope	Pos
Attenuation	1
HF Sense	Off
HF Reject	Off

Procedure: The adjustment locations are shown on page 4-50.

NOTE

It is mandatory that step 1 in this procedure be performed, otherwise the SBIAS adjustment on paragraph 4-13 will fail.

1. Preset LB1 (R153) and OG1 (R113) on Vertical assembly (A2) to mechanical center. The Vertical assembly is on top side of four channel test set.
2. Readjust channel offset to recenter signal on screen.
3. Press ***Delta V*** key.
4. Turn ***V Markers*** on and overlay them on channel 1.
5. Press ***Preset Levels*** until variable is highlighted.
6. Preset Variable Levels to -15% and +115%. Use oscilloscope's offset to center signal.
7. Press ***Auto Level Set*** key.
8. Press ***Display Mode*** key.
9. Set Display Mode to a persistence of 300 ms.
10. Preset SRD BIAS (R168) on Horizontal assembly (A1) to mechanical center.
11. Adjust SRD DRIVE (R167) (A1) for a signal amplitude of -15% and +115% on screen.

Note

An offset may exist in the signal during this portion of the adjustments. If the signal peaks do not overlay the -15% and +115% markers, adjust SRD DRIVE for equal amounts of signal above or below the markers. In the following steps. The offset level may be adjusted any time during this procedure.

12. Slowly adjust SRD BIAS (R168) for maximum signal amplitude. The waveform will compress and slightly increase in amplitude, R168 must be adjusted slowly to see the slight amplitude increase.
13. Readjust steps 11 and 12 until maximum signal amplitude is -15% and +115%.
14. Turn ***V Markers*** Off.

4-11. FREQUENCY ADJUSTMENTS

Description:

This adjusts the 250 MHz timebase oscillator inside the timebase hybrid. A trimmer cap (FREQ) on the timebase hybrid is a coarse adjustment, and TB FINE TUNE (A1R54) is a fine adjustment. Anytime this adjustment is performed, the END and 4 ns cal adjustments must also be performed. If this adjustment fails, perform the delta current adjustment in paragraph 4-7, and the range adjustment in paragraph 4-10.

Equipment Recommended and Connections:

Refer to section 4-10.

There is a coarse frequency adjustment on the timebase hybrid (FREQ). This coarse adjustment normally only needs adjusted if the timebase hybrid has been replaced. Normally the TB FINE TUNE adjustment should have enough range to compensate for slight variances in the coarse adjustment. If the coarse adjustment needs to be performed, a non-metallic tool with a blade .010 inches thick and .040 inches wide is used. An HP part number 8710-1300 adjustment tool filed down to fit the adjustment size is adequate.

Equipment Setup:

Signal Source

Frequency	250 MHz
Amplitude	+12 dBm

HP 54120T

Display		Timebase	
Display Mode	Averaged	Time/Div	500 ps/div
No. of Averages	4	Delay	16 ns
Screen	Single	Delay Ref at	Left
Graticule	Grid	Sweep	Trg'd
Bandwidth	12.4 GHz		
Channels		**Trigger**	
Channel 1	On	Trigger Level	0 V
Volts/Div	20 mV/div	Slope	Pos
Offset	0 V	Attenuation	1
Channels 2-4	Off	HF Sense	Off
Attenuation	1	HF Reject	Off

Procedure: The adjustment locations are shown on page 4-50.

NOTE

For best results with this procedure, perform all adjustments with the test set in a normal operating position.

1. Adjust oscilloscope's offset to center signal vertically.
2. Adjust oscilloscope's trigger level until trace's positive or negative slope begins near center horizontal graticule on the screen's left side and remains triggered.
3. Press ***Measure*** key, then ***Frequency*** key.
   If the results are 250 MHz ±250 KHz, go to step 6; otherwise go to step 4.
4. Remove tape from FREQ (frequency) adjustment (trimmer capacitor on U9) on horizontal assembly.
5. Remeasure the frequency while making small incremental adjustments to the FREQ adjustment capacitor on the timebase hybrid with a 40/1000 inch non-metallic alignment tool. After the frequency measures 250 MHz ±250 KHz, proceed with step 6.
6. Change timebase time/div to 200 ns/div.
7. Observe a nearly flat horizontal trace on screen. If the trace is horizontally flat ±1 major division, then go to step 12. Otherwise, go to step 8.
8. Preset TB FINE TUNE (R54) on Horizontal assembly to mechanical center.
9. Adjust FREQ adjustment on timebase hybrid until the trace is flat ±1 major division.
10. Replace tape over FREQ. adjustment on U9. Masking tape or electrical tape may be used if the original tape is misplaced or damaged. The tape is needed to prevent air currents from upsetting the thermal stability of the timebase hybrid.
11. Allow 10 minutes for U9 to stabilize its temperature, with tape over Freq. adjustment hole.
12. Change timebase time/div to 1 μs/div.
13. Adjust TB FINE TUNE (R54) for flattest trace possible on screen.

4-12. END and 4 ns CAL ADJUSTMENTS

Description:

The timebase hybrid operates at 250 MHz which is a 4 ns period. END adjusts the timebase ramp's ending point to the next timebase ramp's beginning point. The 4 ns CAL adjusts the discontinuity which occurs at 4 ns intervals after 16 ns. The END adjustment must be performed before the 4 ns CAL adjustment. If this adjustment fails, perform the delta current adjustment in paragraph 4-7, range adjustment in paragraph 4-9, and frequency adjustments in paragraph 4-11

Equipment Recommended and Connections:

Refer to section 4-10.

Equipment Setup:

Signal Source

Frequency	250 MHz
Amplitude	+12 dBm

HP 54120T

Display		Timebase	
Display Mode	Averaged	Time/Div	500 ps/div
No. of Averages	4	Delay	16 ns
Screen	Single	Delay Ref. at	Left
Graticule	Grid	Sweep	Trg'd
Bandwidth	12.4 GHz		
Channels		Trigger	
Channel 1	On	Trigger Level	0 V
Volts/Div	20 mV/div	Slope	Pos
Offset	Center signal	Attenuation	1
Channels 2-4	Off	HF Sense	Off
Attenuation	1.0	HF Reject	Off

Procedure: The adjustment locations are shown on page 4-50.

1. Preset 4 ns CAL (R62) on Horizontal assembly (A1) to mechanical center.
2. Adjust END (R61) for a small amount of trace discontinuity at beginning of eighth vertical graticule division. See figure 4-1. If necessary, adjust oscilloscope's trigger level to center trace discontinuity vertically on screen.
3. Change timebase time/div to 10 ps/div and delay to 59.95 ns.
4. Change volts/div to 2 mV/div.
5. If necessary, adjust oscilloscope's trigger level in order to center trace discontinuity vertically on screen. See figure 4-2.
6. Readjust END (R61) to eliminate trace discontinuity. See figure 4-3.
7. Change timebase delay to 19.95 ns.
8. Adjust 4 ns cal (R62) on Horizontal assembly to eliminate discontinuity.
9. Change timebase delay to 59.95 ns. If necessary repeat steps 6 through 8 until discontinuity at both 19.95 ns and 59.95 ns is minimized.

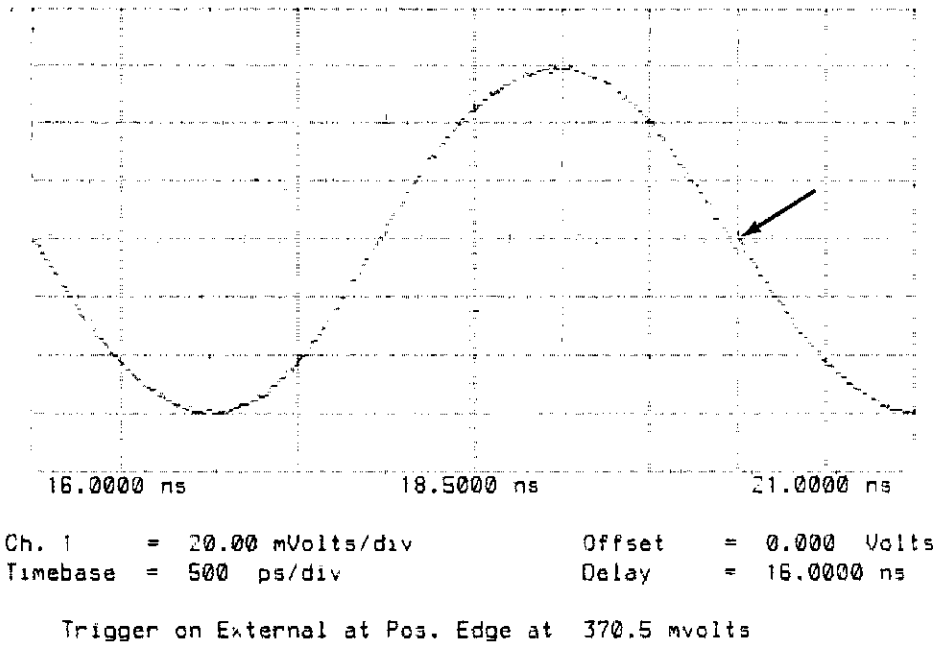


Figure 4-1. Small Amount of Trace Discontinuity on Eighth Graticule.

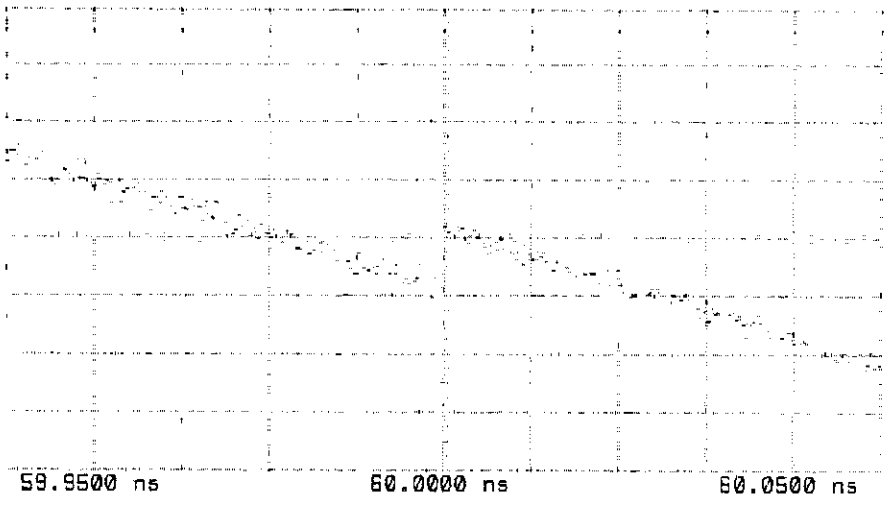


Figure 4-2. Expanded Trace Discontinuity.

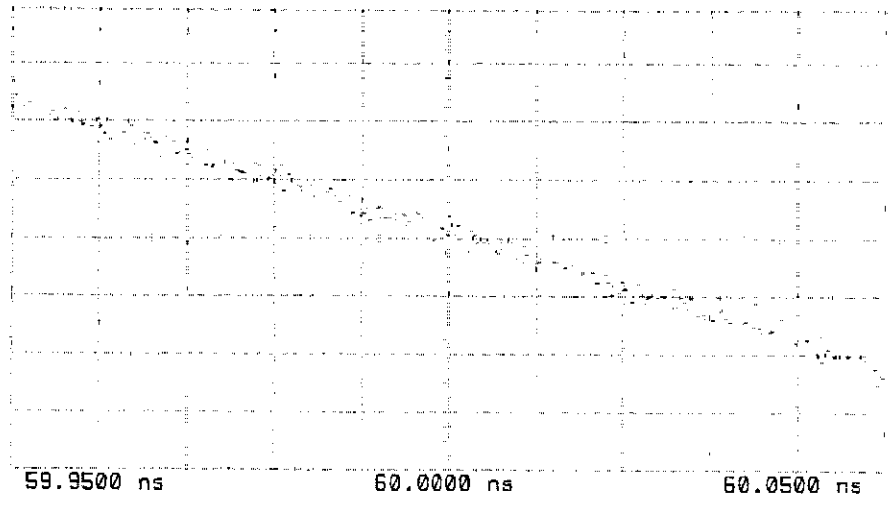


Figure 4-3. Correct END Adjustment, No Remaining Trace Discontinuity.

4-13. SAMPLER BIAS ADJUSTMENTS

Description:

This procedure adjusts the bandwidth of individual channels for low bandwidth (12.4 GHz) and for high bandwidth (20 GHz). If this adjustment fails, perform the 10 V reference adjustment on paragraph 4-8, and SRD bias adjustments in paragraph 4-10.

Equipment Recommended and Connections:

Refer to section 4-10.

NOTE

If this adjustment is performed out of the normal adjustment sequence, (refer to table 4-2) a two key-down powerup must be performed first.

Equipment Setup:

Signal Source

Frequency	250 MHz
Amplitude	+12 dBm

HP 54120T

Display		Timebase	
Display Mode	Averaged	Time/Div	1 ns/div
No. of Averages	4	Delay	16 ns
Screen	Single	Reference at	Left
Graticule	Grid	Sweep	Trg'd
Bandwidth	12.4 GHz		
Channels		**Trigger**	
Channel 1	On	Trigger Level	0 V
Volts/Div	20 mV/div (on all 4 channels)	Slope	Pos
		Attenuation	1
Offset	Center signal	HF sense	Off
Channels 2-4	Off	HF reject	Off
Attenuation	1		

Procedure: The adjustment locations are shown on page 4-50.

1. Press ***Delta V*** key.
2. Turn ***V Markers on*** and overlay them on channel 1.
3. Press ***Preset Levels*** until 0-100% is highlighted.
4. Press ***Auto Level Set*** key.
5. Change Display Mode to 300 ms persistence.
6. Adjust LB1 (R153) on Vertical assembly (A2) for a signal amplitude of 0 to 100%. Adjustment LB1 is Low Bandwidth for channel 1 only. See figure 4-4. If the signal does not line up with the markers, adjust for equal amounts above or below the markers.

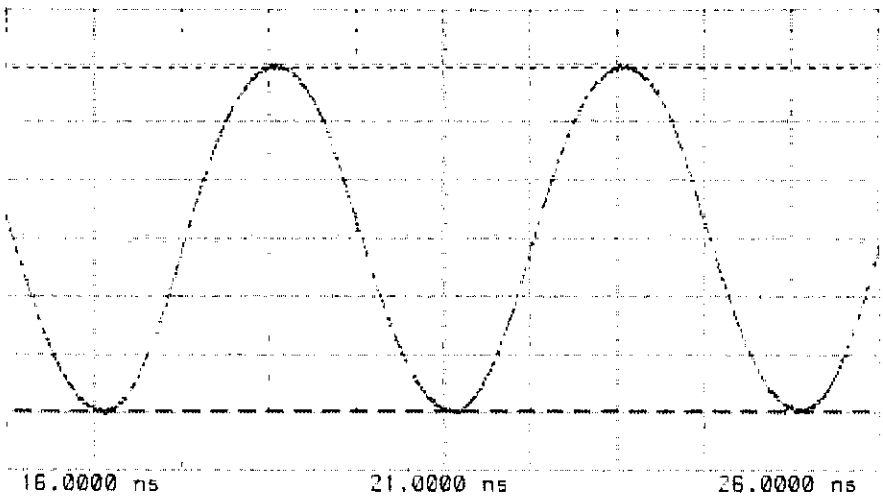


Figure 4-4. Low Bandwidth Adjustment with 0 to 100% Delta V Markers.

7. Change Display Mode to Averaged.
8. Change Bandwidth to 20 GHz.
9. Press ***Delta V*** key.
10. Press ***Preset Levels*** key until variable is highlighted.
11. Press ***Variable*** key and set levels to 30%-70%.
12. Press ***Auto Level Set*** key.
13. Press ***Clear Display*** key and notice that trace on screen temporarily decreases in size.
14. Continue to press ***Clear Display*** key (about 2 times a second) while making small adjustment increments to HB1 (R161) until signal amplitude overlays the 30% and 70% markers. See figure 4-5. Adjustment HB1 is High Bandwidth adjustment for channel 1 only.

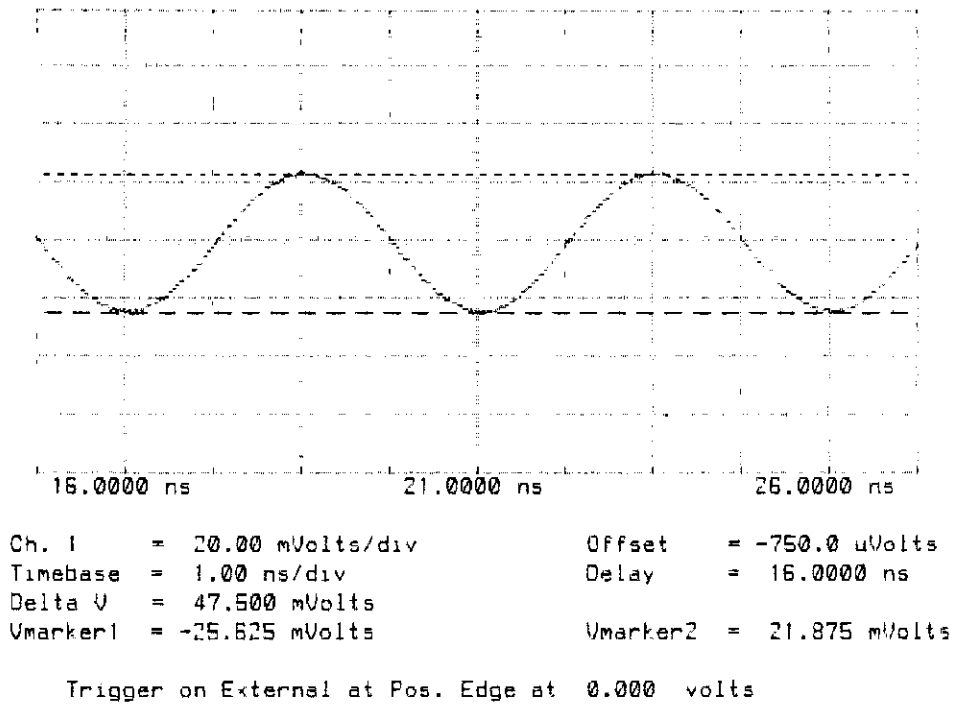


Figure 4-5. High Bandwidth Adjustment with 30 to 70% Delta V Markers.

15. Turn channel 1 display off and channel 2 display on. Change Bandwidth to 12.4 GHz.
16. Move input signal from channel 1 to channel 2.
17. Repeat steps 1-13 for channel 2 except use adjustments LB2 (R154) and HB2 (R162).
18. Turn channel 2 display off and channel 3 display on. Change Bandwidth to 12.4 GHz.
19. Move input signal from channel 2 to channel 3.
20. Repeat steps 1-13 for channel 3 except use adjustments LB3 (R155) and HB3 (R163).
21. Turn channel 3 display off and channel 4 display on. Change Bandwidth to 12.4 GHz.
22. Move input signal from channel 3 to channel 4.
23. Repeat steps 1-13 for channel 4 except use adjustments LB4 (R156) and HB4 (R164).
24. Turn ***Delta V Markers*** Off.
25. Press ***Utility*** key.
26. Press ***Cal Menu*** key.
27. Press ***Vertical Cal*** key and follow instructions on screen.

4-14. OFFSET GAIN ADJUSTMENTS

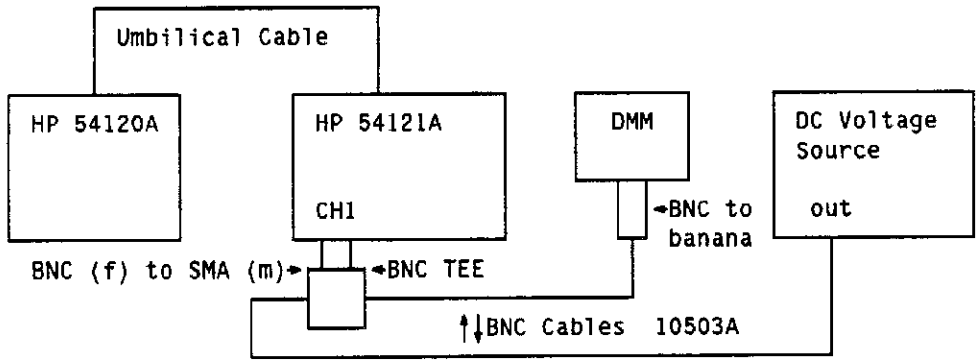
Description:

With the HP 54120T set to the same offset value as a dc voltage source, the OFFSET GAIN for each channel is adjusted until the trace overlays center screen.

Equipment Recommended:

EQUIPMENT REQUIRED	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
DC voltage source	1 mV resolution less than 100 μV ripple	HP 3325A/001
DMM	10 mV accuracy	HP 3478A
ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
BNC (f) to SMA (m)	Adapt dc voltage source to APC 3.5	HP part number 1250-1200
BNC Tee	1 (m) end and 2 (f) ends	1250-0781
BNC cables	Quantity = 2	10503A
Adapter BNC to banana		1250-2277

Equipment Connections:



Equipment Setup:

HP 54120T

Display		Timebase	
Display Mode	Averaged	Time/Div	1 μs/div
No. of Averages	8	Delay	200 ns
Screen	Single	Delay Ref at	Left
Graticule	Grid	Sweep	Freerun
Bandwidth	12.4 GHz	Freerun Rate	10 KHz
Channels		Network	
Channel 1	On	Reflect/Trans/CAL	Reflect
Channels 2-4	Off	Step & Chan 1	Off
Volts/Div	1 mV/div		
Offset	0 V		

Procedure: The adjustment locations are shown on page 4-50.

CAUTION

Exceeding 2 V on the dc power supply may damage the oscilloscope's input.

1. Disconnect all input signals from oscilloscope and perform a vertical CAL routine. Press ***Utility*** menu key, ***Cal Menu*** key, ***Channel Vertical Cal*** key, and follow the screen's instructions.
2. Set dc voltage source for approximately 490 mV.
3. Read dc voltage source's output on DMM to 100 μV accuracy.
4. Change oscilloscope's offset to within 100 μV of reading obtained on DMM.
5. Adjust OG1 (R113) on Vertical assembly (A2) until trace is on center graticule. Adjustment OG1 is Offset Gain adjustment for channel 1 only. Adjust OG1 slowly in small increments, and wait for averages to accumulate.
6. Turn channel 1 off and channel 2 on, then move signal to channel 2's input.
7. Repeat steps 1-4 for channel 2 except adjust OG2 (R114).
8. Turn channel 2 off and channel 3 on, then move signal to channel 3's input.
9. Repeat steps 1-4 for channel 3 except adjust OG3 (R115).
10. Turn channel 3 off and channel 4 on, then move signal to channel 4's input.
11. Repeat steps 1-4 for channel 4 except adjust OG4 (R116).
12. Press ***Utility*** key.
13. Press ***Cal Menu*** key.
14. Press ***Vertical Cal*** key and follow instructions on screen.

4-15. TDR STEP ADJUSTMENTS

Description:

This procedure adjusts the TDR pulse for a risetime of approximately 45 ps, an overshoot between 2.5% and 3.5% in the average mode, and a flat pulse top.

Equipment Setup:

HP 54120T

Display		Timebase		
Display Mode	Averaged	Time/Div	200 ps/div	
No. of Averages	16	Delay	16 ns	
Screen	Single	Delay Ref at	Left	
Graticule	Frame	Sweep	Freerun	**NOTE**
Bandwidth	12.4 GHz	Freerun Rate	10 KHz	
				*Repeatedly pressing the **Clear Display*** key will help in performing the adjustment.
Channels		Network		
Channel 1	On	Reflect/Trans/CAL	Reflect	
Volts/Div	30 mV/div	Step & Chan 1	On	
Offset	100 mV			
Channels 2-4	Off			
Attenuation	1			

Procedure: The adjustment locations are shown on page 4-50.

1. Connect an APC 3.5 precise (m) 50 Ω termination to channel 1.

2. Adjust timebase delay until rising edge is approximately two divisions from left side of screen. See figure 4-6

3. Preset TDR DRIVE (R44) on Horizontal assembly (A1) fully clockwise. Reposition the delay setting to place the edge two divisions from the screen's left side.

4. Preset TDR BIAS (R45) fully counter-clockwise, then slowly adjust TDR Bias clockwise until pulse overshoot just starts to appear (first overshoot). See Figure 4-6. If overshoot is already on screen with TDR BIAS fully counter-clockwise, turn TDR DRIVE slightly counter-clockwise until overshoot disappears. Then increase TDR BIAS clock-wise until overshoot reappears.

5. Press ***Delta T*** key and turn markers on.

6. Set Start Marker to step's leading edge and set Stop Marker 500 ps to right of Start Marker. See figure 4-6.

7. Adjust TDR BIAS until step's rising edge coincides with Stop Marker. See figure 4-7. If this adjustment does not line up with the Stop Marker, return to step 4 and turn TDR DRIVE slightly more counter-clockwise.

8. Adjust TDR DRIVE so pulse overshoot is between 2.5 to 3.5%, use the ***Measure*** menu to check your adjustment. If the TDR DRIVE adjustment moves the edge offscreen, reposition the edge with the more delay.

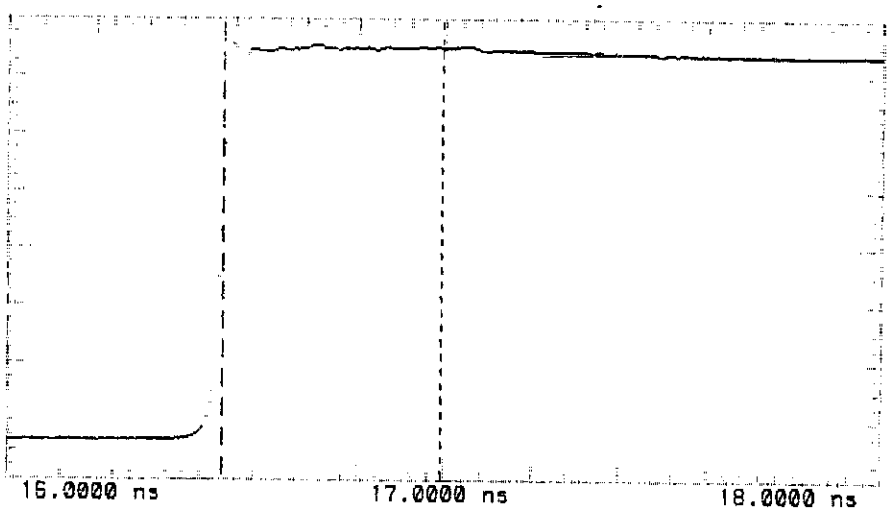


Figure 4-6. Setting Start Marker on TDR Pulse with Some Overshoot and Stop Marker 500 ps Later.

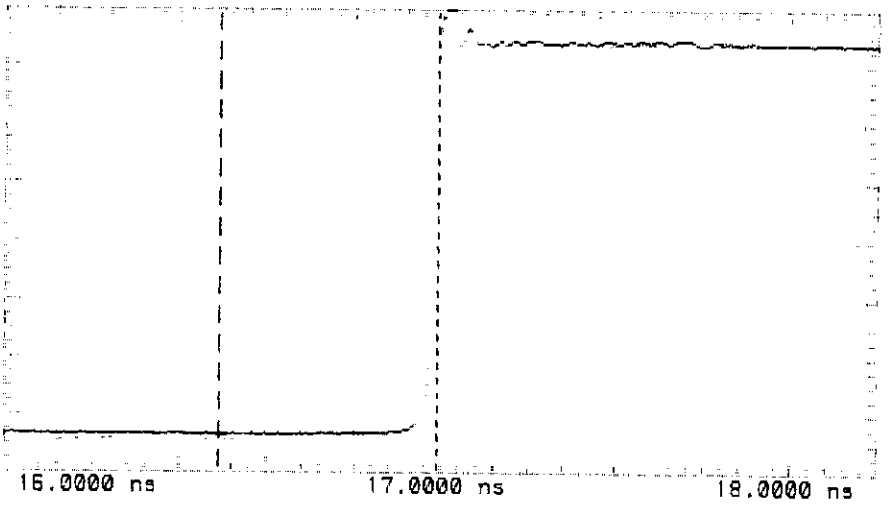


Figure 4-7. Adjusting TDR Pulse to Stop Marker.

9. Select Delta V menu and press ***Preset Levels*** key until ***50-50%*** is highlighted.
   Press ***Auto Level Set*** key.

10. Select Delta T menu and press ***Start on Edge*** key until ***Pos 1*** is highlighted.
    Press ***Stop on Edge*** key until ***Pos 1*** is highlighted.
    Press ***Precise Edge Find*** key.

11. Turn channel 1 off, than turn channel 1 back on again.
    Change Channel 1 sensitivity to 5 mV/div and offset to 0 V.

12. Select Delta V menu and press ***Preset Level*** key until ***50-50%*** is highlighted.
    Press ***Auto Level Set*** key.
    Change marker 1's value to 200 mV and adjust front panel RPG control until Delta V equals -200 mV.

13. Select Network menu and press ***Reflect/Trans/Cal*** key until ***Reflect*** is highlighted.
    Press ***Step & Chan 1*** key until ***On*** is highlighted.

14. Select Delta T menu and change Stop marker's value to Start marker's value plus 1 ns.

15. Change timebase sweep speed to 100 ns/div, delay to Stop marker's value, and channel 1 offset to 200 mV.

16. Select Delta V menu and ensure that marker 1's position is highlighted.

17. Adjust TOP (R169) on Horizontal Assembly (A1) until trace on right edge of screen coincides with marker 1's position. Refer to figure 4-8.

18. Change timebase sweep speed to 50 ps/div, delay to 16 ns, and channel 1 offset to 0 V.

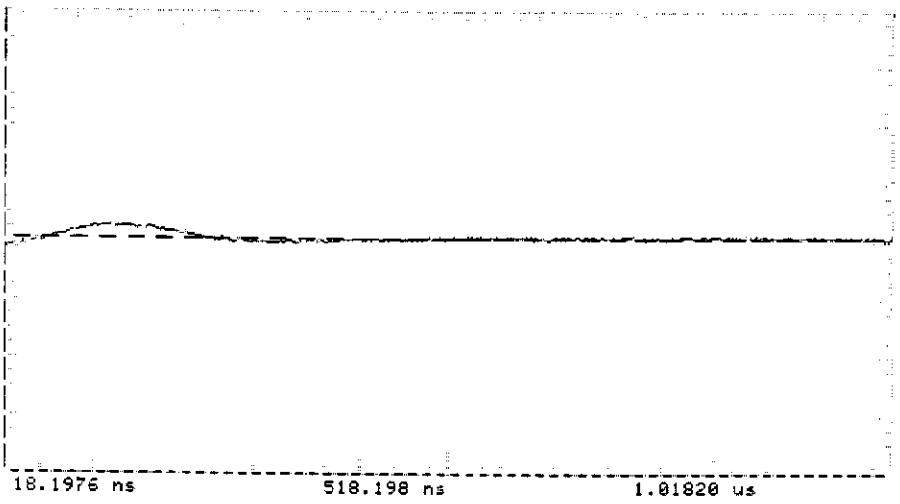
19. Select Delta V menu and ensure marker 2's position is highlighted.

20. Adjust BOTTOM (R170) on Horizontal Assembly (A1) until trace coincides with marker 2's position.

21. Change timebase delay to Start marker's value, and channel 1 offset to 200 mV.

22. Change marker 2's value equal to marker 1's value.
    Adjust front panel RPG control for a Delta V reading of between 5 to 7 mV
    (this will correspond to an overshoot of about 2.5 to 3.5%).

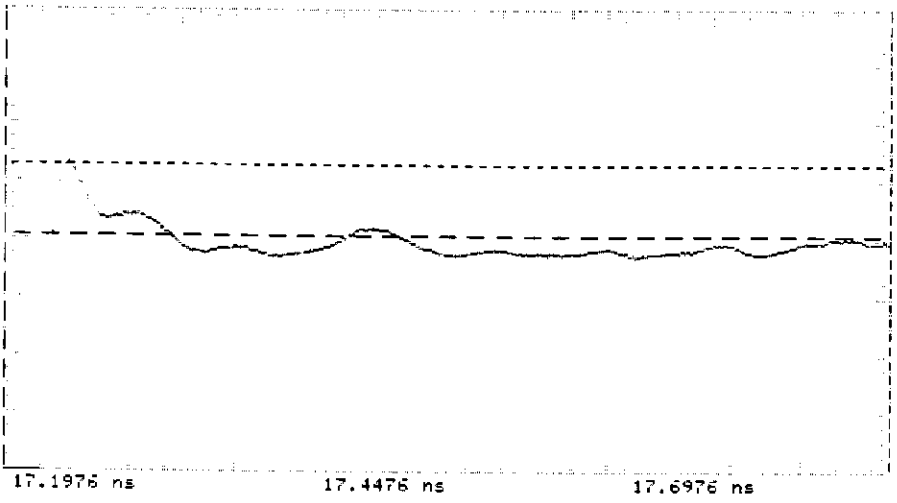
23. Slowly adjust TDR Drive (R44) on Horizontal Assembly (A1) until the peak of the overshoot coincides with marker 2's position. Refer to figure 4-9.
    If the overshoot moves off screen, reposition the waveform with delay.
    If this adjustment fails, repeat the TOP and BOTTOM adjustments.



Ch. 1	=	5.000 mVolts/div	Offset	=	200.0 mVolts
Timebase	=	100 ns/div	Delay	=	18.1976 ns
Delta V	=	-200.00 mVolts			
Vmarker1	=	200.31 mVolts	Vmarker2	=	312.50 uVolts
Delta T	=	1.0000 ns			
Start	=	17.1976 ns	Stop	=	18.1976 ns

Trigger is Freerunning at 10.0 kHz with Step on

Figure 4-8. TOP Adjustment.



Ch. 1	=	5.000 mVolts/div	Offset	=	200.0 mVolts
Timebase	=	50.0 ps/div	Delay	=	17.1976 ns
Delta V	=	6.0937 mVolts			
Vmarker1	=	200.31 mVolts	Vmarker2	=	206.40 mVolts
Delta T	=	1.0000 ns			
Start	=	17.1976 ns	Stop	=	18.1976 ns

Trigger is Freerunning at 10.0 kHz with Step on

Figure 4-9. Overshoot Fine Adjustment.

4-16. FEEDTHROUGH COMPENSATION ADJUSTMENTS

Description:

When the sampler's are turned off, there is a small amount of parasitic (unwanted) feedthrough of signals or noise through the samplers. This is caused by parasitic capacitive and resistive coupling near the samplers. This procedures nulls passive feedthrough of the input signal through the samplers.

Equipment Recommended:

ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
Semi-rigid U cable	No substitute	54121-61601
Semi-rigid S cable	No substitute	54121-61602

Equipment Setup:

HP 54120T

Display
- Display Mode: Persistence
- Display Time: 500 ms
- Screen: Single
- Graticule: Grid

Channels
- Channel 1: On
- Volts/Div: 10 mV/div
- Offset: 200 mV
- Channels 2-4: Off
- Attenuation: 1

Timebase
- Time/Div: 20 µs/div
- Delay: 16 ns
- Delay Ref at: Left
- Sweep: Freerun
- Freerun Rate: 3 KHz

Network
- Reflect/Trans/Cal: Reflect
- Step & Chan 1: On

Procedure: The adjustment locations are shown on page 4-50.

1. Connect the semi-rigid S and U cables from channel 1 to channel 2.
2. Preset eight adjustments on Vertical assembly (A2), RC1-4 (R5-8) and CC1-4 (R9-12) fully counter-clockwise.
3. Signal on screen should resemble figure 4-10.

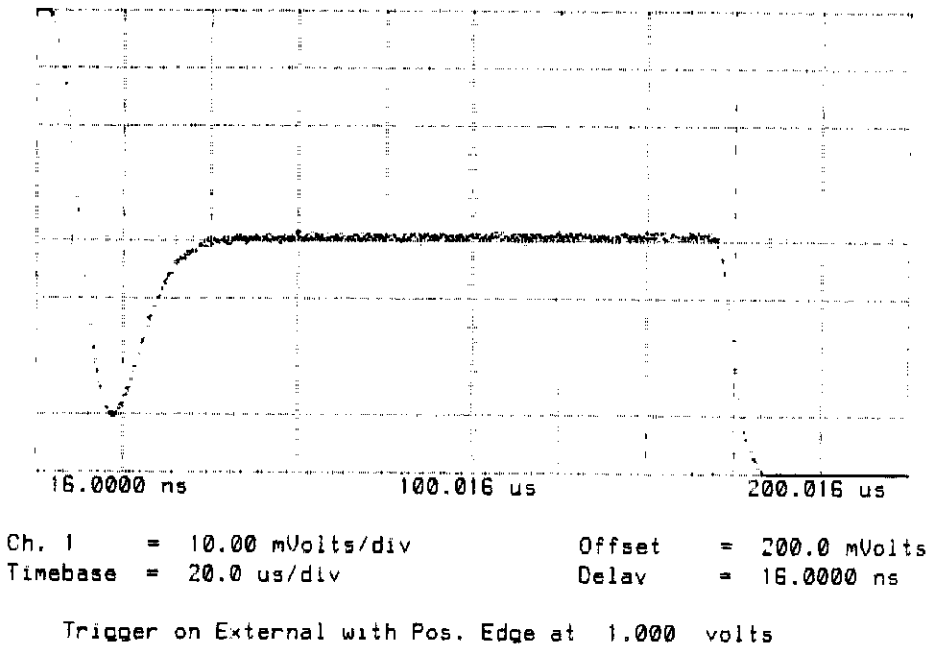


Figure 4-10. Feedthrough Not Compensated.

4. Adjust RC1 (R5) until the positive and negative pulse peaks are equidistant from the flat portion of the pulse, $V_P = V_N$. The Delta V markers may help determine when the pulse peaks are equidistant. See figure 4-11.

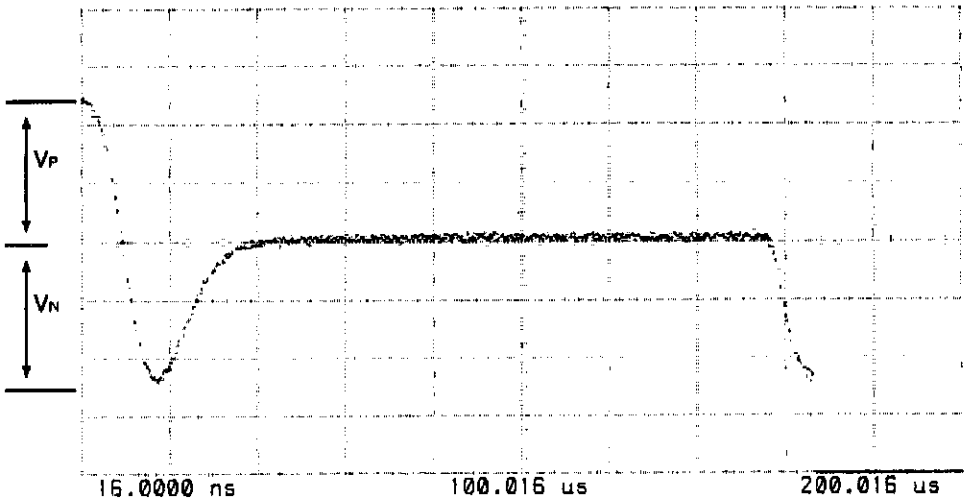


Figure 4-11. Adjusting RC1 for Equidistant Pulse Peaks.

5. Adjust CC1 (R9) until the positive and negative pulse peaks are the lowest in amplitude.
6. Re-adjust RC1 and CC1 until pulse top is as flat as possible.
7. Set channel 1 to 1 mV/div and offset to 300 mV (do not turn channel 1 off).
8. Turn channel 2 on and move semi-rigid cable from channel 1 to channel 2.
9. Repeat steps 4-6 except use adjustments RC2 (R6) and CC2 (R10).
10. Turn channel 2 off and channel 3 on.
11. Move semi-rigid cables from channel 2 to channel 3's input.
12. Repeat steps 4-6 except use adjustments RC3 (R7) and CC3 (R11).
13. Turn channel 3 off and channel 4 on.
14. Move semi-rigid cables from channel 3 to channel 4's input.
15. Repeat steps 4-6 except use adjustments RC4 (R8) and CC4 (R12).
16. Remove semi-rigid cables from oscilloscope.
17. Turn Network ***Step & Chan 1*** Off.

4-17. TRIGGER HYSTERESIS AND OFFSET NULL ADJUSTMENTS

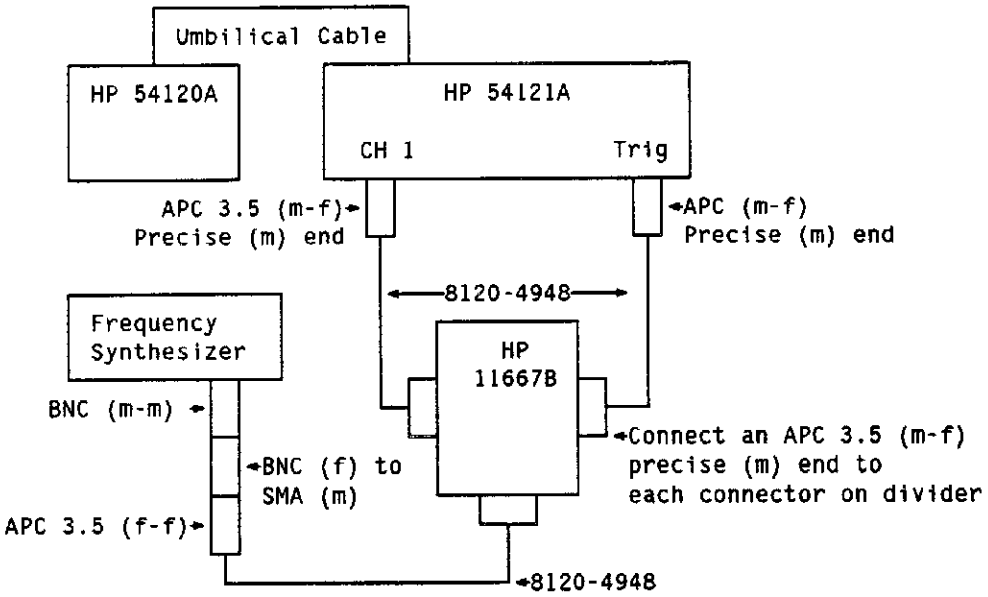
Description:

HYSTERESIS and OFFSET are adjusted by observing the voltage level where the displayed waveform crosses the time reference, which is set to the screen's left side.

Equipment Recommended:

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Power divider	APC 3.5 connectors	HP 11667B
Frequency Synthesizer	100 KHz at 100 mV p-p amplitude	HP 3325A
ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
Adapter BNC (f) to SMA (m)		1250-1200
Adapter APC 3.5 (m-f)	26.5 GHz (male end precise) Quantity needed - 5	1250-1866
Adapter APC 3.5 (f-f)		1250-1865
Adapter BNC (m-m)		1250-0216
Coaxial cable APC 3.5 (m-m)	18 GHz Quantity needed - 3	8120-4948

Equipment Connections:



Equipment Setup:

Signal Source

Function	Sine Wave
Frequency	100 KHz
Amplitude	100 mV p-p

HP 54120T

Display	
Display Mode	Averaged
No. of Averages	4
Screen	Single
Graticule	Grid
Bandwidth	12.4 GHz
Channels	
Channel 1	On
Volts/Div	20 mV/div
Offset	0
Channels 2-4	Off
Attenuation	1

Timebase	
Time/Div	1 μs/div
Delay	16 ns
Delay Ref at	Left
Sweep	Trg'd
Trigger	
Trigger Level	0 V
Slope	Pos
HF Sense	Off
HF Reject	Off
Attenuation	1
Network	
Reflect/Trans/Cal	Reflect
Step & Chan 1	Off

Procedure: The adjustment locations are shown on page 4-50

1. There should be a trace at center screen.
2. Connect signal generator to oscilloscope's input.
3. There should be one period of a 100 KHz sine wave with an amplitude of approximately 50 mV p-p.
4. While switching slope between positive and negative, adjust trigger hysteresis (R48 HYST) on the Horizontal assembly (A1) until there is 20 mV (four minor divisions or 1 major division) between the sine wave's starting point on left side of screen.
5. Continue switching slope between positive and negative as you adjust OFFSET NULL (R47) until the sine wave's starting point is centered vertically around center screen.

4-18. CHANNEL SKEW CALIBRATION

Description:

For routine calibration, the channel skew calibration need not be done. It is recommended that the operator do a channel skew calibration with signals and cables similar to those with which the oscilloscope will be used.

Equipment Recommended and Connections:

Refer to section 4-10.

Equipment Setup:

Signal Source

Frequency	250 MHz
Amplitude	+ 12 dBM

HP 54120T

Channels	
Channel	1-4
Display	On
Volts/Div	2 mV/div
Offset	0
Attenuation	1
Timebase	
Time/Div	20 ps/div
Delay	19.9 ns
Delay Ref at	Left
Sweep	Trg'd
Trigger	
Trigger Level	0 V
Slope	Pos
Display	
Display Mode	Averaged
No. of Averages	64
Network	
Reflect/Trans/Cal	Reflect
Step & Chan. 1	Off

Procedure:

1. Press ***Utility*** key.
2. Press ***Cal Menu*** key.
3. Press ***Channel Skew Cals*** key.
4. Select reference to be channel 1 and trigger skew to be channel 1.
5. Adjust channel skew with RPG knob or arrow keys in order to align trace's 0 V crossing at center screen.
6. Move input to next channel and select reference and trigger skew for that channel.
7. Repeat steps 5 and 6 until all channels have been skewed.
8. Press ***Exit Cal Menu*** key.

4-19. CRT COLOR MODULE INTRODUCTION

The CRT color module requires no adjusting when used in a normal environment. The procedure given here is for CRT color convergence. Do not perform these adjustments as part of regular maintenance.
Observe the following rules before making the adjustments:

- Do not perform this procedure as normal maintenance.
- Make adjustments only if the instrument has been subjected to extreme magnetic environments and the colors are incorrect.
- Before making any adjustments, try degaussing the unit using the rear panel degaussing switch or a color television type degaussing coil (refer to the degaussing procedure paragraph 4-2, this section).
- Only qualified personnel who are familiar with color CRT convergence procedures should perform this adjustment.
- Before adjustments are made, mark the position where potentiometers are. This allows you to return the adjustments to their original starting position.

4-20. DEGAUSSING THE DISPLAY

After the instrument has been used for a while, the CRT may become magnetized and color or other data may become distorted. To correct, press the Degauss button on the rear panel several times.

If the instrument has been subjected to strong magnetic fields, it may be necessary to degauss the CRT with a conventional television type degaussing coil.

4-21. SAFETY CONSIDERATIONS

Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with the precautions listed in the Safety Summary at the front of this manual, or with specific warnings given throughout this manual, could result in serious injury or death. Service adjustments should be performed only by qualified service personnel.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures. The apparatus shall be disconnected from all voltage sources before it is opened for any adjustment, replacement, maintenance, or repair.

4-22. CRT COLOR MODULE ADJUSTMENTS

NOTE

DO NOT PERFORM THESE ADJUSTMENTS DURING ROUTINE CALIBRATION. *The earth's magnetic field or the user's environment may cause an unstable display which cannot be corrected by degaussing the screen. The following procedures are provided for those few extreme cases.*

Description:

The CRT Color Module is adjusted to compensate for external magnetic influences causing mis-convergence.

NOTE

DO NOT *continue with this procedure before first degaussing the CRT screen with the rear panel degaussing switch. In extreme cases of magnetism, it may be necessary to degauss the CRT with a conventional external television-type degaussing coil.* ***During any of the following adjustments, the CRT module must face west.***

Equipment Recommended:

ACCESSORIES	CRITICAL SPECIFICATIONS	RECOMMENDED HP PART NUMBER
Alignment tool	non-metallic	8710-1355

Procedure:

NOTE

The following adjustments are broken down in groups. Follow their sequence because they interact and depend on each other. Figure 4-12 is a drawing of the adjustment sequence. In some cases not all the adjustment groups are used. For example, if the Geometry Adjustment Group corrects the problem, this will be the only group used.

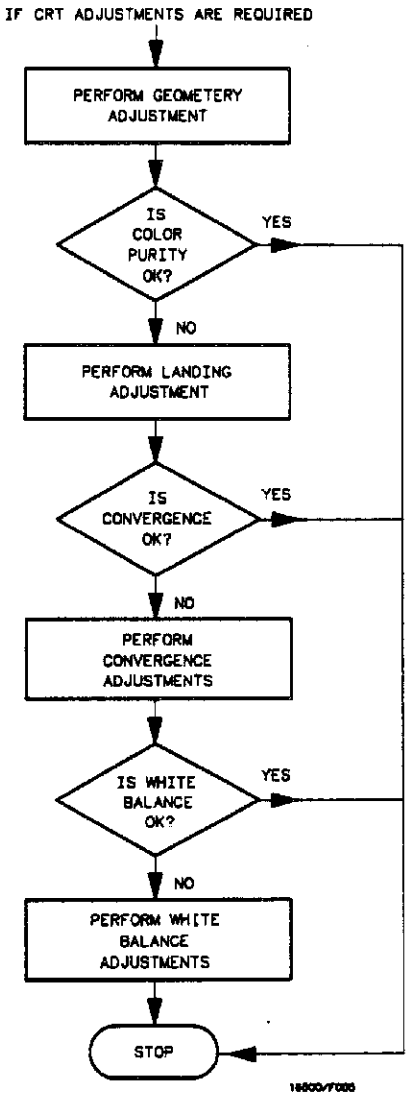


Figure 4-12. CRT Module Adjustment Flow Diagram.

Geometry Adjustments

1. Press ***Utility*** menu key and ***CRT SETUP*** key.
   Press ***CRT PATTERN*** key until a white cross hatch is displayed on CRT.

2. Preset front-panel BACKGROUND control to mechanical center.

3. Preset front-panel CONTRAST control maximum clockwise.

4. Preset H.SUB SHIFT (RV006) and V.SUB SHIFT (RV008) on bottom PC board to mechanical center.

5. With a flexible ruler, adjust H.SIZE (RV504) and V.HEIGHT (RV502) on left hand side PC board so cross-hatch pattern's border displayed on CRT is 120.5 mm (4.74 in.) vertically and 161 mm (6.34 in.) horizontally.

6. Adjust V.CENT (RV510) and H.CENT (RV503) on left hand side PC board to center pattern.

7. Adjust PIN AMP (RV506) on left hand side PC board to eliminate pincushion distortion in the vertical lines of the cross-hatch pattern. See figure 4-13.

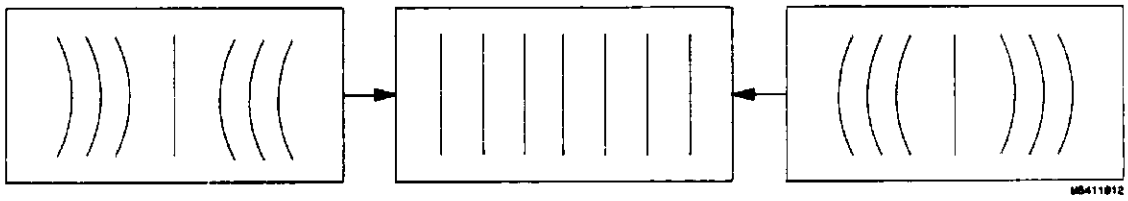


Figure 4-13. PIN AMP Adjustment.

Geometry Adjustments (Continued)

8. Adjust PIN PHASE (RV505) on left side PC board to eliminate pin phase distortion in vertical lines of cross-hatch pattern. See figure 4-14.

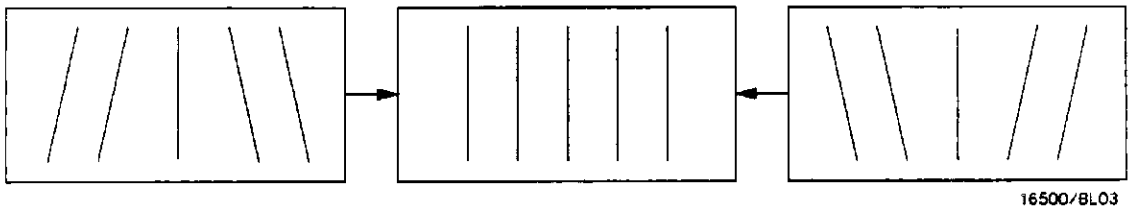


Figure 4-14. PIN PHASE Adjustment.

9. Adjust TOP PIN (RV511) on left hand side PC board until the horizontal line is parallel with center horizontal line.

10. Adjust BOTTOM PIN (RV512) on left hand side PC board until the bottom horizontal line is parallel with center horizontal line.

Landing, Convergence, and Focus Adjustment Preparation:

1. Remove CRT Display Module from instrument. See mainframe disassembly section 6A-9.

2. Reconnect instrument front panel, re-install front panel and CRT bezel (using two screws to temporarily hold front panel in place).

Steps 3-5 are performed only when the CRT has been replaced.

3. Loosen deflection yoke clamp screw.

4. With CRT Display Module placed to mainframe's left, reconnect module.

NOTE

Note the original routing of the module power cable for proper routing when module is re-installed in instrument. Then, re-route the module power cable from inside the module to the outside (left side) of module for reconnection to the power supplies.

5. Remove deflection yoke spacers by moving deflection yoke rearward and removing spacers.

NOTE

The deflection yoke spacers are tapered rubber blocks between front of yoke and rear of CRT funnel.

6. Apply power and allow instrument to thermally restabilize for 20 minutes.

Focus Adjustment:

NOTE

Perform the geometry adjustments before making focus adjustment.

1. Press ***Utility*** menu key and ***CRT SETUP*** key.
   Press ***CRT PATTERN*** key until a white cross-hatch is displayed on CRT.

2. Adjust FOCUS (RV701) on rear PC board for best overall focus.

Landing Adjustment:

1. Press ***Utility*** menu key and ***CRT SETUP*** key.
   Press ***COLOR PURITY*** key until a white raster is displayed on CRT.

2. Turn front panel CONTRAST control fully clockwise.

3. Degauss entire CRT screen by pressing DEGAUSSING switch on instrument's rear panel.

NOTE

In cases where the user's environment or shipping environment has caused high levels of magnetization to take place, it may be necessary to externally degauss the CRT with a conventional television-type degaussing coil to completely degauss the CRT.

4. Set purity magnet tabs to mechanical center. See figure 4-15.

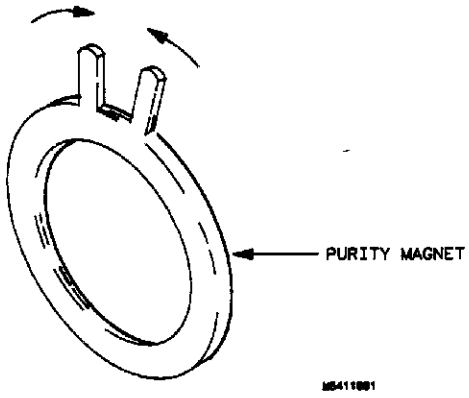


Figure 4-15. Purity Magnet Centering.

5. Press ***COLOR PURITY*** key until a green raster is displayed on CRT.

Landing Adjustment: (Continued)

Step 6 is performed only if the CRT has been replaced.

6. Move deflection yoke rearward until left edge of raster turns red and right side of raster turns blue. See figure 4-16.

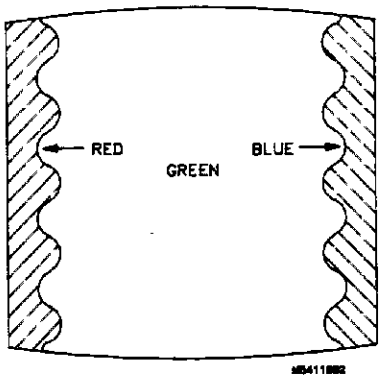


Figure 4-16. Purity Magnet Adjustment Raster.

7. Adjust purity magnets until green is in center of raster with red and blue bands evenly distributed on sides. See figure 4-16.

Step 8 is performed only if CRT has been replaced.

8. Move deflection yoke forward until entire raster is green.

NOTE

Landing adjustment is easier if yoke is moved all the way forward, then moved rearward until raster is completely green.

9. With COLOR PURITY key, replace green raster with red, then with blue raster. Check each raster for proper landing adjustment or color purity.

Landing Adjustment: (Continued)

10. If landing is not correct in step 9, repeat steps 6 through 9 for best compromise. See figure 4-17.

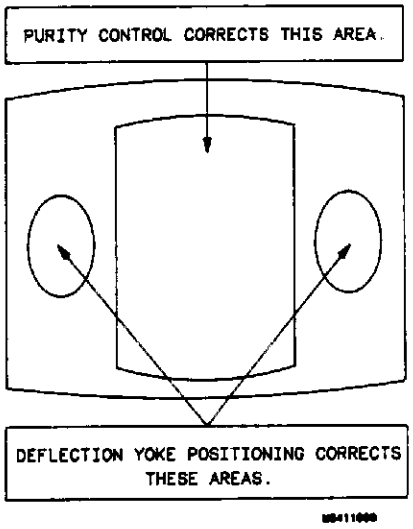


Figure 4-17. Landing and Purity Adjustment Guide.

11. If landing is not correct in step 10, readjust purity magnets for best landing of each color.

Step 12 is performed only if the CRT has been replaced.

12. When landing adjustment is complete, tighten deflection yoke clamp screw just enough to keep yoke from moving. **DO NOT over tighten.**

NOTE

While moving deflection yoke forward and rearward, rotate yoke as necessary to make vertical edges of raster parallel to the sides of the instrument frame.

Static Convergence:

1. Preset front-panel BACKGROUND control to mechanical center.

2. Preset front-panel CONTRAST control maximum clockwise.

3. Temporarily disconnect power from instrument and remove PC board shield cover from rear of CRT Display Module by prying evenly on all four sides.

4. Re-apply power and press ***Utility*** menu key and ***CRT SETUP*** key.
   Press ***CRT PATTERN*** key until a white cross-hatch pattern is displayed.

5. Check four dots which are around center intersection of cross-hatch pattern for coincidence of blue, red, and green dots. If the dots are not coincident, adjust H.STAT (RV703) on rear PC board to obtain horizontal coincidence and V.STAT (RV803) on bottom PC board to obtain vertical coincidence. See figure 4-18.

NOTE

Due to interaction, BEAM LANDING will need to be re-adjusted if either H.STAT or V.STAT adjustments are made. Once BEAM LANDING is re-adjusted, repeat step 5 above if necessary to obtain center screen coincidence of the dots.

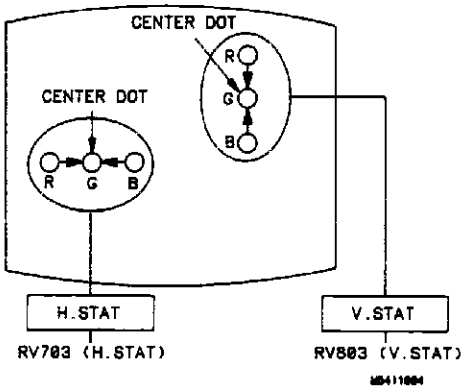


Figure 4-18. Static Convergence.

Dynamic Convergence:

1. Press ***Utility*** menu key and ***CRT SETUP*** key.
   Press ***CRT PATTERN*** key until a white cross-hatch pattern is on CRT.

2. Adjust Y BOW (RV805) on bottom PC board to eliminate red, green, and blue bowing at top and bottom of center vertical line See figure 4-19.

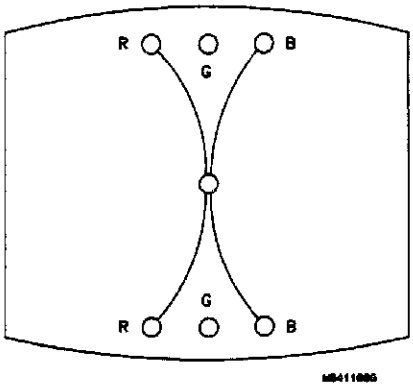


Figure 4-19. Y BOW Adjustment.

3. Adjust Y BOW CROSS (RV804) on bottom PC board to eliminate red, green, and blue orthogonal mis-alignment at top and bottom of center vertical line. See figure 4-20.

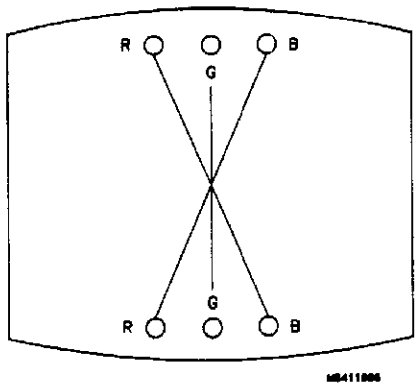


Figure 4-20. Y BOW CROSS Adjustment.

Dynamic Convergence: (Continued)

4. Adjust V.STAT TOP (RV801) and V.STAT BOTTOM (RV802) on bottom PC board to obtain coincidence of red, blue, and green at intersection of top and bottom horizontal lines with center vertical line. See figures 4-21 and 4-22.

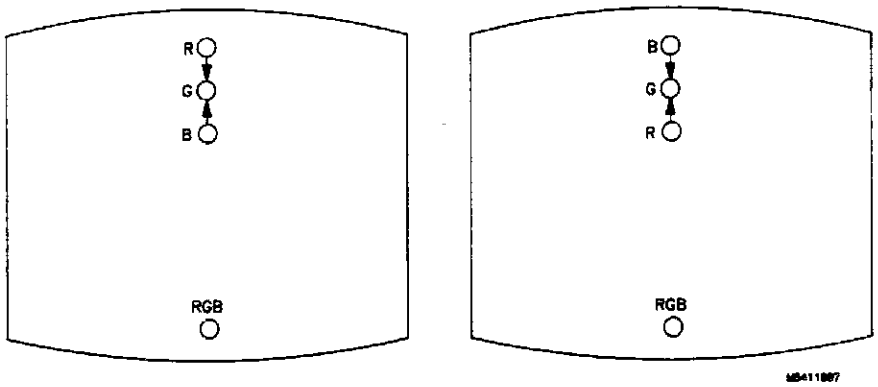


Figure 4-21. V.STAT TOP Adjustment.

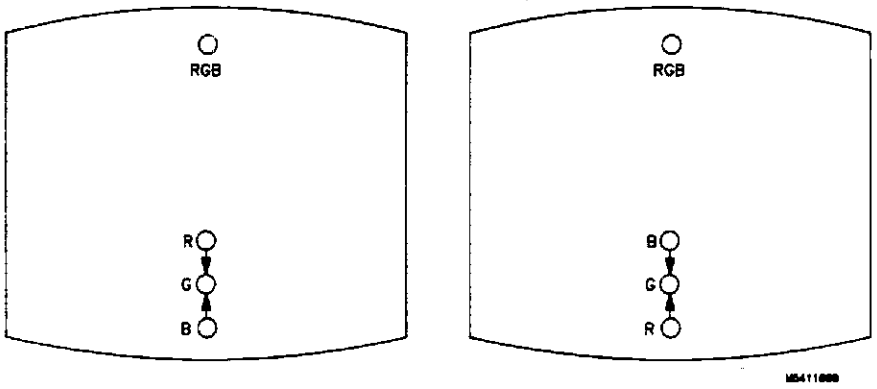


Figure 4-22. V.STAT BOTTOM Adjustment.

Dynamic Convergence: (Continued)

5. Adjust H.AMP (RV807) on bottom PC board for equal amounts of mis-convergence at right and left sides of screen. See figure 4-23.

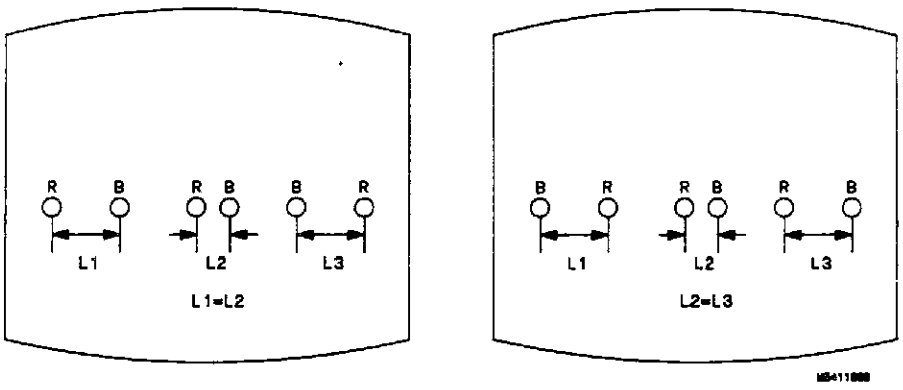


Figure 4-23. H.AMP Adjustment.

6. Adjust H.TILT (RV806) on bottom PC board for coincidence of red, green, and blue at right and left sides of screen. See figure 4-24.

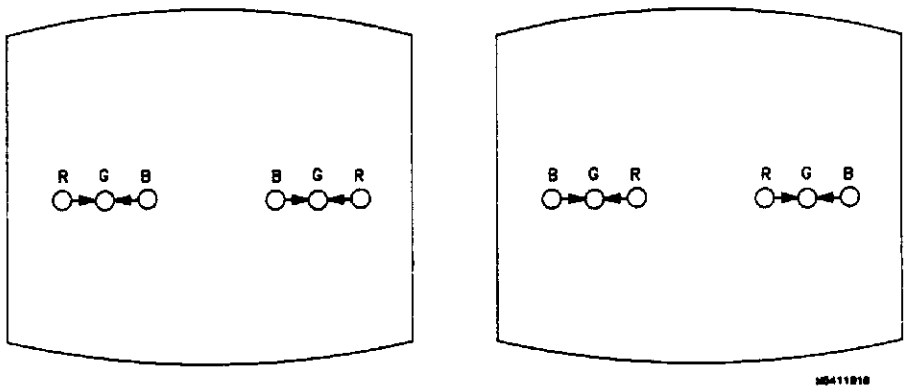


Figure 4-24. H.TILT Adjustment.

White Balance:

1 Press ***Utility*** menu key
Press ***LIGHT OUTPUT*** key until a blank raster is on CRT.

NOTE

The completely blank raster will contain a test for the function keys on the right side of the display, however, it will not affect this adjustment.

2. Set front-panel BACKGROUND and SUB BRT (RV901) on bottom PC board to mechanical center.

3. Set front-panel BRIGHTNESS and SUB CONT (RV902) on bottom PC board to mechanical center.

4. Set G. DRIVE (RV921), B. DRIVE (RV9310), and R. DRIVE (RV911) on bottom PC board to mechanical center.

5. Set G.BKG (RV721), B.BKG (RV731), and R.BKG (RV711) on rear PC board fully counterclockwise (CCW).

6. Adjust SCREEN (RV702) on rear PC board until either a red, green, or blue raster just starts to become visible. Note which color becomes visible first and do not adjust background control (BKG) for that color in the step 7.

7. Adjust other two background (BKG) controls for best white balance.

8. Press ***Utility*** menu key.
Press ***COLOR PURITY*** key until a white raster is on CRT.

9. Set front panel BRIGHTNESS control at maximum.

10. Observe screen and adjust DRIVE controls (RV921, RV931, and RV911) on bottom PC board for best white balance.

NOTE

White balance is checked in two ways. First, with an average piece of white photocopy paper, compare the white on the CRT to the paper. Second, in the CONFIDENCE TEST function, the gray scale blocks are checked to make sure the block at the far left of the CRT is visible.

11. Repeat steps 1 through 3 and 6 through 10 for best overall white balance.

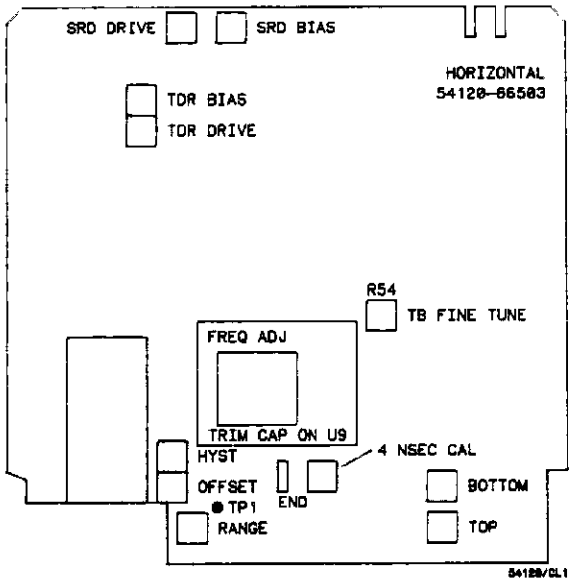


Figure 4-25. Horizontal Assembly Adjustment Locations.

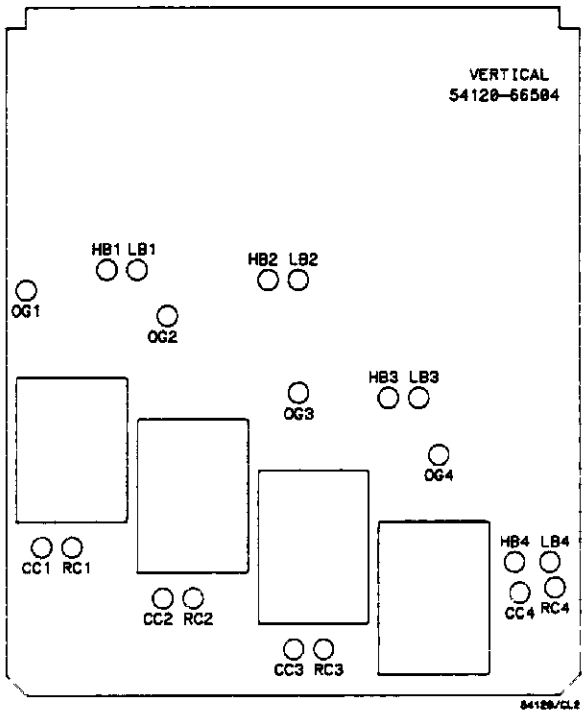


Figure 4-26. Vertical Assembly Adjustment Locations.

TABLE OF CONTENTS

REPLACEABLE PARTS

SECTION 5

REPLACEABLE PARTS

5-1. INTRODUCTION

This section contains information for ordering parts. Table 5-1 lists the names and addresses that correspond to the manufacturers' code numbers. Table 5-2 lists the abbreviations used in the parts list and throughout this manual. Figures 5-1 through 5-6 are drawings of the various mainframe parts with reference designators. Table 5-3 is the mainframe's replaceable parts list. Figures 5-7 through 5-12 are drawings of the various four channel test set parts with reference designators. Table 5-4 is the four channel test set's replaceable parts list. Replaceable parts for individual assemblies are included in the HP 54120T Service Data Supplement.

5-2. ABBREVIATIONS

Table 5-2 lists the abbreviations used in the replaceable parts list. Abbreviations in the replaceable parts list are always in capital letters. In other sections of this manual abbreviations may be in capital or lower case letters.

5-3. REPLACEABLE PARTS LIST

Tables 5-3 and 5-4 are lists of replaceable parts and are organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

Information given for each part consists of the following:

a. Hewlett-Packard part number and the check digit (for HP internal use).

b. Total quantity (Qty) in the instrument, given only once at the part number's first appearance in the list.

c. Description of part.

d. A typical manufacturer of a given part in a five digit code. Refer to table 5-1 for a cross reference from code number to manufacturer name.

e. The manufacturers' part number.

5-4. EXCHANGE ASSEMBLIES

Some of the assemblies used in this instrument have been set up on the exchange program. This allows the customer to exchange his faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Exchangeable assemblies are listed at the beginning of the replaceable parts table with a star (*) before the reference designator. They have a part number in the form XXXXX-695XX.

Before ordering an exchange assembly, check with you're local parts or repair organization for the procedures associated with the exchange assembly program.

5-5. ORDERING INFORMATION

To order a part listed in the replaceable parts table, indicate the Hewlett-Packard part number, check digit, and quantity required. Send the order to the nearest Hewlett-Packard office.

To order a part that is not listed in the replaceable parts table, include the instrument model number, serial number, description and function of part, and total quantity required. Address an order to the nearest Hewlett-Packard sales office. The model number for Table 5-3 is HP 54120A Digitizing Oscilloscope Mainframe. The model number for Table 5-4 is HP 54121A Four Channel Test Set.

5-6. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

a. Direct ordering and shipment from HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through local HP offices when orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local HP offices.

Table 5-1. List of Manufacturers' Codes.

Mfr No.	Manufacturer Name	Address	Zip Code
04713	Motorola Semi Conductor Products	Phoenix Az	85008
06915	PPPM Pan Asian Paper Product MFG SDN BHD	Pinang	Malaysia
28480	Hewlett-Packard Co. Corporate HQ	Palo Alto Ca	94304
86928	Seastrom MFG Co.	Glendale Ca	91201

Table 5-2. Reference Designators and Abbreviations.

REFERENCE DESIGNATORS

A	=assembly	**F**	=fuse	**Q**	=transistor,SCR, triode thyristor	**U**	=integrated circuit, microcircuit
B	=fan,motor	**FL**	=filter	**R**	=resistor	**V**	=electron tube, glow lamp
BT	=battery	**H**	=hardware	**RT**	=thermistor	**VR**	=voltage regulator, breakdown diode
C	=capacitor	**J**	=electrical connector (stationary portion);jack	**S**	=switch,jumper	**W**	=cable
CR	=diode diode thyristor, varactor	**L**	=coil,inductor	**T**	=transformer	**X**	=socket
DL	=delay line	**MP**	=misc. mechanical part	**TB**	=terminal board	**Y**	=crystal unit(piezo-electric or quartz)
DS	=annunciator;lamp,LED	**P**	=electrical connector (moveable portion);plug	**TP**	=test point		
E	=misc. electrical part						

ABBREVIATIONS

A	=amperes	**DWL**	=dowel	**MFR**	=manufacturer	**RND**	=round
A/D	=analog-to-digital	**ECL**	=emitter coupled logic	**MICPROC**	=microprocessor	**ROM**	=read-only memory
AC	=alternating current	**ELAS**	=elastomeric	**MINTR**	=miniature	**RPG**	=rotary pulse generator
ADJ	=adjust(ment)	**EXT**	=external	**MISC**	=miscellaneous	**RX**	=receiver
AL	=aluminum	**F**	=farads,metal film (resistor)	**MLD**	=molded	**S**	=Schottky-clamped; seconds(time)
AMPL	=amplifier	**FC**	=carbon film/ composition	**MM**	=millimeter	**SCR**	=screw;silicon controlled rectifier
ANLG	=analog	**FD**	=feed	**MO**	=metal oxide	**SEC**	=second(time);secondary
ANSI	=American National Standards Institute	**FEM**	=female	**MTG**	=mounting	**SEG**	=segment
ASSY	=assembly	**FF**	=flip-flop	**MTLC**	=metallic	**SEL**	=selector
ASTIG	=astigmatism	**FL**	=flat	**MUX**	=multiplexer	**SGL**	=single
ASYNCHRO	=asynchronous	**FM**	=foam;from	**MW**	=milliwatt	**SHF**	=shift
ATTEN	=attenuator	**FR**	=front	**N**	=nano(10^{-9})	**SI**	=silicon
AWG	=American wire gauge	**FT**	=gain bandwidth product	**NC**	=no connection	**SIP**	=single in-line package
BAL	=balance	**FW**	=full wave	**NMOS**	=n-channel metal-oxide-semiconductor	**SKT**	=skirt
BCD	=binary-code decimal	**FXD**	=fixed	**NPN**	=negative-positive-negative	**SL**	=slide
BD	=board	**GEN**	=generator	**NPRN**	=neoprene	**SLDR**	=solder
BFR	=buffer	**GND**	=ground(ed)	**NRFR**	=not recommended for field replacement	**SLT**	=slot(ted)
BIN	=binary	**GP**	=general purpose	**NSR**	=not separately replaceable	**SOLD**	=solenoid
BRDG	=bridge	**GRAT**	=graticule	**NUM**	=numeric	**SPCL**	=special
BSHG	=bushing	**GRV**	=groove	**OBD**	=order by description	**SQ**	=square
BW	=bandwidth	**H**	=henries,high	**OCTL**	=octal	**SREG**	=shift register
C	=ceramic,cermet (resistor)	**HD**	=hardware	**OD**	=outside diameter	**SRQ**	=service request
CAL	=calibrate;calibration	**HOND**	=hardened	**OP AMP**	=operational amplifier	**STAT**	=static
CC	=carbon composition	**HG**	=mercury	**OSC**	=oscillator	**STD**	=standard
CCW	=counterclockwise	**HGT**	=height	**P**	=plastic	**SYNCHRO**	=synchronous
CER	=ceramic	**HLCL**	=helical	**P/O**	=part of	**TA**	=tantalum
CFM	=cubic feet/minute	**HORIZ**	=horizontal	**PC**	=printed circuit	**TBAX**	=tubeaxial
CH	=choke	**HP**	=Hewlett-Packard	**PCB**	=printed circuit board	**TC**	=temperature coefficient
CHAM	=chamfered	**HP-IB**	=Hewlett-Packard Interface Bus	**PD**	=power dissipation	**TD**	=time delay
CHAN	=channel	**HR**	=hour(s)	**PF**	=picofards	**THD**	=thread(ed)
CHAR	=character	**HV**	=high voltage	**PI**	=plug in	**THK**	=thick
CM	=centimeter	**HZ**	=Hertz	**PL**	=plate(d)	**THRU**	=through
CMOS	=complementary metal-oxide-semiconductor	**I/O**	=input/output	**PLA**	=programmable logic array	**TP**	=test point
CMR	=common mode rejection	**IC**	=integrated circuit	**PLST**	=plastic	**TPG**	=tapping
CNDCT	=conductor	**ID**	=inside diameter	**PNP**	=positive-negative-positive	**TPL**	=triple
CNTR	=counter	**IN**	=inch	**POLYE**	=polyester	**TRANS**	=transformer
CON	=connector	**INCL**	=include(s)	**POS**	=positive,position	**TRIG**	=trigger(ed)
CONT	=contact	**INCAND**	=incandescent	**POT**	=potentiometer	**TRMR**	=trimmer
CRT	=cathode-ray tube	**INP**	=input	**POZI**	=pozidrive	**TRN**	=turn(s)
CW	=clockwise	**INTEN**	=intensity	**PP**	=peak-to-peak	**TTL**	=transistor-transistor
D	=diameter	**INTL**	=internal	**PPM**	=parts per million	**TX**	=transmitter
D/A	=digital-to-analog	**INV**	=inverter	**PRCN**	=precision	**U**	=micro(10^{-6})
DAC	=digital-to-analog converter	**JFET**	=junction field-effect transistor	**PREAMP**	=preamplifier	**UL**	=Underwriters Laboratory
DARL	=darlington	**JKT**	=jacket	**PRGMBL**	=programmable	**UNREG**	=unregulated
DAT	=data	**K**	=kilo(10^3)	**PRL**	=parallel	**VA**	=voltampere
DBL	=double	**L**	=low	**PROG**	=programmable	**VAC**	=volt,ac
DBM	=decibel referenced to 1mW	**LB**	=pound	**PSTN**	=position	**VAR**	=variable
DC	=direct current	**LCH**	=latch	**PT**	=point	**VCO**	=voltage-controlled oscillator
DCDR	=decoder	**LCL**	=local	**PW**	=potted wirewound	**VDC**	=volt,dc
DEG	=degree	**LED**	=light-emitting diode	**PWR**	=power	**VERT**	=vertical
DEMUX	=demultiplexer	**LG**	=long	**R-S**	=reset-set	**VF**	=voltage,filtered
DET	=detector	**LI**	=lithium	**RAM**	=random-access memory	**VS**	=versus
DIA	=diameter	**LK**	=lock	**RECT**	=rectifier	**W**	=watts
DIP	=dual in-line package	**LKWR**	=lockwasher	**RET**	=retainer	**W/**	=with
DIV	=division	**LS**	=low power Schottky	**RF**	=radio frequency	**W/O**	=without
DMA	=direct memory access	**LV**	=low voltage	**RGLTR**	=regulator	**WW**	=wirewound
DPDT	=double-pole, double-throw	**M**	=mega(10^6);megohms, meter(distance)	**RGTR**	=register	**XSTR**	=transistor
DRC	=DAC refresh controller	**MACH**	=machine	**RK**	=rack	**ZNR**	=zener
DRVR	=driver	**MAX**	=maximum	**RMS**	=root-mean-square	**°C**	=degree Celsius (Centigrade)
						°F	=degree Fahrenheit
						°K	=degree Kelvin

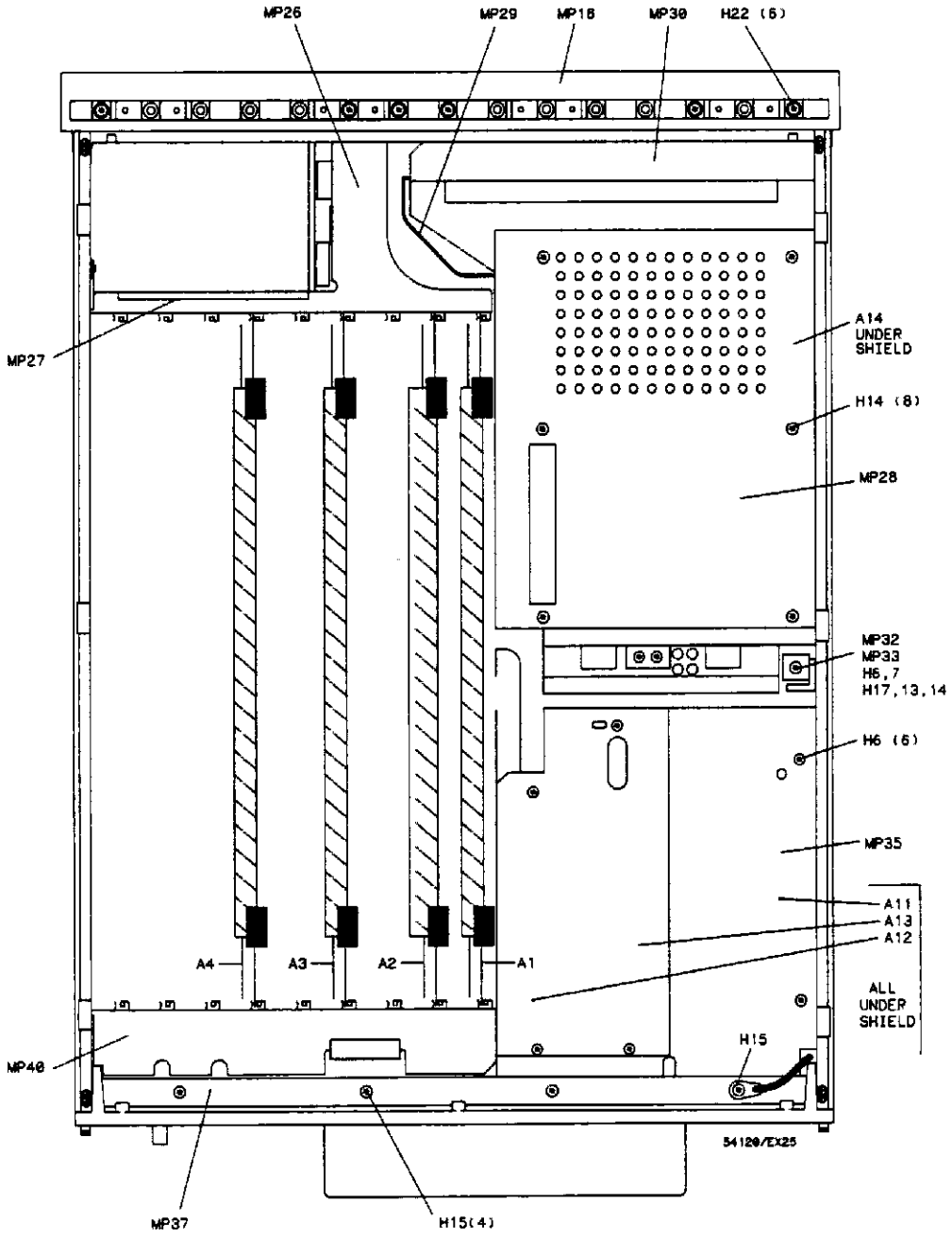


Figure 5-1. Mainframe Top View

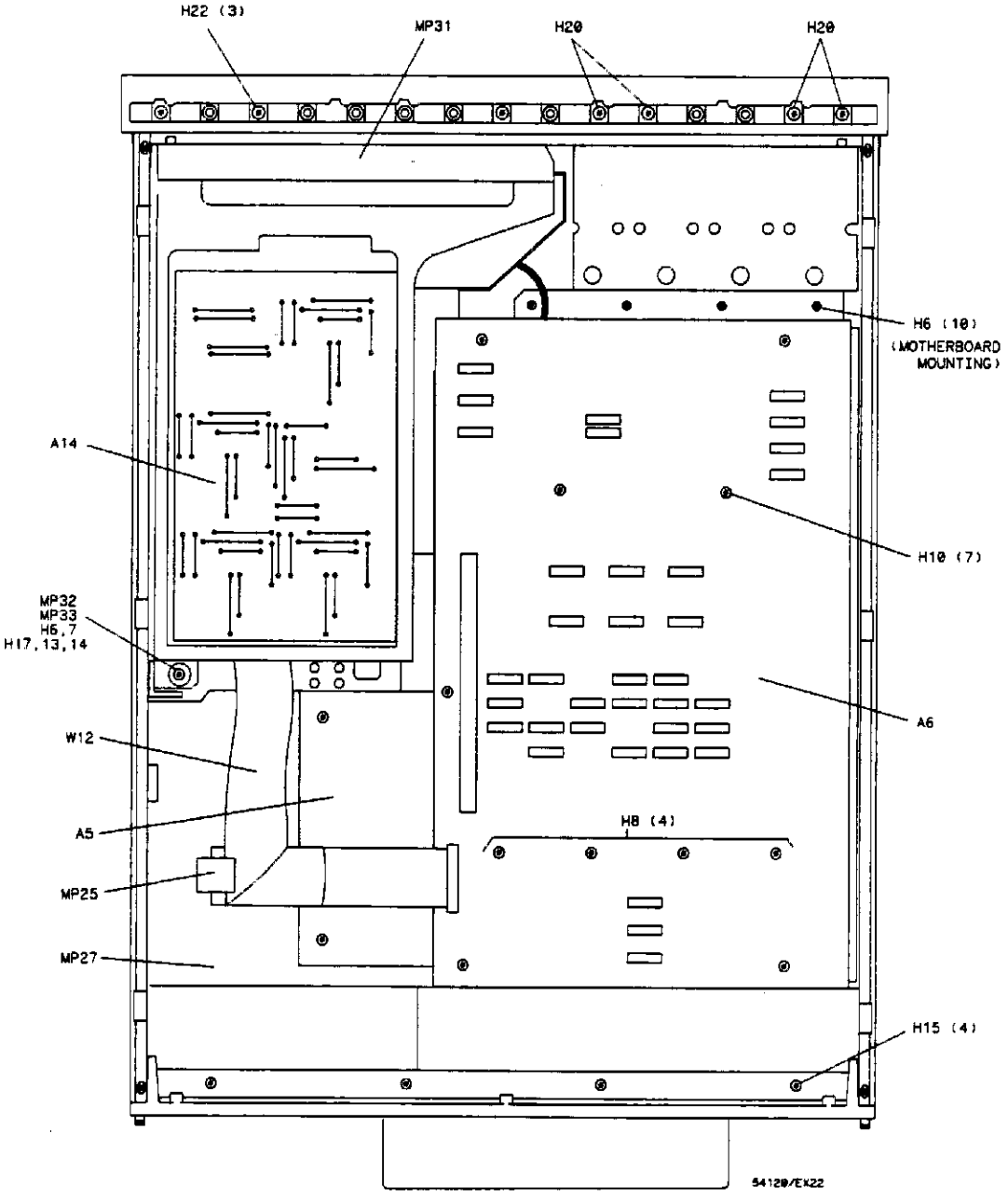


Figure 5-2. Mainframe Bottom View.

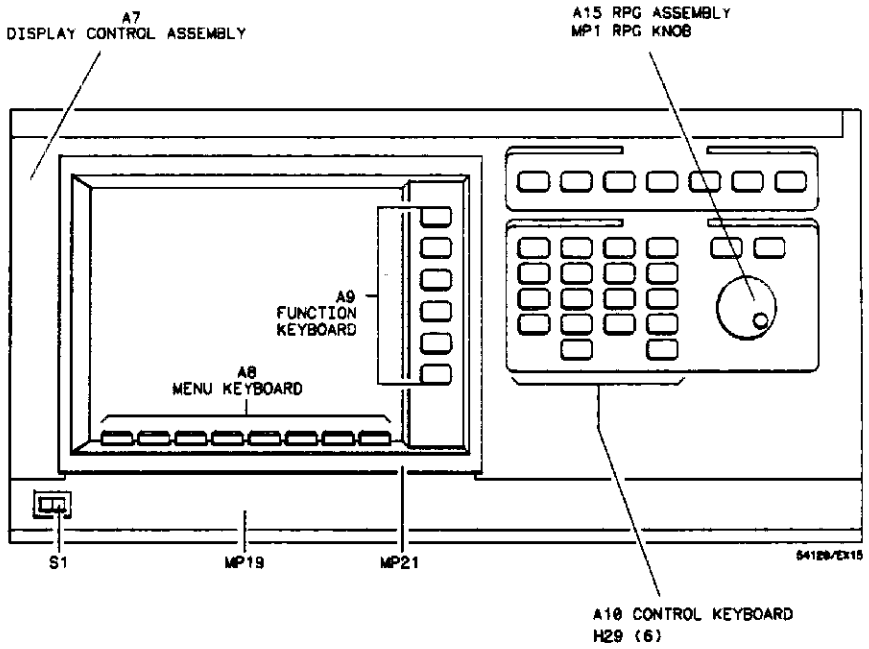


Figure 5-3. Mainframe Front Panel.

H5 Cover screw
H8 Retainer ring for cover screw
H9 Foot screw

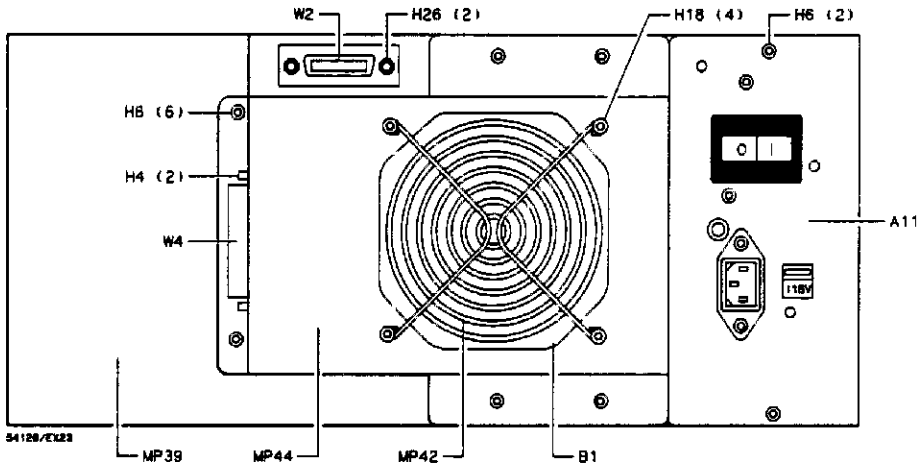


Figure 5-4. Mainframe Rear Panel.

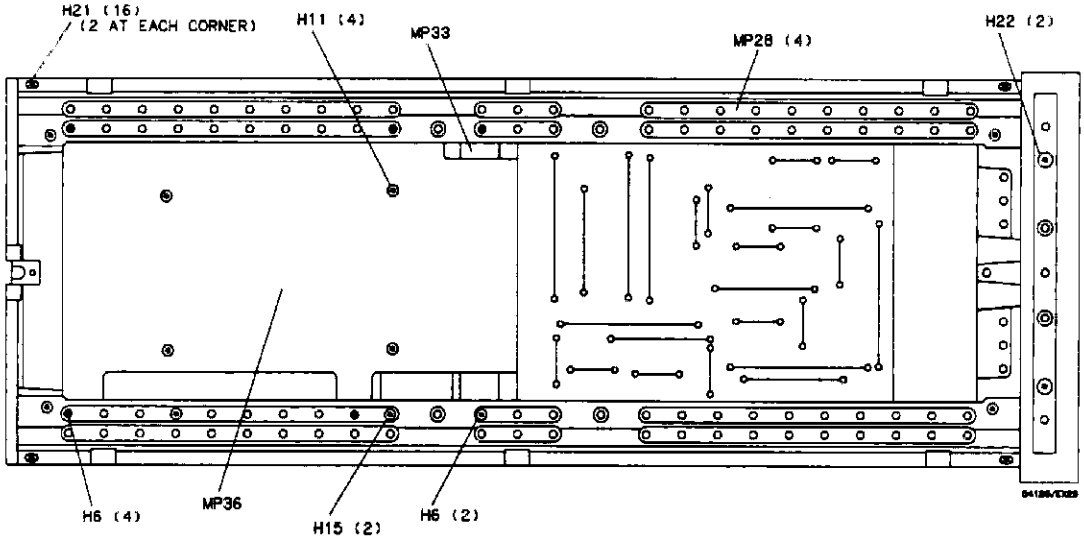


Figure 5-5. Mainframe Left Side View.

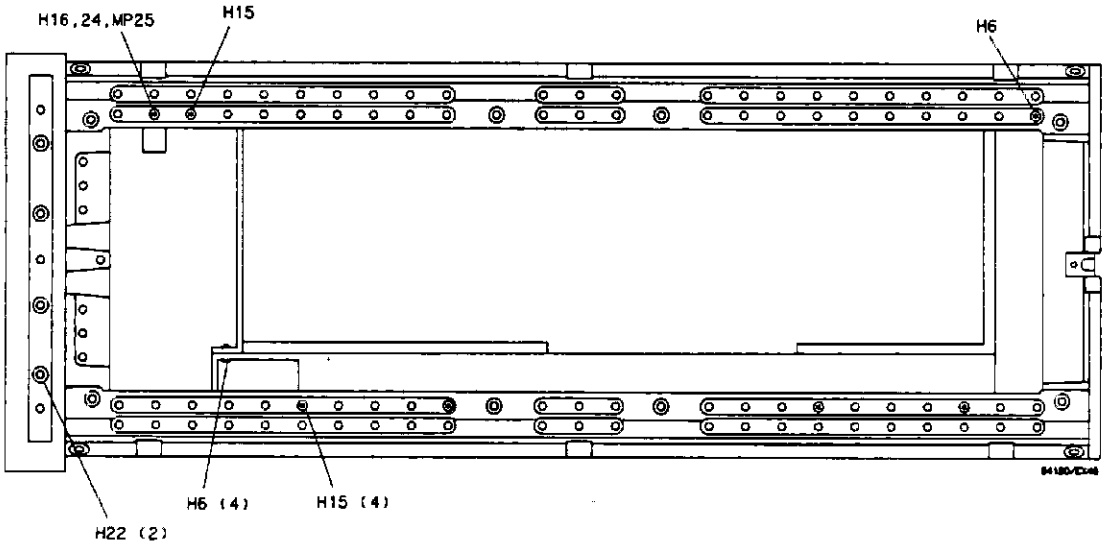


Figure 5-6. Mainframe Right Side View.

Table 5-3. HP 54120A Mainframe Replaceable Parts.

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
				* EXCHANGE ASSEMBLIES		
* A1	54111-69508	8	0	I/O ASSEMBLY	28480	54111-69508
* A2	54111-69510	4	0	MICROPROCESSOR ASSEMBLY	28480	54111-69510
* A3	54120-69501	4	0	HORIZONTAL CONTROL ASSEMBLY	28480	54120-69501
* A4	54120-69502	6	0	ADC ASSEMBLY	28480	54120-69502
* A9	54110-69512	5	0	COLOR DISPLAY ASSEMBLY	28480	54110-69512
* A11	54110-69513	6	0	PRIMARY POWER SUPPLY ASSEMBLY	28480	54110-69513
* A12	54110-69510	3	0	ANALOG POWER SUPPLY ASSEMBLY	28480	54110-69510
* A13	54110-69506	7	0	DIGITAL POWER SUPPLY ASSEMBLY	28480	54110-69506
A1	54111-66506	2	1	I/O ASSEMBLY	28480	54111-66506
A2	54111-66510	5	1	MICROPROCESSOR ASSEMBLY	28480	54111-66510
A3	54120-66501	5	1	HORIZONTAL CONTROL ASSEMBLY	28480	54120-66501
A4	54120-66502	9	1	ADC ASSEMBLY	28480	54120-66502
A5	54110-66511	8	1	MOTHER BOARD ASSEMBLY	28480	54110-66511
A6	54110-66512	9	1	COLOR DISPLAY ASSEMBLY	28480	54110-66512
A7	54110-66509	4	1	CRT CONTROL ASSEMBLY	28480	54110-66509
A8	54100-66520	7	1	MENU KEYBOARD	28480	54100-66520
A9	54110-66502	7	1	FUNCTION KEYBOARD	28480	54110-66502
A10	54100-66505	8	1	CONTROL KEYBOARD	28480	54100-66505
A11	54110-66513	0	1	PRIMARY POWER SUPPLY ASSEMBLY	28480	54110-66513
A12	54110-66510	7	1	ANALOG POWER SUPPLY ASSEMBLY	28480	54110-66510
A13	54110-66506	1	1	DIGITAL POWER SUPPLY ASSEMBLY	28480	54110-66506
A14	2090-0092	3	1	COLOR CRT MODULE	28480	2090-0092
A15	01980-61062	5	1	RPG ASSEMBLY	28480	01980-61062
B1	3160-0521	3	1	FAN-TUBEAXIAL	28480	3160-0521
E1	8160-0577	4	1	RFI GROUND STRIP	28480	8160-0577
H1	0515-1384	8	2	SCREW-MACH M5 X 0.8 10MM-LG	28480	0515-1384
H2	0515-1444	1	4	SCREW-MACH M3.5 X 0.6 25.4MM-LG PAN-HD	28480	0515-1444
H3	0515-1319	9	6	SCREW-MACH M3 X 0.5 20MM-LG PAN-HD	28480	0515-1319
H4	1251-2942	7	2	SCREW LOCK KIT-SUBMIN D CONN	28480	1251-2942
H5	1251-1245	7	3	COVER SCREW	28480	1251-2945
H6	0515-0372	2	49	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-LG	28480	0515-0372
H7				NOT ASSIGNED		
H8	0515-1253	0	3	RETAINER RING FOR COVER SCREW	28480	0515-1253
H9	0515-1444	1	4	FOOT SCREW	28480	0515-1444
H10	0515-1410	1	7	SCREW-MACHINE ASSEMBLY M3 X 0.5 20MM-LG	28480	0515-1410
H11	0515-1025	4	4	SCREW-MACHINE ASSEMBLY M3 X 0.5 26MM-LG	28480	0515-1025
H12	5061-6138	2	4	NUT-INSERT M4 X 0.7 X 4.6 OD	28480	5061-6138
H13	2190-0763	7	2	WASHER-FL MTLC NO. 6 .14-IN-ID .5-IN-OD	28480	2190-0763
H14	3050-1236	5	2	WASHER-FL NM 9/64 .148-IN-ID .475-IN-OD	88928	3050-1236
H15	0515-0433	6	15	SCREW-MACHINE ASSEMBLY M4 X 0.7 8MM-LG	28480	0515-0433
H16				NOT ASSIGNED		
H17	0515-0641	6	2	SCREW-THD-RLG M4 X 0.7 10MM-LG PAN-HD	28480	0515-0641
H18	0515-0435	8	4	SCREW-MACHINE ASSEMBLY M4 X 0.7 14MM-LG	28480	0515-0435
H19				NOT ASSIGNED		
H20	0515-1228	9	4	SCREW-MACH M4 X 0.7 6MM-LG 90-DEG-FLH-HD	28480	0515-1228
H21	0515-1403	2	16	SCREW-SPCL M4 X 0.7 6MM-LG 90-DEG-FLH-HD	28480	0515-1403
H22	0515-1259	6	16	SCREW-MACH M4 X 0.7 10MM-LG	28480	0515-1259
H23	0535-0031	2	9	NUT-HEX W/LKWR M3 X 0.5 2.4MM-THK	28480	0535-0031
H24				NOT ASSIGNED		
H25	2950-0043	8	1	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	28480	2950-0043
H26	0380-1586	6	2	STANDOFF-HEX 6.5-MM-LG M3 X 0.5-THD	28480	0380-1586
H27	2190-0016	3	1	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
H28	3050-1176	3	1	WASHER-FL NM 3/8 IN .39-IN-ID .562-IN-OD	88928	3050-1176
H29	0515-0664	5	5	SCREW M3 12MM-LG PAN-HP T10	28480	0515-0664
MP1	01650-47401	7	1	RPG KNOB	28480	01650-47401
MP2	5061-9448	3	1	BOTTOM COVER	28480	5061-9448
MP3	5040-7201	8	2	BOTTOM FEET	28480	5040-7201
MP4	5040-7222	3	2	BOTTOM NON SKID FEET	28480	5040-7222
MP5	1460-1345	6	2	TILT STAND SST	28480	1460-1345
MP6	8160-0590	1	2	GROUND RFI STRIP	28480	8160-0590
MP7	54110-04103	4	1	TOP COVER	28480	54110-04103
MP8	0890-0029	0	1	TUBING-HS .187-IN-D/.093-IN-RCVD	28480	0890-0029
MP9	5001-0441	2	2	TRIM STRIP SIDE	28480	5001-0441
MP10	5040-7202	9	1	TOP TRIM STRIP	28480	5040-7202
MP11	54110-40502	3	4	REAR FEET	28480	54110-40502
MP12	5060-9946	6	1	LEFT SIDE COVER-PERFORATED	28480	5060-9946
MP13	5061-9523	5	1	RIGHT SIDE COVER-PERFORATED	28480	5061-9523
MP14	5060-9805	4	1	STRAP HANDLE	28480	5060-9805
MP15	5041-6819	4	1	FRONT CAP FOR STRAP HANDLE	28480	5041-6819
MP16	5041-6820	7	1	REAR CAP FOR STRAP HANDLE	28480	5041-6820
MP17	1400-0053	4	1	CLMP-CA .187-DIA .375-WD NYL	28480	1400-0053
MP18	5021-5807	6	1	FRONT FRAME	28480	5021-5807
MP19	54120-00202	8	1	FRONT PANEL	28480	54120-00202
MP20	54111-00203	8	1	FRONT SUB PANEL	28480	54111-00203
MP21	54110-40501	2	1	DISPLAY BEZEL	28480	54110-40501
MP22	16500-00603	3	1	FAN SCREEN	28480	16500-00603
MP23	0403-0092	6	1	BUMPER FOOT-PRS-IN	28480	0403-0092

Table 5-3. HP 54120A Mainframe Replaceable Parts (Continued).

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
MP24	1400-1382	0	2	CLAMP-CABLE .35-DIA .51-WD NYL	28480	1400-1382
MP25	1400-0611	0	2	CLAMP-FL-CA 1-WD	06915	1400-0611
MP26	54111-01203	0	1	FRONT CARD CAGE BRACKET	28480	54111-01203
MP27	54111-00101	5	1	MAIN DECK	28480	54111-00101
MP28	5021 5838	3	4	SIDE STRUT	28480	5021-5838
MP29	4320-0242	6	1	U CHANNEL NPRN .062-IN-WD-CHAN	28480	4320-0242
MP30	54110-01201	7	1	TOP CRT BRACKET	28480	54110-01201
MP31	54110-01202	8	1	BOTTOM CRT BRACKET	28480	54110-01202
MP32	54110-01210	8	1	BRACKET-COLOR CRT MOD REAR-ON MODULE	28480	54110-01210
MP33	54110-04702	9	1	BRACKET-COLOR CRT MOD REAR-ON FRAME	28480	54110-04702
MP34	1400-0679	0	4	CLIP-CABLE 'U' SHP, PNL MTG TYPE	28480	1400-0679
MP35	54111-04104	6	1	POWER SUPPLY COVER-TOP	28480	54111-04104
MP36	54110-04106	7	1	POWER SUPPLY COVER-SIDE	28480	54110-04106
MP37	5021 5806	7	1	REAR FRAME	28480	5021-5806
MP38	54110-94302	4	1	WARNING LABEL	28480	54110-94302
MP39	54120-00201	7	1	REAR PANEL	28480	54120-00201
MP40	54111-05201	8	1	AIR PLENUM	28480	54111-05201
MP41	7120-4835	0	1	LABEL-INFORMATION .75-IN-WD 2-IN-LG PPR	28480	7120-4835
MP42	3160-0092	3	1	FAN GUARD	28480	3160-0092
MP44	54120-04103	6	1	FAN COVER	28480	54120-04103
MP45	54120-04702	1	1	FAN SPACER	28480	54120-04702
S1	3101 2911	5	1	ROCKER SWITCH (STANDBY)	28480	3101-2911
W1	8120-1521	6	1	POWER CABLE	28480	8120-1521
W2	54100-61602	6	1	HPIB CABLE	28480	54100-61602
W3	54120-61618	8	1	UMBILICAL CABLE 2 METRE	28480	54120-61618
W4	54120-61612	2	1	MAINFRAME CABLE ASSEMBLY	28480	54120-61612
W5	54100-61601	5	1	RIBBONCABLE-I/O TO FRONT PANEL	28480	54100-61601
W6	54100-61612	6	2	CABLE AC SD CO ANAL & DIG SD	28480	54100-61612
W7				NOT ASSIGNED		
W8	54110-61601	7	1	3 WIRE CABLE - COLOR DISPLAY MODULE POWE	28480	54110-61601
W9	54111-61610	9	1	POWER SWITCH CABLE 2 WIRE-FRONT PANEL ST	28480	54110-61610
W10	54111-61611	0	1	2 WIRE CABLE-REAR CABLE STBY SWITCH	28480	54111-61611
W11	54110-61611	9	1	DISPLAY CONTROL CABLE	28480	54110-61611
W12	54110-61607	3	1	RIBBON CABLE DISP ASSY TO COLOR MODULE	28480	54110-61607

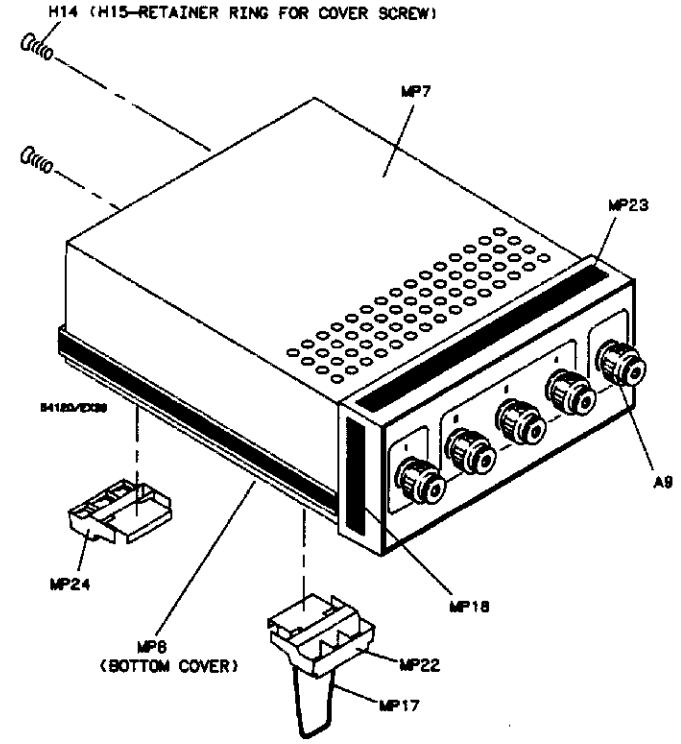


Figure 5-7. Four Channel Test Set Assembled View.

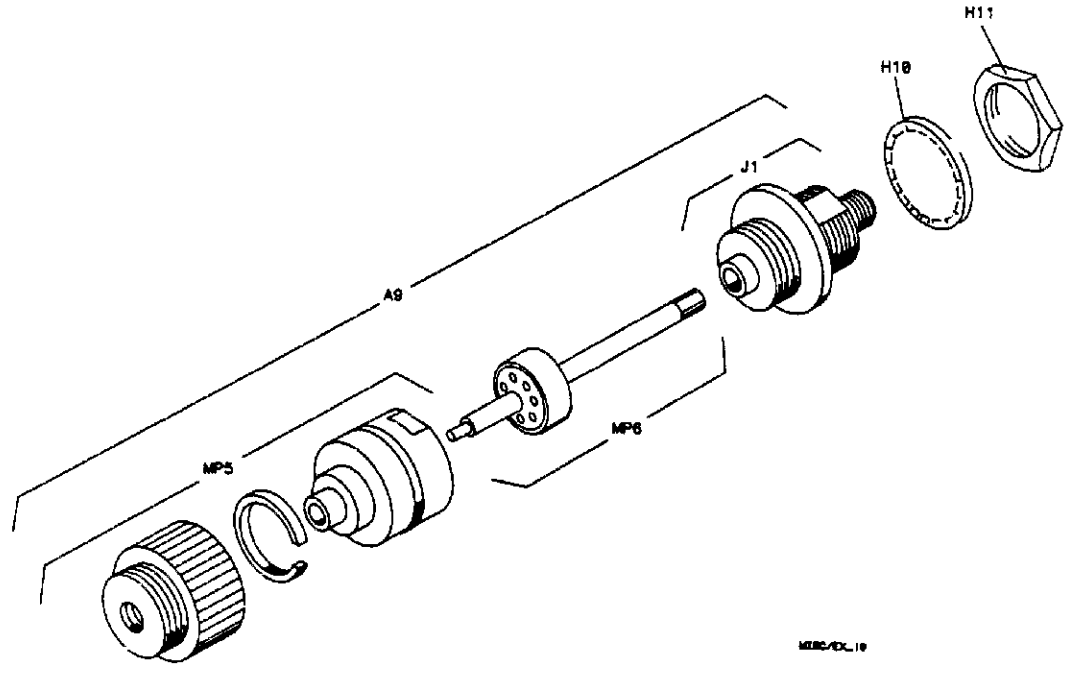


Figure 5-8. APC 3.5 Connector Exploded View.

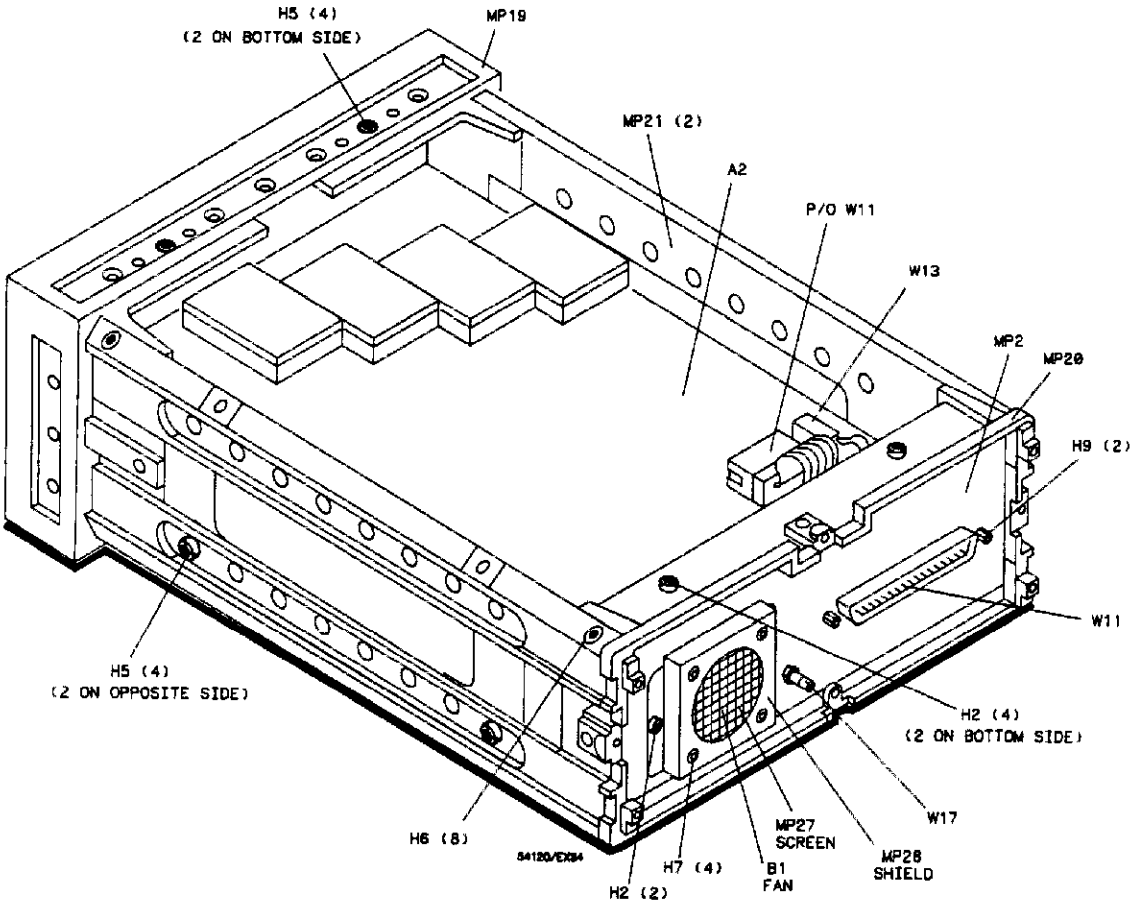


Figure 5-9. Four Channel Test Set Top View.

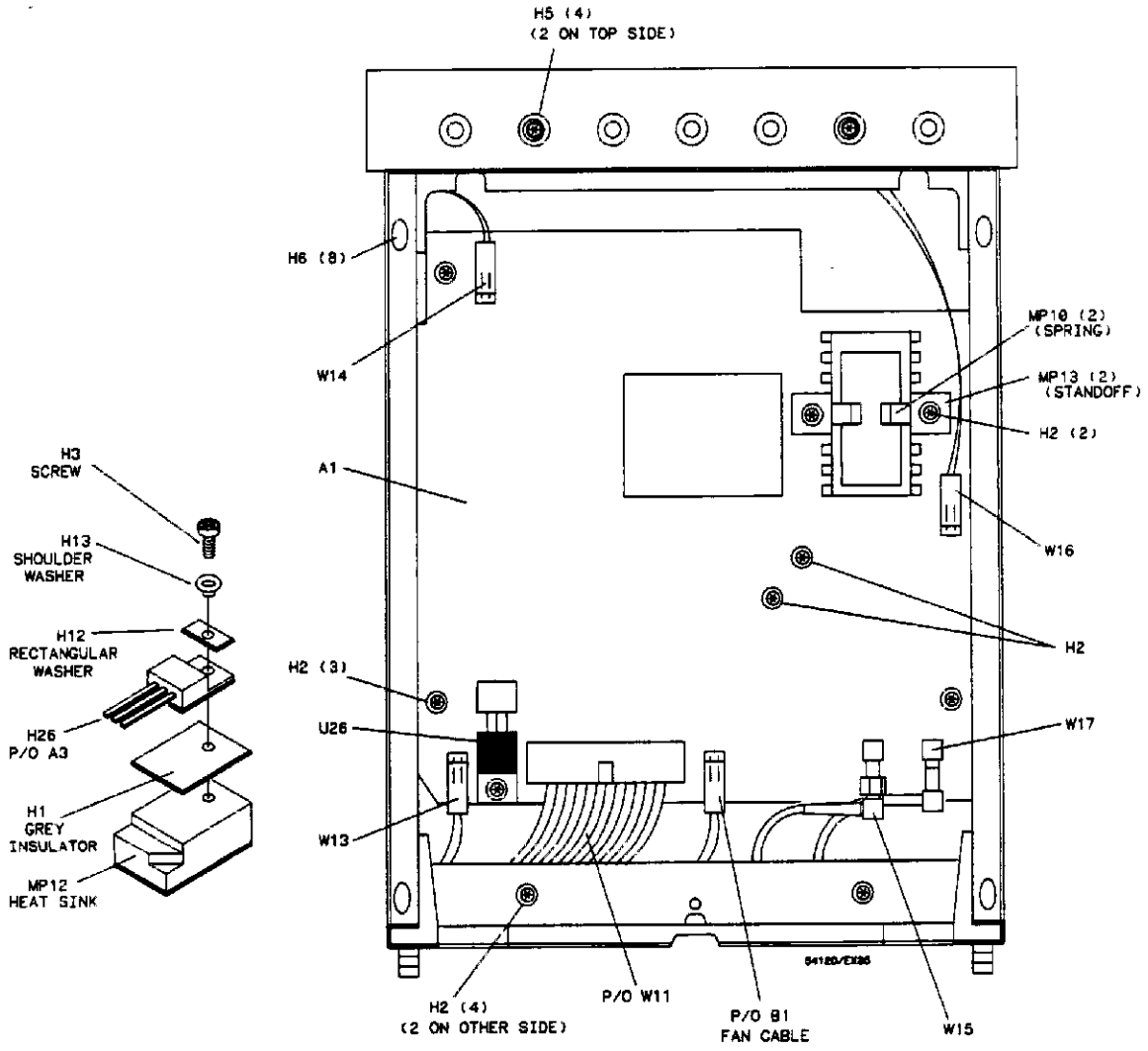


Figure 5-10. Four Channel Test Set Bottom View.

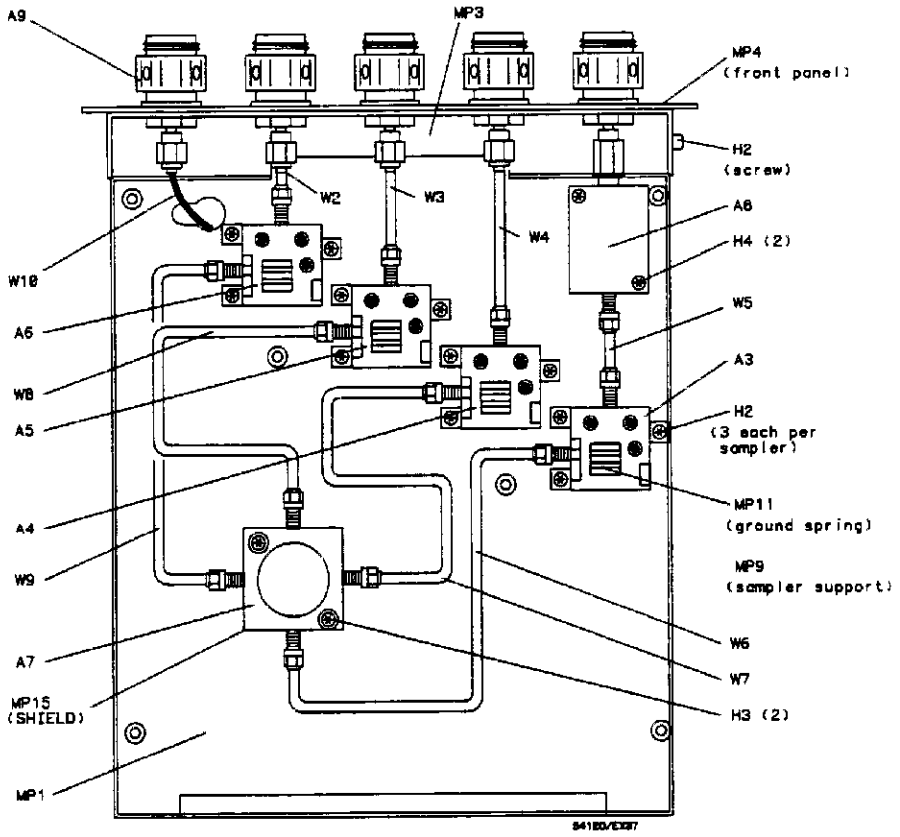


Figure 5-11. Four Channel Test Set Main Deck Top View.
(These Parts are Under the Vertical Assembly)

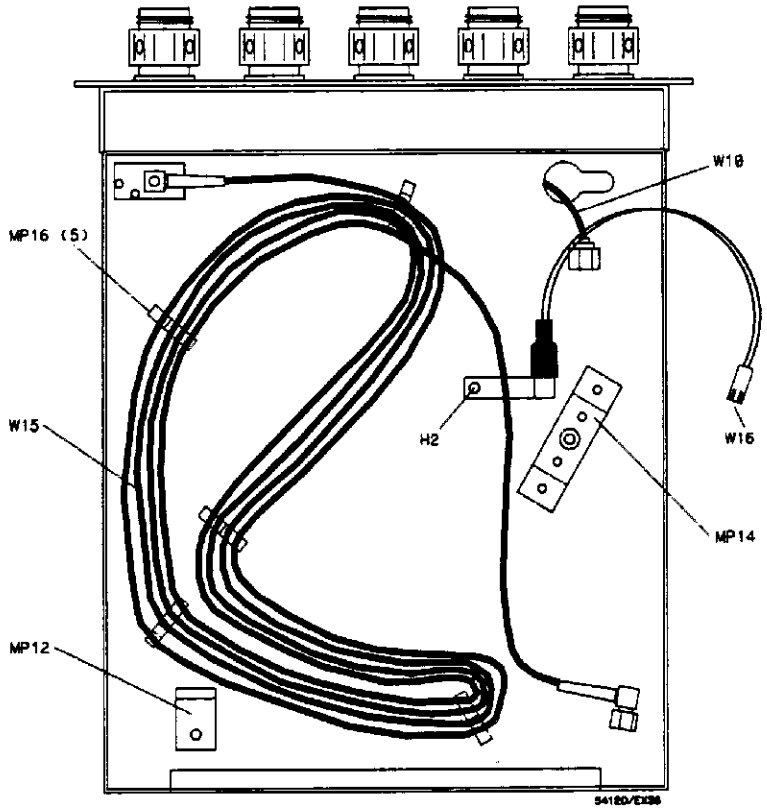


Figure 5-12. Four Channel Test Set Main Deck Bottom View.
(These Parts are Under the Horizontal Assembly)

Table 5-4. HP 54121A Four Channel Test Set Replaceable Parts.

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
				* EXCHANGE ASSEMBLIES		
* A1	54120-69507	0	0	HORIZONTAL ASSEMBLY	28480	54120-69507
* A2	54120-69506	9	0	VERTICAL ASSEMBLY	28480	54120-69506
A1	54120-66507	4	1	HORIZONTAL ASSEMBLY	28480	54120-66507
A2	54120-66506	3	1	VERTICAL ASSEMBLY	28480	54120-66506
A3	5086-7460	7	4	SAMPLER	28480	5086-7460
A4	5086-7460	7		SAMPLER	28480	5086-7460
A5	5086-7460	7		SAMPLER	28480	5086-7460
A6	5086-7460	7		SAMPLER	28480	5086-7460
A7	5086-7461	8	1	PULSE FILTER	28480	5086-7461
A8	5086-7471	3	1	TDR STEP GENERATOR	28480	5086-7471
A9	5062-1247	6	5	FRONT PANEL APC 3.5 CONNECTOR ASSEMBLY	28480	5062-1247
A1U1	INB7-8160	6	1	500 MHZ TRIGGER HYBIRD	28480	INB7-8160
B1	54121-88501	5	1	FAN-TUBAXIAL WITH CONNECTOR	28480	54121-88501
H1	0340-1074	2	1	INSULATOR-XSTR THRM-CNDCT	28480	0340-1074
H2	0515-0372	2	35	SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H3	0515-0664	5	6	SCREW-MACHINE ASSEMBLY M3 X 0.5 12MM-LG	28480	0515-0664
H4	0515-0666	7	2	SCREW-MACHINE ASSEMBLY M3 X 0.5 18MM-LG	28480	0515-0666
H5	0515-1031	2	4	SCREW-MACH M3 X 0.5 6MM-LG 90-DEG-FLH-HD	28480	0515-1031
H6	0515-1403	2	8	SCREW-SPCL M4 X 0.7 8MM-LG 90-DEG-FLH-HD	28480	0515-1403
H7	0515-1038	9	4	M3 PANHEAD 35L	28480	0515-1038
H7-8				NOT ASSIGNED		
H9	1251-2942	7	2	SCREW LOCK KIT-SUBMIN D CONN	28480	1251-2942
H10	2190-0914	0	5	WASHER-LK INTL T 7/16 IN .472-IN-ID	28480	2190-0914
H11	2950-0132	8	5	NUT-HEX-DBL-CHAM 7/16-28-THD .094-IN-THK	28480	2950-0132
H12	3050-1071	7	1	WASHER-RECTANGULAR 10.28 MM LG, 5.59 MM	04713	3050-1071
H13	3050-1140	1	1	WASHER-SHLDR 3.0 MM 3-MM-ID 3.58-MM-OD	28480	3050-1140
H14	0515-1245	0	2	COVER SCREW	28480	0515-1245
H15	0515-1253	0	2	RETAIN RING FOR COVER SCREW	28480	0515-1253
J1	08513-20017	6	5	APC 3.5 BULKHEAD CONNECTOR P/O A9	28480	08513-20017
MP1	54120-00102	7	1	MAIN DECK	28480	54120-00102
MP2	54120-00206	3	1	REAR PANEL	28480	54120-00206
MP3	54120-00204	0	1	SUB PANEL LOWER BRACKET	28480	54120-00204
MP4	54120-00205	1	1	FRONT PANEL	28480	54120-00205
MP5	5062-1245	4	5	APC 3.5 CONNECTOR BODY P/O A9	28480	5062-1246
MP6	5062-1243	2	5	APC 3.5 CENTER CONDUCTOR P/O A9	28480	5062-1243
MP7	54120-04104	7	1	TOP COVER	28480	54120-04014
MP8	54120-04105	8	1	BOTTOM COVER	28480	54120-04105
MP9	54120-04701	0	4	SAMPLER SUPPORT	28480	54120-04701
MP10	54120-09101	4	2	TRIGGER SPRING	28480	54120-09101
MP11	54120-09102	5	4	SAMPLER GROUND SPRING	28480	54120-09102
MP12	54120-21102	1	1	HEATSINK	28480	54120-21102
MP13	0380-1949	4	2	TRIGGER STANDOFF	28480	0380-1949
MP14	54120-24701	2	1	PULSE FILTER GROUND BLOCK	28480	54120-24701
MP15	54120-45401	3	1	PULSE FILTER SHIELD	28480	54120-45401
MP16	1400-0866	7	5	CLAMP-CABLE .187-DIA .25-WD NYL	28480	1400-0866
MP17	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP18	5001-0438	7	2	SIDE TRIM STRIP	28480	5001-0438
MP19	5021-5813	4	1	FRONT FRAME	28480	5021-5813
MP20	5021-5814	5	1	REAR FRAME	28480	5021-5814
MP21	5021-5884	9	2	SIDE STRUT	28480	5021-5884
MP22	5040-7201	8	2	BOTTOM FEET	28480	5040-7201
MP23	5040-7203	0	1	TOP FRONT TRIM STRIP	28480	5040-7203
MP24	5040-7222	3	2	NON SKID FOOT	28480	5040-7222
MP25	0960-0055	1	5	CAP-COAX TO FIT F-SMA SHTG	28480	0960-0055
MP26	54121-04701	1	1	FAN SPACER	28480	54121-04701
MP27	54120-00604	4	1	FAN SCREEN	28480	54120-00604
MP28	54120-00605	5	1	FAN SHIELD	28480	54120-00605
W1				NOT ASSIGNED		
W2	54120-61602	0	1	SEMI-RIGID CABLE CH4 SAMPLER TO FRONT PANEL	28480	54120-61602
W3	54120-61603	1	1	SEMI-RIGID CABLE CH3 SAMPLER TO FRONT PANEL	28480	54120-61603
W4	54120-61604	2	1	SEMI-RIGID CABLE CH2 SAMPLER TO FRONT PANEL	28480	54120-61604
W5	54120-61605	3	1	SEMI-RIGID CABLE CH1 SAMPLER TO TDR	28480	54120-61605
W6	54120-61606	4	1	SEMI-RIGID CABLE CH1 SAMPLER TO PULSE FILTER	28480	54120-61606
W7	54120-61607	5	1	SEMI-RIGID CABLE CH2 SAMPLER TO PULSE FILTER	28480	54120-61607
W8	54120-61608	6	1	SEMI-RIGID CABLE CH3 SAMPLER TO PULSE FILTER	28480	54120-61608
W9	54120-61609	7	1	SEMI-RIGID CABLE CH4 SAMPLER TO PULSE FILTER	28480	54120-61609
W10	54120-61610	0	1	SEMI-RIGID CABLE TRIGGER TO FRONT PANEL	28480	54120-61610
W11	54120-61611	1	1	TEST SET CABLE ASSEMBLY	28480	54120-61611
W12				NOT ASSIGNED		
W13	54120-61613	3	1	2 WIRE INTERCONNECT CABLE VERTICAL TO HORIZON	28480	54120-61613
W14	54120-61614	4	1	2 WIRE CABLE TDR TO HORIZONTAL ASSEMBLY	28480	54120-61614
W15	54120-61615	5	1	TDR DELAY LINE COAXIAL CABLE-ON MAIN DECK	28480	54120-61615
W16	54120-61616	6	1	2 WIRE CABLE TEMPERATURE SENSE TO HORIZON	28480	54120-61616
W17	54120-61617	7	1	TRIGGER CABLE-REAR PANEL	28480	54120-61617

TABLE OF CONTENTS

MAINFRAME DISASSEMBLY

SECTION 6A. MAINFRAME DISASSEMBLY

6A-1. INTRODUCTION

This section contains removal and replacement procedures for HP 54120A Digitizing Oscilloscope Mainframe assemblies.

6A-2. SAFETY CONSIDERATIONS

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

WARNING

This instrument is equipped with a standby switch on the front panel that DOES NOT de-energize the power supply. To avoid shock hazards capable of causing injury or death, the main power switch on the rear panel must be used to de-energize the instrument or the power cable must be disconnected when the instrument must be de-energized.

WARNING

These procedures are used while repairing an instrument that has protective covers removed and may have had power applied. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Read the Safety Summary in the front of this manual.

CAUTION

Do not remove or replace any of the circuit board assemblies in the instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

CAUTION

The HP 54121A Four Channel Test Set is very sensitive to static discharge. Failure to observe proper antistatic methods may result in damage to the gallium arsenide samplers All maintenance or operation should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

6A-3. TOOLS REQUIRED

The hardware requires TORX® type tools for removal and replacement. Sizes required for the procedures in this section are #10 and #15. A medium posi drive is used for the top cover.

If the display must be replaced, an 8 mm wrench or driver is also required.

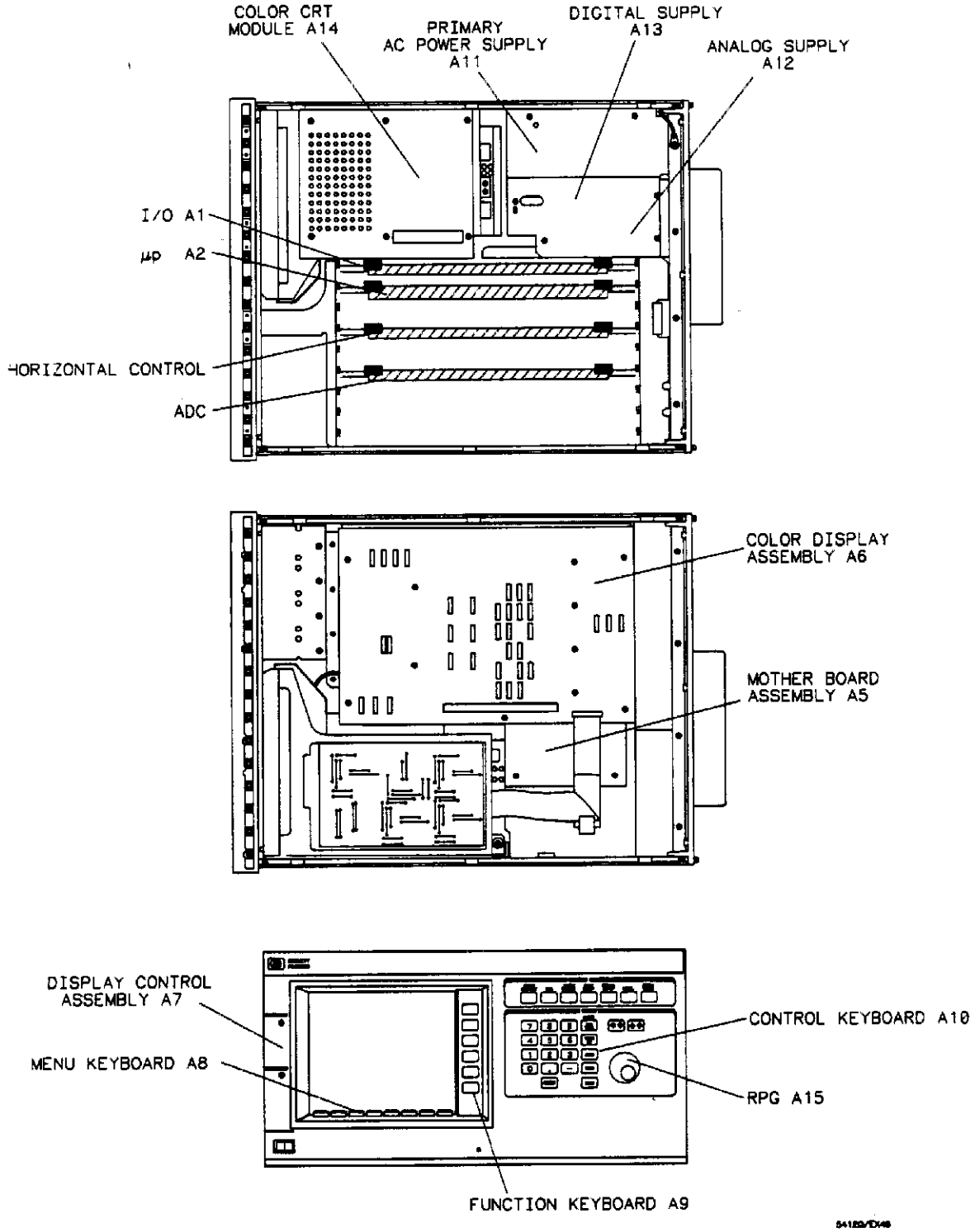


Figure 6A-1. Major Assembly Locations.

6A-4. MAJOR ASSEMBLY REMOVAL PROCEDURES

The following procedures should be followed when disassembling the instrument. Particular care should be taken when inserting the card cage assemblies into the mainframe to avoid bending the connector pins. There are only four cables connecting to the card cage assemblies. These four cables are different in size and it's impossible to connect the cables wrong.

6A-5. Card Cage PC Assemblies

REMOVAL

1. Disconnect power cable.
2. Remove top rear feet and top cover.
3. Disconnect any cables from assembly to be removed.
4. Refer to the illustration on top of the power supply shield. Release PC assembly by pulling the flexible plastic extractors away from the assembly shield, then up.
5. Remove the assembly from the connector by pulling up on the extractors.

REPLACEMENT

1. Insert PC assembly shield edges in proper guides.
2. Keep the extractors up while sliding the assembly in.
3. While keeping assembly properly aligned in guides, push it in. As the top edge of the assembly becomes level with the top of the card cage the connector will start to engage. Keep assembly level and apply even pressure until connector is seated.
4. Reconnect all cables which were disconnected from any assemblies.

CAUTION

Do not use the extractors to lever the assembly into the connector. *Using the extractors makes it too easy to apply excessive force that might bend misaligned connector pins. If the connector will not seat, remove the assembly and check for bent pins. Bent pins are very expensive and time consuming to replace on a motherboard SIB connector.*

Avoid pinching cabling between the assembly and the mainframe.

6A-6. Primary Power Supply

REMOVAL

1. Disconnect power cable.
2. Remove rear feet from top right corner and left side.
3. Remove top and left side covers.

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

4. Through the hole in the top power supply shield, observe the red LED on the primary power supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding (approximately three minutes).
5. Remove top power supply shield (six screws).
6. Remove the screw that attaches the ground wire (green/yellow) to top corner of rear frame.
7. Remove the three cables at the top front of the primary power supply PC assembly.
8. Remove four screws from power supply side cover (figure 6A-2).
9. Remove two screws which attach power supply assembly to rear panel (figure 6A-2).
10. Turn instrument onto its left side. Pull the power supply assembly rearward until the STBY switch cable at the rear of power supply assembly can be disconnected. Disconnect the cable.
11. Pull supply rearward until it clears the instrument.

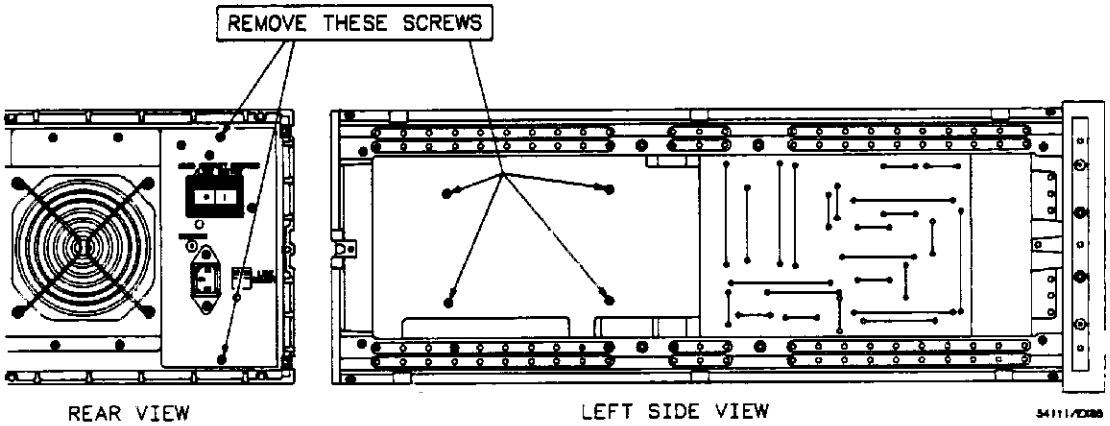


Figure 6A-2. Primary Power Supply Mounting Screws.

PRIMARY POWER SUPPLY REPLACEMENT

Reverse removal procedure to install supply.

WARNING

Power supply safety grounding will be defeated if ground wire removed in step 6 above is not reconnected. To avoid a defeated ground, make sure this green/yellow wire is re-attached to top rear corner of the rear frame.

6A-7. Analog Power Supply

REMOVAL

1. Disconnect power cable.
2. Remove top rear feet and top cover.

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

3. Through the hole in the top power supply shield, observe the red LED on the primary power supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding (approximately three minutes).
4. Remove top power supply shield (six screws).
5. Disconnect the analog power supply input cable from the top front corner of the primary power supply.
6. Use a flat-blade screwdriver to loosen the captive screw at the bottom front of the supply.
7. It may be easier to remove the analog supply by first removing the I/O assembly from the mainframe. However, this will cause a loss of all front panel cals, any stored front panel setups, and all stored waveforms.
8. Release power supply board connector by pulling board straight up and off the guide posts.

REPLACEMENT

Reverse the removal procedure to install assembly.

6A-8. Digital Power Supply

REMOVAL

1. Disconnect power cable.
2. Remove top rear feet and top cover.

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

3. Through the hole in the top power supply shield, observe the red LED on the primary power supply. This LED indicates the presence of 300 volts. It will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding (approximately three minutes)
4. Remove top power supply shield (six screws).
5. Disconnect the Digital Power Supply input cable from the top front corner of the Primary Power Supply.
6. Use a flat-blade screwdriver to loosen the captive screw at the front bottom of the supply.
7. Release power supply board connector by pulling board straight up and off guide posts.
8. Remove the supply from the instrument by lifting front edge of board first then rotating board up and out.

REPLACEMENT

Reverse removal procedure to install board.

6A-9. CRT Bezel, Function and Menu Keyboards

The keyboards at the side and bottom of the CRT can be removed by first removing the CRT bezel.

REMOVAL

1. While pushing down on top edge of bezel (see figure 6A-3), pull top edge away from front panel until holding tabs are clear of the front panel.
2. Lift bezel slightly and pull bottom of bezel away from front panel.
3. Pull bezel away from front panel just far enough to gain access to the ribbon cable connectors on control keyboard. They are just to the right of the bezel opening in the front panel.
4. Disconnect the two ribbon cable connectors from the control keyboard.
5. If either the function or menu keyboard needs replaced, they are each attached to the bezel with two screws.

REPLACEMENT

Reverse the removal procedure to install bezel.

NOTE

The ribbon cables must be reconnected as follows: function keyboard cable (right side of bezel) to top connector on control keyboard and menu keyboard cable (bottom of bezel) to bottom connector on control keyboard.

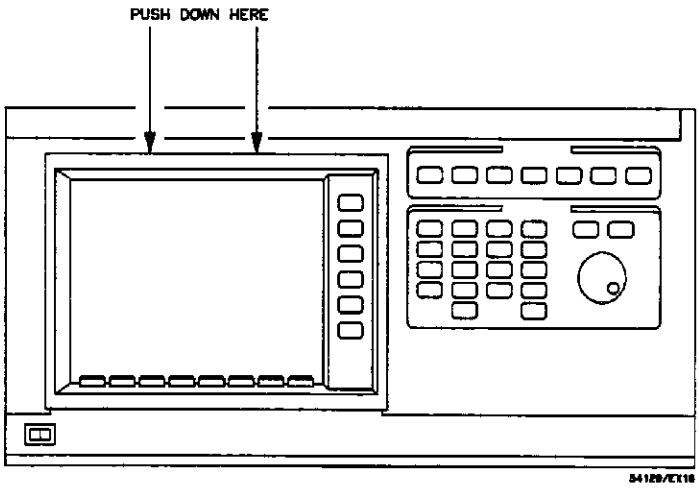


Figure 6A-3. CRT Bezel Removal Pressure Locations.

6A-10. Front Panel, Control Keyboard, and Display Control

Use steps 1 through 10 to remove front panel, steps 1 through 11 to remove display control, and steps 1 through 10 and steps 12 and 13 to remove control keyboard.

NOTE

It is not necessary to remove the front panel to remove the keyboards around the CRT bezel. See the previous removal procedure.

FRONT PANEL REMOVAL

1. Disconnect power cable.
2. Remove rear feet and top, bottom, and side covers.
3. Remove top, and side trim strips from the front frame by carefully prying up at the strip's ends with a flat blade screwdriver.
4. Remove two front panel screws that are under each side trim strip.
5. Remove six front panel screws as shown in figure 6A-4.

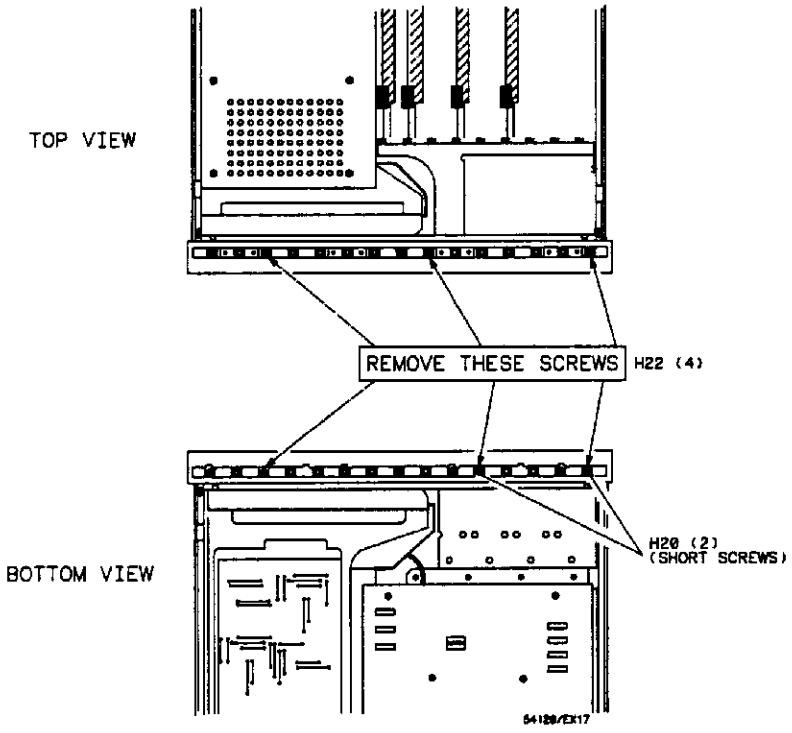


Figure 6A-4. Top and Bottom Front Panel Mounting Screws.

6. Set instrument in its normal operating position.

7. Disconnect the STBY switch by separating the two-wire interconnect just to the right of the CRT.

8. Pull front panel just far enough to gain access to the cable connector on the CRT control board (left side of front panel) and disconnect the cable.

9. Open the two cable ties: top left, inside front panel and top right of CRT, and remove the cables.

10. Disconnect the large ribbon cable from the control keyboard and remove the front panel from the instrument.

DISPLAY CONTROL REMOVAL

11. Remove two screws attaching the display control assembly.

CONTROL KEYBOARD REMOVAL

12. Disconnect the RPG cable at the control keyboard and the two cables from the CRT bezel keyboards.

    The menu keyboard (right side of bezel) cable connects to the top connector and the function keyboard (bottom of bezel) cable connects to the bottom connector on the control keyboard.

13. Remove five screws to remove the board.

    Pass RPG cable through hole in control keyboard.

ASSEMBLY REPLACEMENT

Reverse the procedure to replace any of these assemblies.

6A-11. Color CRT Module

The color CRT module is replaceable only as a complete unit.

COLOR CRT MODULE REMOVAL

1. Remove front panel (refer to the appropriate paragraph in this section).
2. Disconnect the flat wide ribbon cable from the color display assembly and remove cable from clip.
3. Remove four screws that attach the color display module to the front frame. Refer to figure 6A-5.
4. Remove two screws attaching side of module to left side corner struts. Refer to figure 6A-5.
5. Slowly pull module forward until the power cable (small three-wire) can be disconnected at the primary power supply board.
6. Continue pulling module forward until it clears the instrument.

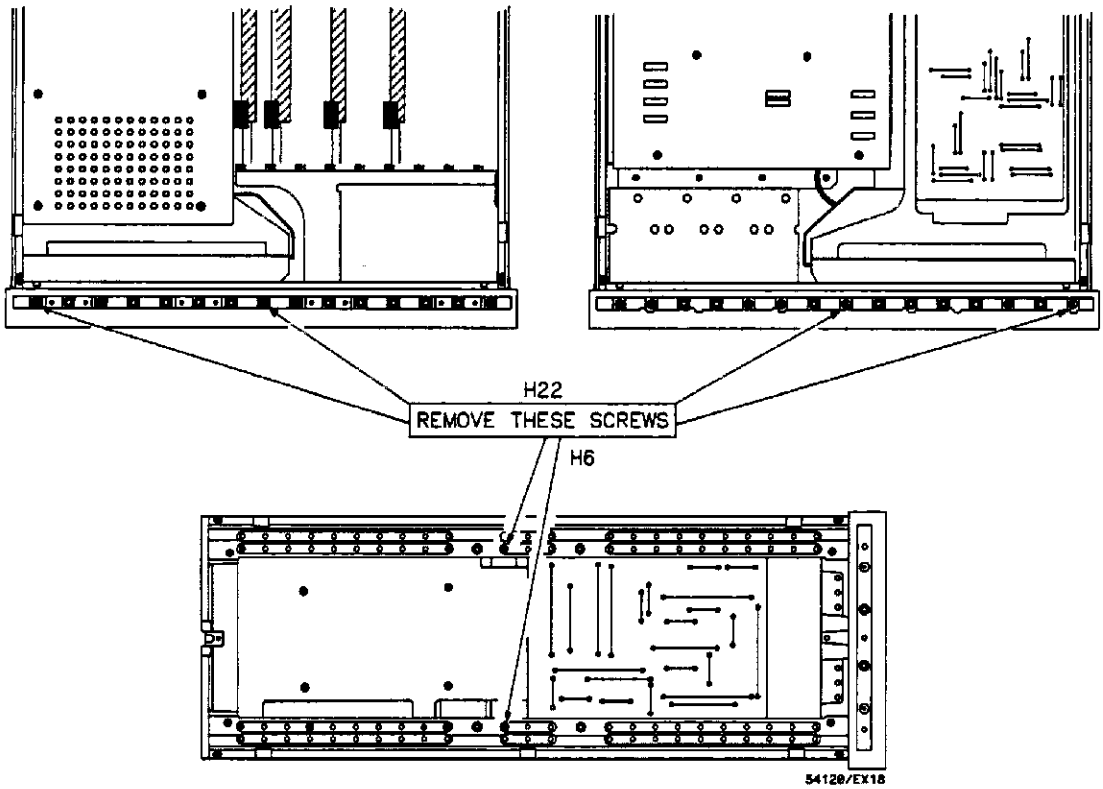


Figure 6A-5. Color CRT Module Mounting Screws.

REPLACEMENT

It is necessary to use the following procedure to remove several items from the inoperative color CRT module and install them on the new one. These parts are not included with a new color monitor module.

TRANSFER PARTS TO NEW MODULE

1. Remove the eight small screws that hold the shield to the top and side of the inoperative module.

   THESE SCREWS ARE SPECIAL self-tapping screws, different from the screws in the rest of the instrument. They must be used for mounting the shield on the new module. Do not use them for any other purpose.

2. Use an 8 mm wrench to remove the four nuts on the front of the inoperative module and remove the shield.

3. Remove the front mounting brackets and put the 8 mm nuts back on the module.

4. Remove the 8 mm nuts from the new module, do not remove any other hardware, and install the front mounting brackets.

5. Install the shield on the new module. Place it over the two front mounting screws and front mounting brackets.

6. Install the four 8 mm nuts but leave them loose so the shield can move.

7. Use the special self-tapping screws (step 1) to fasten the top and side of the shield. They will be hard to start while they are tapping the holes. Be careful that excessive tightening does not strip the self- tapped holes.

8. Tighten the 8 mm nuts at the front of the module.

9. The rear bracket is two brackets connected together by shock mounting hardware. Remove the two screws that hold the bracket assembly to the rear of the inoperative module.

   THESE SCREWS ARE SPECIAL self-tapping screws that must be used for mounting the bracket assembly on the new display. Do not use them for any other purpose.

10. Mount the rear bracket assembly on the new module. The screws will be hard to start because they must self-tap the mounting holes. Be careful that excessive tightening does not strip the self-tapped holes.

11. Note the routing of the power cable and CRT control cable and one at a time, remove them and install them on the new module.

12. Remove the wide flat ribbon cable from the old module and install it on the new one.

INSTALL NEW MODULE

13. Install the new module most of the way into the instrument. Avoid pinching cables as module is being installed.

14. Connect the power cable to the appropriate connector at the top front corner of the primary power supply and slide module the rest of the way in.

15. Install, but do not tighten, the two rear and four front mounting screws. Refer to figure 6A-5.

16. Install the front panel. Use the steps given in the front panel procedure except for steps 3, 2, and 1.

17. Push the module forward, closing as much as possible the gap between the CRT and the bezel. Tighten the two rear and four front mounting screws.

18. Complete the rest of the instrument assembly by doing steps 3, 2, and 1 of the front panel procedure.

6A-12. Fan

REMOVAL

1. Disconnect power cable.
2. Remove bottom rear feet and bottom cover.
3. Disconnect fan power cable from rear corner of motherboard.
4. Remove fan housing mounting screws as shown in in the figure 6A-6.
5. While noting fan cable routing, carefully remove fan housing from instrument.

REPLACEMENT

Reverse removal procedure to install fan. Be sure fan power cable does not get pinched between fan and rear panel.

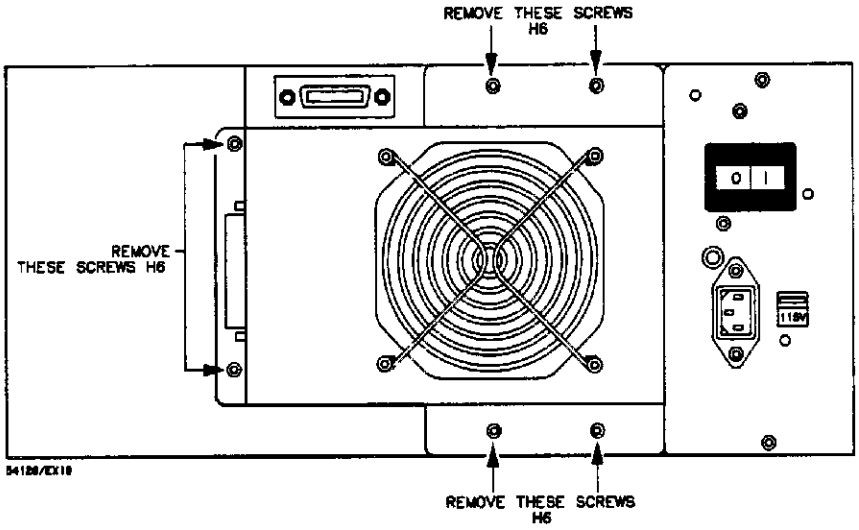


Figure 6A-6. Fan Housing Mounting Screws.

6A-13. Color Display Assembly

REMOVAL

1. Disconnect power cable.
2. Remove bottom rear feet and bottom cover.
3. Disconnect wide ribbon cable from color display assembly.
4. Refer to figure 6A-7 to remove eleven assembly mounting screws.
5. Carefully lift board straight up to disengage motherboard connector.

NOTE

The display assembly to motherboard connector will exhibit some removal resistance while the board is being removed. It is recommended the major lifting force be exerted on the edge of the color display assembly at the connector.

6. Note the "comb" type connector used between the color display assembly and motherboard. It consists of two separate combs held in place on the color display assembly by a connector guide and two screws. **If the assembly is being replaced, this connector guide and the two comb connectors must be removed from the old assembly and installed on the new one. The connector DOES NOT come with the new assembly.**

REPLACEMENT

Reverse removal procedure to install assembly. Use additional care when inserting the connector pins into connector on motherboard.

NOTE

Power for the color display assembly is obtained from the motherboard by the four short mounting screws. Their positions are marked +5 and GD on the board. These mounting screws must be installed and tightened before proper operation of the instrument can be expected.

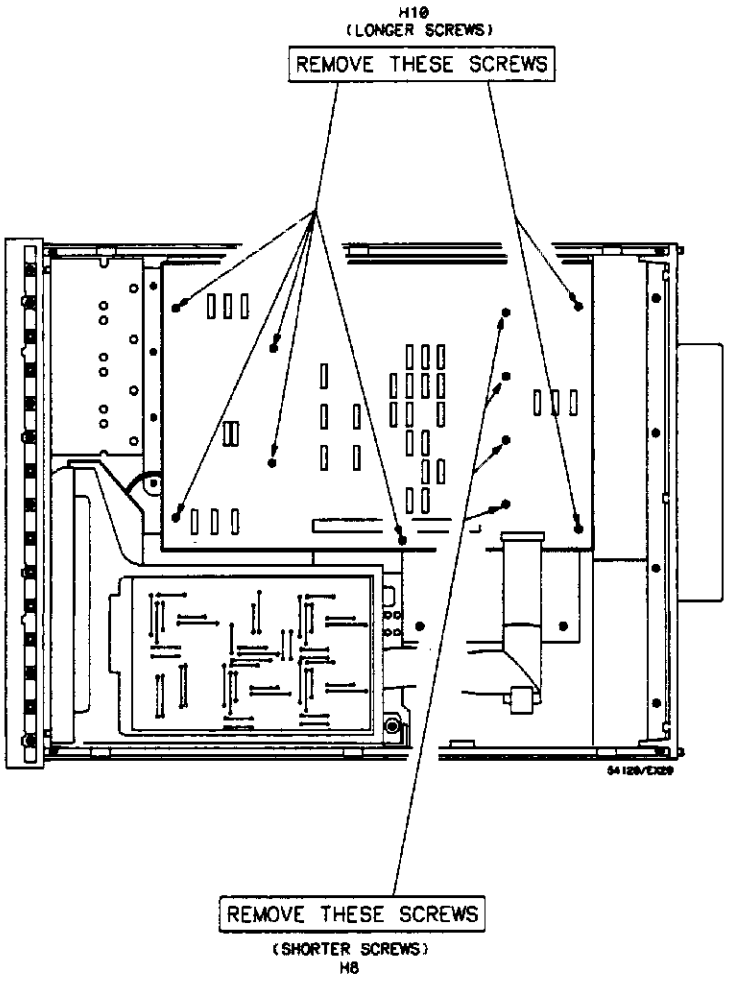


Figure 6A-7. Color Display Assembly Mounting Screws.

6A-14. Motherboard

REMOVAL

1. Disconnect power cable.
2. Remove rear feet and all covers.
3. Remove all card cage PC boards (refer to earlier paragraph).
4. Remove analog power supply and digital power supply (refer to earlier paragraphs).
5. Remove color display assembly (refer to earlier paragraph).
6. Disconnect fan power cable connector from rear corner of motherboard.
7. Loosen the STBY switch cable by removing the two nylon cable clamps from bottom of motherboard. Squeeze the clamps and pull them from the holes in the board.
8. Remove the remaining mounting screws and remove board. Refer to figure 6A-8.

REPLACEMENT

Reverse removal procedure to install board.

NOTE

The motherboard and display board share some of the same mounting screws. Therefore, when installing the motherboard install only the screws removed in step 8 above. Refer to figure 6A-8.

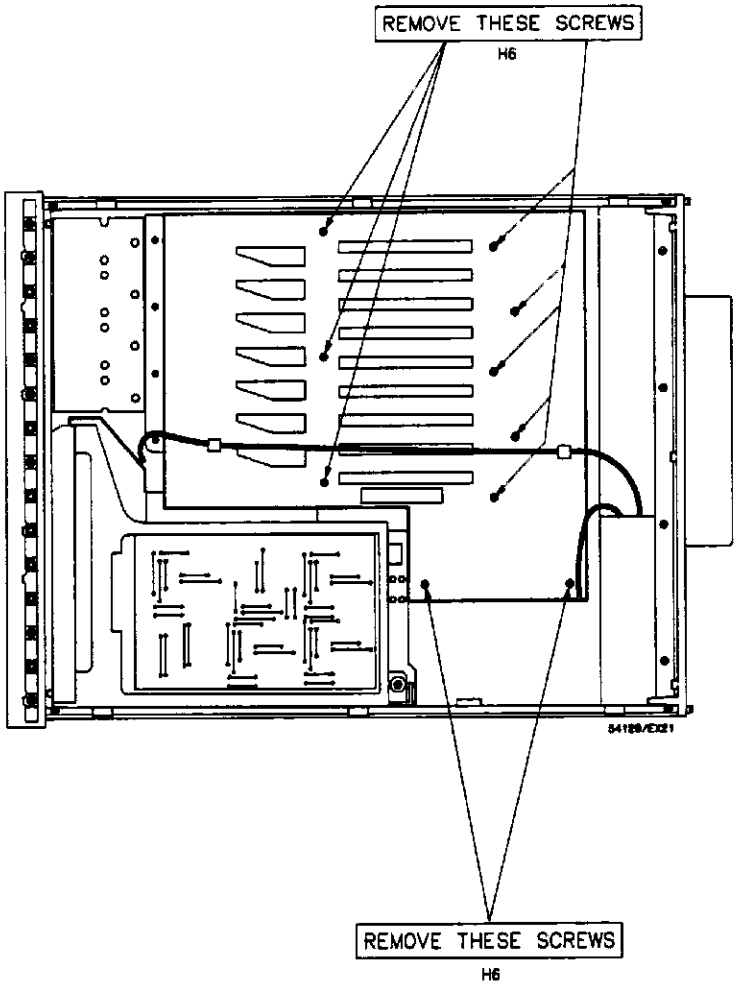


Figure 6A-8. Motherboard Mounting Screws.

TABLE OF CONTENTS

TEST SET DISASSEMBLY

SECTION 6A. TEST SET DISASSEMBLY

6A-17. INTRODUCTION

This section contains removal and replacement procedures for HP 54121A Four Channel Test Set assemblies.

6A-18. SAFETY CONSIDERATIONS

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

WARNING

This instrument is equipped with a standby switch on the front panel that DOES NOT de-energize the power supply. To avoid shock hazards capable of causing injury or death, the main power switch on the rear panel must be used to de-energize the instrument or the power cable must be disconnected when the instrument must be de-energized.

WARNING

These procedures are used while repairing an instrument that has protective covers removed and may have had power applied. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Read the Safety Summary in the front of this manual.

CAUTION

Do not remove or replace any of the circuit board assemblies in the instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

CAUTION

The HP 54121A Four Channel Test Set is very sensitive to static discharge. Failure to observe proper antistatic methods may result in damage to the gallium arsenide samplers. All maintenance or operation should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

6A-19. TOOLS REQUIRED

The hardware requires TORX® type tools for removal and replacement. Sizes required for the procedures in this section are #10 and #15. A medium posi drive is used for the covers. The other tools used in this section are: 5/16 inch open end wrench, 9/16 inch open end wrench (this wrench is a thin wrench HP part number 8710-1770), used in paragraph 6A-31), 1/4 inch nut driver, 5 mm nut driver, and torque wrench set to 5 in/lbs.

6A-20. TEST SET FAN

REMOVAL

1. Disconnect power cable.
2. Remove bottom cover.
3. Remove two screws holding fan assembly to rear panel. Refer to figure 6A-9
4. Unplug fan cable from J6 on the horizontal assembly.
5. Slowly pull fan assembly away from test set while feeding fan cable through fan opening in rear panel.
6. Remove four screws which hold fan to fan assembly.

REPLACEMENT

1. Reverse removal procedure to install fan.

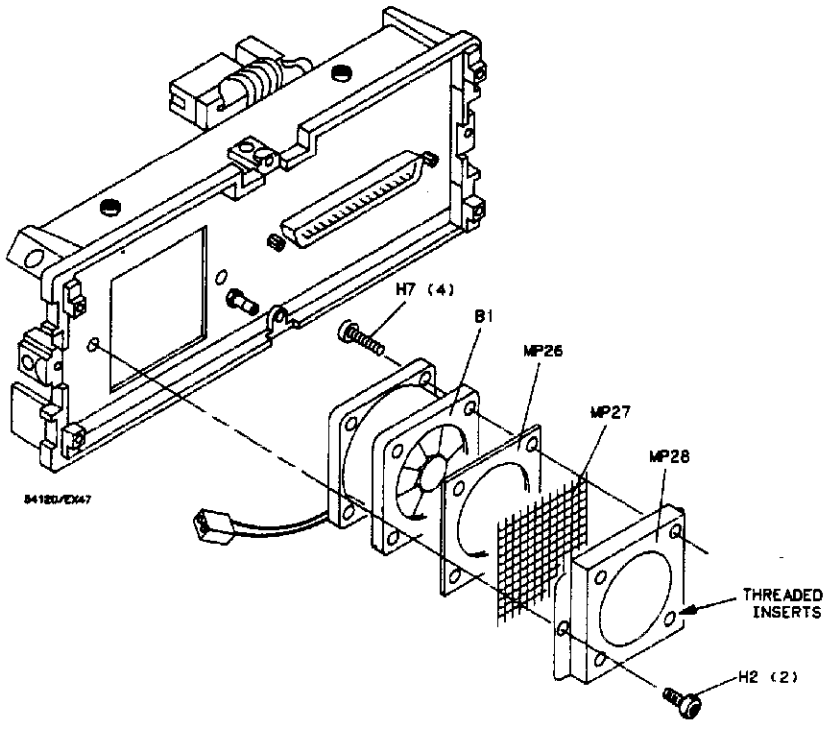


Figure 6A-9. Test Set Fan Removal.

6A-21. REAR PANEL

REMOVAL

1. Disconnect power cable.
2. Remove top and bottom covers.
3. Remove four screws from top and bottom of rear casting. Refer to figure 6A-10.
4. Disconnect fan cable from J6 on the horizontal assembly.
5. Disconnect ribbon cables from J7 on the horizontal assembly and J1 on the vertical assembly.
6. Disconnect trigger power cable from connector J3 on the horizontal assembly.
7. Pull rear panel away from test set.

REPLACEMENT

1. Reverse removal procedure to install rear panel.

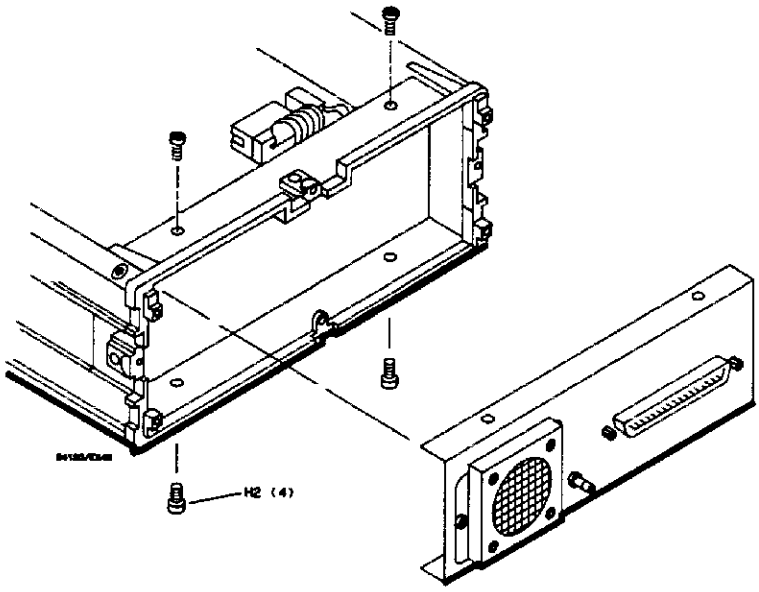


Figure 6A-10. Rear Panel Removal.

6A-22. TEST SET CABLE ASSEMBLY

REMOVAL

1. Disconnect power cable.
2. Remove umbilical cable from the test set.
3. Remove rear panel from test set. Refer to paragraph 6A-21.
4. Remove two screws which attach test set cable assembly to the rear panel with a 5 mm nut driver or wrench. Refer to figure 6A-11.

REPLACEMENT

1. Reverse removal procedure to install cable.

NOTE

The factory applies a small amount of loctite on each screw's threads before installing screws. This prevents the screws from loosening after repeated removal and installing of the umbilical cable.

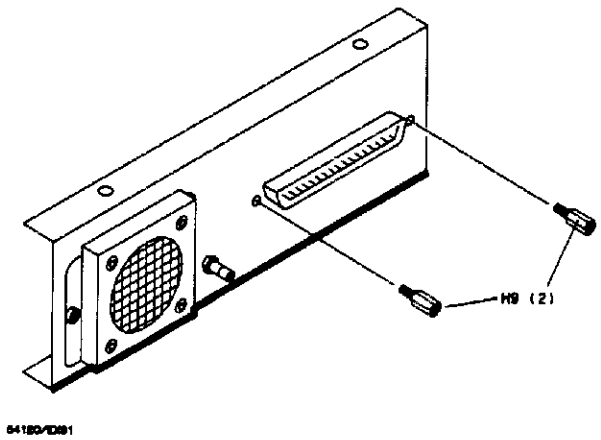


Figure 6A-11. Test Set Cable Assembly Removal.

6A-23. TRIGGER POWER CABLE

REMOVAL

1. Disconnect power cable.
2. Remove rear panel from test set. Refer to paragraph 6A-21.
3. Use a 1/4" nut driver or wrench to remove hex nut and washer which attach the trigger power cable to the rear panel. Refer to figure 6A-12.

REPLACEMENT

1. Reverse removal procedure to install cable.

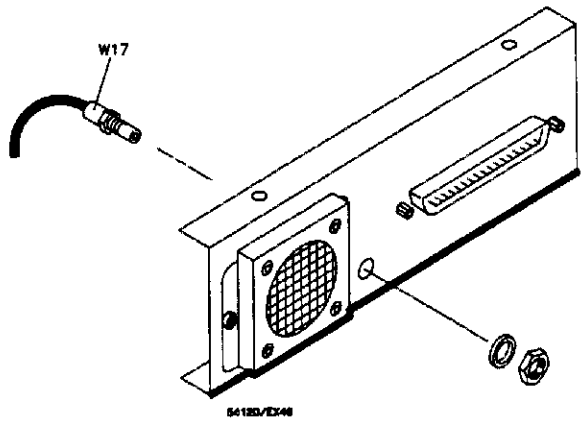


Figure 6A-12. Trigger Power Cable.

6A-24. MAIN DECK ASSEMBLY

REMOVAL

1. Disconnect power cable.
2. Remove top and bottom covers.
3. Remove two screws from each side rail. Refer to figure 6A-13.
4. Remove four screws from top and bottom of front casting. Refer to figure 6A-13.
5. Disconnect fan assembly cable from J6 on horizontal assembly.
6. Disconnect TDR delay line from connector J4 on the horizontal assembly.
7. Disconnect ribbon cables from J1 on vertical and J7 on horizontal assembly.
8. Slowly pull main deck assembly out of frame, to avoid snagging parts on frame.

REPLACEMENT

1. Reverse removal procedure to install main deck assembly.

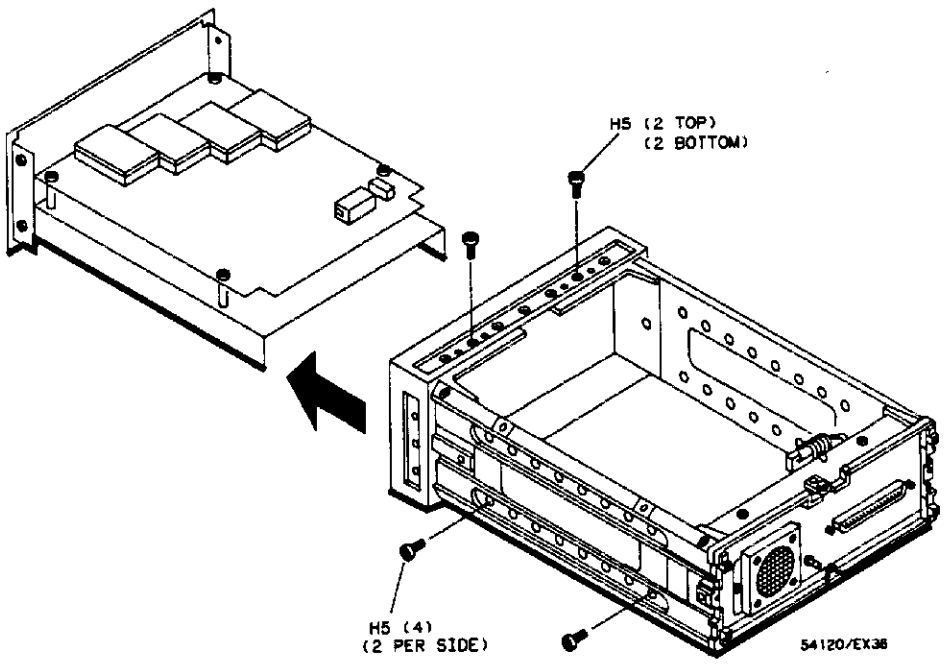


Figure 6A-13. Main Deck Assembly Removal.

6A-25. VERTICAL ASSEMBLY

REMOVAL

1. Disconnect power cable.
2. Remove main deck assembly. Refer to paragraph 6A-24.
3. Remove six screws holding vertical assembly to main deck. Refer to figure 6A-14.
4. Disconnect interconnect cable connected to J2 on vertical assembly.
5. Slowly pull vertical assembly straight up, while gently rocking assembly from side to side, until assembly is free of main deck. The rocking motion will help free the assembly from the sampler pins.

CAUTION

The exposed sampler pins are very sensitive to electrostatic damage (ESD).

REPLACEMENT

1. Reverse removal procedure to install main deck assembly. Be very careful not to bend any of the sampler hybrid pins when pushing the vertical assembly onto the main deck.

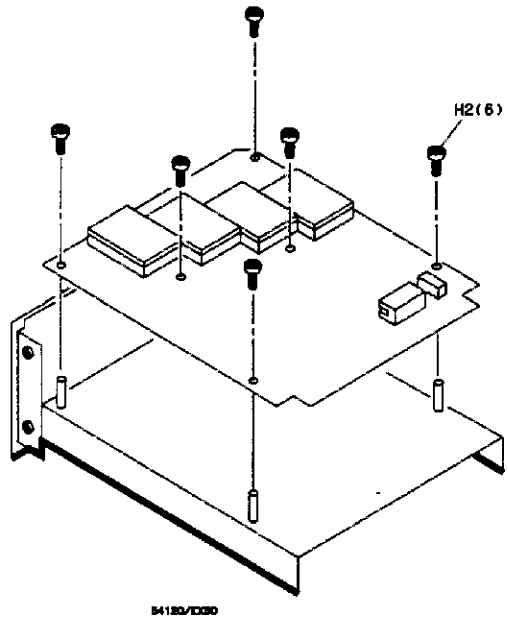


Figure 6A-14. Vertical Assembly Removal.

6A-26. SAMPLER, TDR, PULSE FILTER ASSEMBLY REMOVAL

SAMPLER AND PULSE FILTER REMOVAL

1. Disconnect power cable.

2. Remove main deck assembly and vertical assembly. Refer to paragraphs 6A-24 and 6A-25.

CAUTION

The exposed sampler, pulse filter, and TDR pins are very sensitive to electrostatic damage (ESD). All maintenance should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

3. Use a 5/16" open end wrench to unscrew rigid cables from assembly. **DO NOT** disconnect the semi-rigid cables from the assembly yet. The semi-rigid cables should not be stressed or bent.

4. Loosen screws holding assembly to main deck. The semi-rigid cables can now be slipped out of the assembly.

SAMPLER AND PULSE FILTER REPLACEMENT

1. Attach replacement assembly to main deck with screws but **DO NOT** tighten screws.

2. Install semi-rigid cable into assembly. When pushing semi-rigid cables into connectors, a definite slight snap sound will be heard as the cable and connector are seated together.

3. Tighten assembly screws.

4. Torque semi-rigid cables to 5 in/lbs.

5 Reverse remainder of assembly removal to complete installation of the assembly.

TDR (STEP GENERATOR) REMOVAL

1. Remove channel 1's sampler. Refer to sampler removal procedure above.

2. Remove delay line from TDR (step generator) with a 5/16 inch open end wrench. The horizontal assembly may be removed if you require additional room for the wrench. To remove the horizontal assembly refer to paragraph 6A-28.

3. Disconnect TDR levels cable (W14) from TDR.

4. Loosen connection between the TDR and the front panel bulk head connector with a 5/16 inch open end wrench.

5. Remove two screws holding the TDR to main deck.

6. Gently pull TDR from the bulkhead connector and lift the TDR from the main deck.

TDR REPLACEMENT

1. Install TDR into bulkhead connector and loosely connect to TDR.
2. Install two screws which hold TDR to main deck, **DO NOT TIGHTEN SCREWS.**
3. Reconnect TDR levels cable to TDR and loosely connect TDR delay line to TDR.
4. Reinstall channel 1's sampler. Refer to sampler replacement procedure above.
5. Tighten screws which hold TDR to main deck.
6. Tighten bulkhead and delay line SMA connectors to 5 in/lbs.

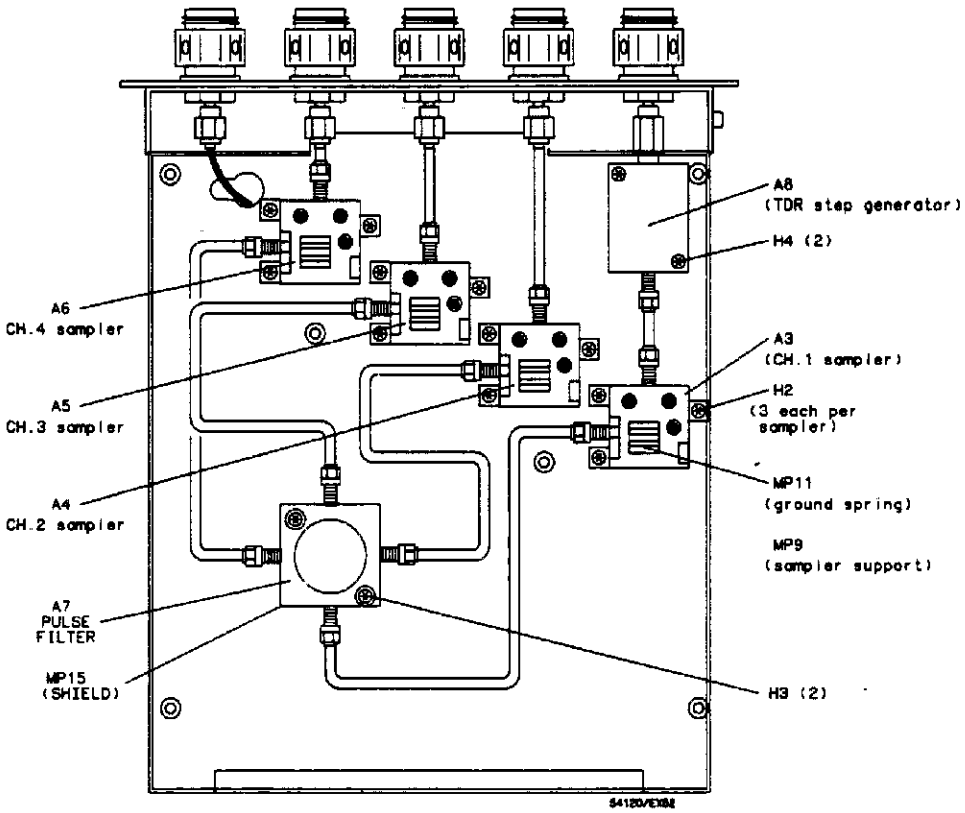


Figure 6A-15. Assembly Locations.

6A-27. TRIGGER HYBRID REMOVAL

REMOVAL

CAUTION

The exposed hybrid pins are very sensitive to electrostatic damage (ESD). All maintenance should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

1. Disconnect power cable.
2. Remove bottom cover.
3. Use a 5/16" wrench to disconnect SMA connector from trigger hybrid.
4. Remove two screws and two springs which hold trigger hybrid in place.
5. Gently lift trigger hybrid from horizontal assembly. Refer to figure 6A-16. There will be some resistance from the socket holding the trigger hybrid in place. Gently rocking the trigger hybrid while lifting may help in removal. There is a large heat sink on the bottom side of the trigger hybrid.

REPLACEMENT

1. Reverse removal procedure to install trigger hybrid. Torque the SMA connector to 5 in/lbs.

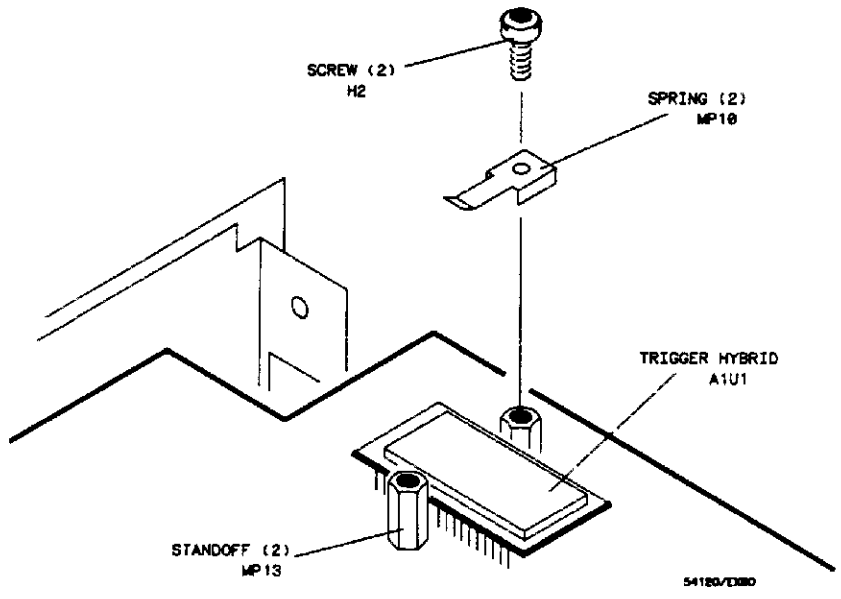


Figure 6A-16. Trigger Hybrid Removal.

6A-28. HORIZONTAL ASSEMBLY

REMOVAL

1. Disconnect power cable.
2. Remove main deck assembly. Refer to paragraph 6A-25.
3. Remove trigger hybrid. Refer to paragraph 6A-27. The replacement horizontal assembly **WILL NOT** be shipped with a trigger hybrid.
4. Remove five screws and two standoffs which hold the horizontal assembly to the main deck. Refer to figure 6A-17.
5. Disconnect interconnect cable connected to J9 on the horizontal assembly.
6. Disconnect temperature cable connected to J2 on the horizontal assembly.
7. Use a 5/16" wrench to disconnect TDR delay line cable from SMA connector J4 on horizontal assembly.
8. Disconnect TDR levels cable from J8 on the horizontal assembly.
9. Slowly pull horizontal assembly straight up until free of main deck.

REPLACEMENT

1. If the horizontal assembly is returned as an exchange assembly, the trigger hybrid must be removed from the horizontal assembly. The replacement horizontal assembly will be shipped without a trigger hybrid. Refer to paragraph 6A-27 for trigger hybrid removal procedure.
2. Reverse removal procedure to install horizontal assembly. The SMA connectors are torqued to 5 in/lbs.

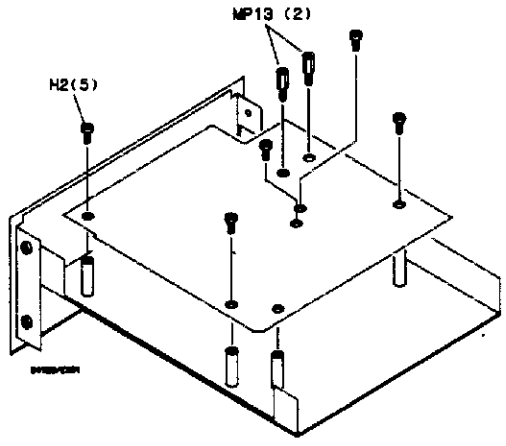


Figure 6A-17. Horizontal Assembly Removal.

6A-29. TEMPERATURE SENSE THERMISTOR

THERMISTOR REMOVAL

1. Disconnect power cable.
2. Remove main deck assembly. Refer to paragraph 6A-24
3. Remove horizontal assembly. Refer to paragraph 6A-28.
4. Disconnect thermistor from main deck. Refer to figure 6A-18.

REPLACEMENT

1. Apply a small amount of thermal compound to the thermistor.
2. Reverse removal procedure to install thermistor. All SMA connectors are torqued to 5 in/lbs.

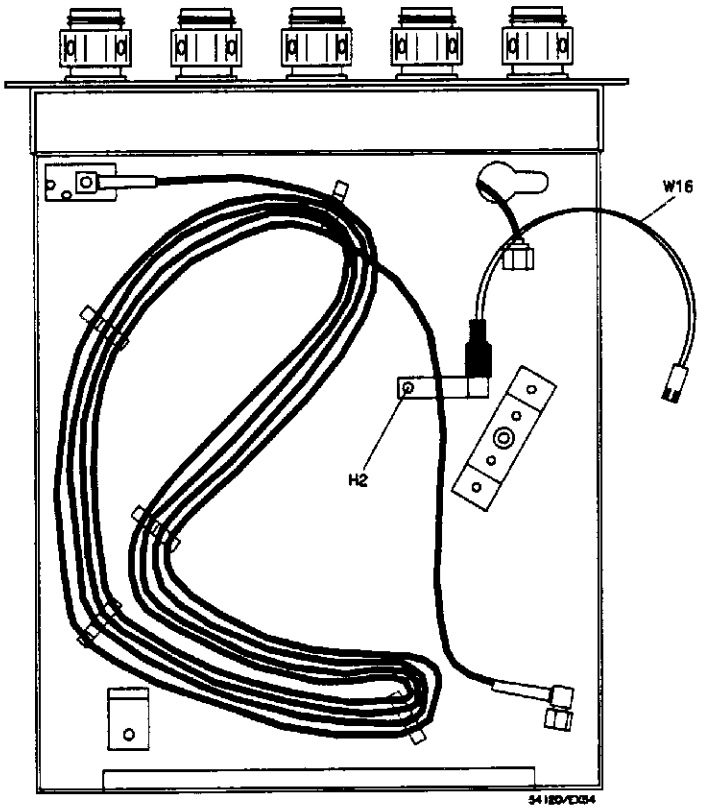


Figure 6A-18. Temperature Sense Thermistor.

6A-30. TDR DELAY LINE

DELAY LINE REMOVAL

1. Disconnect power cable.
2. Remove main deck assembly. Refer to paragraph 6A-24.
3. Remove horizontal assembly. Refer to paragraph 6A-28.
4. Use a 5/16" wrench to disconnect TDR delay line connected to TDR on main deck. Refer to figure 6A-19.
5. Unwind TDR delay line while paying attention to how delay line was wound. It will be rewound in the same fashion.

REPLACEMENT

1. Reverse removal procedure to install TDR delay line. All SMA connectors are torqued to 5 in/lbs.

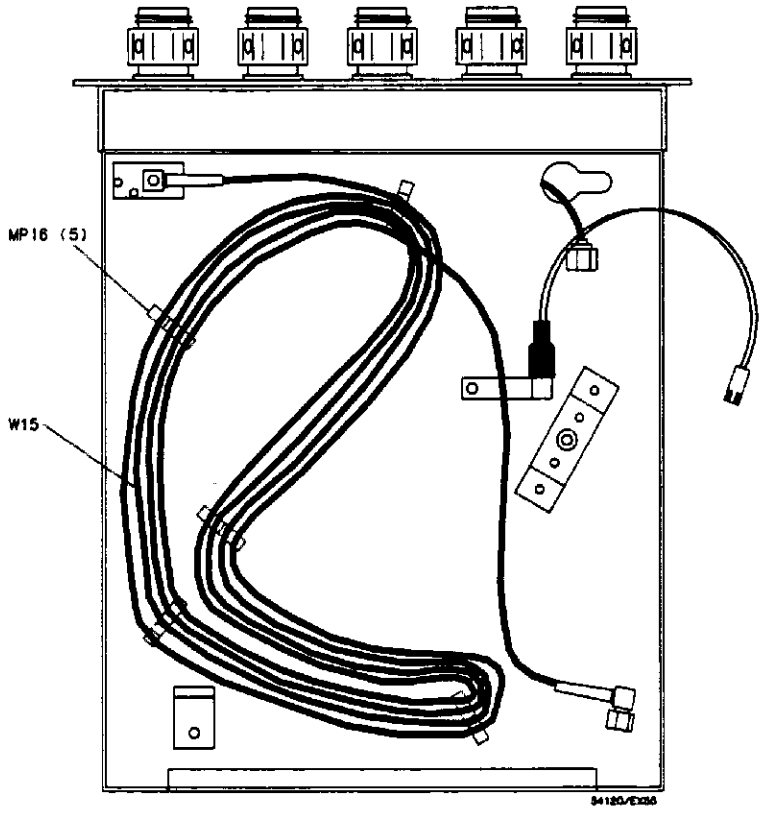


Figure 6A-19. TDR Delay Line.

6A-31. APC 3.5 CENTER CONDUCTOR REPLACEMENT

REMOVAL

CAUTION

The APC 3.5 center conductor assembly connect directly to either a sampler or trigger hybrid input. These inputs are very sensitive to electrostatic damage (ESD). All maintenance should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

1. Use antistatic mat with wrist strap to avoid damage to the gallium arsenide samplers, pulse filter, or TDR assemblies.
2. Use a thin 9/16 inch open end wrench (HP part number 8710-1770) to turn brass nut between APC 3.5 connector and front panel counter-clockwise. Refer to figure 6A-20.
3. Remove front portion of APC 3.5 connector from front panel.
4. Remove center conductor assembly from front panel.

REPLACEMENT

1. Place center conductor assembly into APC 3.5 connector.
2. Thread APC 3.5 connector onto front panel and tighten with a 9/16" wrench.

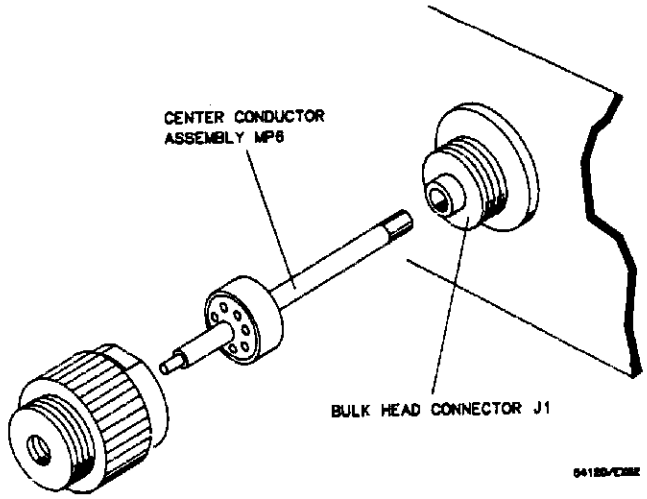


Figure 6A-20. APC 3.5 Center Conductor Removal.

6A-32. APC 3.5 CONNECTOR REMOVAL

REMOVAL

CAUTION

The APC 3.5 center conductor assemblies connect directly to the sampler and trigger hybrid inputs. These inputs are very sensitive to electrostatic damage (ESD). All maintenance should be performed while using an antistatic mat and wrist strap which are supplied with the instrument.

1. Use antistatic mat with wrist strap to avoid damage to the gallium arsenide samplers, pulse filter, TDR, and trigger hybrid.
2. Disconnect power cable.
3. Remove main deck assembly. Refer to paragraph 6A-24.
4. Remove vertical assembly from main deck. Refer to paragraph 6A-25.
5. Use a 5/16" open end wrench to unscrew semi-rigid cable from defective APC 3.5 connector. Refer to figure 6A-21.
6. Use a 9/16" open end wrench to unscrew damaged APC 3.5 connector.
7. Remove APC 3.5 connector from front panel.

REPLACEMENT

1. Reverse removal procedure to install APC 3.5 connectors. When pushing semi-rigid cables into connectors, a definite slight snap sound will be heard as the cable and connector are seated together. The semi-rigid cables are torqued to 5 in/lbs.

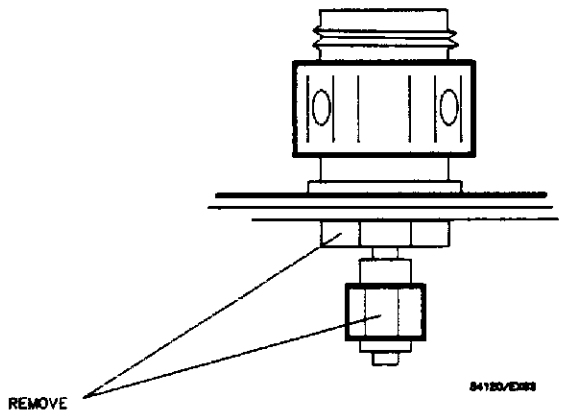


Figure 6A-21. APC 3.5 Connector Removal

6A-33. FRONT PANEL

REMOVAL

1. Disconnect power cable.
2. Remove main deck assembly. Refer to paragraph 6A-24.
3. Remove vertical assembly from main deck. Refer to paragraph 6A-25.
4. Remove all five APC 3.5 connectors. Refer to paragraph 6A-32.
5. Remove two screws from each side of front panel. Refer to figure 6A-22.

REPLACEMENT

1. Reverse removal procedure to install front panel.

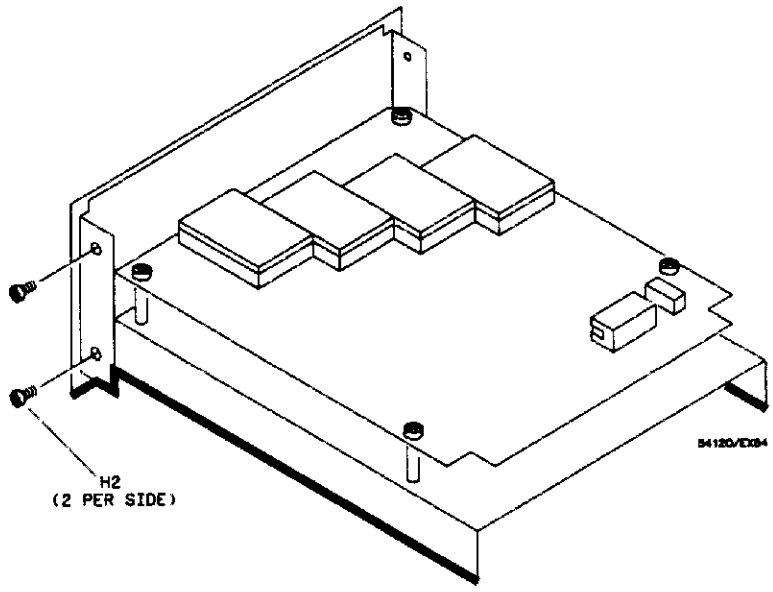


Figure 6A-22. Front Panel Removal.

TABLE OF CONTENTS

THEORY OF OPERATION

SECTION 6B

THEORY

6B-1. INTRODUCTION

This section is the theory of operation for the HP 54120A Mainframe and HP 54121A Four Channel Test Set. It includes overall system block diagrams and system theory of operation, printed circuit assembly (PCA) block diagrams and PCA block level theory of operation. Table 6B-1 is a listing of all the assemblies in the mainframe and the four channel test set.

6B-2. SYSTEM THEORY

This theory of operation refers to the System Block Diagram, figure 6B-1. It includes the mainframe and four channel test set, and is presented in block diagram format with a brief description of each block's basic functions. The theory's purpose is to help give a basic understanding of the instrument's overall operation as an aid in troubleshooting to the board level.

Table 6B-1. List of Assemblies for HP 54120T.

HP 54120A Mainframe		
A1	I/O	54111-66506
A2	Microprocessor	54111-66510
A3	Horizontal Control	54120-66501
A4	ADC	54120-66502
A5	Mother Board	54110-66511
A6	Display	54110-66512
A7	CRT Control Board	54100-66505
A8	Function Keyboard	54110-66502
A9	Menu Keyboard	54100-66520
A10	Control Keyboard	54100-66505
A11	Primary Supply	54110-66513
A12	Digital Supply	54110-66506
A13	Analog Supply	54110-66510
A14	Color CRT Module	2090-0092
A15	RPG Assembly	01980-61602
HP 54121A Four Channel Test Set		
A1	Horizontal Assembly	54120-66505
A2	Vertical Assembly	54120-66504

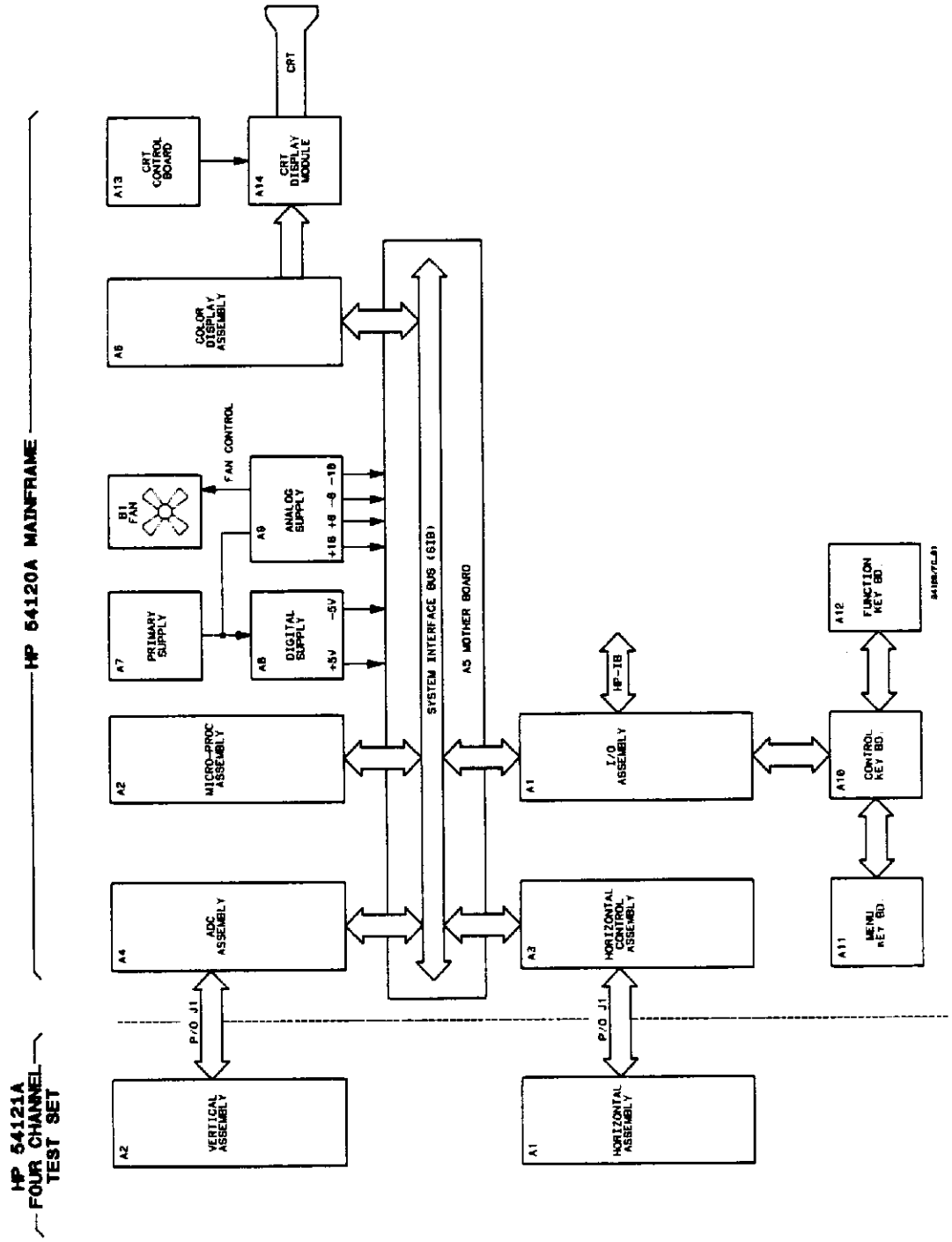


Figure 6B-1. System Block Diagram.

Motherboard (A5)

Each of the four card cage boards (A1 through A4) plug into the motherboard (A5). The 9 motherboard connectors each have a hard-wired identification code (0 through 8). Each plug-in board has a built-in identification code. Therefore, any board can be placed in any motherboard connector and the microprocessor (CPU) can identify what type of board is in each slot. This information can be displayed on the HP 54120A CRT by pressing ***Utility*** menu, then ***Test*** menu, then ***Display Configuration***. Note that the microprocessor's position is displayed as an empty slot. The factory configuration is the preferred board locations. For troubleshooting purposes, any board may be temporarily placed in any location. However, some cables may be too short to reach all motherboard locations.

Power Supplies (A11-13)

There are three power supply boards within the HP 54120A mainframe system. The primary power supply (A11) receives its input from the power line on the rear panel. The rear panel contains an EMI circuit and the main circuit breaker. The primary power supply board contains voltage regulation to output 300 volts used by the analog supply (A13) and digital supply (A12), and 120 volts used by the color CRT module A14. The analog power supply board regulates the 300 volt input, and supplies ±18 volts and ±8 volts for the instrument's analog circuits. The digital power supply board regulates the 300 volts to supply ±5 volts for the instrument's digital circuits. Both of these power supplies have their own ground systems which are isolated from each other. Therefore, voltage measurements must be made to the proper common points.

Front Panel Interface

The front panel contains system control keys, softkeys, a keypad, and a knob. All these devices are on or wired through the control keyboard (A10).

All information from the control keyboard is input to the I/O board through a large ribbon cable connected near the front of the I/O board. The keypad and softkeys are set up in a matrix so that the I/O board can scan the lines of keys by outputting a pulse on each line. If a key is closed (pressed), the I/O board will detect the return of the pulse on a line. By knowing which line the pulse was output on and which line the pulse was returned on, the I/O board can determine which key is closed. These key scan lines are passed through the large ribbon cable from the I/O board.

Display System (A14)

The color CRT module receives horizontal and vertical sync pulses, and character and graphics data from the color display assembly (A6). These signals are connected to the color CRT module through a ribbon cable from the side of the color display assembly. The color CRT module creates the sweep signals, blanking, and voltages required to display information on the CRT.

HP-IB System

The HP-IB connector on the rear panel of the instrument is connected by a ribbon cable to the top rear of the I/O board. The I/O board contains an HP-IB interface integrated circuit to convert data to proper HP-IB format.

System Interface Bus

All digital data is moved between the HP 54120A mainframe boards over the system interface bus (SIB). The SIB has data, address, and control lines. The SIB data, address, and control signals are under the CPU's control. Many of the boards have a local data bus (LDB) which is under the board's own control. The SIB and the local data buses must not be confused. In most cases data and addresses are accepted by a board from the SIB under CPU control, then the data is manipulated by that board on its local data bus.

Microprocessor Board (A2)

The microprocessor board has a 68000 microprocessor, 384k bytes of ROM, 32k bytes of non-volatile RAM (battery back-up), programmable timer, and bus request/bus grant circuits. The board has an internal data bus, so it can process data without tying up the System Interface Bus. Data is moved on the SIB under control of the 68000 microprocessor. The board also has logic circuits so it can operate with another microprocessor on the SIB, in which case the bus request/bus grant circuits would be used. In the HP 54120A only one microprocessor is used, therefore the bus request/bus grant signals are tied to the proper logic levels so the 68000 microprocessor will have control of the SIB when required.

Display Board (A6)

The display board has 128k bytes of dynamic RAM (DRAM) used as the dot memory to store signal data to be displayed. It also has a character generator and character refresh circuits for the characters that will be displayed. The board produces vertical and horizontal sync signals so signal and character data are displayed on the CRT at the proper place and time.

I/O Board (A1)

The I/O board has interface circuits to read the front panel devices, including softkeys, RPG knob, system control keys, and keypad. The board also has HP-IB interface logic, clock circuit which produces the required microprocessor clocks, power on reset circuit which resets the microprocessor, additional CPU dynamic RAM memory, other logic which starts up the CPU to a known condition, and a battery which powers the non-volatile RAM on the CPU board.

Horizontal Control Assembly (A3)

A user inputs various timebase and trigger selections to the HP 54120A. The CPU communicates these selections and acquisition control signals to the horizontal control assembly over the SIB. The horizontal control assembly translates these CPU instructions into various trigger and timebase signals for the horizontal and vertical assemblies located in the four channel test set. These signals control the sampling and data acquisition process. An acquisition cycle is defined as the sequence of events that must occur in order to acquire a SINGLE data point per enabled channel. It will normally be the case that several acquisition cycles will be required to adequately display a waveform.

Horizontal Assembly (A1)

The horizontal assembly has the trigger and timebase hybrids. After a trigger occurs and delay has reached terminal count, the horizontal assembly enables the sample pulse generator. The sample pulse generator momentarily turns the samplers on.

Vertical Assembly (A2)

The vertical assembly momentarily samples incoming signals during a very narrow time window, 17 ps. It then amplifies and converts the sample to a bipolar pulse. A bipolar pulse is easier for the ADC assembly's track and hold circuitry to follow the pulse's peak amplitude. A bipolar pulse is shown in figure 6B-3.

ADC Assembly (A4)

The ADC assembly has track and hold circuitry which tracks the bipolar pulse's amplitude and holds the peak value. It also contains an analog to digital converter which converts incoming analog signals into a digital word. This digital word is read by the CPU and is either displayed on the CRT or used in waveform math functions.

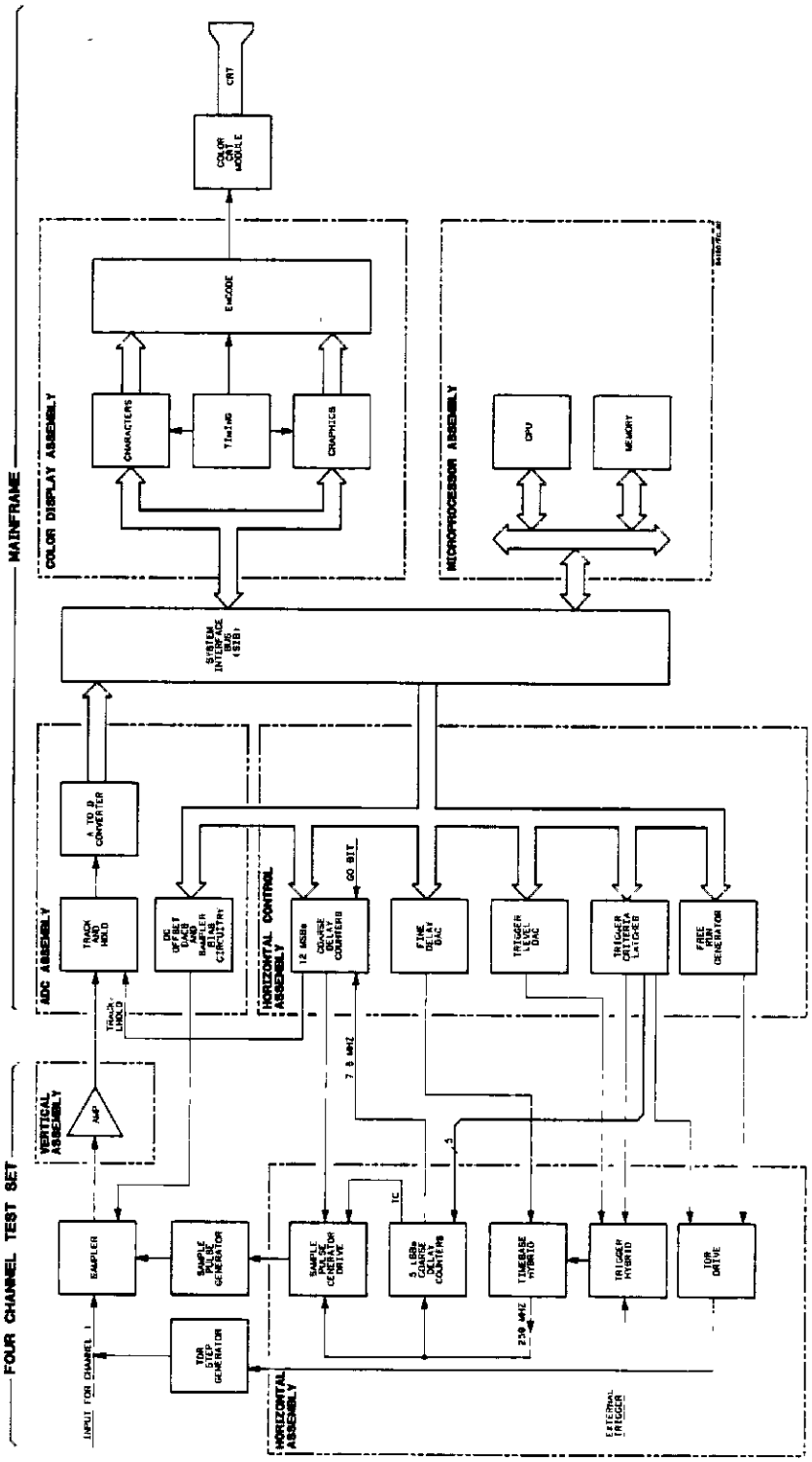


Figure 6B-2. Simplified Signal Flow Diagram

6B-3. SIMPLIFIED SIGNAL FLOW

The following theory refers to figure 6B-2 Simplified Signal Flow Diagram and tracks a signal through the entire HP 54120T. The signal flow only refers to channel 1 and the external trigger path. Channels 1-4 operate identically except channel 1 has the TDR hybrid in its input signal path. The TDR is discussed at the end of the simplified signal flow theory.

An acquisition cycle is defined as the sequence of events that must occur in order to acquire a SINGLE data point per enabled channel. It will normally be the case that several acquisition cycles will be required to adequately display a waveform.

The microprocessor (CPU) starts an acquisition cycle by programming the fine delay DAC and the coarse delay counters. The CPU then enables the trigger hybrid. The next external trigger edge which meets the criteria set by the trigger criteria latches will cause the trigger hybrid to output an edge. This edge enables the timebase hybrid to start the fine delay ramp. The fine delay DAC signal sets the starting point for the fine delay ramp. This fine delay ramp represents fine delay, which has a range from 0 to 3.99975 ns. When the fine delay ramp reaches 0 volts, the 250 MHz startable oscillator starts running. The sample pulse generator drive is enabled when all the coarse delay counters reach terminal count. The 250 MHz signal clocks the coarse delay counters on the horizontal assembly. These counters continue recounting to zero which results in the output line toggling at a 7.8 MHz rate. The 7.8 MHz clocks the remainder of the coarse delay counters on the horizontal control assembly. When these counters reach terminal count, they output a signal called terminal count back to the horizontal assembly. This is one of the enable signals for the sample pulse generator drive circuit. The coarse delay counters on the horizontal assembly continue to count until they reach terminal count also.

This terminal count is the last enable for the sample pulse generator drive circuit. With all the coarse delay counters at terminal count, one pulse of the 250 MHz is allowed through the sample pulse generator drive circuit. This circuit places 1 A of current for 1 ns into the sample pulse generator. This causes the sample pulse generator to momentarily turn on the sampler hybrids.

The sampler measures the difference between the input signal's present amplitude and the DC offset DAC's level. The difference is amplified and converted to a bipolar pulse. A bipolar pulse is shown in figure 6B-3. It is important to remember that only one data point is digitized for each enabled channel during each acquisition cycle. The bipolar pulse on the vertical board represents only the sampled portion of the incoming signal during a very narrow time window of 17 ps.

The track and hold circuit follows the amplitude of the bipolar pulse. When the bipolar pulse reaches peak amplitude, the track and hold circuit holds the peak analog value. The A to D converter converts the track and hold's level to a 12-bit digital word.

The CPU reads the output of the A to D converter and either uses the digital word in waveform math functions or sends it to the color display assembly.

The display assembly sends the digitized input waveform to the graphics section of the display assembly. The graphics and any associated characters are sent to the CRT display module where they are displayed on the CRT. Another acquisition cycle will then be started.

The TDR generates a fast step pulse for TDR applications. When the TDR is disabled, incoming signals pass unaffected through the TDR, except channel 1's bandwidth is lowered slightly. When the TDR is enabled, it outputs a fast edge pulse which splits two ways. First, the TDR pulse is applied to channel 1's sampler input and is digitized as any other incoming signal. Second, the TDR pulse is an output from channel 1's APC 3.5 input connector.

An important point to remember is that external trigger is not used when the TDR is enabled. Circuitry on the horizontal assembly generates the trigger signal when trigger is enabled. If the external trigger signal is left connected it may cause false triggering.

Another important point about this system is that there is no provision for an internal sync pickoff in the samplers. Only an external trigger is used when incoming signals are to be digitized.

6B-4. ACQUISITION CYCLE

Introduction

The acquisition theory of operation is presented in a program flowchart. The theory applies directly to the infinite persistence mode, which is the simplest flowchart. Variable persistence and average modes have a few added steps to the flowchart. The microprocessor (CPU) controls an acquisition cycle with software instructions. The flowchart is presented from the CPU's point of view. The following steps are software instructions, with added indented comments. The comments will tie the software and hardware theories together.

Infinite Persistence Mode Acquisition Flow Chart.

Start:

Program timebase delay

Program A/D input control switches

The user selects which channels he wants on. The CPU will write to the proper switch enable lines 1-4 (SW1-4) which channels are on and which are off. There are four samplers on the vertical assembly and only one A to D converter on the ADC assembly. All four samplers fire at the same time and the track and hold circuitry will hold the analog values of each channel.

Logic on the ADC assembly will search the SW1-4 lines looking for which channels are on. The A to D converter will process, one at a time, only the on channels. The analog signals are converted to digital words which the CPU can display on the CRT. Data from the off channels is not used.

Wait for timebase to settle

The CPU is waiting for the fine delay DAC (U28) on the horizontal control assembly to settle. The wait time is 50 μs.

Go to Enter1

Loop:

Program A/D input control switches

As earlier, this step reprograms the SW1-4 switches on the ADC assembly.

Enter1:

Reset GO bit

This is the low go reset (LGORESET) on the horizontal control assembly.

Enable trigger, samplers on

This step enables various lines to latches U1 and U2 on the horizontal control assembly. The trigger enable line will go low. The sampler high on/low off line (ON/LOFF) will go high at the end of coarse delay. This allows the samplers to sample incoming signals.

Wait for GO bit

The horizontal control assembly uses the GO bit to signal the CPU to go and process sampled data. The CPU will wait on the GO bit signal before it does any other tasks. If the GO bit is held in a disabled mode, the CPU could hang up in a wait loop. Pressing any front-panel key will exit this wait loop.

Reset GO bit

After the CPU sees the GO bit go high, it resets the GO bit low so the GO bit can signal the CPU when the next sample is taken.

Skip sample

The longest coarse delay word represents 458.752 μs of delay. Longer delays are accomplished by using a software counter. Coarse delay will count down from 458.752 μs to zero. The trigger will fire, and a sample will be taken. Software will check to see if enough delay time has passed. If more delay is needed, then the sample is discarded and the coarse delay counters will start over again.

Disable Trigger

If the trigger is not disabled, then the timebase would continue to count down and enable the trigger every 458.752 μs. This would cause a new set of data points to be acquired by the samplers and the old set of data points would be discarded. By disabling the trigger on the horizontal control assembly, the timebase will be stopped and data points will not be discarded before the CPU has time to process them.

Read A/D

The CPU will read the output of the A to D converter for the first channel that is on. Then the A to D converter will process the signal from the next channel that is on. The Track and Hold ICs have a capacitor which holds the sampled data value. The acquisition cycle is interrupt driven with the acquisition interrupt (GO bit) having the highest priority.

Program timebase delay for next acquisition

This is a repeat of the timebase set-up in the Start routine discussed earlier. While the CPU is processing sampled data it allows enough time for the fine delay DAC to settle within the 50 μs time frame.

If channel 1 is on, then

Wait for A to D to finish a conversion.

The CPU is monitoring the status line (STS) from the ADC assembly. Status tells the CPU that an A to D conversion is finished, and it is time to read the A to D's digital output word.

Read A to D converter.

After the CPU reads the A to D converter's output, the low chip select analog to digital converter (LCSAD) will signal the A to D to do a conversion on the next channel which is on.

Plot data if appropriate.

The CPU does not always plot digitized data. It depends on what functions the user selected. The data may be used in waveform math and only the results would be plotted on the CRT. Data may also be acquired specifically to be sent over the HP-IB.

If channel 2 is on, then

The steps for channels 2-4 are identical to the steps for channel 1.

Wait for A to D to finish a conversion.
Read A to D converter.
Plot data if appropriate.

If channel 3 is on, then

Wait for A to D to finish a conversion.
Read A to D converter.
Plot data if appropriate.

If channel 4 is on, then

Wait for A to D to finish a conversion.
Read A to D converter.
Plot data if appropriate.

If the trace is at the end of a sweep, then

Plot any functions which are on. It takes the CPU a long time to finish plotting functions. The acquisition hardware may have a block of dead time waiting for the CPU to finish plotting functions.

Go to Loop

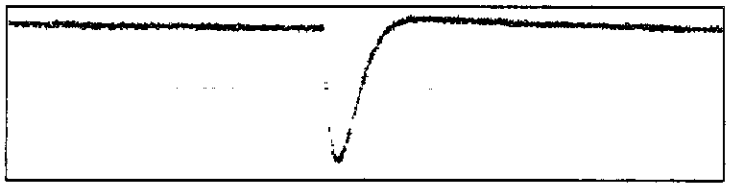
Variable Persistence

For variable persistence mode there is an added step before the "GO to loop" step. This step checks if it is time to erase any of the old data points. The CPU may spend as much time erasing old data points as acquiring new data points.

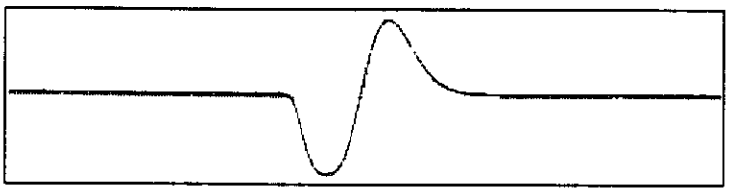
Average Mode

In the average mode software feedthrough compensation is done. With the samplers turned off, the output of the samplers is digitized through the A to D converters. This first value is the result of sampler feedthrough. Then the samplers are turned on and their outputs are digitized again. This second value is the sum of sampler feedthrough and an actual data point. The first value is subtracted from the second, and the result is the actual digitized point.

Monopolar Pulse



Bipolar Pulse



Tailpulse

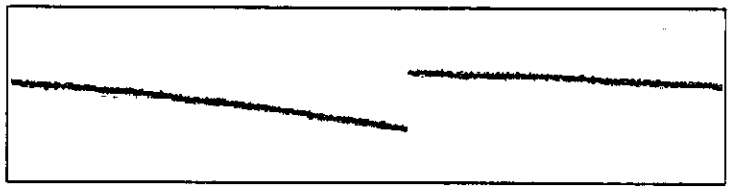


Figure 6B-3. Vertical Assembly Pulse Shapes

6B-5. VERTICAL ASSEMBLY

Introduction

The following block level theory of operation refers to the vertical assembly block diagram in figure 6B-4.

TDR

The time domain reflectometry (TDR) step generator is a thru-line current switching circuit. It is used to create a fast step for TDR applications.

Sampler

A pulse from the sample pulse generator momentarily turns the sampler diodes on. The sampler measures the difference between an input signal and dc offset at a specific point in time (approximately 17 ps window) and converts this difference to a differential charge on both IF outputs.

Sampler Bias Network

This circuitry combines the offset, bias and temperature compensation inputs to produce the proper voltages to bias the sampler IF pins. H/LL selects either the high or low bandwidth bias modes.

Feedthrough Compensation Network

When the sampler is turned off, there will be passive feedthrough of the input signal through the sampler by parasitic capacitive and resistive coupling. The circuit corrects for this passive feedthrough of the sampler diodes to a bandwidth greater than the matched filter's bandwidth.

Charge Sensitive Amps

The charge sensitive amps measure the differential charge on the IF outputs and converts this to differential tail pulses with time constants of approximately 100 μs. A tail pulse is shown in figure 6B-3.

Summation Amp

The summation amp combines the differential tail pulses from the charge sensitive amps into a single-ended tail pulse. It also subtracts effects of changes in dc offset signal on the charge sensitive amps.

Amp and Matched Filter

The matched filter converts and amplifies the tail pulse from the summation amp and converts the tail pulse to a bipolar pulse which drives the track and hold circuitry on the ADC assembly. A bipolar pulse is illustrated in figure 6B-3.

Table 6B-2. Vertical Assembly Mnemonics.

MNEMONICS	DEFINITION
CC1	Capacitive Compensation for channel 1
HB1	High Bandwidth adjust for channel 1
LL/H	Low enables Low bandwidth bias adjust and a High enables High bandwidth bias adjust
LB1	Low Bandwidth bias adjust for channel 1
OG1	Offset Gain adjust for channel 1
RC1	Resistive Compensation for channel 1
VHB	High Bandwidth bias enable
VLB	Low Bandwidth bias enable
V Temp	Temperature compensation voltage from horizontal assembly
10.000 V	Precise 10 volts from horizontal assembly

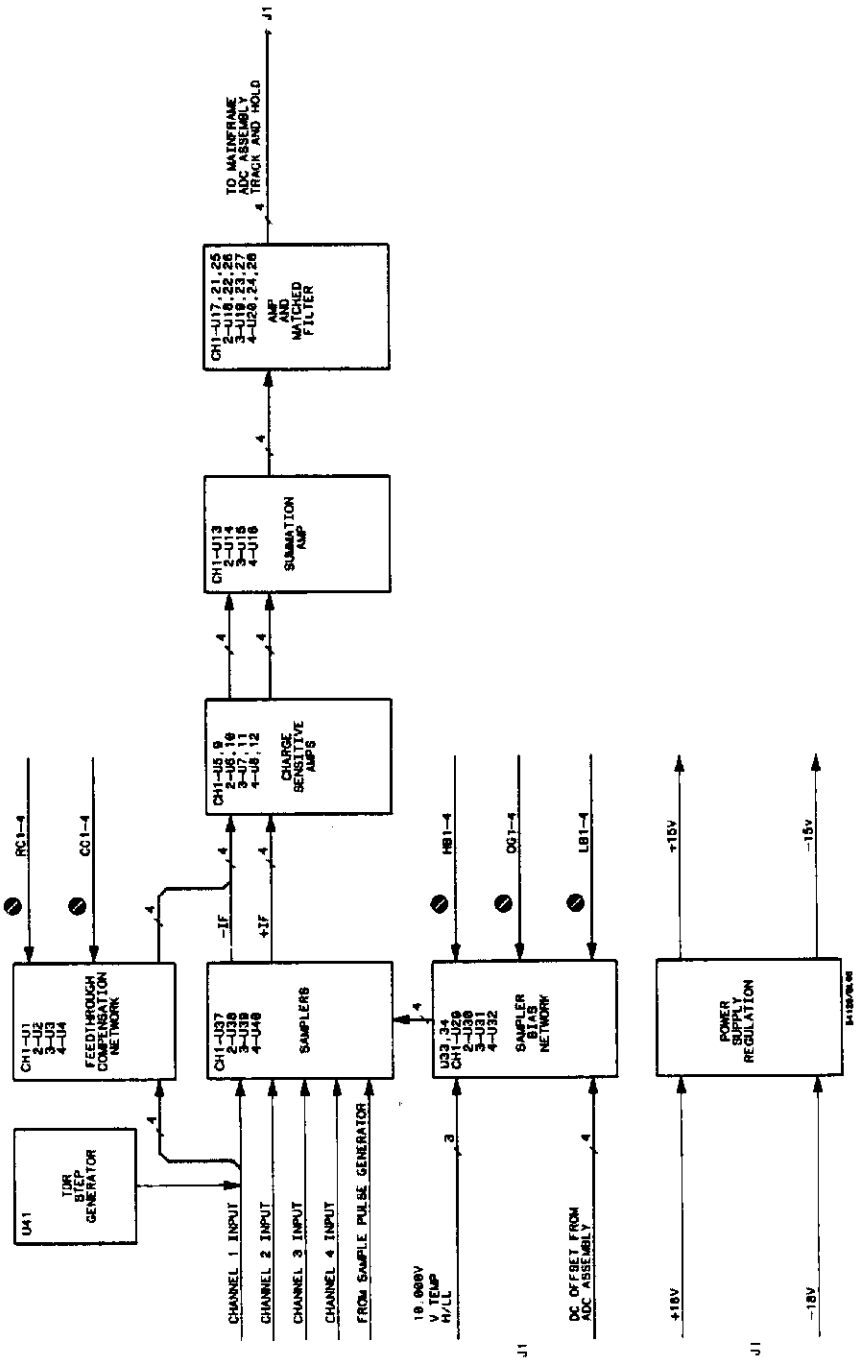


Figure 6B-4. Vertical Assembly Block Diagram.

6B-6. ADC ASSEMBLY

Introduction

The following block level theory of operation refers to the analog to digital converter (ADC) assembly block diagram in figure 6B-5.

Track and Hold

The track and low hold (T/LH) signal from the horizontal control assembly enables the track and hold circuitry to detect the first half cycle of the bipolar pulse's amplitude and hold its peak analog value.

Analog Switch Enable

The microprocessor (CPU) enables one or more of the four vertical channels by enabling the proper SW1-4 lines. The combinational logic circuit searches for which channels are on by looking at which of the SW1-4 lines were enabled by the CPU.

Combinational Logic

When enabled by T/LH, the combinational logic circuit searches for the first channel that is on. After the first channel on is found, the combinational logic circuit enables the A to D to convert that channel's track and hold output to a 12-bit digital word. After the A to D conversion is finished, the CPU reads the A to D's output. The combinational logic circuit then continues to search for the next channel on. This process continues until reset by the T/LH signal, at which time the sequence is started over again.

Analog Switch

The analog switch sends the track and hold outputs, one at a time as directed by the combinational logic circuit, to the 12-bit analog to digital converter (A to D).

A to D

The A to D converts analog signals to a 12 bit digital word. This digital word is sent through bidirectional bus drivers U37 and U38. The CPU transfers these digital words over the system interface bus (SIB) to the display assembly.

Status

The CPU waits until status indicates that the A to D is done with a conversion before reading the A to D's digital lines.

Board ID

The CPU knows the location of each card cage assembly by asking each board for its unique ID number during the initial power-up sequence. Each assembly accessed by the CPU over the SIB has a unique board ID number.

Offset DAC Enable

The offset DAC (digital to analog converter) enable decodes address lines A4-6 into four lines called low chip select offset DAC lines 1-4 (LCSOD1-4). The CPU accesses each offset DAC by enabling one of these four lines.

Offset DACs

There is an offset DAC for each of the four channels. The offset DAC converts 14-bit digital (DAD0-13) words to an analog voltage. The analog voltage is then converted to a current with a range of ±50 mA. Current drive is used to help reduce cable noise pickup while the offset current is sent through the umbilical cable to the vertical assembly.

Slot Decode

The CPU accesses this board by sending out the board's slot ID code over address lines A19-22. U36 is a four bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When the two codes are equal, U36 pin 6 enables other circuitry.

D Latch

The D Latch signals the CPU that it has received data with the LDTACK (low data acknowledge) line.

Table 6B-3. ADC Assembly Mnemonics

MNEMONICS	DEFINITION
A19-22	Address lines 19-22
CCLK1	C Clock 1
CCLK2	C Clock 2
LCSAD	Low Chip Select Analog to Digital converter
DAD0-13	Digital to Analog Data lines 0-13
D0-15	Data lines 0-15
DTRC	Delay To Read Convert
H/LL	High for high bandwidth enable, Low for low bandwidth enable
H/LT	Hold/Low Track
LCSOD1-4	Low Chip Select Offset DAC's 1-4
LD0-15	Local Data lines 0-15
LDTACK	Low Data Acknowledge
LNCH	Low Next Channel High
R/LC	Read/Low Convert
STS	Status
SW1-4	Analog Switch lines 1-4

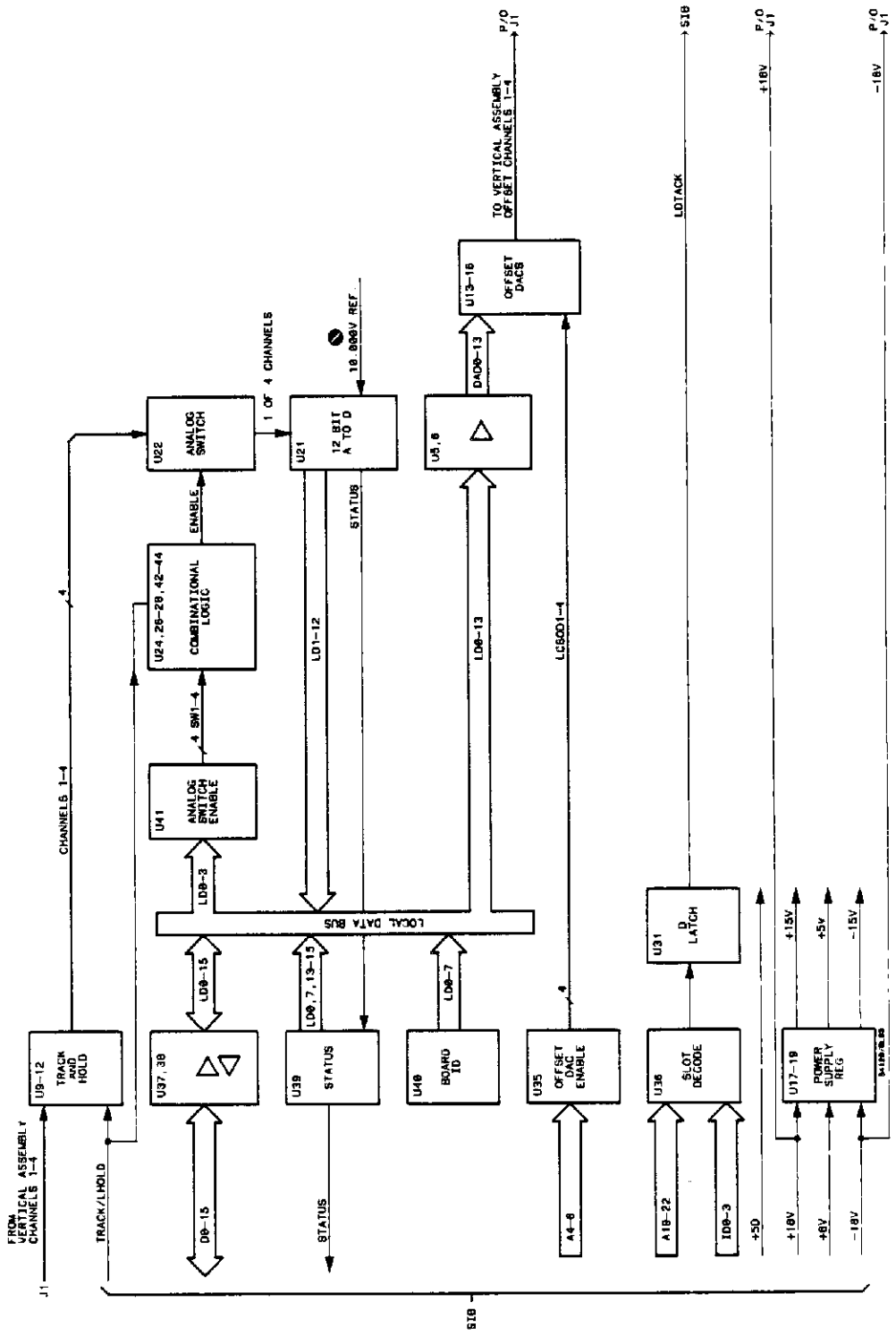


Figure 6B-5. ADC Assembly Block Diagram.

6B-7. HORIZONTAL CONTROL ASSEMBLY

Introduction

The following block level theory of operation refers to the horizontal control assembly block diagram in figure 6B-6.

Board ID

The microprocessor (CPU) knows the location of each card cage assembly by asking each board for its unique ID number during the initial power-up sequence. Each assembly accessed by the CPU over the SIB has a unique board ID number. The horizontal control assembly generates board ID by pull-up resistors on the LD0-3 data lines, which will be all logic high levels.

Slot Decode

The CPU accesses this board by sending out the board's slot ID code over address lines A19-22. U23 is a 4-bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When the two codes are equal, U23 pin 6 enables other circuitry.

D Latch

The D Latch signals the CPU it has received data with the low data acknowledge (LDTACK) line.

Coarse Delay Counters

U10, 12, and U13 use the 12 most significant bits (MSB) of the 17-bit coarse delay word (LD4-15). When the counters have counted down to zero, a low terminal count signal (LTC2) is generated for the horizontal assembly in the four channel test set. The remaining 5 bits of the coarse delay word are used on the horizontal board in the four channel test set. The total length of time for the coarse delay counters is 4 ns to 458.752 μs. Longer delay times are achieved with software counters.

Latches

U1 and U2 latch various trigger status signals to the horizontal assembly. These signals are: high frequency reject, trigger enable, TDR on or off, trigger hysteresis, and trigger slope. U11 latches four of the five LSBs of the coarse delay word going to the horizontal assembly. These are timebase bits 1-4 (TB1-4) and correspond to bits 0-3 of the coarse delay word.

4 ns Bit

The fifth LSB of the coarse delay word going to the horizontal assembly is a sub LSB of the coarse delay word. It is TB0 SET and RESET and corresponds to bit 15 of the fine delay word. It is called the 4 ns bit because it is the fourth ns of the coarse delay time interval.

Fine Delay DAC

U28 is a 12-bit DAC using LD2-13 to produce a level representing fine delay from 0 to 3.99975 ns. U31 uses LD0 and 1 as sub LSBs to give the DAC more resolution, 1/4 ps steps. This gives the trace a more uniform appearance.

Trigger Level DAC

The trigger level DAC is a 12-bit DAC which generates trigger level as selected by the front-panel. Trigger level is used by the trigger hybrid on the horizontal assembly in the four channel test set.

Freerun Clock Generator

U30 divides a 2 MHz clock to give a frequency range of 15.3 Hz to 500 KHz, selectable by the front-panel controls. The freerun clock signal drives the TDR generator and trigger hybrid located in the four channel test set. The freerun clock frequency directly affects the output frequency of the TDR generator.

Go Bit Generator

Generates the GO bit which tells the CPU to process sampled data. When the GO bit is high, analog information is being held by the track and hold circuitry on the ADC assembly. This analog information is waiting to be converted into digital information by the A to D converter on the ADC assembly. When the GO bit goes true (low) it generates an interrupt which tells the CPU a sample has been taken (interrupt 7).

Track and Hold Generator

Generates the track and low hold signal for the ADC assembly. Track means to track the output of vertical assembly. Hold means to hold the peak analog value until the A to D converter has time to do a conversion.

Status

Status is the only block which transfers data back to the CPU. The GO bit tells the CPU to process sampled data on the ADC assembly.

Table 6B-4. Horizontal Control Assembly Mnemonics

MNEMONICS	DEFINITION
A19-22	Address lines 19-22
D0-15	Data lines 0-15
GO	Tells the CPU to go and process sampled data
H/LT	Hold/Low Track
HF REJECT	Trigger High Frequency Reject
ID0-3	Board ID lines 0-3
LD0-15	Local Data Lines 0-15
LLDS	Low Lower Data Strobe
LDTACK	Low Data Acknowledge
LGO	Low GO
LGORESET	Low GO Reset
LIRQ7	Low Interrupt Request Line 7
LPWRONRST	Low Power On Reset
LSB	Least Significant Bit
LTC2	Low Terminal Count line 2
MSB	Most Significant Bit
Neg/LPOS	Trigger slope select high for Negative/low for Positive
OFF/LON	Turns TDR generator Off and On
R/LW	Read/Low Write
SELECT	Board Select
LENABLE/RESET	Trigger Low Enable/Reset
T/LH	Track/Low Hold
Sampler ON/LOFF	Turns Sampler ON and Off
SIB	System Interface Bus

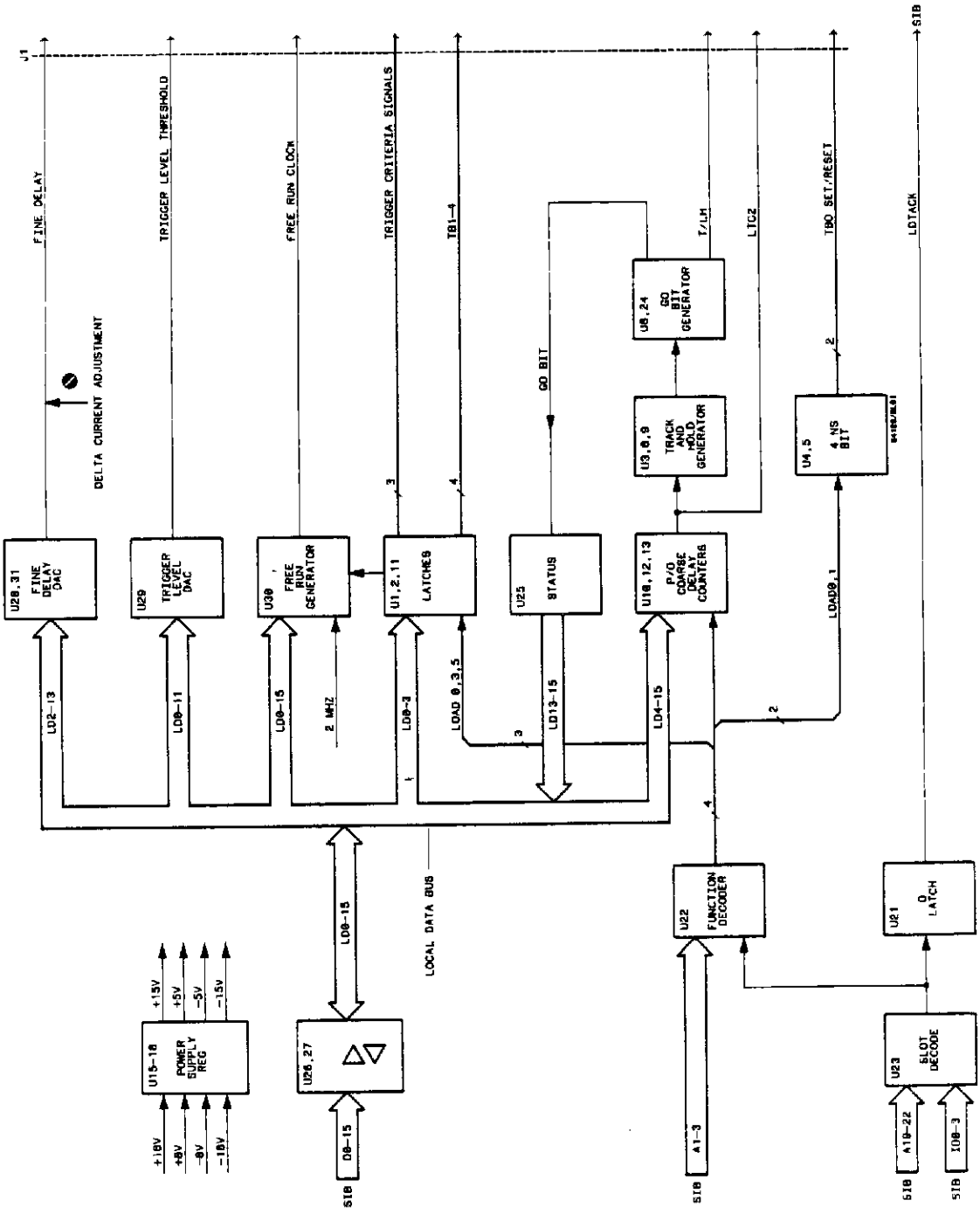


Figure 6B-6. Horizontal Control Assembly Block Diagram.

6B-8. HORIZONTAL ASSEMBLY

Introduction

The following block level theory of operation refers to the horizontal assembly block diagram in figure 6B-7.

Trigger Hybrid

When the TDR is disabled, the trigger enable line enables the trigger hybrid. The next external trigger edge which meets the criteria set up by the trigger criteria signals will cause the trigger hybrid to output an edge. The trigger criteria signals are: trigger slope select, high frequency reject, hysteresis on or off, and a separate signal called trigger level. Trigger level sets a threshold which the incoming trigger signal must cross for a trigger to occur. When the trigger hybrid triggers, it outputs an edge to the timebase hybrid.

Trigger Source for TDR Mode

When the TDR is enabled, external trigger pulses are inhibited from causing U1 to trigger. The CPU sets the trigger level high enough so that any incoming external trigger pulses would not be expected to cross the trigger level threshold. This keeps any external trigger pulses from causing the trigger hybrid to trigger. It is essential that when the TDR is enabled all external trigger sources be disconnected from the instrument, otherwise the instrument will not trigger properly and will appear inoperative. When the trigger enable line enables U2 and U3, the next positive edge of freerun clock will cause the trigger hybrid to trigger. The trigger hybrid will output an edge to the timebase hybrid.

TDR Drive

When the TDR OFF/LON line is low, U4 and Q2 allow the freerun clock signal to drive the TDR on and off at the freerun clock rate. The freerun clock rate is determined by the freerun rate selected in the front-panel timebase menu.

Timebase Hybrid

Fine delay sets the starting point for the fine delay ramp. This fine delay ramp represents a fine delay range from 0 to 3.99975 ns. When the timebase hybrid receives the trigger edge from the trigger hybrid, it starts the fine delay ramp. When the fine delay ramp reaches 0 volts, the 250 MHz startable oscillator inside the timebase hybrid will start running. The timebase hybrid outputs 250 MHz to the sample pulse generator drive circuitry and to the coarse delay counters on the horizontal board.

Coarse Delay Counters

The part of the coarse delay counters, which counts the 5 LSB's of the 17-bit coarse delay word is on the horizontal assembly. The 250 MHz signal from the timebase hybrid clocks these counters. Each time the 5 LSBs are counted and the counters roll over, the output of the counter's last stage toggles at a rate of 7.8 MHz (250 MHz divided by five counter stages is 7.8 MHz). The 7.8 MHz clocks the rest of the coarse delay counters which are on the horizontal control assembly. They count the 12 MSBs of the coarse delay word. Eventually the counters reach terminal count and pull the LTC2 line to a logic low level. The next time the 5 LSB counters reach terminal count, they pull their own terminal count line to a logic low level. With all the coarse delay counters momentarily reaching terminal count at the same time, the sample pulse drive circuitry will pass one cycle of the 250 MHz.

Sample Pulse Generator Drive

When all 17 bits of the coarse delay word have reached terminal count, the sample pulse generator drive circuitry will allow one pulse of the 250 MHz to pass. The sample pulse generator drive circuitry places 1 amp of current for 1 ns in the sample pulse generator. The sample pulse generator outputs a fast edge pulse (rise time of about 50 ps), which momentarily turns on all four samplers at the same time.

Table 6B-5. Horizontal Assembly Mnemonics

MNEMONICS	DEFINITION
HF REJECT	Trigger High Frequency Reject
LSB	Least Significant Bit
LTC2	Low Terminal Count line 2
MSB	Most Significant Bit
Slope Neg/LPOS	Trigger Slope Select Negative or Positive
SRD	Step Recovery Diode (part of sample pulse generator)
TB0 SET	Timebase Bit 0 Set (TB0-4 are the 5 LSB's of the)
TB0 RESET	Timebase Bit 0 Reset (17 bit coarse delay word)
TB LOAD	Timebase Bit Load
TB1-4	Timebase Bits 1-4
TDR OFF/LON	Turns TDR Generator Off and On
LENABLE/RESET	Trigger Low Enable/Reset

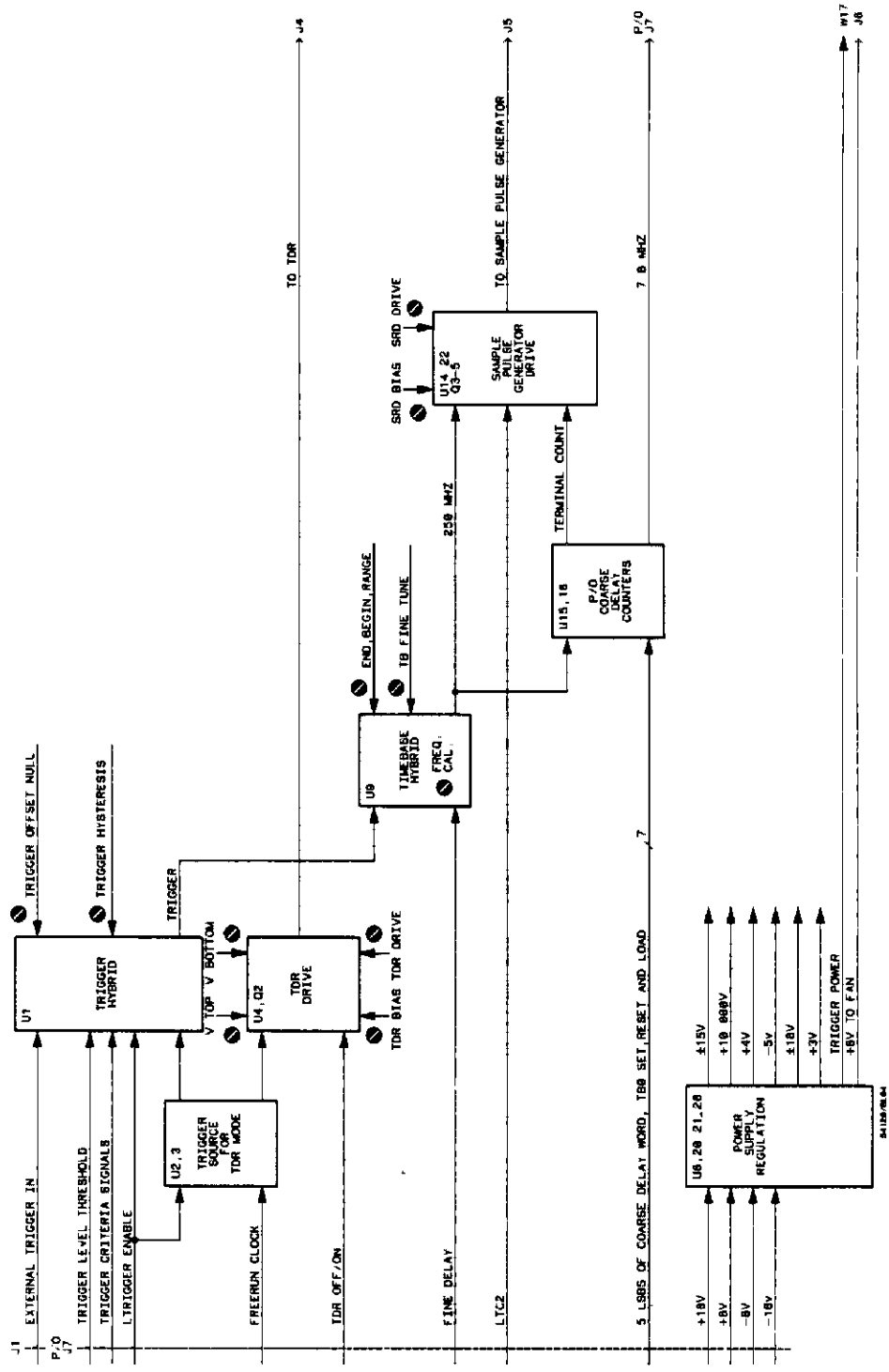


Figure 6B-7. Horizontal Assembly Block Diagram

6B-9. I/O ASSEMBLY

Introduction

The following block level theory applies to figure 6B-9. The I/O Assembly serves two major purposes. First, it provides instrument interface to the keyboard and HP-IB by two ribbon cables. Second, it provides several system functions, all of which are described below. In addition the I/O contains passive pull-up resistors for the data, address, and control lines for the System Interface Bus, (SIB).

HP-IB

U1 interprets HP-IB commands and controls the direction of data flow from an external controller to the local data bus. One side of U1, LD0-7, connects to the local data bus. The other side of U1 connects to two bidirectional data transceivers, U4 for data and U5 for control commands. Because HP-IB addressing is accomplished by software, no address lines are carried on the ribbon cable.

RPG

The RPG outputs two out-of-phase pulses. Direction of rotation is determined by the difference in phase angle between both pulses. The pulse frequency is a function of rotation speed and this tells the microprocessor (CPU) what size of incremental steps to take. Part of U13 detects RPG activity and interrupts the CPU by IRQ3 line.

Keyboard Controller

Keyboard controller U21 sees a key closure and interrupts the CPU by IRQ4 line. U21 detects which key was pressed by scanning column lines with pulses and sensing rows for a return path. When U21 is enabled, it converts key closure scan data to parallel data and places this data on the local data bus.

System Interrupt Latch

System interrupt latch allows one CPU to interrupt any other in a multiprocessor system. This is not used in the HP 54120T system.

Function Decoder

Function decoder U10 decodes address lines A12-A14 to enable, keyboard controller, RPG counter, HP-IB controller, board type, and power supply status.

Slot Decode

The CPU accesses this board by sending out the board's slot ID code over address lines A19-A22. U45 is a 4-bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When the two codes are equal, U45 pin 6 will output a pulse which enables other circuitry.

Board Type

One side of U305 is hardwired to represent the board ID number. When the CPU asks for board type, U305 places a board ID number on the local data bus.

LDTACK Generator

U35 generates LDTACK, which is sent back to the CPU indicating data was received. This signal also resets the bus error timer.

Bus Error Timer

Under normal operation U18 should be reset by LDTACK before a time constant set by R19 and C40 times out. If U18 is not reset, it will generate LBUSERR. This keeps the CPU from getting hung up in an instruction cycle. This could happen if any addressed board does not generate LDTACK or if the CPU tries to access a nonexistent board.

TTL Oscillator

The TTL oscillator is a crystal-controlled 16 MHz oscillator. A binary counter divides this into 8 MHz, 4 MHz and 2 MHz. All four signals are placed on the system interface bus for use by other assemblies.

Power-on Reset

The power-on reset circuit provides a glitch-free pulse shortly after power up and power down. This sets many devices to a known state and prevents the CPU from taking damaging action during power up. This also provides a means to reset the system with a push button, without powering down the instrument.

Power Detect

The power detect circuit samples all six supply voltages. If one or more fails, the LED on top of the I/O assembly will not illuminate.

Non-Volatile RAM Power Supply

A battery provides the necessary power for RAM on the CPU assembly to retain basic setup information and system configuration for several years. The circuit also provides for smooth transfer of power from the battery to the power supplies after initial power up.

Dynamic RAM

The I/O assembly provides 256k words of additional CPU memory used for waveform storage and other purposes. The memory is an array of sixteen 64k by 4-bit dynamic RAMs. Dynamic RAM is addressed in rows and columns with low row address strobe (LRAS1-4) and low column address strobes (LCAS1-8). Dynamic memory must be refreshed at regular intervals to maintain memory. This is accomplished with refresh counters U19-31.
From the CPU's perspective the dynamic RAM is a slot by itself, irrespective of the slot for the I/O assembly. The other assemblies are identified by their slot ID code. U51 is a 4-bit comparator which compares address lines A19-22 with code 10 decimal which is hardwired on the other comparator input. The CPU sees the dynamic RAM at "slot" 10 no matter which slot the I/O board is in.

Table 6B-6. I/O Assembly Mnemonics

MNEMONICS	DEFINITION	MNEMONICS	DEFINITION
DI1-8	HP-IB Data lines 1-8	LRHPIB	Low Read HP-IB
D0-7	SIB Data lines 0-7	LRKEY	Low Read Keyboard
DS	Data Strobe	LRPWR	Low Read Power
IDO-3	Board ID lines 0-3	LRRPG	Low Read RPG
LIRQ1-7	Low Interrupt Request lines 1-7	LSB	Least Significant Bit
LA1-3	Local Address lines 1-3	LSTROBE	Low Strobe
LAS	Low Address Strobe	LUDS	Low Upper Data Strobe
LCAS1-8	Low Column Address Strobe lines 1-8	LWHPIB	Low Write HP-IB
LDTACK	Low Data Acknowledge	LWKEY	Low Write Keyboard
LD0-7	Local Data lines 0-7	LWRPG	Low Write RPG
LEN	Low Enable	R/LW	Read Low Write
LLDS	Low Lower Data Strobe	RPG	Rotary Pulse Generator
LRAS1-4	Low Row Address Strobe lines 1-4	SIB	System Interface Bus

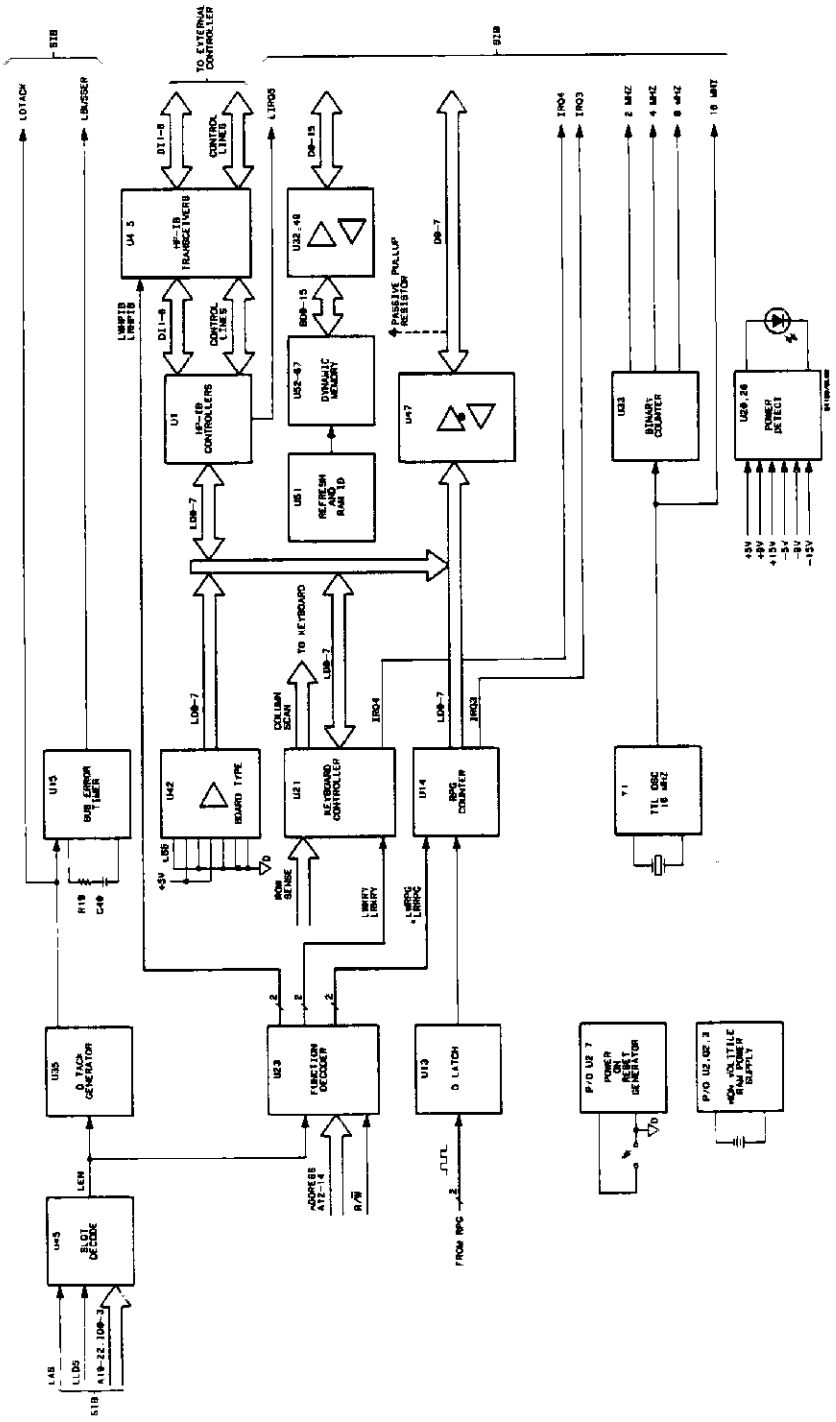


Figure 6B-8. I/O Assembly Block Diagram.

6B-10. MICROPROCESSOR ASSEMBLY

Introduction

The following theory applies to figure 6B-9. The microprocessor (CPU) has two major functions, data acquisition and I/O interfacing. It starts an acquisition cycle by resetting the GO bit to a logic low level. The CPU then waits for the GO bit to go high again. The GO bit going high tells the CPU to go and process sampled data. I/O interfacing involves updating display information, interpreting key closure data, RPG data, and HP-IB commands. In remote mode the CPU takes commands from an external controller.

CTC

The counter timer chip (CTC) contains three counters. The CPU programs and reads each counter over LD0-7 lines. Each counter has an output which is used as an interrupt to the CPU. All three counter outputs are ORed through U35 and U42. The result is ORed through U40 with LIRQ6 from the SIB and applied to the system interrupt latch.

System Interrupt Latch

The system interrupt latch allows the CPU to mask off any or all interrupt lines. The CPU sends data to U1 on LD0-7 lines. For normal operation all outputs of U1 are normally a zero, and all incoming SIB interrupt lines are normally a one. When an interrupt occurs on the SIB that interrupt line will be a zero, the corresponding output of U17 or U18 will also be a zero. The CPU can mask off any interrupt lines by simply writing a one to U17 or U18 through U1. This will guarantee that corresponding output levels of U17 or U18 will also be a one regardless of what the SIB interrupt lines are doing.

Priority Encoder

This circuit encodes all seven incoming interrupt lines into three lines for the CPU. If more than one interrupt occurs at the same time, U34 will prioritize them so the interrupt with the highest priority will be processed first. When an interrupt occurs, the system is vectored to a predetermined software location.

Bus Arbitration

This board contains circuitry so it will operate in a multiprocessor system. Since only one CPU is used, the bus request and bus grant signals are tied to the proper logic levels to ensure this board will have control over the SIB when required.

Bus Buffers

They enhance the drive capabilities of the CPU. When enabled, they connect the CPU with the correct bus, these are:

- U48 and U49 for SIB data bus
- U45, U46 and U47 for SIB address bus
- U4 and U21 for local data bus
- U5, U6, U22 and U23 for local address bus

Decoders

U36 decodes PA16-18 to enable ROM pairs 0-7. U19 decodes PA14-16 to enable RAM pairs 0 and 1, interrupt latch, and counter timer chip.

CPU

This chip is a Motorola 68000 microprocessor running at 8 MHz. Main characteristics are, 16-bit data bus, 23-bit address bus, and 3 interrupt lines. At initial power up condition, power on reset (POR) insures the CPU will start-up in a known condition. The CPU will then run several routines, some of which are: determine which board type is in which slot, system selfdiagnostics, and setup display information. The CPU will now respond to system interrupts, HP-IB, keyboard, or RPG. To the CPU all boards connected to the SIB look like memory locations.

When A23 is a logic high level, the CPU is accessing system memory over the SIB. When A23 is a zero, then the CPU is accessing local processor board memory locations. After the CPU sends data over the SIB, LDTACK returns from the addressed board and signals the CPU the information was received. LDTACK also goes to the I/O board and resets a buserror timer. If the buserror timer is not reset, BUSERR is sent to the CPU. The CPU will display a SOFTWARE ERROR message on the CRT.

Memory

The ROMs and RAMs have 8-bit data lines. The 16-bit words are divided into a lower portion LD0-7, and an upper portion LD8-15. All the ROMs or RAMs are read in pairs. Software instructions for the CPU are contained in ROM memory. There is space for eight ROM pairs, but not all of the space is used. Non-volatile battery backed-up RAM memory contains stack registers, status registers, scratch pad memory, instrument serial number, and soft-cal information.

Table 6B-7. Microprocessor Assembly Mnemonics

MNEMONICS	DEFINITION
CPU	Central Processing Unit
CTC	Counter Timer Chip
LD0-15	Local Data lines 0-15
LDTACK	Low Data Acknowledge
LIRQ1-7	Low Interrupt Request lines 1-7
PA1-22	Microprocessor Address lines 1-22
PD0-15	Microprocessor Data lines 0-15
POR	Power On Reset
SIB	System Interface Bus
1LA1-15	Lower Local Address lines 1-15
2LA1-15	Upper Local Address lines 1-15

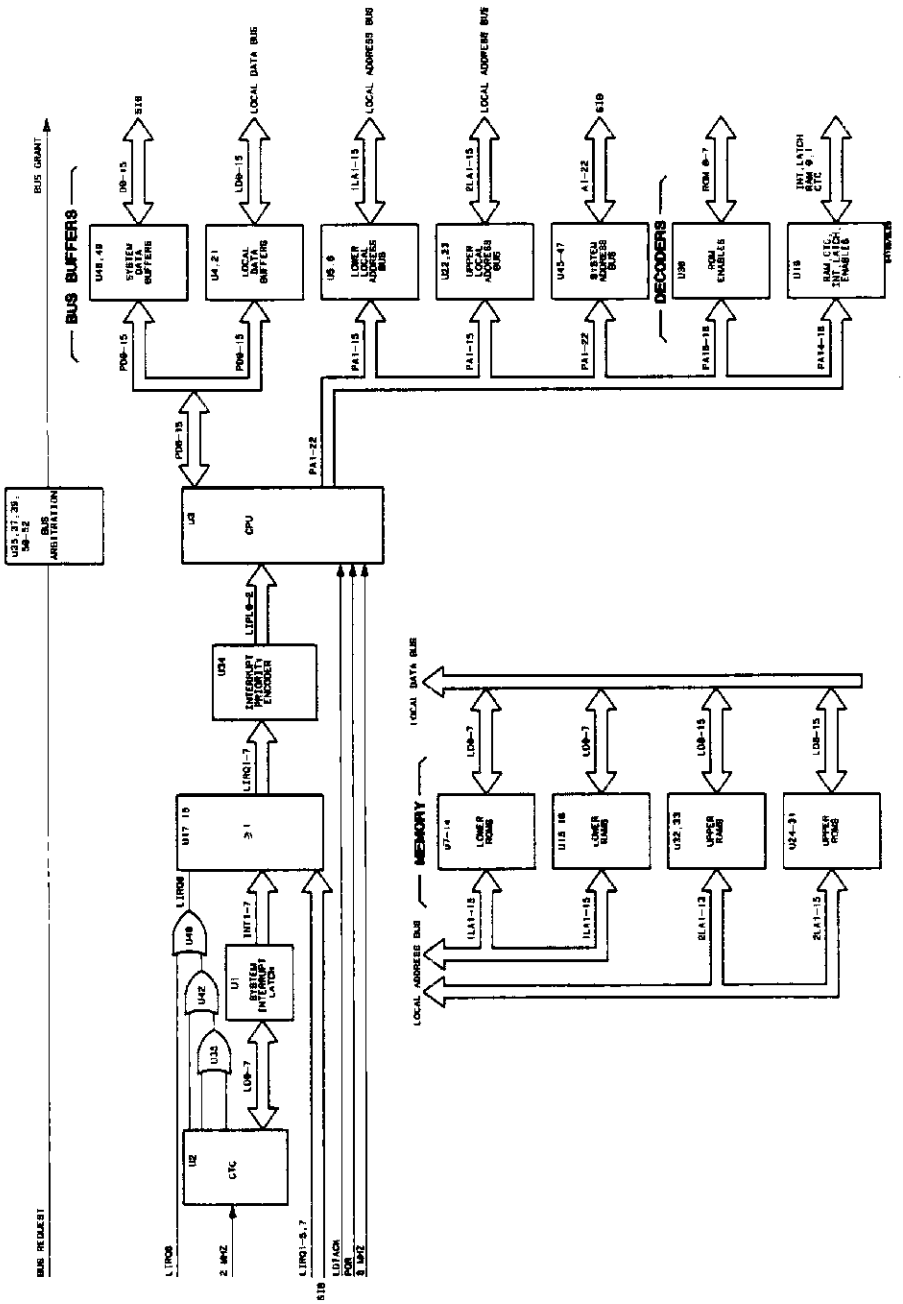


Figure 6B-9. Microprocessor Assembly Block Diagram.

6B-11. COLOR DISPLAY ASSEMBLY

Introduction

This theory refers to figure 6B-10. The board is the interface between the host microprocessor and color monitor. It has graphics memory, timing generator, character generator, prioritizing circuitry, color map, and color output DACs.

CRT Controller

The CRT controller controls several board functions, timing signals for the color monitor, blanking, horizontal drive, vertical drive, and character control functions.

Character RAM

Characters are stored in RAM as a 16-bit word, eight bits for an ASCII word and eight bits for character attributes.

Bit number	Function
TD0-6	ASCII character
TD7	Not used
TD8	Inverse video
TD9	Blink
TD10	Underline
TD11-14	Color
TD15	Priority bit

Character ROM

It functions as a character generator by decoding ASCII data, TD0-7, from character RAMs and sending it through character shift registers to the encode circuit.

Character Shift Registers

They are parallel loaded with character data and output character video in serial format.

Attribute Logic

It converts TD8-15 to attributes, four bits for color and four bits for other attributes. To define these bits, refer to the table under Character RAM heading discussed earlier.

Dual Port Arbiter

The dual port arbiter outputs addresses from either the host CPU or from an outside controller and places graphics on the CRT.

Display Address Counters

They are 4-bit counters which generate graphic address lines GA0-13.

Graphics RAM

They are six planes of dynamic memory where graphics data is stored.

Plane	Information
0	Graticules
1	Stored Traces
2	Channel 1
3	Channel 2
4	Channel 3
5	Channel 4

Graphics Shift Registers

This circuit is parallel loaded with graphics data and it serially outputs graphics video.

Color Map and Output DAC

The color map consists of three color RAMs which convert the encoded addresses to a digital value. There is one output DAC for each color RAM. The output DACs convert this digital value to red, green, or blue levels for the color monitor.

D Latch

This circuit outputs LDTACK over the SIB indicating data was received from the CPU.

Trace Priority Encode

This is a high speed RAM whose function is to map outputs from the graphics planes into unique address locations for the color map. It also provides arbitration when more than one plane tries to illuminate the same pixel location. Plane 0 has the lowest priority while the other places have equal priority.

Output Encode

This circuit uses either graphics data or character and attribute data to generate addresses for the color map.

Timing Generation

Timing generation controls timing functions for the display board.

Slot Decode

The CPU accesses this board by sending out the board's slot ID code over address lines A19-22. U141 is a four bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When the two codes are equal, U141 pin 6 enables other circuitry.

Function Decoder

It decodes HA13-15 to enable various board functions, CRTC for the CRT controller, ID for board type, COLOR MAP for the color map and output DACs, priority for RAM.

Board Type

When board type is requested by the CPU, this board will respond with 25 over the LD0-7 lines. LD0, 3 and 4 will be pulled high through U134, LD1 and LD2 will be pulled low through U134. LD0 is the least significant bit so adding LD0, 3 and 4 equals 25.

Table 6B-8. Color Display Assembly Mnemonics

MNEMONICS	DEFINITION
A1-22	SIB Address lines 1-22
CAS 0-5	Column Address Strobe lines 0-5
CCLK	Character Clock
D0-15	SIB Data lines 0-15
DADD0-13	Display Address lines 0-13
DP0-5	Display Planes 0-5
GA0-13	Graphics Address lines 0-13
GRCLK	Graphics Clock
HA1-22	Local Address lines 1-22
HD0-15	Local Data lines 0-15
HIP21	High Priority bit 21 (Disables Graphics)
HSYNC	Horizontal Sync
LDS	Lower Data Strobe
LDTACK	Low Data Acknowledge
MA0-7	Memory Address lines 0-7
MD0-15	Memory Data lines 0-15
RAS 0-5	Row Address Strobe lines 0-5
SIB	System Interface Bus
TD0-15	Text and Attribute lines to character ROM
TXD0-3	Text and Attribute lines to encode circuitry
UDS	Upper Data Strobe
VSYNC	Vertical Sync

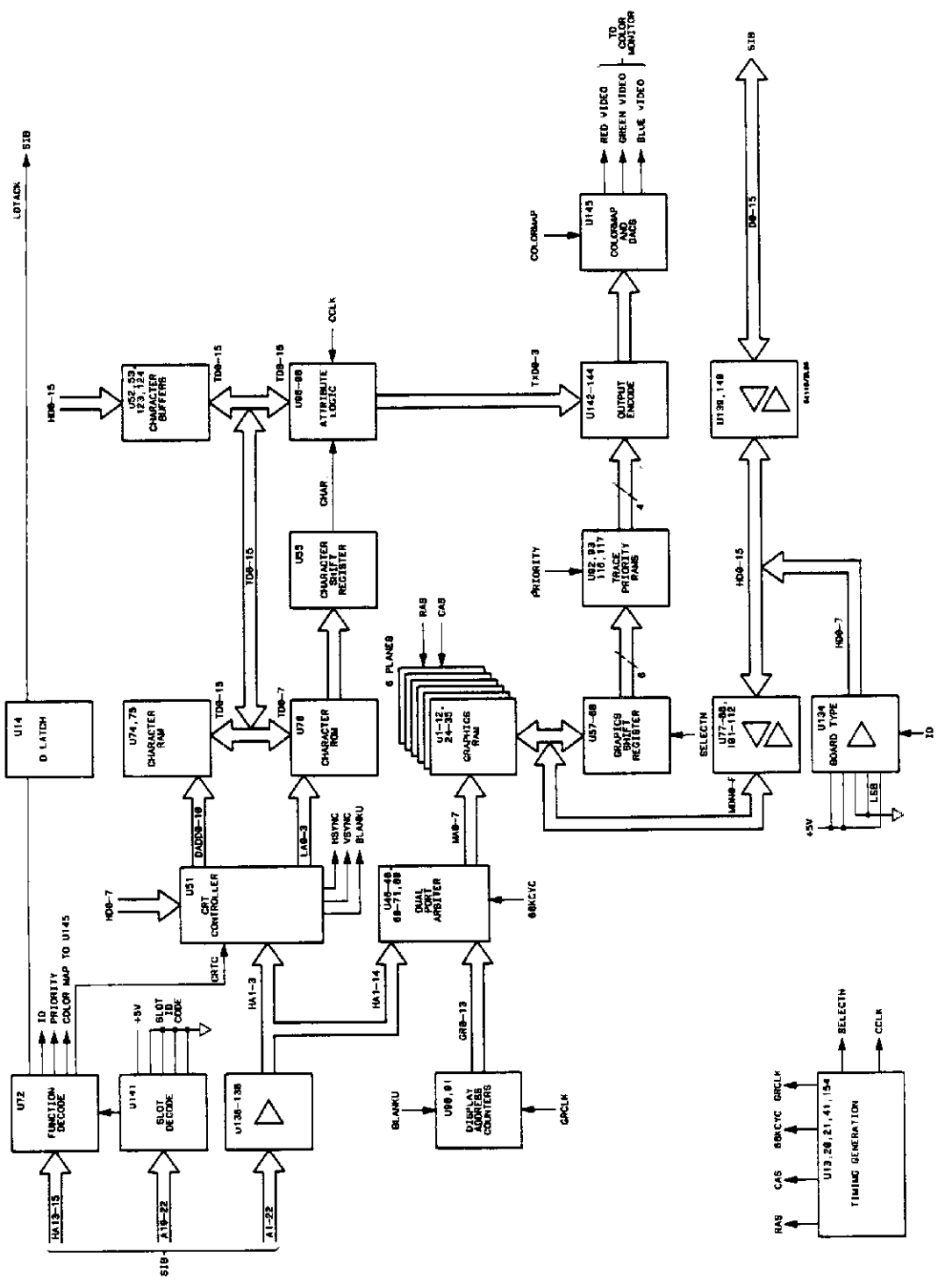


Figure 6B-10. Color Display Assembly Block Diagram.

6B-12. POWER SUPPLY ASSEMBLIES

PRIMARY SUPPLY

This theory refers to figure 6B-11. The primary board rectifies and filters the input ac voltage. When the voltage select switch is in the 230 V position, the ac is bridge rectified and filtered to yield approximately 300 V dc and 120 V dc. 120 V dc is generated by an isolating switching regulator, and is used to power the color monitor. 300V dc is used for the digital and analog supplies. The input voltage is doubled in the 115 V position to yield the same dc voltages. The primary board has surge protection circuitry that protects against ac line voltage transients and current surges. Over-voltage crowbar devices trip the circuit breaker for sustained input over-voltage conditions. The pulse width modulator (PWM) circuitry is powered by a bleeder resistor on one of the bulk storage capacitors. The main EMI (electromagnetic interference) filter is located in a dc current path to reduce component size and to increase the filter's effectiveness.

DIGITAL SUPPLY

The digital power supply is a dc to dc converter which converts 300 V dc to +5 V and -5.2 V dc.

Pulse Width Modulator (PWM)
Is used to achieve voltage and current regulation by changing the PWM's turn-on time. It has an operating frequency of 68 KHz.

Power Stage
Performs the actual conversion of 300 V dc to +5 V and -5.2 V dc. Digital and primary ground planes are kept isolated through transformer T2.

Optical Isolators
Isolates the primary and digital ground planes. Voltage and current feedback control is sent through U2 to control the duty cycle of the PWM. Power supply shutdown is sent by U3.

Loop Control and Supervisory
When excessive output voltage is detected, circuitry sets a latch in the PWM which can only be reset by cycling the circuit breaker off for 60 seconds, or an instantaneous reset by cycling the front panel power switch. Circuitry also senses the current and activates foldback current limiting for excessive current loading.

ANALOG SUPPLY

The analog power supply is a dc-to-dc converter which converts 300 V dc to +18 V, +8 V, -8 V, and -18 V dc.

Pulse Width Modulator (PWM)
Is used to achieve voltage and current regulation by changing the PWM's turn on time. It has an operating frequency of 68 KHz.

Power Stage
Performs the actual conversion of 300 V dc to +18 V, +8 V, -8 V, and -18 V dc. Plus a fan drive output that increases fan speed with ambient temperature. Analog and primary ground planes are kept isolated through transformer T2.

Optical Isolators
Isolates the primary and analog ground planes. Voltage and current feedback control is sent through U2, to control the duty cycle of the PWM. Power supply shutdown is sent through U3.

Loop Control and Supervisory
When excessive over-voltage is detected, circuitry sets a latch in the PWM which can only be reset instantaneously by cycling the front panel power switch to standby and then to on, or by turning the circuit breaker to the off position for 60 seconds. +18 V is regulated and the other outputs are semi-regulated outputs which follow the +18 V. Each output is current-limited. The -8 V output has foldback current limiting.

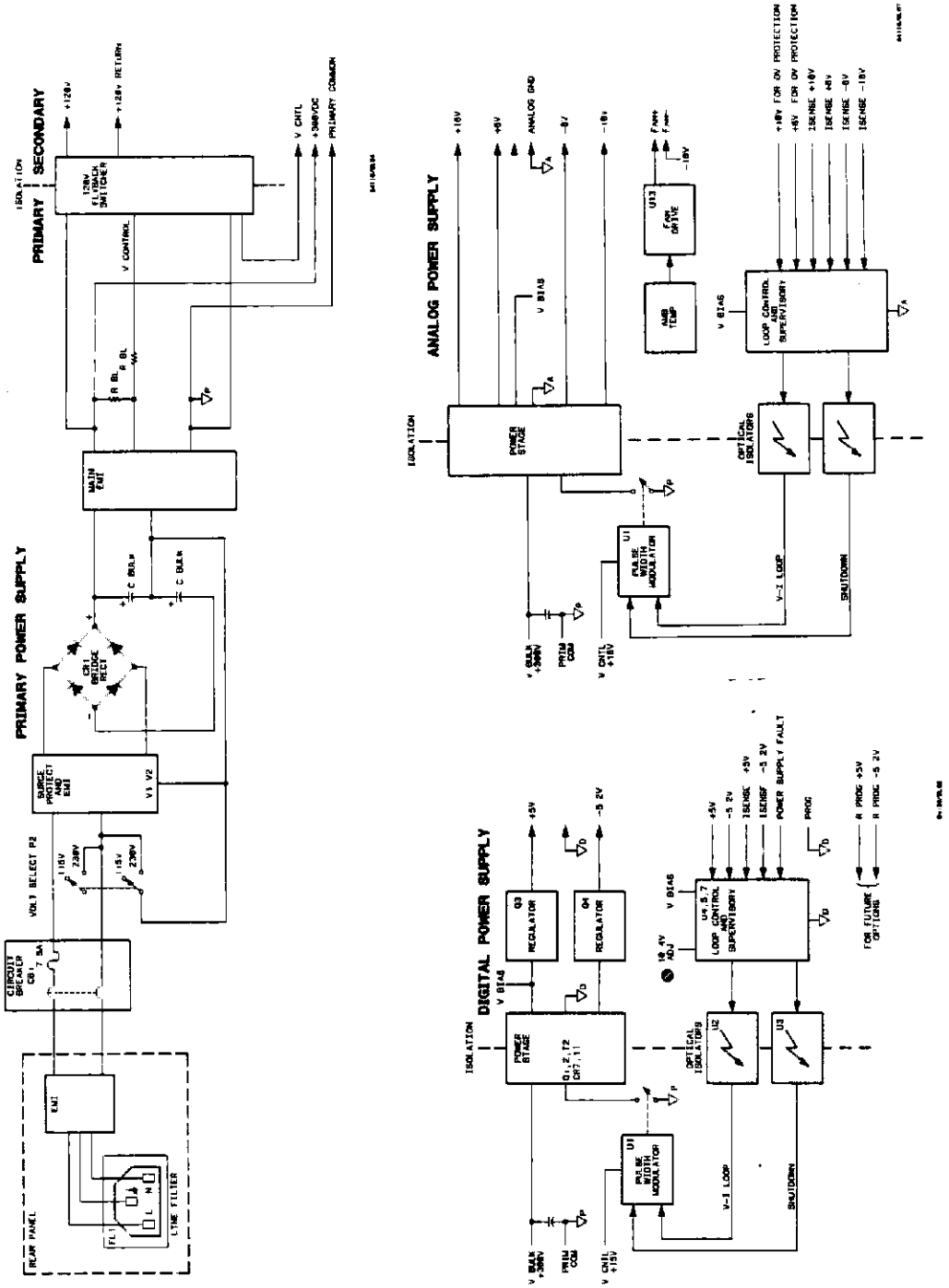


Figure 6B-11. Power Supply Assembly Block Diagrams.

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SERVICE MENU KEYS

SECTION 6C

SERVICE MENU KEYS

6C-1. INTRODUCTION

This section describes the service menus and keys that are available for calibration, troubleshooting, and CRT display alignment. A basic understanding of these will be helpful in troubleshooting failures, however, Self-Test and Troubleshooting is covered specifically in Section 6D.

6C-2. SERVICE MENUS

The service menus are part of the Utility menu, in the second level of the menu softkeys. Once Utility is pressed, five function keys will be displayed: Cal Menu, Test Menu, CRT Setup, Color Cal Menu, HP-IB Menu.

CAL MENU. The Cal Menu is used to calibrate the instrument. The calibration factors are stored in non-volatile memory. Use of this menu is covered in the *HP 54120T Operating and Programming Manual*". Basic functions of the Cal menus are covered in this section.

TEST MENU. The Test Menu provides several functions used to set up and run internal diagnostics test and view the results. Use of these functions is covered briefly in this section and comprehensively in the Self-Tests/Troubleshooting, section 6D.

CRT SETUP. The CRT Setup Menu provides several functions that provide confidence testing as well as test patterns for adjusting the Color CRT Module. These functions are discussed in this section.

COLOR CAL MENU. The Color Cal Menu provides functions used to set the characteristics of the colors displayed. These characteristics include hue, saturation, and luminosity. This menu is covered in detail in the Operating and Programming manual.

HP-IB MENU. The HP-IB Menu provides keys that are used to set the HP-IB attributes. These attributes are address number, Talk/Listen, and EOI. This menu is discussed in detail in the Operating and Programming manual.

6C-3. ONE-KEY POWERUP

A one-key powerup is performed to return the instrument setup to default conditions. This is done as follows:

1. Set the front panel POWER switch to STBY,
2. Press and hold any front panel key,
3. Turn front panel POWER switch to ON.
4. Release key when display shows "Powerup Self Test Passed!" or Failed.

6C-4. TWO-KEY POWERUP

CAUTION

Using the two-key powerup will leave the instrument in an uncalibrated state Effort needed for recalibration should be considered before using this mode to reset the instrument.

A two-key powerup is a basic reset of the entire operating system of the HP 54120T. All volatile and non-volatile RAM is cleared. As a result, all calibration factors are purged, front panel setups are erased, and the instrument must be recalibrated.

1. Set the front panel POWER switch to STBY.
2. Press and hold the top and bottom function keys. Refer to figure 6C-1.
3. Turn front panel POWER switch to ON.
4. Release keys when display shows "Powerup Self Test Passed!" or Failed.

6C-5. CAL MENUS

Vertical Cal

Vertical Cal sets software calibration factors to correct for sampler gain and offset errors. The cal is run by pressing the appropriate menu and function keys. All front panel inputs must be disconnected from the instrument.

Channel Skew Calibration

The channel skew calibration is a user cal which minimizes the delays between channels and also the external trigger input. If this cal is performed in a calibration facility, use cables and signals similar to what the user will use with the oscilloscope.

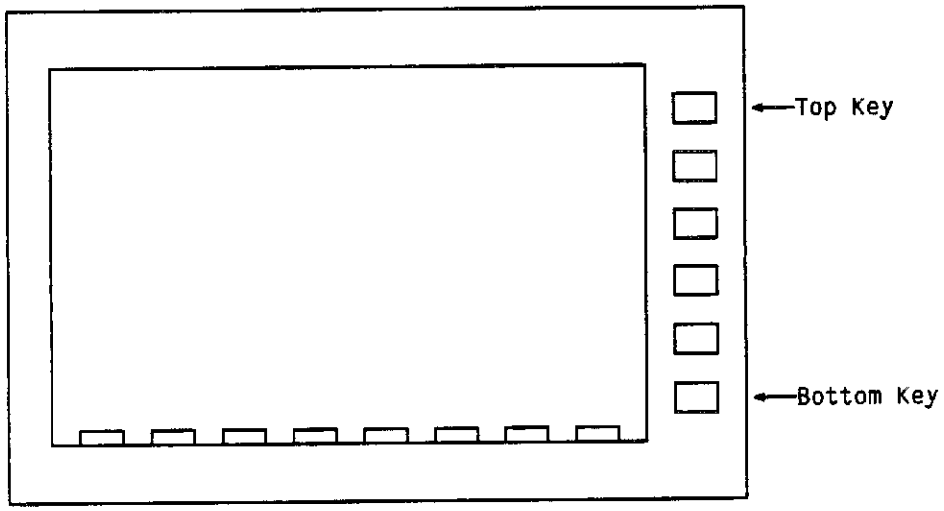

Figure 6C-1. Keys to Hold Down for Two-Key Powerup.

6C-6. TEST MENU

Five sub-menus are available when the Test Menu is selected. The menus allow the user to access and run internal diagnostics and view the results. In addition, the position of each card cage printed circuit board can be read and displayed, and the firmware revision date is displayed.

Use of the test menus is covered in depth in section 6D, Troubleshooting.

6C-7. Repeat Loop/Run From Loop

The top key toggles between REPEAT LOOP and RUN FROM LOOP. These keys in conjunction with Loop Number = [0-43] and the Start/Stop Test key will execute internal self-test diagnostic routines. All input signals must be disconnected from the instrument for these tests.

REPEAT LOOP. Selecting this mode will continuously execute the Loop # entered at RUN FROM LOOP. Pressing ***Start Test*** will start execution and the loop will continuously run until the ***Stop Test*** key is pressed. Pressing ***Display Errors*** will show how many times the loop was executed and the number of times the loop failed.

There are a number of loops that will blank or over-write the Stop Test key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

RUN FROM LOOP. Selecting this mode will start execution from the loop entered and will proceed to execute all higher numbered loops. Upon reaching the last test, the cycle will be repeated.

If any test should fail, the instrument will change from RUN FROM LOOP to REPEAT LOOP and will repeatedly execute the loop that failed until the ***Stop Test*** key is pressed.

6C-8. Extended Tests

When this key is chosen there are 13 internal instrument tests that may be selected by entering the test number with the entry devices. The tests are numbered 0 through 12. All input signals must be disconnected from the instrument for these tests.

Many of the extended tests are useful only at the factory. Those that are of use to field service personnel are covered in the troubleshooting in section 6D.

6C-9. Start/Stop Test

This key is used to initiate any test where a test number is entered by one of the entry devices. Once the test number is entered, pressing ***Start Test*** initiates the test and the key toggles to ***Stop Test***. Pressing ***Stop Test*** stops the test in progress and the key toggles back to ***Start Test***.

There are a number of tests that will blank or over-write the ***Stop Test*** key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

6C-10. Display Errors

Pressing this key will display the number of any loops which failed. The tests which test for loop failures are:

- Powerup self test
- EXTENDED tests
- REPEAT and RUN FROM LOOP tests
- HP-IB commanded self test

This display shows the current loop or last loop executed, the number of times the loop was executed, and the number of times that it failed. The bottom portion of the display shows all loops that failed starting with the first loop failure. These are cummulative failures and they are erased only on power up or I/O assembly reset.

The four STATUS x = xxxxx lines in the Display Errors field are primarily for factory use. Any field usable information in this part of the display is covered in the troubleshooting, section 6D.

To return to the Test Menu, press ***Exit Display***" key.

6C-11. Display Configuration

Most of the assemblies used in the mainframe have circuitry that allows them to be interrogated directly by the microprocessor. The exception being the microprocessor assembly. The mainframe card cage has 9 slots, but only four assemblies are in the card cage. When the ***Display Configuration***" key is pressed the resulting display shows the location of the card cage assemblies, except the microprocessor. The display assembly is shown as being in slot 14, this is not part of the card cage but is on the instrument's bottom side. The firmware revision date is also displayed.

To return to the Test Menu, press ***Exit Display*** key.

6C-12. CRT SETUP MENU

When CRT Setup Menu is selected, four keys are displayed that allow access to CRT setup displays. The keys available are, from top to bottom, Confidence Test, Pattern Off, Light Output Off, Color Purity Off, and at the bottom, Exit CRT Setup Menu.

Even though some of the patterns overwrite the key display, the functions can be selected. The bottom key can be pressed at any time to exit the CRT Setup Menu.

6C-13. Confidence Test

When this function is selected, the confidence test pattern is displayed. The pattern consists of three parts. At the top is a complete character set, in the center is a group of seven color blocks, and at the bottom a seven block grey-scale.

The top four lines of the character set display include the complete character set. The bottom line displays three sets of numerals. The first set is displayed in inverse video, the second set flashes between normal and inverse video and the third set is normal video and underlined.

The seven color blocks displayed at the center are, from left to right; beige, grey, red, yellow, green, amber, and cyan.

NOTE

Since color perception is subjective, any slight variation in colors from what is described here should be disregarded.

At the bottom of the CRT a seven block grey-scale is displayed, with increasing luminosity from left to right. This grey-scale display is used if Color CRT Module adjustments are necessary.

6C-14. Pattern

These patterns are used when Color CRT Module adjustments are necessary. When CRT Setup Menu is selected, this key is initially ***Pattern Off***

Pressing ***Pattern Off*** once will display a white cross-hatch pattern over the entire CRT and the Pattern Off key changes to Pattern White. Inside the cross-hatch pattern there are dots at the center, corners, and at the 12, 3, 6 and 9 o'clock positions. Additionally, there are test matrices in the center and corners.

Pressing ***Pattern White*** key changes the pattern color to red and the key label changes to "Pattern Red". Repeatedly pressing this key will change the color of the pattern to green then blue. The name of the Pattern key is the color displayed.

Pressing ***Pattern Blue*** key changes the display to the white cross- hatch pattern on the top half of the CRT and white with a dark cross-hatch on the bottom. The key then changes to Pattern HV Reg. This test is used primarily by the factory, however it may indicate the need for service if there are severe high voltage problems.

Pressing ***Pattern HV Reg*** changes the display to a solid white screen with dark cross hatch lines. The key changes to Pattern I White. Successive pressing of this key changes the color to red, green and then blue, the name of the Pattern key is again the color of the display.

Pressing ***Pattern I Blue*** changes the display to a white cross-hatch pattern with the inside flashing between solid white and cross-hatch. The key changes to Pattern Bounce. This test is primarily used by the factory, however, it may indicate the need for service if there are severe high voltage problems.

Pressing ***Pattern Bounce*** exits this set of tests and returns the CRT Setup Menu.

6C-15. Light Output

These displays are used by the factory.

Pressing ***Light Output White*** displays a horizontal band of white half the height of the display. The key display is not overwritten. Repeatedly pressing this key will change the color of this band to red, green, blue and then a grey-scale. Each time the key is pressed it also changes to the appropriate description.

Pressing ***Light Output Grey-Scale*** exits this set of tests and returns the CRT Setup Menu.

6C-16. Color Purity

Pressing ***Color Purity Off*** displays a full white raster. Repeatedly pressing this key changes the color of the raster to red, green and then blue. At each color display the name of the key changes to the appropriate description. These displays are used when Color CRT Module adjustments are necessary.

Pressing ***Color Purity Blue*** exits this set of tests and returns the CRT Setup Menu.

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TROUBLESHOOTING

SECTION 6D

TROUBLESHOOTING

6D-1. INTRODUCTION

This section contains internal diagnostics (Self-Tests) and troubleshooting information for fault location to the PC assembly level. Reading sections 6C, theory of operation, and 6D, service menu keys, will help in understanding this section.

6D-2. SAFETY CONSIDERATIONS

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

WARNING

This instrument is equipped with a standby switch on the front panel that DOES NOT de-energize the power supply. To avoid shock hazards capable of causing injury or death, the main power switch on the rear panel must be used to de-energize the instrument or the power cable must be disconnected when the instrument must be de-energized.

CAUTION

The Four Channel Test Set is very sensitive to static discharge. Failure to observe proper antistatic methods may result in damage to the gallium arsenide samplers. All maintenance or operation should be performed while using an antistatic mat and wrist strap, which are supplied with the instrument.

WARNING

Maintenance described in this section is performed with power supplied to the instrument and with protective covers removed. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed. Read the Safety Summary in the front of this manual.

CAUTION

Do not remove or replace any of the circuit board assemblies in this instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

6D-3. RECOMMENDED TEST EQUIPMENT

Equipment recommended for service is listed in table 1-1. Any equipment that satisfies the critical specifications stated in the table may be substituted.

6D-4. LOGIC FAMILIES USED

Three different logic families are used in the HP 54120T. These include TTL, ECL, and EECL. Table 6D-1 indicates the assemblies where each logic family is used.

TTL ranges from approximately 0 V to 5 V and is used on much of the digital circuitry and the slower speed data acquisition circuitry; such as status registers, RAM addressing, etc.

ECL ranges from -.9 V to -1.7 V and is used more often in the data acquisition circuitry where speed is of great importance.

EECL ranges from 0 V to -.8 V and is used on the outputs of many custom IC's.

Because the ECL high and the EECL low share about the same voltage level, it's possible that a misinterpretation of a logic level could occur. Extra care should be taken when dealing with these levels. Typical monitor oscilloscope offset levels are -1.3 V for ECL and -.4 V for EECL.

Table 6D-1. Logic Families Used in the HP 54120T.

Board	Logic Family
CPU	TTL
Display	TTL
I/O	TTL
Hort Control	TTL
Horizontal	ECL,EECL
A/D	TTL
Vertical	EECL (This assembly is mostly analog signals)

6D-5. DIAGNOSTIC OVERVIEW

The troubleshooting section is divided into three sub-sections for ease of use: main troubleshooting, internal diagnostic loop tests, and extended service test.

Start all diagnostics with the main troubleshooting section. It includes the mainframe system troubleshooting (CPU, I/O, power supplies, keyboards and display system) and data acquisition troubleshooting. This section will refer to particular paragraphs in the other two sub-sections.

Follow these steps when troubleshooting most failures.

1. Verify the failure mode.

2. Start with the main troubleshooting flow diagram figure, 6D-1, to determine if the failure is in the mainframe or data acquisition system.

3. **Mainframe problems**
   The main troubleshooting flow diagram will help solve these failures.

   Data acquisition problems
   Analyze the failure (paragraph 6D-13) and use flow diagrams (figures 6D-11 through 6D-20) to determine which extended service test or loop test to run.

4. The samplers are very susceptible to electrostatic discharge (ESD) and may be the cause of many data acquisition problems.

6D-9. MAINFRAME TROUBLESHOOTING

This portion of the main troubleshooting section contains information to determine the faulty mainframe assembly. The following instrument sections are verified: display system, keyboard system, card cage assemblies (core system), and power supplies.

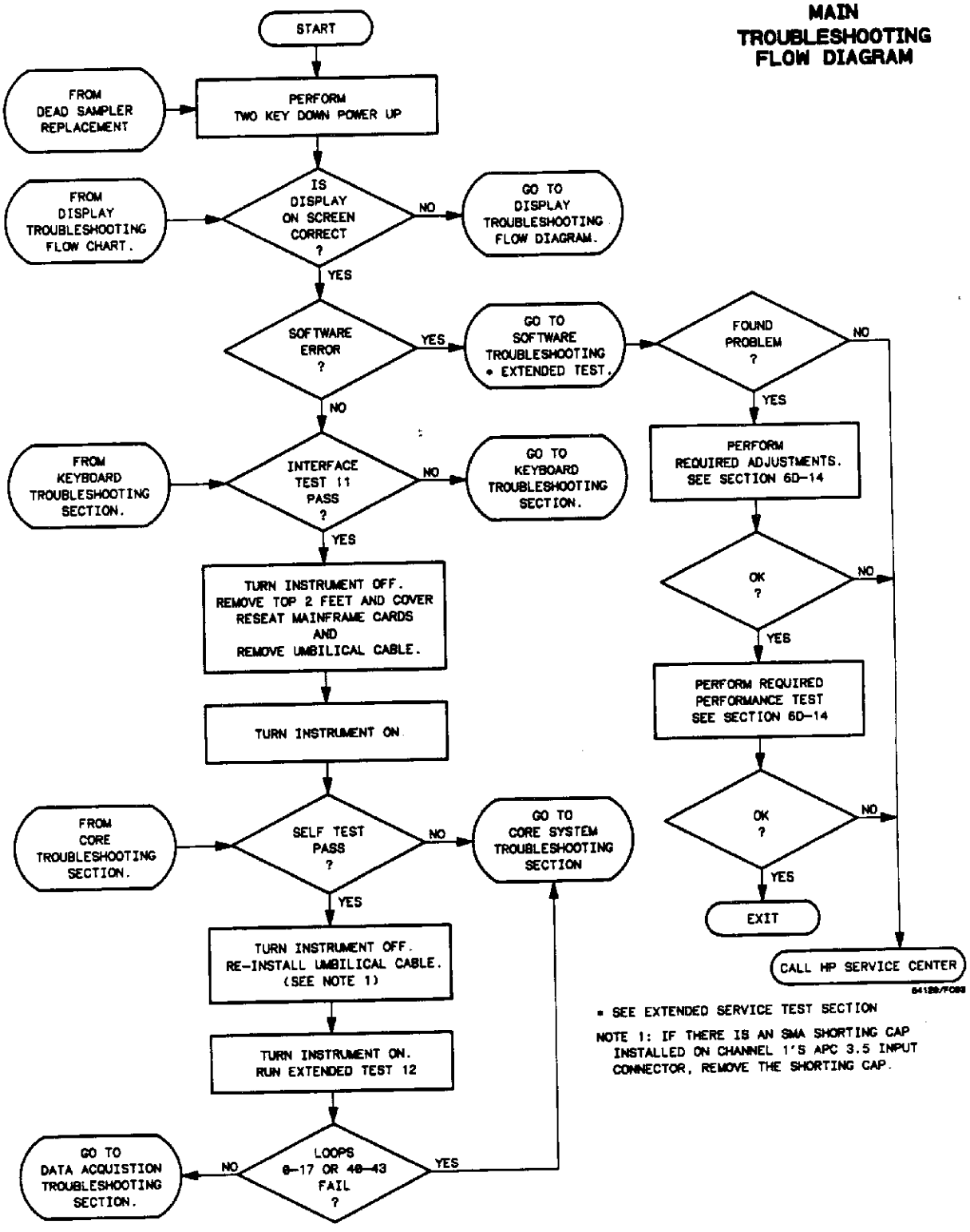


Figure 6D-1. Main Troubleshooting Flow Diagram.

6D-6. ONE KEY-DOWN POWERUP

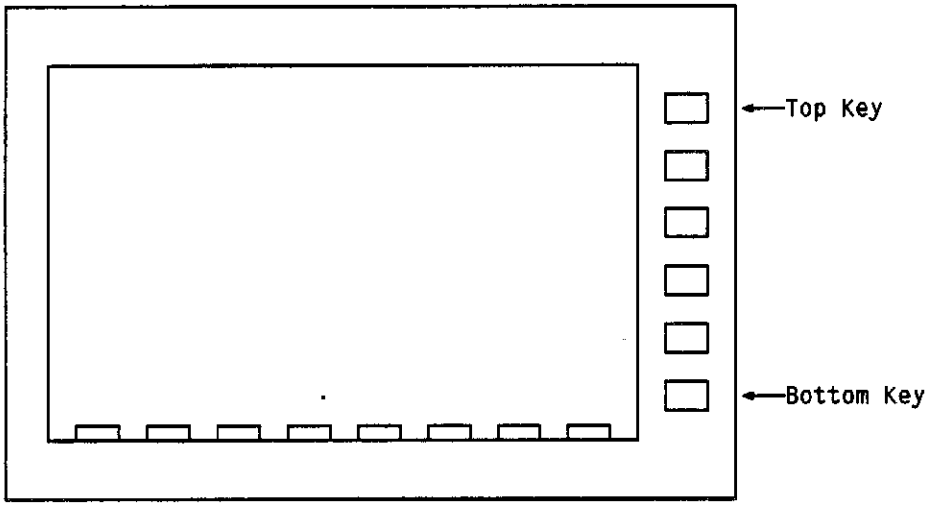
A one key-down powerup places the instrument in a default condition. This default condition is identical to sending an HP-IB "RESET" over the bus. This allows users a known starting point to begin their test procedures from. Hold down any key while cycling the oscilloscope's power off and on. Continue to hold the key down until graticules are displayed on the screen.

6D-7. TWO KEY-DOWN POWERUP

A two key-down powerup sets up the instrument identical to a one key-down powerup and it clears all the RAM memory locations, resets all digital storage devices, clears vertical software calibration factors, and clears the channel to channel skew factors.

a. Turn oscilloscope's power switch to STBY.
b. Hold down the top and bottom function keys immediately screen's right.
c. Turn oscilloscope's power switch to ON.
d. Continue holding function keys until graticule display is on screen.
e. Ignore "Front Panel Cals Lost" warnings on top of screen; CALs will be performed later.

Keys to Hold Down for Two Key-Down Powerup.



6D-8. I/O ASSEMBLY HARD RESET

This reset is similar to powering the instrument off and on, except the power supplies are not lowered to 0 V. The I/O assembly hard reset is useful for two reasons.

1. This is a convenient method for resetting the instrument with the top cover removed.

2. It can be a good troubleshooting aid when there may be a failure with the instrument's normal powerup routine.

Anytime the instrument has a powerup problem it may help isolate the problem by trying the I/O assembly hard reset. Especially if the instrument has intermittent powerup problems.

DISPLAY TROUBLESHOOTING FLOW DIAGRAM

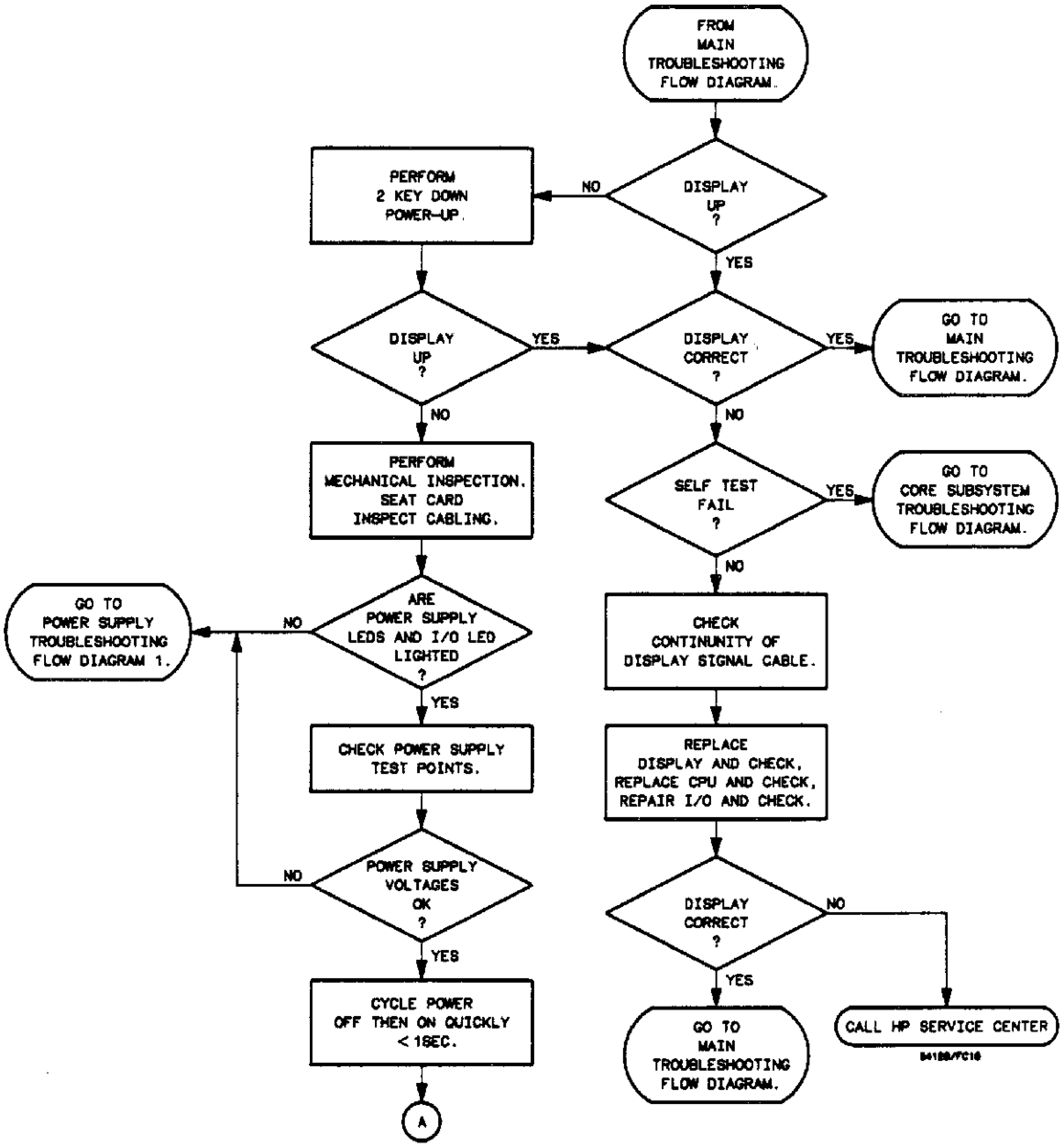


Figure 6D-2. Display Troubleshooting Flow Diagram

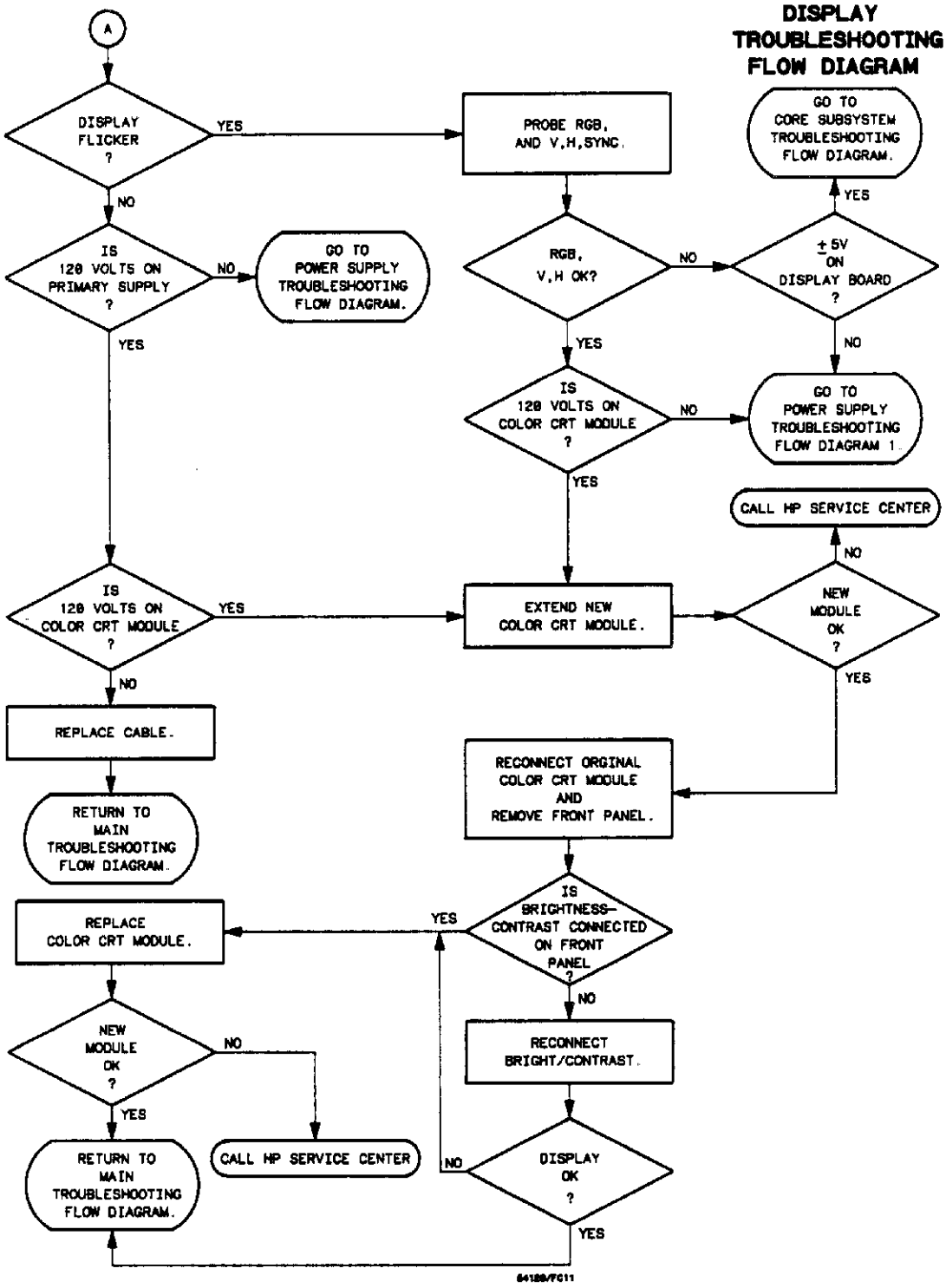


Figure 6D-3. Display Troubleshooting Flow Diagram (continued).

6D-10. KEYBOARD TROUBLESHOOTING

The keyboard troubleshooting uses flow diagram figure 6D-6 to isolate the faulty assembly to the I/O assembly, control keyboard, RPG, function keyboard, menu keyboard, or three interconnecting ribbon cables. Table 6D-2 describes what type signals are on the ribbon cables and figure 6D-5 is the cable's pin descriptions. Table 6D-3 describes which cable row and scan lines are used when the front panel keys are pressed. The softkeys name assignments change with the different menu selections. Figure 6D-4 illustrates a numbering scheme for these softkeys.

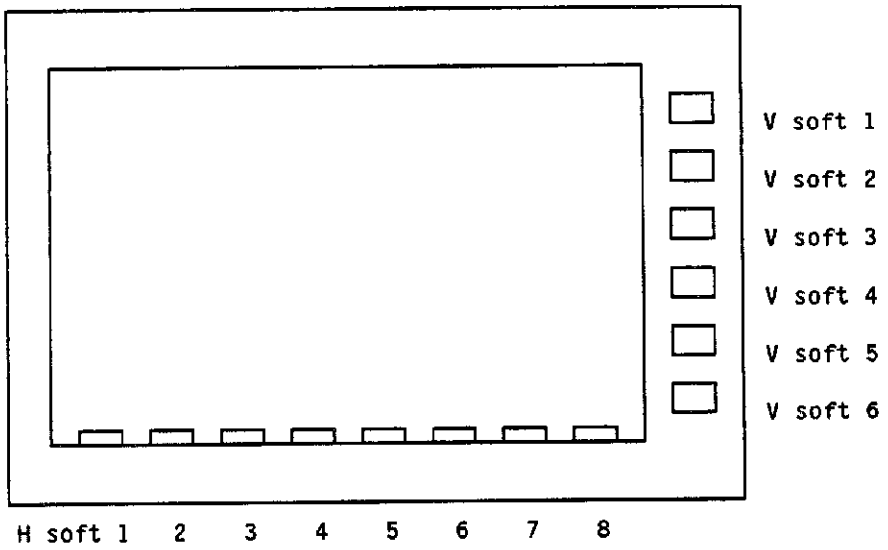


Figure 6D-4. Softkey Number Assignments.

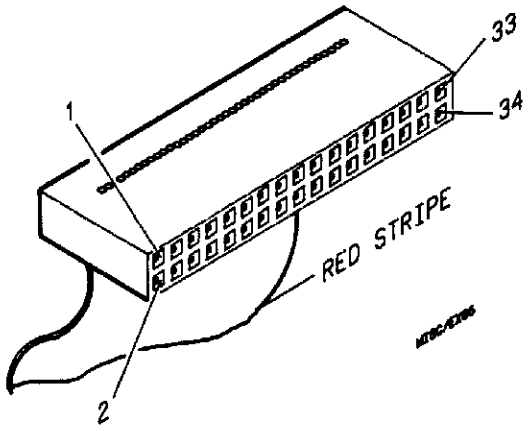


Figure 6D-5. Keyboard Cable W5 Pin Numbers.

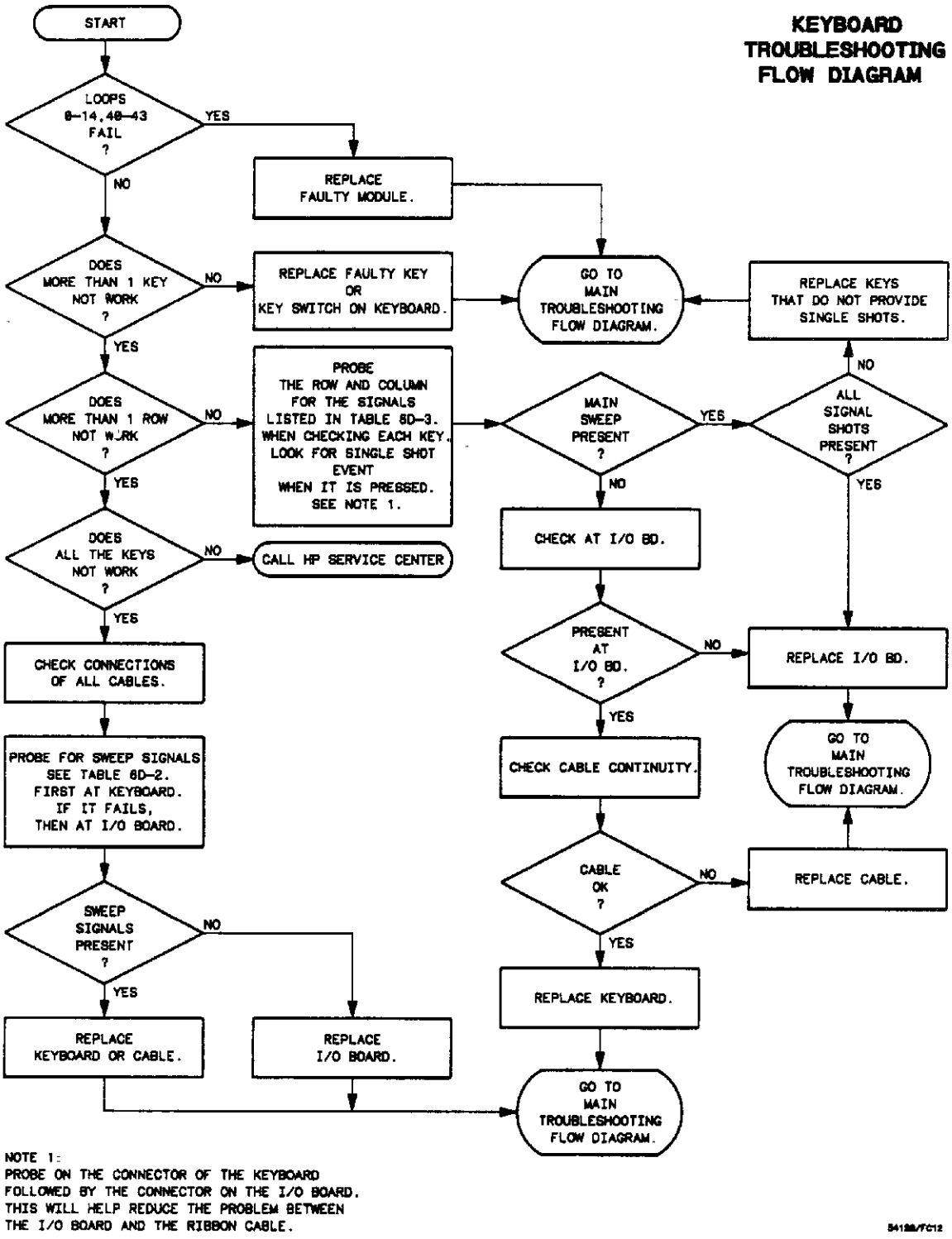


Figure 6D-6. Keyboard Troubleshooting Flow Diagram.

Table 6D-2. Keyboard Ribbon Cable Signal Description.

Pin Description	Cable Pin No.	I/O Bd. Pin No.	Signal
SC0	6	U12 pin 15	195 Hz, 60 mV to 2.8 V, 87% duty cycle,
SC1	5	U12 pin 14	each slightly shifted in phase
SC2	8	U12 pin 13	
SC3	7	U12 pin 12	
SC4	10	U12 pin 11	
SC5	9	U12 pin 10	
SC6	12	U12 pin 9	
SC7	11	U12 pin 7	
RL0	24	U21 pin 38	Single shot when present
RL1	26	U21 pin 39	
RL2	28	U21 pin 1	
RL3	30	U21 pin 2	
RL4	23	U21 pin 5	
RL5	25	U21 pin 6	
RL6	27	U21 pin 7	
RL7	29	U21 pin 8	
RPG	17	U34 pin 2	
RPG	18	U13 pin 12	
NOT USED	13	U40 pin 3	
NOT USED	16	U39 pin 6	
NOT USED	14	U28 pin 11	
+5 V	1-4		+5 V
NOT USED	33,34		
DGND	15,21,22		0 V
DGND	31,32		0 V
NOT USED	19		
NOT USED	20	U20 pin 13	

Table 6D-3. Row and Column Key Assignments.

	SC0	SC1	SC2	SC3	SC4	SC5	SC6	SC7
RL0	H soft 1	H soft 7	Sec/Volt	0	8	Clear	Autoscale	↑ ←
RL1	H soft 2	H soft 8	msec/mV	1	9	Run		← ↓
RL2	H soft 3	V soft 6	μs/μV	2		Stop/Single		
RL3	H soft 4	V soft 5	ns	3		Save		
RL4	H soft 5	V soft 4	ps	4		Recall		
RL5	H soft 6	V soft 3		5		Local		
RL6		V soft 2		6				
RL7		V soft 1		7				

6D-11. CORE SUBSYSTEM TROUBLESHOOTING

There are two core subsystem troubleshooting methods. If the loop test information is on the screen, use table 6D-4. If the display or keyboard systems are locked up, use figure 6D-7.

It is preferable to get the HP 54120T to pass all the Core Tests before going on to fix more complex loops. Occasionally, bent motherboard pins or defects in other system elements will causes these loops to fail. By making a system of the microprocessor assembly, I/O assembly and one other assembly, it is possible to determine which socket or assembly may be causing an interaction that causes one of the core loops to fail. Using this technique, seat each assembly into the motherboard one at a time. Be sure to turn the power off before raising or seating an assembly into the motherboard.

If only the microprocessor and I/O assemblies are seated, the system will go into a repeating multicolored routine with about a two second cycle. This is useful in certain troubleshooting situations but no loop error information will be available.

Table 6D-4. Core Subsystem Diagnostic Routines.

Test Loop	**Probable Failing Assembly**
0-4	Microprocessor assembly
5-9	Display assembly
10-15	I/O assembly
40	Microprocessor assembly
41-42	Display assembly
43	I/O assembly

Table 6D-5. Power Supply Distribution.

	+5V	-5V	+18V	+8V	-8V	-18V	+120V
MICROPROCESSOR	*						
INPUT/OUTPUT †	*	*	*	*	*	*	
HORIZONTAL CTNL	*		*	*	*	*	
ADC ASSEMBLY	*		*	*	*	*	
COLOR DISPLAY	*						
COLOR CRT MOD.							*
TEST SET							
FROM ADC			*			*	
FROM HORIZONTAL			*	*	*	*	

†Only the +5 V is used for power. The other supplies connect for power test only and are high impedance points; the likelihood of loading these supplies is low.

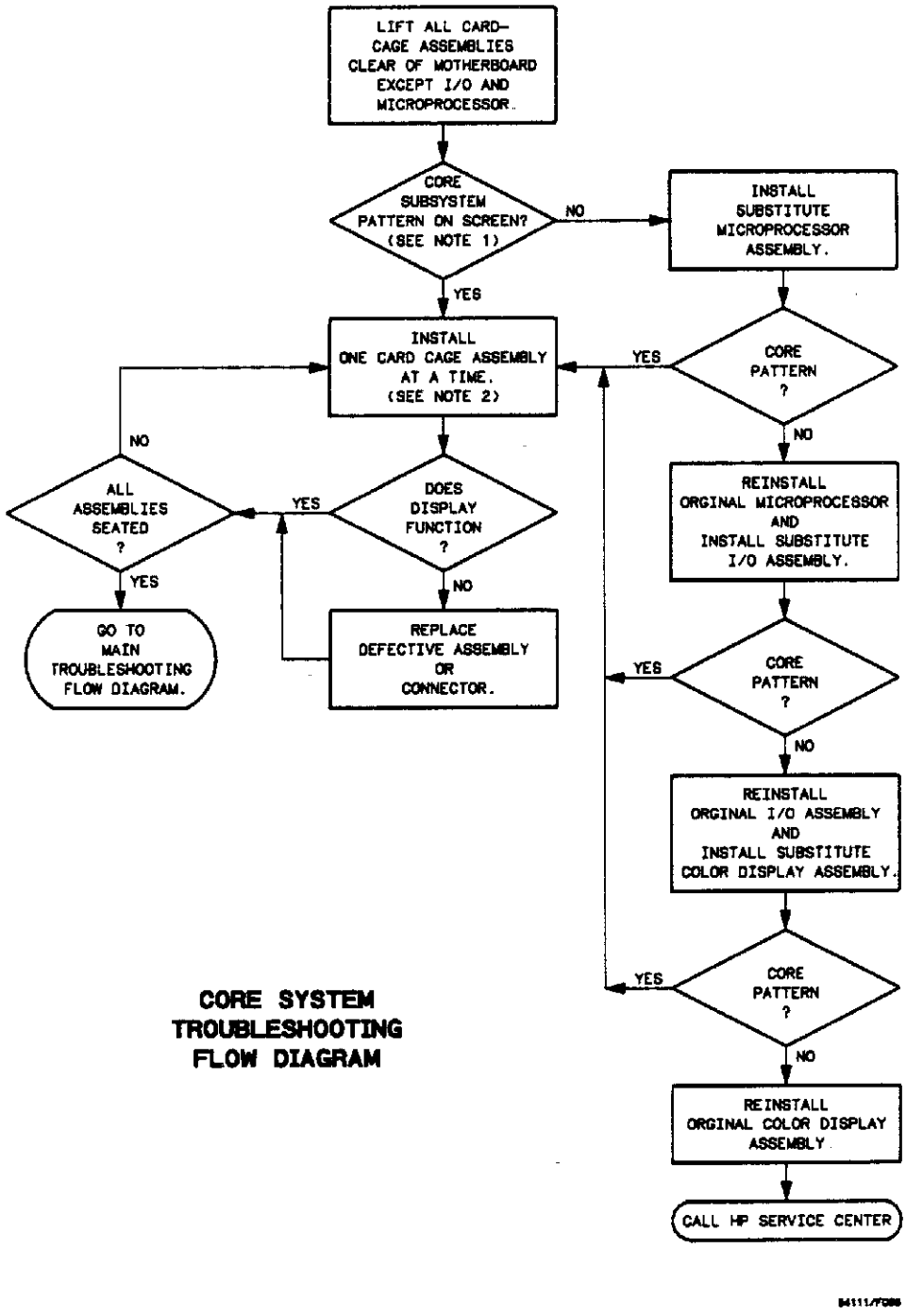


Figure 6D-7. Core Subsystem Troubleshooting Flow Diagram.

6D-12. POWER SUPPLY TROUBLESHOOTING

When a power supply problem is suspected, it is first important to make sure that no unusual load is keeping the supply in a current limited condition. Table 6D-5 indicates which supplies are used on each assembly.

1. If the 300V LED on the Primary Supply is not lit go directly to the Power Supply Troubleshooting Flow Diagram on the next page.

2. If the 300V LED is lit, find the LEDs on the Analog and Digital supplies and I/O assembly. The LEDs are near the top-front of each assembly, if you cannot see them they are probably not lit.

3. If the LEDs are lit and you still suspect a supply problem, go to the Power Supply Troubleshooting Flow Diagram on the next page.

4. If the LEDs are not lit continue with this procedure before going to the Power Supply Troubleshooting Flow Diagram on the next page.

5. Disconnect the two ribbon cables which connect to the rear of the A/D and horizontal control assemblies.

6. If the three LED's are not lit continue with step 10; otherwise reconnect the two ribbon cables and continue with step 7.

7. Disconnect the two ribbon cables which connect the umbilical cable to the horizontal and vertical assemblies in the test set.

8. If the three LED's are lit, proceed with step 9. If the three LED's are not lit, the failure is either the mainframe ribbon cable, umbilical cable, or test set ribbon cable. Connect and disconnect the cables until you've isolated the faulty cable.

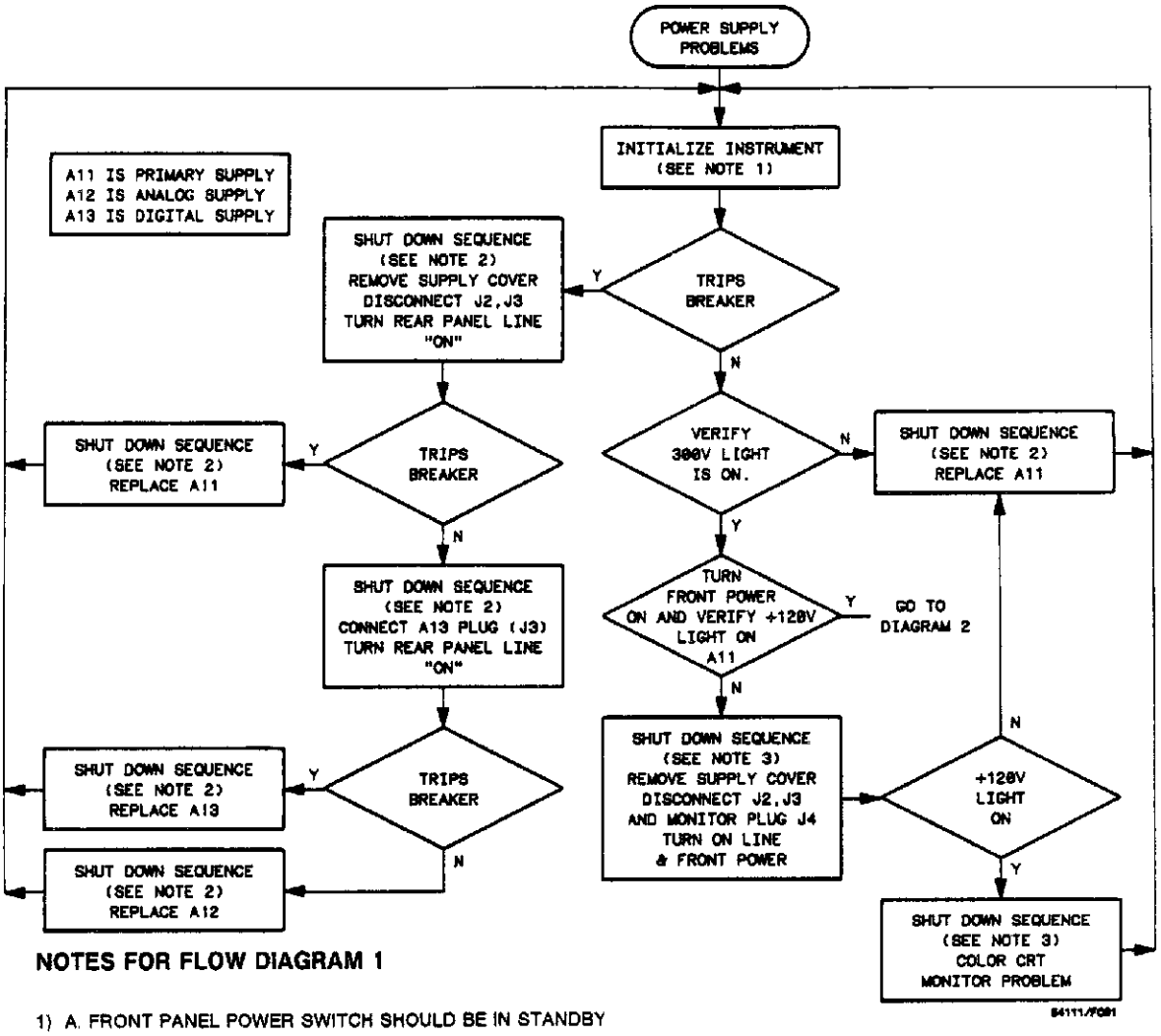
9. Connect the ribbon cable to the horizontal assembly. If the three LED's are not lit, replace the horizontal assembly; otherwise replace the vertical assembly and check to see if the supply problem is fixed.

10. At the right side of the instrument, pull up the horizontal control assembly until it clears the motherboard connector, about one half inch.

11. Check to see if the LEDs are lit. If the LEDs are lit troubleshoot the horizontal control for excessive loading. If they are not lit, leave the assembly up and go to the next step.

12. Working from right to left, pull up each card cage assembly while watching for the LEDs to light. If they light, troubleshoot for excessive loading on the last assembly pulled up.

13. After the I/O assembly is pulled up, watch only for the supply LEDs. If all nine card cage assemblies are up, and the supply LEDs are not lit, go to the ower Supply Troubleshooting Flow Diagram.



NOTES FOR FLOW DIAGRAM 1

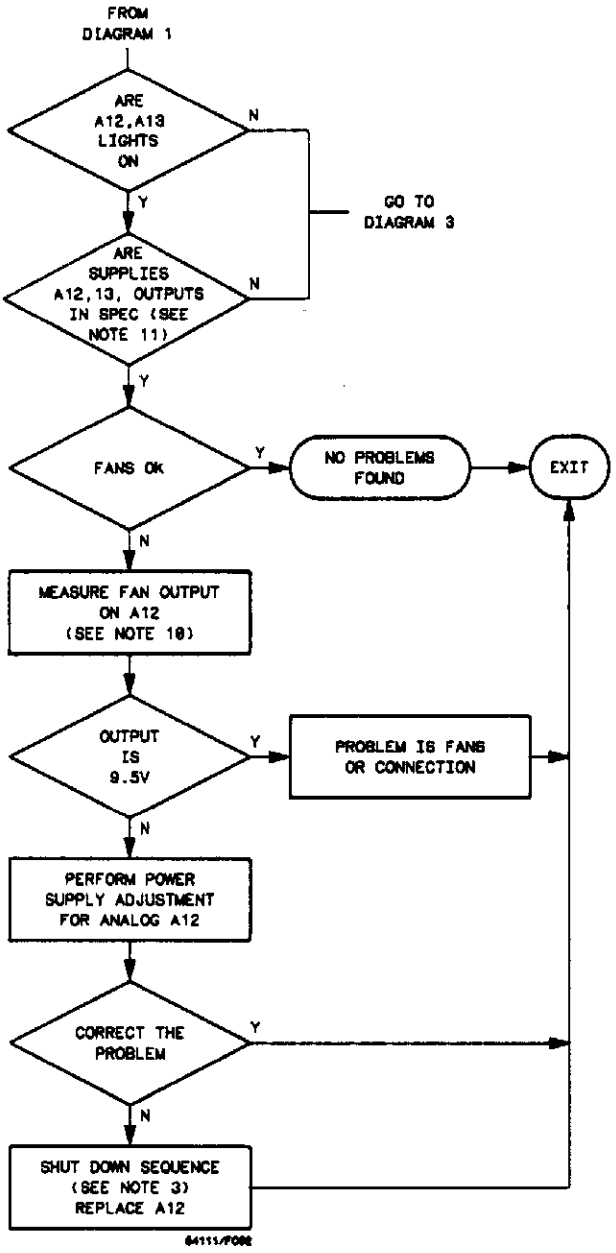
1) A. FRONT PANEL POWER SWITCH SHOULD BE IN STANDBY
   B. REAR PANEL LINE SWITCH SHOULD BE OFF "0"
   C. CONNECT AC POWER SOURCE
   D. TURN REAR PANEL LINE SWITCH TO ON "1"

2) A. TURN REAR PANEL LINE SWITCH TO OFF "0"
   B. ALWAYS UNPLUG AC POWER SOURCE
   C. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

WARNING
EXTREME CAUTION MUST BE TAKEN WHEN REMOVING POWER SUPPLY COVER.

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

Figure 6D-8. Power Supply Troubleshooting Flow Diagram 1.



A11 IS PRIMARY SUPPLY
A12 IS ANALOG SUPPLY
A13 IS DIGITAL SUPPLY

NOTES FOR FLOW DIAGRAM 2

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

10) CONNECT THE VOLTMETER (+) LEAD TO THE "FAN" TEST POINT AND THE (-) LEAD TO THE -18V TEST POINT. THE READING SHOULD BE 9.5V. THIS VOLTAGE WILL INCREASE WITH INCREASING AMBIENT TEMPERATURE. SEE THE POWER SUPPLY ADJUSTMENT PROCEDURE FOR THE ANALOG SUPPLY.

11) FOR POWER SUPPLY TEST POINTS AND SPECIFICATIONS SEE TABLE BELOW.

DIGITAL SUPPLY TST PTS (+) LEAD	(-) LEAD	VOLTAGE
+5V	GND	+5.10 ±0.1V
-5V	GND	-5.30 ±0.1V
+14B	GND	>+5V
ANALOG SUPPLY TST PTS (+) LEAD	**(-) LEAD**	**VOLTAGE**
+18V	GND	+18.5 ±0.3V
+8V	GND	+8.9 ±1V
-8V	GND	-8.5 ±1V
-18V	GND	-18.5 ±0.3V
FAN	-18V	+9.5 ±0.3V
+26B	GND	>+5V

Figure 6D-9. Power Supply Troubleshooting Flow Diagram 2.

NOTES FOR FLOW DIAGRAM 3

3) A. TURN FRONT PANEL SWITCH TO STANDBY
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

4) THE NOMINAL OUTPUT FOR +14B IS 21V. HOWEVER, WHEN THE SUPPLY IS OPERATING IN THE CURRENT LIMIT MODE, IT CAN BE AS LOW AS +5V. THE NOMINAL OUTPUT FOR +25B IS 26V. IT CAN ALSO BE AS LOW AS +5V WHEN IN CURRENT LIMIT

5) MEASURE OUTPUTS +5V AND -5V ON THE DIGITAL POWER SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES. IF OUTPUTS ARE GREATER THAN HALF THE ANSWER IS NO.

6) WHEN THE SUPPLIE(S) ARE RUNNING IN THE CURRENT MODE THIS MAY MEAN THAT AN EXTERNAL LOAD IS PULLING DOWN THE SUPPLY OUTPUT(S). AN EXTERNAL LOAD COULD BE A BOARD IN THE CARD CAGE OR THE COLOR DISPLAY ASSEMBLY (NOT THE COLOR CRT MODULE). THE ONLY WAY TO ISOLATE THE COLOR DISPLAY ASSEMBLY IS TO COMPLETELY REMOVE IT FROM THE MAINFRAME. THE FANS CAN ALSO PUT THE ANALOG BOARD INTO THE CURRENT MODE. YOU CAN DISCONNECT THE FANS BY REMOVING THE BOTTOM COVER AND DISCONNECTING THE FAN CABLE

   TO ISOLATE A CURRENT PROBLEM, FIRST DISCONNECT THE TEST SET. THEN REMOVE ONE LOAD AT A TIME UNTIL THE PROBLEM IS FOUND. PROBLEMS COULD INCLUDE BENT PINS ON THE MOTHERBOARD OR A BAD COMPONENT ON A PC ASSEMBLY. SEE THE ADJACENT TABLE FOR POWER DISTRIBUTION TO THE VARIOUS ASSEMBLIES

7) MEASURE OUTPUTS ±18V AND ±8V ON THE ANALOG SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES. IF OUTPUTS ARE GREATER THAN HALF THE ANSWER IS NO

8) THE TEST POINTS TO MEASURE +14.6V ARE AT THE BACK OF THE BOARD CLOSE TO THE TOP. CONNECT THE VOLTMETER COMMON LEAD TO THE COM TEST POINT ON THE BOARD. **CAUTION!!!** ***USE CAUTION WHEN MEASURING THIS VOLTAGE. IT IS NOT ISOLATED FROM THE LINE (MAINS) INPUT AND THE PRIMARY SUPPLY IS EXPOSED WITH THE POWER SUPPLY COVER REMOVED.***

9) BY REMOVING THE CONNECTORS AT J2 AND J3 YOU ARE CHECKING IF EITHER THE ANALOG OR DIGITAL SUPPLY IS LOADING VCNTL.

   EXTREME CAUTION MUST BE TAKEN WHEN MEASURING VCNTL ON THE PRIMARY SUPPLY. THE TOP PIN ON CONNECTORS J2 AND J3 IS VBULK WHICH IS +300V. THE PINS BELOW ARE VCNTL, THEN GROUND.

   TO MEASURE VCNTL, TURN THE POWER OFF AND MAKE SURE THE +300V LAMP (NEAR TOP OF BOARD) IS OFF. CONNECT THE VOLTMETER (+) LEAD TO VCNTL (SECOND PIN FROM TOP) AND THE (-) LEAD TO GROUND (BOTTOM PIN). APPLY POWER AND OBSERVE THE METER READING. WITH ONE SUPPLY CONNECTED THE READING SHOULD BE ABOUT +25V AND WITH NEITHER CONNECTED ABOUT +42V. TURN OFF POWER (+300V LAMP IS OFF) BEFORE REMOVING THE VOLTMETER LEADS

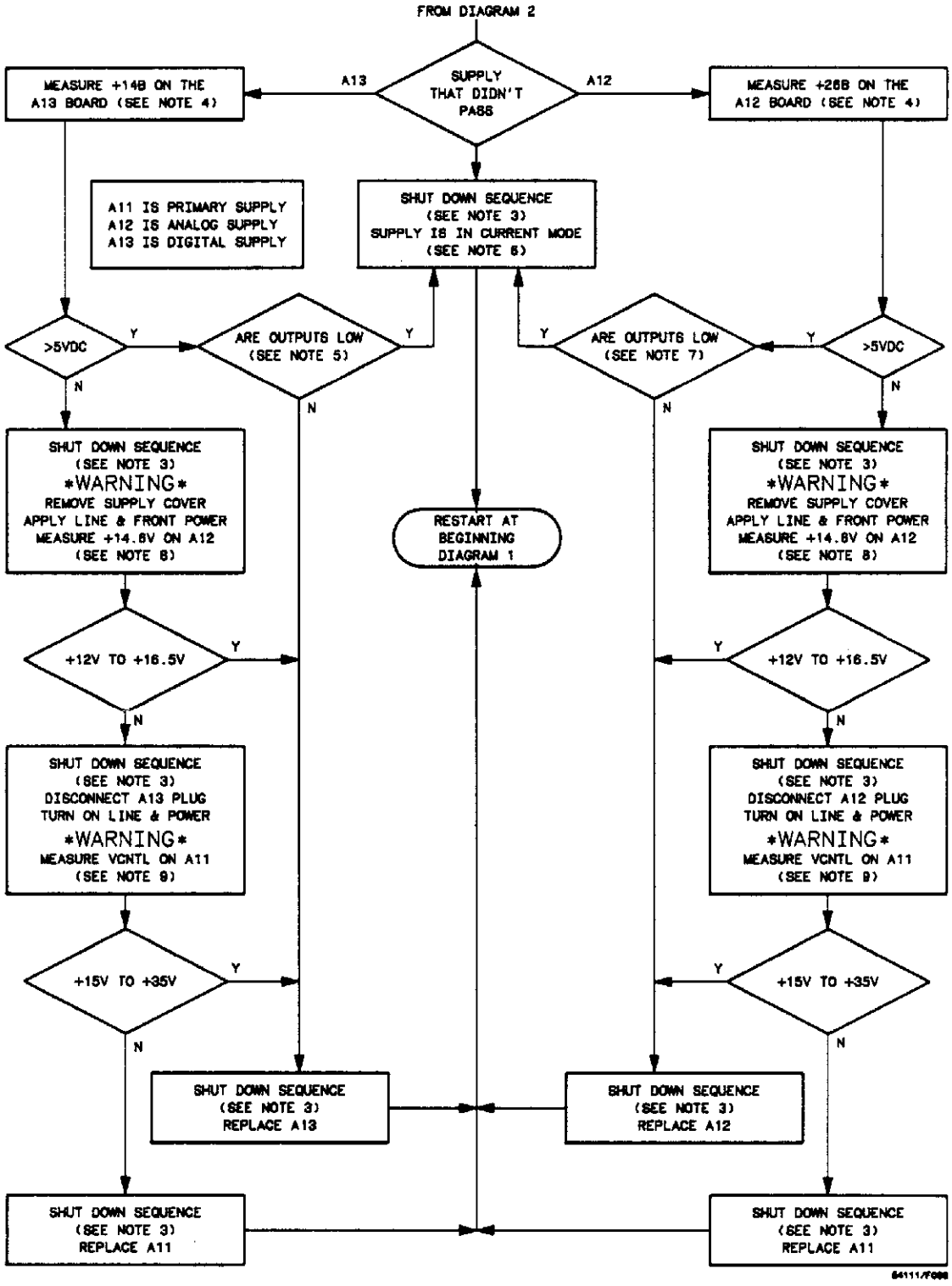


Figure 6D-10. Power Supply Troubleshooting Flow Diagram 3.

6D-13. DATA ACQUISITION TROUBLESHOOTING

Data acquisition troubleshooting involves three processes: preliminary investigation, internal diagnostic loop test evaluation, and extended service test evaluation.

Preliminary Investigation
Preliminary investigation involves three processes: determining which data acquisition assemblies are operating properly, making an informed decision on which assembly or assemblies might be causing the fault, checking some common failure mechanisms. To achieve these results loop test failures are compared against the assemblies which might cause the failure, loop failure patterns are compared against a known set of loop failure patterns, and the functional block diagram is used to decide the fault's probable location.

Internal Diagnostic Loop Test
Internal diagnostic loop tests evaluate why a particular loop failed. The preliminary investigation may indicate which loop to evaluate first; however, the lowest numbered loop is usually evaluated first. When evaluating loop failures, first decide why this loop failed and why others may have passed. This will often indicate the possible failing assembly. Second, use the loop failure status codes to indicate why this loop is failing. Third, probe specific interconnect points to verify which assembly is faulty.

Extended Service Test
Extended service tests execute routines which check if assemblies are supplying the correct signals to other assemblies. This may indicate why a loop failed and the probable faulty assembly. Executing all the extended service tests would take more time than an analysis of the internal individual diagnostic loop tests. There are two reasons for the extended service tests. First, for persons familiar with the oscilloscope it may be a troubleshooting short cut because they sometimes can predict which extended service test to execute for particular failure symptons. Second, internal diagnostic loop tests do not cover all instrument failures.

EVALUATING SAMPLER FAILURES

The test set contains gallium arsenide samplers and are very sensitive to electrostatic discharge (ESD) damage. Before analyzing other data acquisition failures, the extended service sampler test, paragraph 6D-21, should be run.

ANALYZING DATA ACQUISITION FAILURES

1. Analyze the functional block diagram and the simplified assembly interconnect diagram, figures 6D-11 and 6D-12, to determine which assemblies could cause the failure.

2. Analyze the failing loop tests and refer to tables 6D-6 and 6D-7 to determine which assembly might be failing.

3. Refer to the troubleshooting hints, paragraph 6D-15.

4. Eliminate working assemblies and eliminate assemblies that appear to fail but are failing because of a different problem.

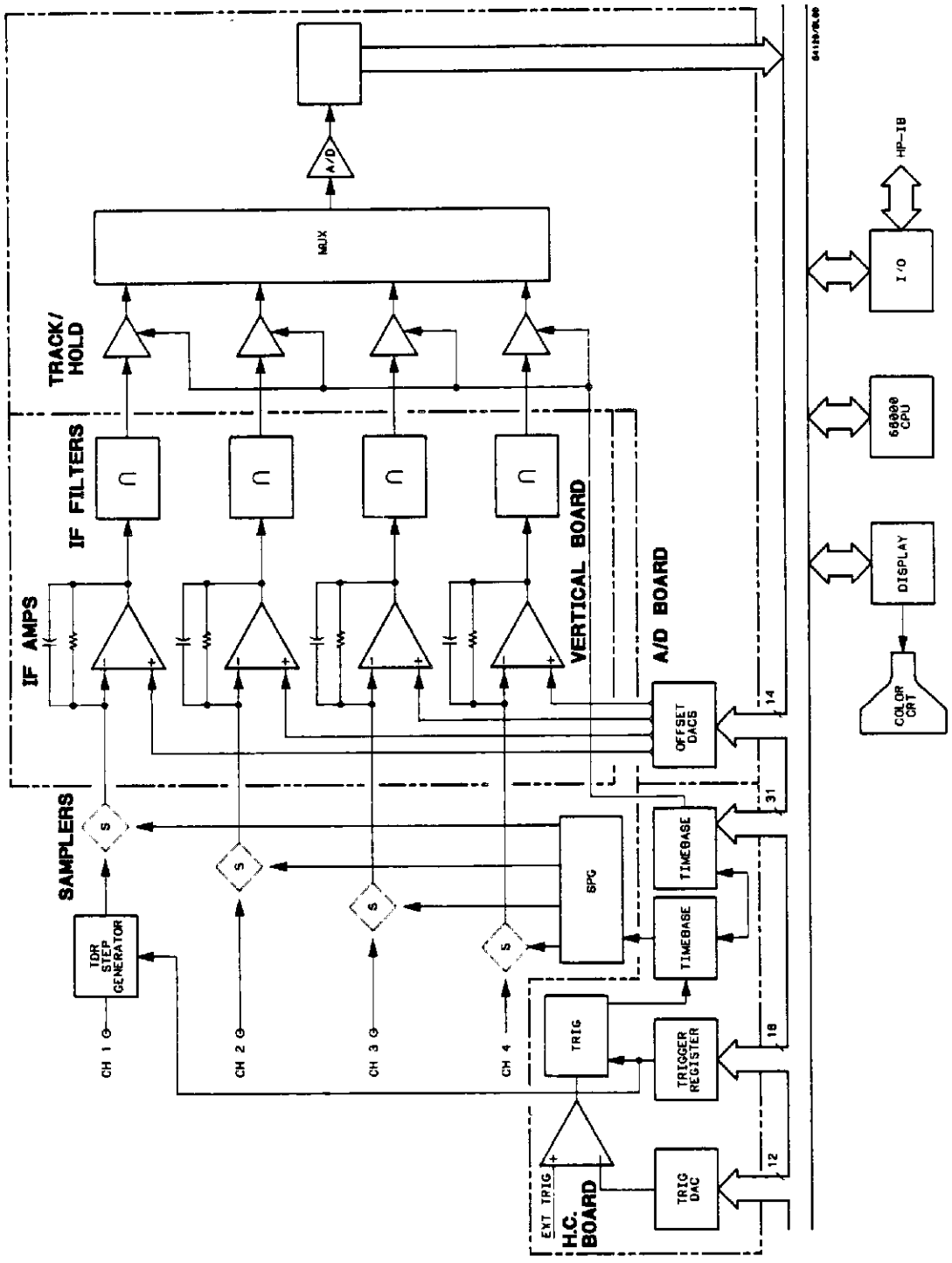


Figure 6D-11. HP 54120T Functional Block Diagram.

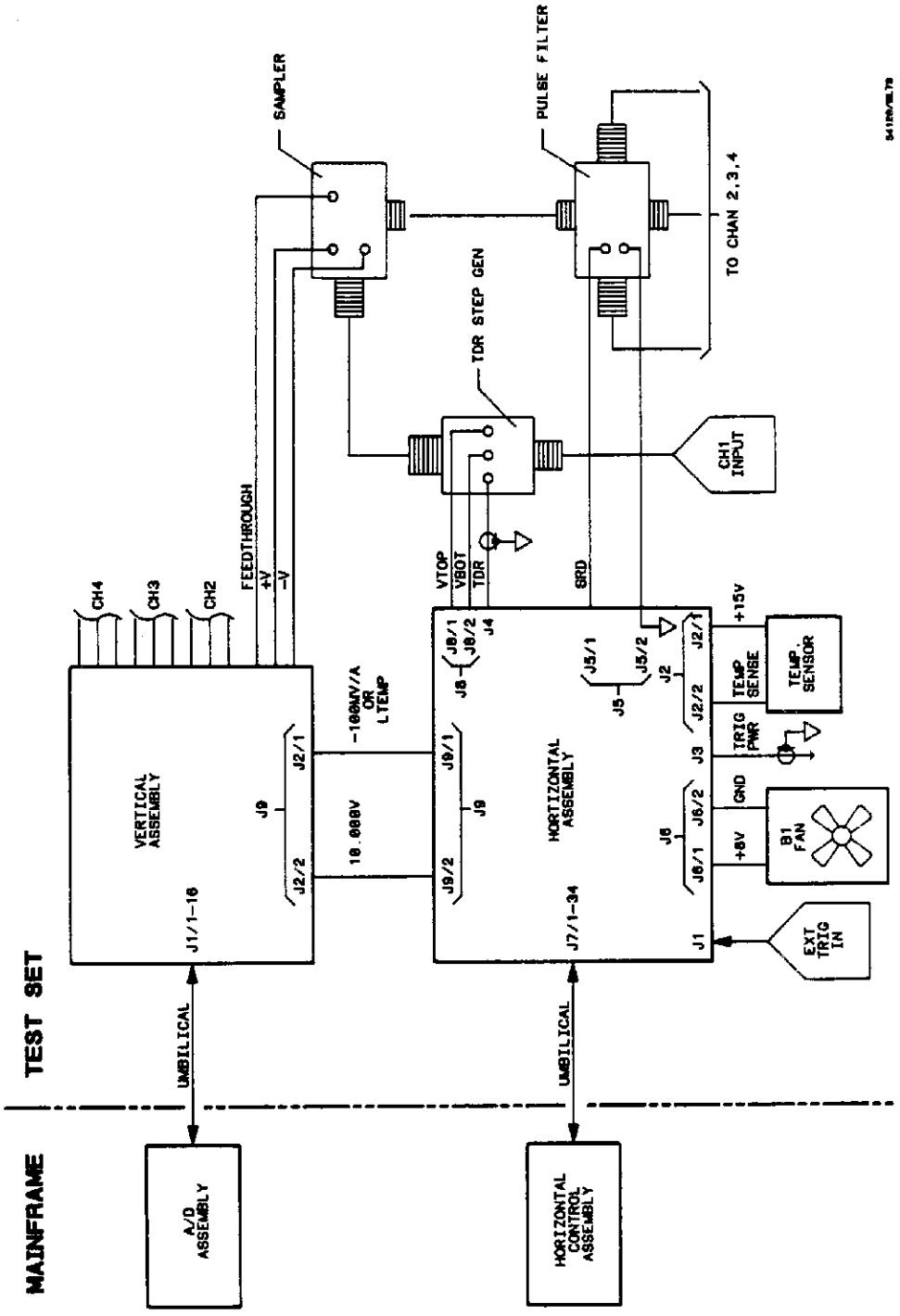


Figure 6D-12. Simplified Assembly Interconnect Diagram.

Table 6D-6. Which Assemblies are Tested By Various Loop Tests.

Assembly	Loop Number
TDR	39
A/D	16, 28-39
Horizontal control	17, 20, 22-30
Vertical	35-38
Horizontal	20, 22-29
Samplers	31-39
Pulse filter	31-39
Trigger hybrid	20, 21-38
Display	5-9, 41, 42
I/O	10-15, 43
CPU	0-4, 40
RPG	15

Table 6D-7. Adjustments That May Cause Loop Failures.

Loop No.	Adjustment
1-17	None
18-19	Loop not used
20	Hysteresis
21	None
22-25	Hysteresis (loop 24 - trigger offset also)
26	None
27-30	Hysteresis (loop 30 - offset gain also)
31-34	SRD Drive and Sampler Bias, Hysteresis
35	SRD Drive and Sampler Bias, Hysteresis, LB1, HB1
36	SRD Drive and Sampler Bias, Hysteresis, LB2, HB2
37	SRD Drive and Sampler Bias, Hysteresis, LB3, HB3
38	SRD Drive and Sampler Bias, Hysteresis, LB4, HB4
39	SRD Drive and Sampler Bias, V top and bottom
40-43	None

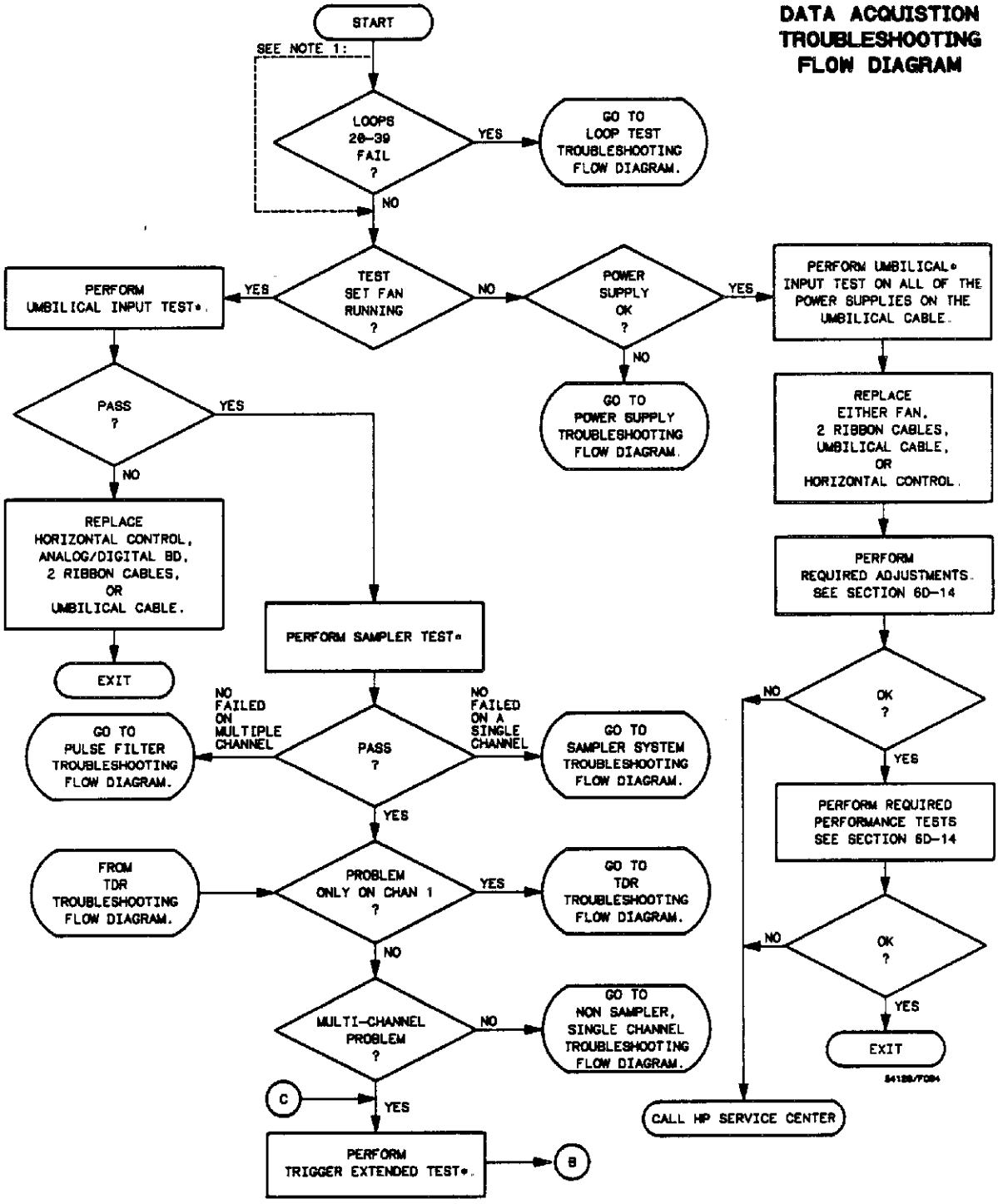


Figure 6D-13. Data Acquisition Troubleshooting Flow Diagram.

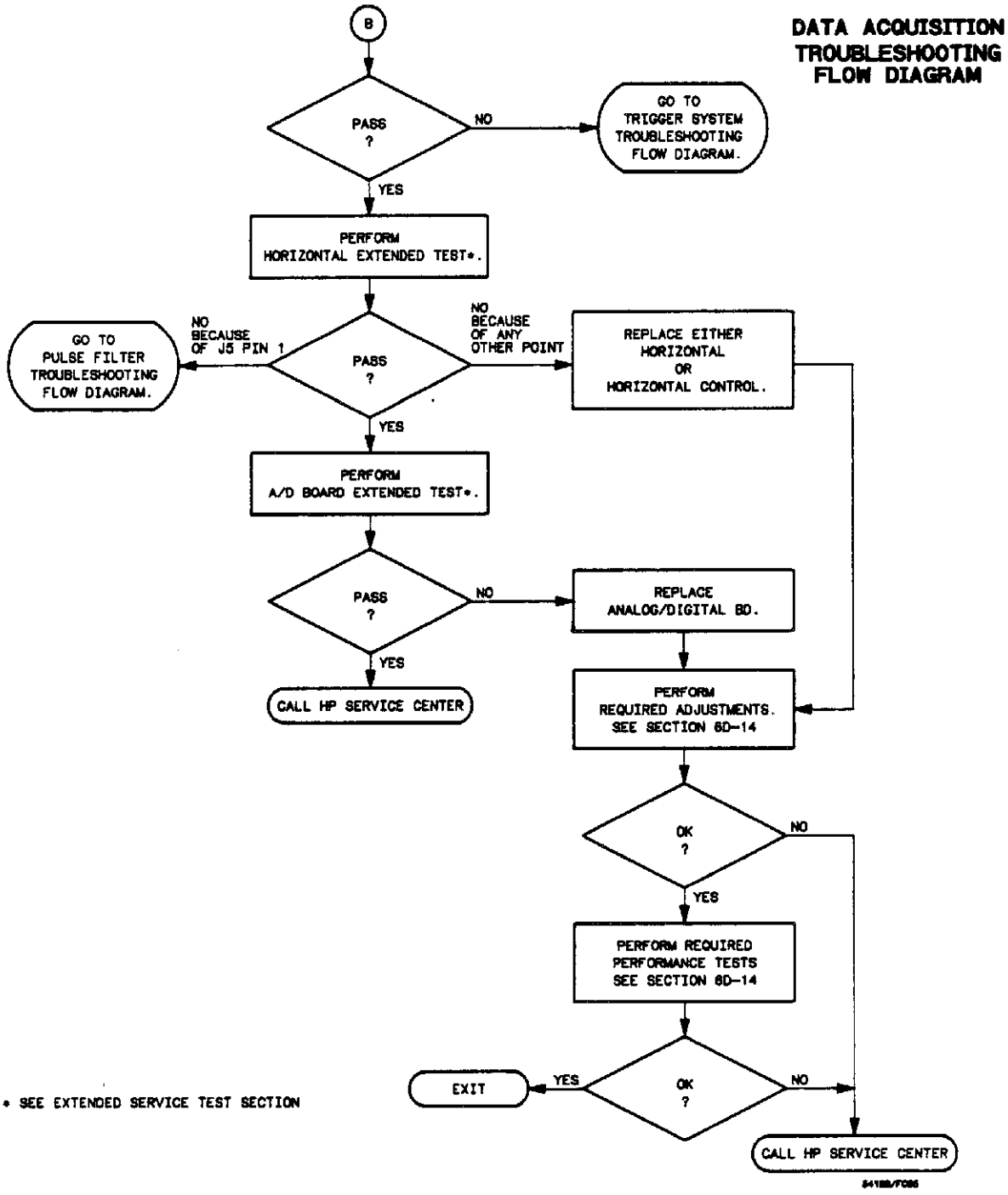


Figure 6D-14. Data Acquisition Troubleshooting Flow Diagram (continued).

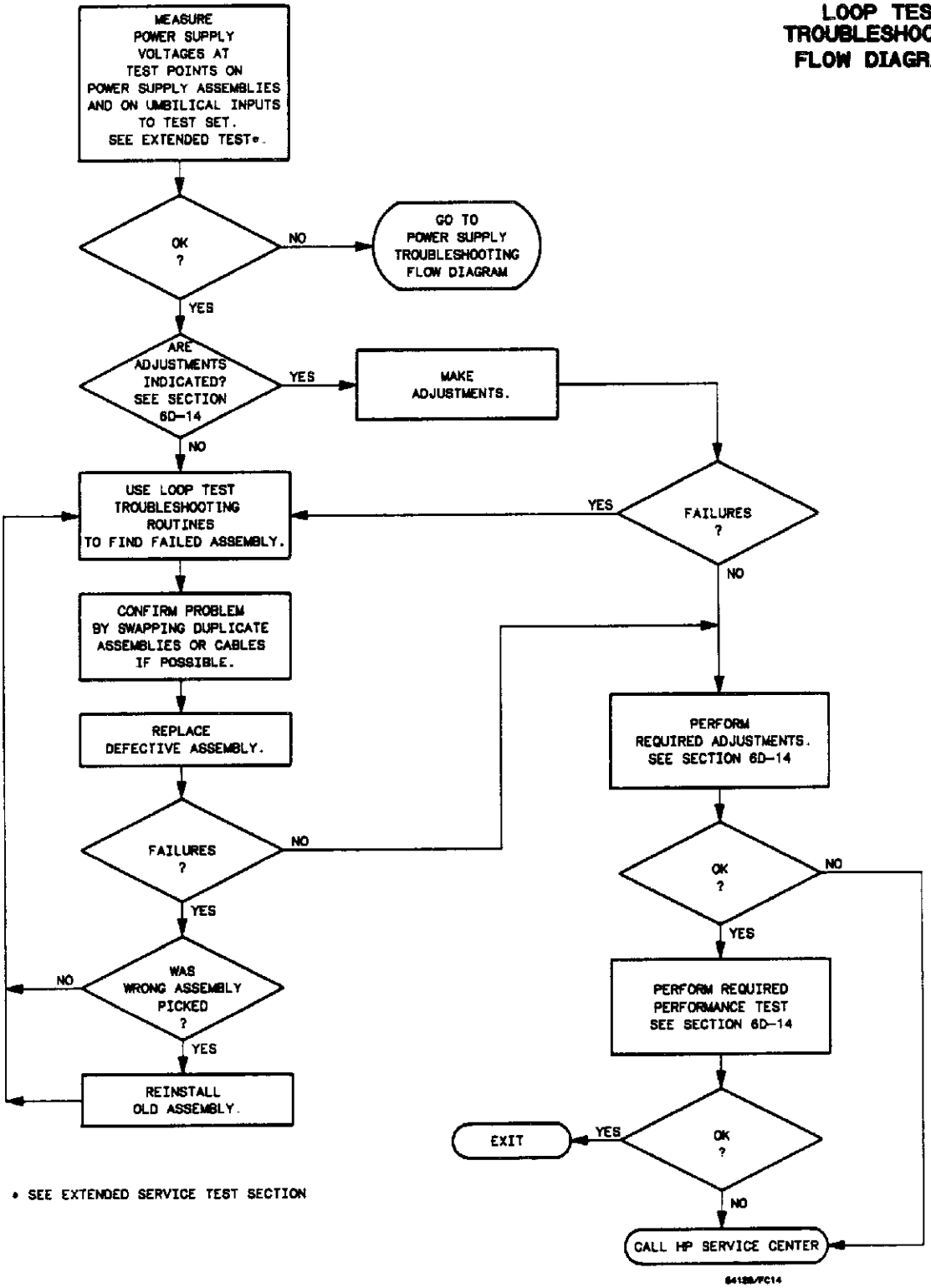


Figure 6D-15. Internal Diagnostic Subsystem Troubleshooting Flow Diagram.

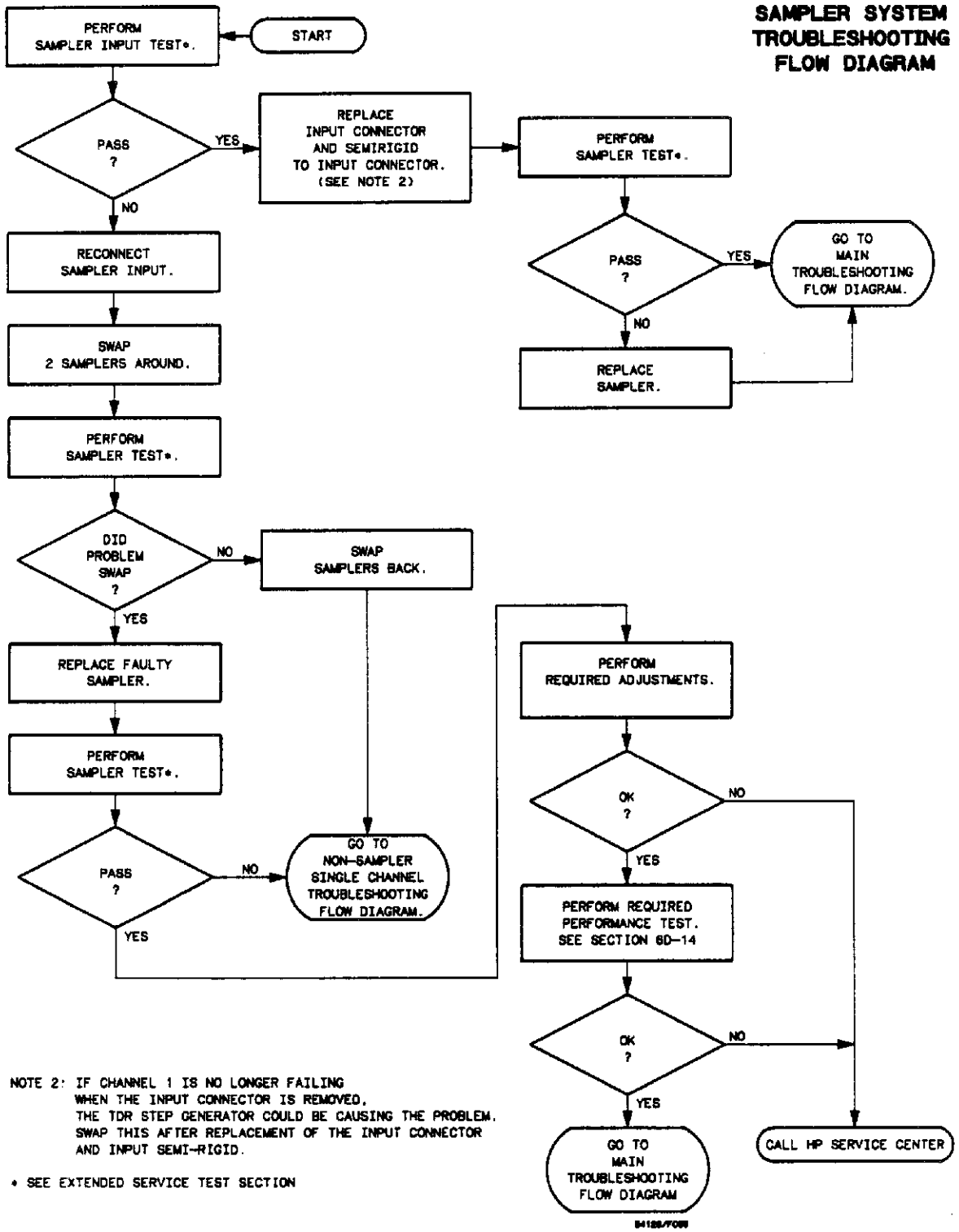


Figure 6D-16. Sampler System Troubleshooting Flow Diagram.

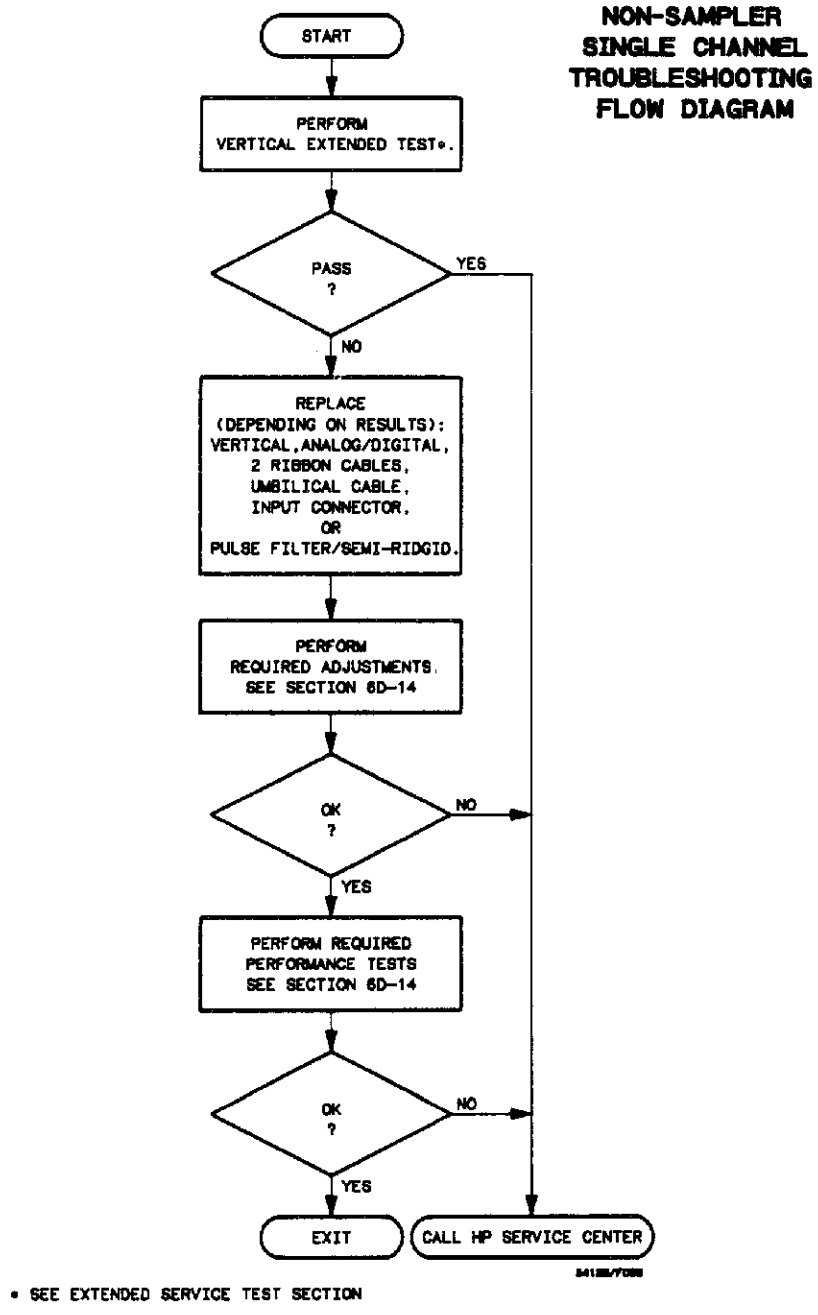


Figure 6D-17. Non-Sampler Single Channel Troubleshooting Flow Diagram.

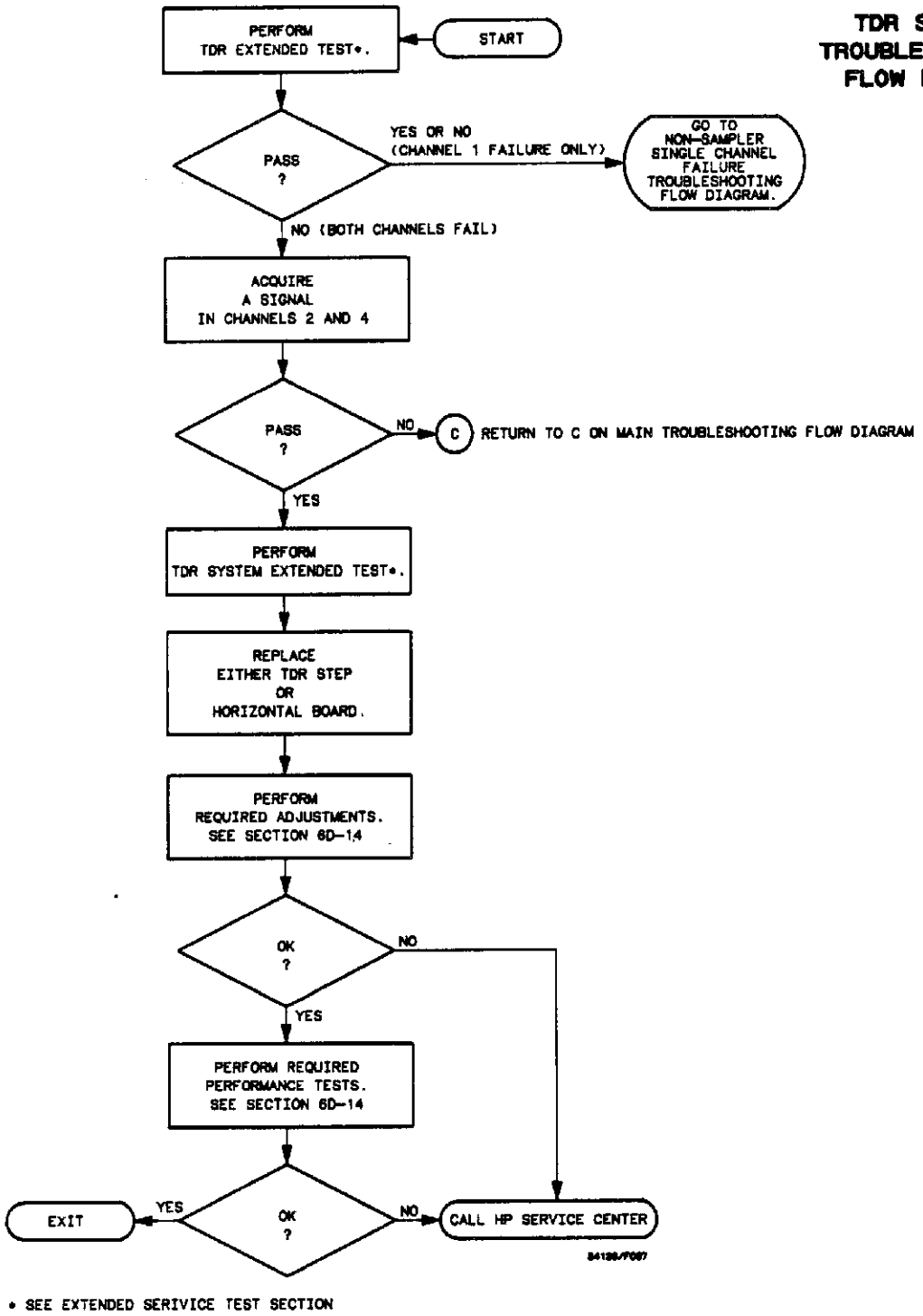


Figure 6D-18. TDR System Troubleshooting Flow Diagram.

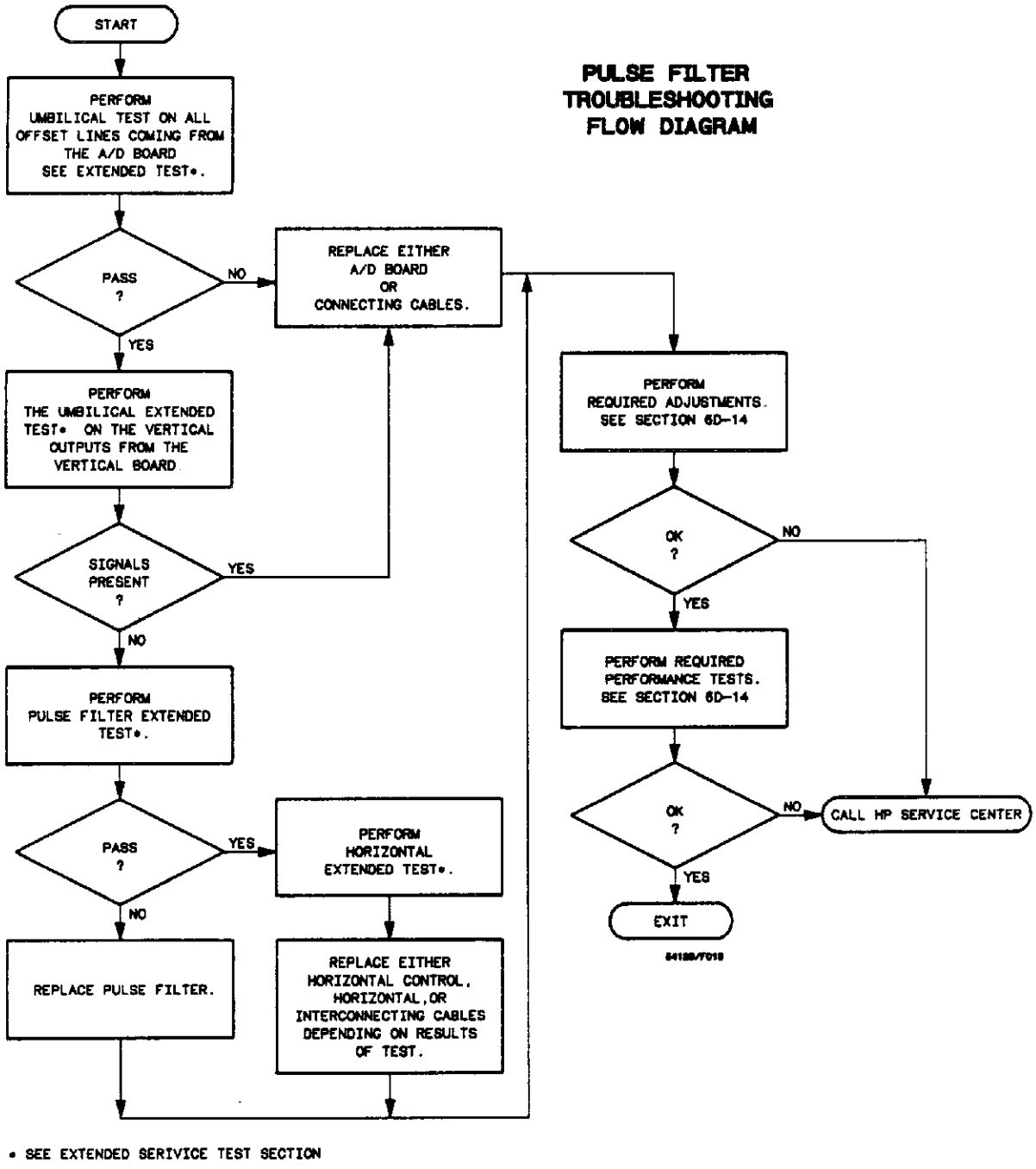


Figure 6D-19. Pulse Filter Troubleshooting Flow Diagram.

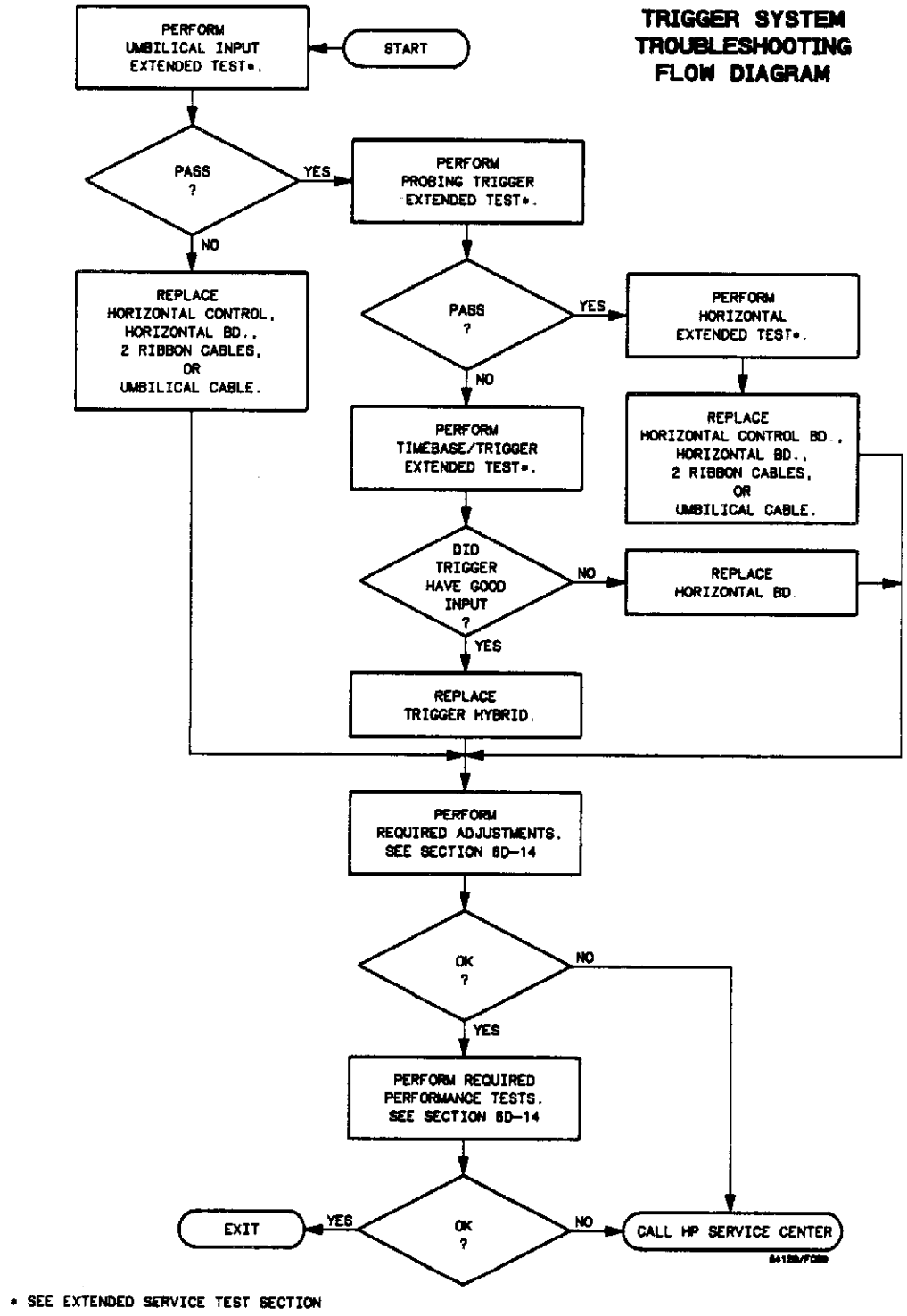


Figure 6D-20. Trigger System Troubleshooting Flow Diagram.

6D-14. AFTER THE HP 54120T IS REPAIRED

After the faulty assembly has been found, the following three tables should be used. Table 6D-8 cross references which adjustments to perform after replacing an assembly. Table 6D-9 cross references which performance tests to after performing adjustments. Table 6D-10 cross references which performance tests to perform after replacing an assembly.

Table 6D-8. Adjustments to Check after Replacing Assemblies.

Assembly Replaced	Adjustments that should be performed
A/D Assembly	10 V reference, Software calibration
Horizontal Control	Delta Current, Software calibration
Horizontal Assembly	All horizontal adjustments, vertical adjustments, software calibration
Vertical Assembly	LB1-4, HB1-4, OG1-4, RC1-4, CC1-4, Software calibration
Sampler	LB, HB, OG, RC, CC, and Softcal (only on channel where sampler was replaced)
TDR Step Generator	TDR Bias and Drive, V top and bottom, Software calibration
Pulse Filter	SRD Drive and Bias, Sampler Bias, Offset Gain, vertical software calibration
Display Assembly	No adjustments need to be performed.
I/O	Software calibration
CPU	Software calibration
Color CRT Assembly	No adjustments need to be performed.
Trigger Hybrid	Trigger hysteresis and offset null.

Table 6D-9. Performance Tests to Check after Adjustments.

Adjustment Made	Performance Test to Perform
Power supply	None
Delta current	Timebase accuracy
10 V reference	dc measurement accuracy
Range	Timebase accuracy
SRD	Bandwidth, dc measurement accuracy
Frequency,END, 4 ns cal	Timebase accuracy
Sampler Bias	Adjusted channel only: bandwidth, dc measurement accuracy
TDR	TDR
Feedthrough Compensation	Adjusted channel only: bandwidth, dc measurement accuracy
Trigger	Trigger sensitivity, jitter
Channel to channel skew	None
Vertical software cal.	None
Display	Color confidence test

Table 6D-10. Performance Tests to Check After Replacing Assemblies.

Assembly Replaced	Performance tests that should be performed
Vertical	Bandwidth, dc Measurement Accuracy, Input Reflection on channels only
A/D	Bandwidth, dc Voltage Measurement Accuracy.
Horizontal	Timebase Accuracy, Input Reflection on external trigger input only, Trigger Sensitivity, Jitter, TDR.
Horizontal Control	Timebase Accuracy
Sampler	Bandwidth, dc Voltage Measurement Accuracy, Input Reflection, Jitter (perform these tests on channel with replaced sampler).
TDR Step Generator	TDR
Pulse Filter	Jitter
Trigger Hybrid	Input Reflection on external trigger input only.
CPU	None
I/O	None
Display	Color Confidence Test
Color CRT Assembly	Color Confidence Test

6D-15. TROUBLESHOOTING HINTS.

The instrument is not triggering.

This could be caused by the trigger hybrid, timebase hybrid, A/D assembly, pulse filter, interconnecting ribbon cables, horizontal assembly, or horizontal control assembly.

The problem is vertical.

This could be caused by the sampler, vertical assembly, A/D assembly, or interconnecting cables.

The problem is horizontal.

This could be caused by the trigger hybrid, horizontal assembly, horizontal control assembly, or interconnecting cables.

The failure is on multiple channels.

If the oscilloscope is triggering and the horizontal is working, the problem could be the A/D assembly. If the oscilloscope is not triggering, the fault may be the trigger hybrid, horizontal assembly, horizontal control assembly, or interconnecting cables.

The failure is on a single channel.

This could be caused by the sampler, vertical assembly, A/D assembly, umbilical cable, pulse filter, or semi-rigid cables.

Failure is on channel 1 only.

In addition to the single channel failures listed above, possibly the TDR step generator.

TDR problem only, all other scope functions work properly.

This could be caused by the TDR step generator, horizontal assembly, horizontal control assembly, umbilical cable, and two ribbon cables which connect the umbilical cable to the vertical and horizontal assemblies.

There is an offset problem on only one channel.

Probably caused by the sampler hybrid. Other failures may be the A/D assembly, vertical assembly, umbilical cable, or interconnecting cables.

Table 6D-11. Loops Affected by Hardware Problems.

Hardware		Loop	Status lines
A to D converter on A/D assembly		28	STS 1 = -4
		29	
		30	
		31-34	STS 1 = -4, STS 3 = -4
		35-38	STS 1 = -6, STS 3 = -6
		39	STS 1 = -5, STS 4 = 0
A/D assembly output wrong bit pattern		28	STS 2 = read pattern
Offset DAC on A/D assembly	Chan 1	31,35	STS 1 = -4, -5, STS 3 = -4, -5
	Chan 2	32,36	STS 1 = -4, -5, STS 3 = -4, -5
	Chan 3	33,37	STS 1 = -4, -5, STS 3 = -4, -5
	Chan 4	34,38	STS 1 = -4, -5, STS 3 = -4, -5
Bandwidth bias		35-38	STS 1 = -5, STS 3 = -5
Samplers	Chan 1	31,35	
		39	STS 1 = -5, STS 4 = 0
	Chan 2	32,36	
	Chan 3	33,37	
	Chan 4	34,38	
SRD not generating a pulse		31-34	
		35-38	
		39	STS 1 = -5, STS 4 = 0
TDR pulse not getting to samplers		39	STS 1 = -5, STS 4 = 0
Timebase on horizontal or horizontal control assemblies		20	STS 1 = -2
		22	STS 1 = -3
		23	STS 1 = -3, STS 2 = -3
		24	STS 1 = -2
		25	STS 1 = -2, STS 2 = -2
		26	STS 1 = -3
		27	STS 1 = -2
		28	STS 1 = -2
		29	STS 1 = 8002H, STS 2-4 = 8002H
		30	STS 1 = 8002H
		31-39	STS 1 = -2
Freerun Clock Not being generated		26	STS 1 = -3
		39	STS 1 = -2

Table 6D-11. Loops Affected by Hardware Problems (continued).

Hardware	Loop	Status lines
Trigger Hybrid slope not changeable	20	STS 1 = -2
	23	STS 1 = -3 or STS 2 = -3
	25	STS 1 = -2 or STS 2 = -2
	27	STS 1 = -2
	28	STS 1 = -2
	29	STS 1 = 8002H, STS 2-4 = 8002H
	30	STS 1 = 8002H
	31-38	STS 1 = -2
Trigger level DAC level not changeable, on horizontal control assembly Or trigger hybrid not responding to changing trigger level	22	STS 1 = -3
	23	STS 1 = -3, STS 2 = -3
	24	STS 1 = -2
	27	STS 1 = -2
RPG cannot be reset	15	STS 1 = -1
Static RAM's	2	Chip problems
	40	Address line problem
Graphics RAM's	8	Chip problems
	41	Address line problem
I/O RAM's	11	Chip problems
	43	Address line problem
Priority RAM's	9	Chip problems
	42	Address line problem
Character RAM's	7	Chip problems

6D-16. REPAIRING TEMPERATURE FAILURES IN THE TEST SET.

The HP 54121A Four Channel Test Set contains two temperature compensation networks. The first is a temperature sensor attached to the test set's main deck and is used to vary some operating bias levels with changing instrument temperatures. The second is a temperature sensing network for keeping the timebase hybrid working consistently with changes in temperature.

When a temperature problem occurs in the test set, first verify that the fan is operating by visually checking to see if its blades are turning. If the fan seems inoperative, than measure between J6 pins 1 and 2 on the horizontal assembly. The voltage level should be approximately 8 V dc.

If the fan is operating, replace temperature sensor and cable W16 fastened to the test set's main deck. If temperature problems persist, then monitor U5 pins 6 and 13 on the horizontal control assembly while using a heat source and cool spray on the timebase hybrid (U9) on the horizontal assembly in the test set. U5 pin 6 should change -100 mV per degree C, and U5 pin 13 will change +100 mV per degree C.

Table 6D-12. Adjustment's Effect on Displayed Performance.

Several adjustments directly influence the performance of the waveform displayed on the screen. The following is a list of common symptoms which are caused by misadjustments. Many adjustments interact with other adjustments and should not be varied without first referring to the description of each adjustment.

Symptom	**Adjustment to check**
Unstable out of specification timebase measurements	Range
Stable out of specification timebase measurements	Frequency
Discontinuites on sine waves > 250 MHz	END and 4 ns cal
TDR levels not 0 V and 200 mV	TDR top and bottom
TDR overshoot not between 2.5% and 3.5%	TDR bias and drive
TDR pulse response not flat	TDR bias and drive
Channel to channel skew off	Timebase software calibration
Gain difference between the 12.4 GHz and 20 GHz or between persistence and average modes	Vertical software calibration
Minimum trigger sensitivity >1 division	Trigger
Trigger offset problems	Trigger
Not triggering at center screen (remember there is always 16 ns minimum delay)	Trigger
Faulty color purity	Color monitor
Faulty contrast or brightness	Front panel display controls
Faulty low frequency square wave response	Feedthrough compensation
Faulty gain tracking between 12.4 GHz and 20 GHz bandwidth modes	Sampler bias
Loops 31-38 failing	Sampler bias
Faulty gain on all channels or loops 31-38 failing	SRD
Faulty performance when swapping test sets	10 V reference and delta current

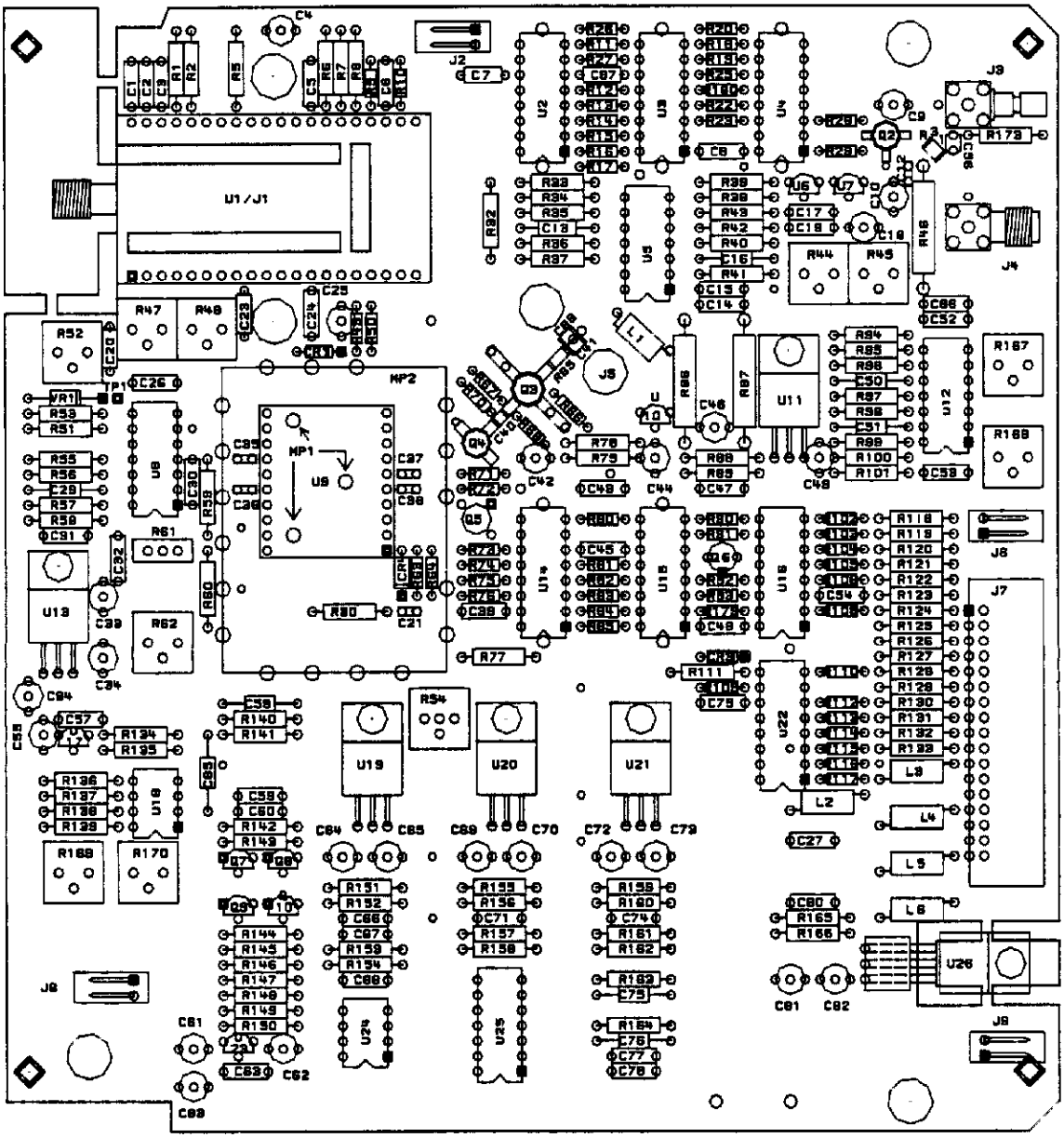


Figure 6D-22. Horizontal Assembly Component Locations.

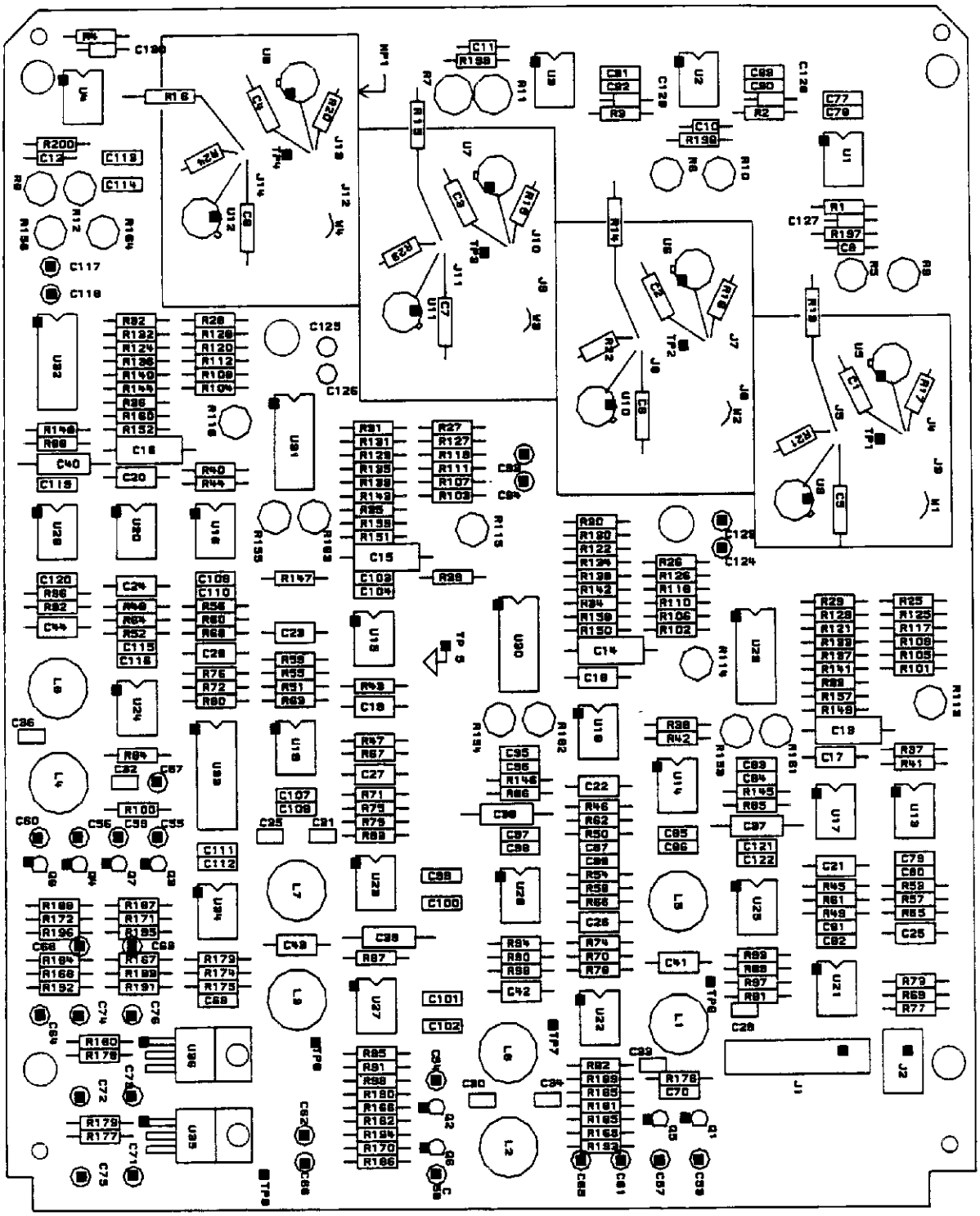


Figure 6D-23. Vertical Assembly Component Locations.

6D-17. INTERNAL DIAGNOSTIC LOOP TESTS

The HP 54120T contains 44 (0-43) internal diagnostic loop tests. When these loop tests pass, the instrument is considered functionally operational to a 90% confidence level. The loop tests are also a major troubleshooting tool for the instrument.

To run the loop tests follow these five steps.

1. Perform a one key-down powerup and remove the SMA short from channel 1 (if one is installed).

2. Press the ***More*** menu key, ***Utility*** menu key, and ***Test Menu*** key, and ***Extended Tests*** key.
   Press *1* and *2* keys, and press the ***Enter*** key.
   Press ***Start Test*** key.

3. The instrument will run loops 0-43 executing each loop once whether they pass or fail.

4. Wait a few seconds until the oscilloscope displays graticules on the screen.

5. Press the ***More*** menu key, ***Utility*** menu key, and ***Test Menu*** key.
   Press ***Display Errors*** key. The failing loops will be displayed on the screen.

REPEAT LOOP. Selecting this mode continuously executes the Loop number entered at RUN FROM LOOP. Pressing ***Start Test*** will start execution and the loop will continuously run until the ***Stop Test*** key is pressed. Pressing ***Display Errors*** will show how many times the loop was executed and the number of times the loop failed.

There are a number of loops that will blank or over-write the Stop Test key display on the CRT. However, the test can still be terminated by pressing the third function key from the top.

RUN FROM LOOP. Selecting this mode starts execution from the loop entered and will proceed to execute all higher numbered loops. Upon reaching the last test, the cycle will be repeated.

If any test should fail, the instrument will change from RUN FROM LOOP to REPEAT LOOP and will repeatedly execute the loop that failed until the ***Stop Test*** key is pressed.

6D-18. TROUBLESHOOTING TEST LOOP CONSIDERATIONS

Troubleshoot the lowest loop numbers first. Higher loop numbers are usually dependent on lower loops numbers passing. Table 6D-14 cross references which assemblies are tested by which loops.

Some loops may fail if the adjustments are misadjusted. Before replacing costly assemblies refer to table 6D-13 to find out if any adjustments are causing loop failures.

The powerup self test routine includes only loops 0-17.

Before analog loops 20-39 are executed, loops 16 and 17 must pass. Loops 20-39 also require a trigger pulse for the samplers and A/D. There are three ways to generate this trigger.

1. FR - Freerun clock
2. SL - switching the trigger slope, this toggles the trigger slope line to the trigger comparator
3. TL - Changing the trigger level, this changes the trigger level DAC's output.

Table 6D-15 describes which of these trigger generation methods is used for each of the loop tests.

If the SMA short is not removed from channel 1's input connector, loop 39 will fail and display a caution message on the screen.

Loops 20-24 test the oscilloscope's triggering capability. For these loops to pass, the following must be operating: horizontal control assembly, umbilical cable, ribbon cables connecting umbilical cable to horizontal and vertical assemblies, trigger hybrid, trigger input, and horizontal assembly. The vertical assembly, A/D assembly, samplers, pulse filter, and vertical input circuitry are not checked by these loops.

Loops 25-26 test the oscilloscope's horizontal assembly. Loops 20-24 must pass before loops 25-26 will pass. The circuitry tested and not tested for loops 25-26 are the same as loops 20-24.

Loop 27 tests the operation of HF reject and trigger sensitivity. For this loop to pass, loops 20-26 must pass. The circuitry tested and not tested in loop 27 are the same as loops 20-24.

Loops 28-30 test the vertical signal path with signals at ground levels. This requires that all the data acquisition modules are functional. If loops 20-27 pass, then the failure of loops 28-30 usually indicates the failure is in the vertical signal path: sampler, vertical assembly, A/D assembly. Loop 28 also checks the A/D assembly timing between channels during the A to D conversion.

Loops 31-38 test the data acquisition system's ability to acquire data. It tests the samplers, vertical assembly, and A/D assembly.

Loop 39 tests the TDR step's high and low levels. This loop requires all the data acquisition loops to pass. If only this loop fails, it probably indicates a failure in the TDR step generator system, horizontal assembly's TDR bias circuitry, or possibly a problem in channel 1.

Table 6D-13. Adjustments That May Cause Loop Failures.

Loop No.	Adjustment
1-17	None
18-19	Loop not used
20	Hysteresis
21	None
22-25	Hysteresis (loop 24 - trigger offset also)
26	None
27-30	Hysteresis (loop 30 - offset gain also)
31-34	SRD Drive and Sampler Bias, Hysteresis
35	SRD Drive and Sampler Bias, Hysteresis, LB1, HB1
36	SRD Drive and Sampler Bias, Hysteresis, LB2, HB2
37	SRD Drive and Sampler Bias, Hysteresis, LB3, HB3
38	SRD Drive and Sampler Bias, Hysteresis, LB4, HB4
39	SRD Drive and Sampler Bias, V top and bottom
40-43	None

Table 6D-14. Which Assemblies are Tested by Which Loop Tests.

Assembly	Loop Number
TDR	39
A/D	16, 28-39
Horizontal control	17, 20, 22-39
Vertical	31-39
Horizontal	20, 22-39
Samplers	31-39
Pulse filter	31-39
Trigger hybrid	21-39
Display	5-9, 41, 42
I/O	0-43, especially 10-15, 43
CPU	0-43, especially 0-4, 40
RPG	15

Table 6D-15. Loop Descriptions.

Loop No.	Loop Name	Trigger Source
0	Bus error check	N/A
1	ROM checksum	N/A
2	Static RAM R/W	N/A
3	N/A	N/A
4	CTC (counter timer chip)	N/A
5	Display assembly ID	N/A
6	CRTC (CRT controller)	N/A
7	Character RAM R/W	N/A
8	Graphics RAM R/W	N/A
9	Priority RAM R/W	N/A
10	I/O assembly ID	N/A
11	I/O RAM R/W	N/A
12	HP-IB chip	N/A
13	Keyboard controller chip	N/A
14	Power detect circuitry	N/A
15	RPG counter reset	N/A
16	A/D assembly ID	N/A
17	Horizontal control assembly ID	N/A
18	N/A	N/A
19	N/A	N/A
20	Data Acquisition (1)	SL
21	Trigger off/freerun off	N/A
22	Trigger level (1)	TL
23	Pos/Neg slope	TL
24	Trigger level (2)	TL
25	Coarse delay counters	SL
26	Rate generator/multi sample period	FR
27	Hysteresis band off	TL
28	A/D	SL
29	Feedthrough compensation	SL
30	Data acquisition (2)	SL
31	Channel 1 check	SL
32	Channel 2 check	SL
33	Channel 3 check	SL
34	Channel 4 check	SL
35	Channel 1 sampler gain	SL
36	Channel 2 sampler gain	SL
37	Channel 3 sampler gain	SL
38	Channel 4 sampler gain	SL
39	TDR	FR
40	Static RAM addressing test	N/A
41	Graphics RAM addressing test	N/A
42	Priority RAM addressing test	N/A
43	I/O RAM addressing test	N/A

LOOP 20 DATA ACQUISITION

This loop tests if the GO bit can be reset. This is done by toggling the trigger slope bit to create triggers which toggles the GO bit. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the time in μs between trigger and the GO bit.
-1 GO bit turns true while the trigger and freerun was off.
-2 GO bit never turns true.

The following initial setup is used for the majority of the loops.
Initial setup - Trigger disabled, freerun off, samplers off, HF reject off,
coarse delay = 1 (16 ns), fine delay = 0, trigger level = 1V,
trigger slope = pos, hysteresis = 0 (max), TDR = off, freerun rate = 500 KHz,
channel 1 on, channels 2-4 off, bandwidth bias = 12.4 GHz (low),
all channel offset levels set to 0 V.

Troubleshooting Procedure

Use an oscilloscope to probe the points in figures 6D-24 through 6D-28. on the horizontal assembly.

If U1 pin 35 is bad, suspect one of the following: horizontal control assembly, umbilical cable, ribbon cables. Go to the extended service section and perform the umbilical cable test to determine the faulty module.

If U1 pin 19 is bad, go to the extended service section and perform the umbilical cable test. If umbilical cable test passes, then perform timebase/trigger test and replace either the trigger hybrid or the horizontal assembly as indicated by the test results. If the umbilical cable test fails, use the following test to determine the faulty module.

Perform umbilical cable extended service test on the trigger level input line only. If this test fails, use the umbilical test to determine the faulty module.

If the trigger hybrid's output is bad, probe the following trigger hybrid input pins on the horizontal assembly.

Location	Signal	Signal Name
U1 pin 3	2.8 V	Trigger level
U1 pin 33	-.8 V	High frequency reject
U1 pin 32	-.8 V	Sensitivity
U1 pin 22	See figure 6D-28	Enable/disable
U1 pin 24	-.6 V	Freerun on/off
U1 pin 35	See figure 6D-28	Trigger slope

If the trigger hybrid inputs are good, replace the trigger hybrid; otherwise replace the horizontal assembly.

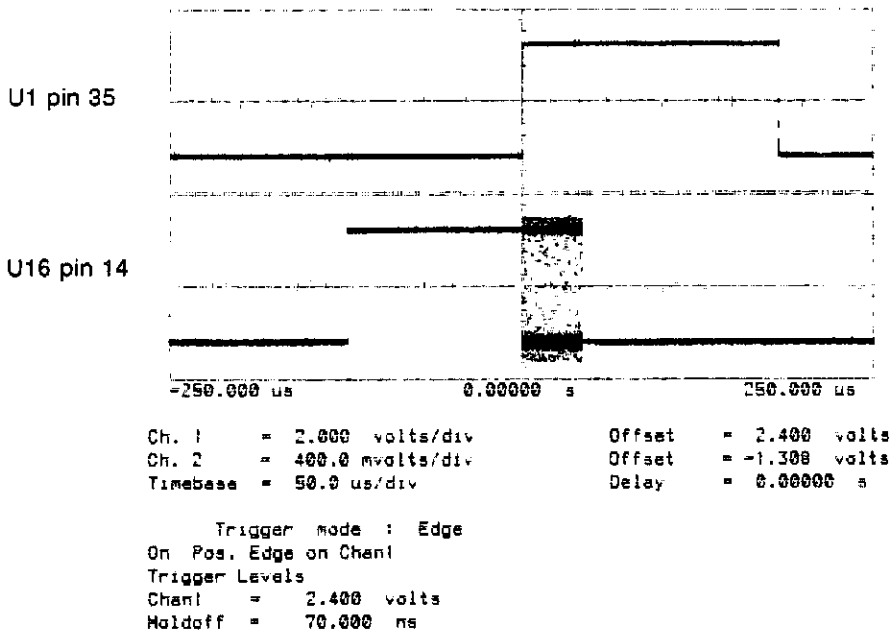


Figure 6D-24. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly.

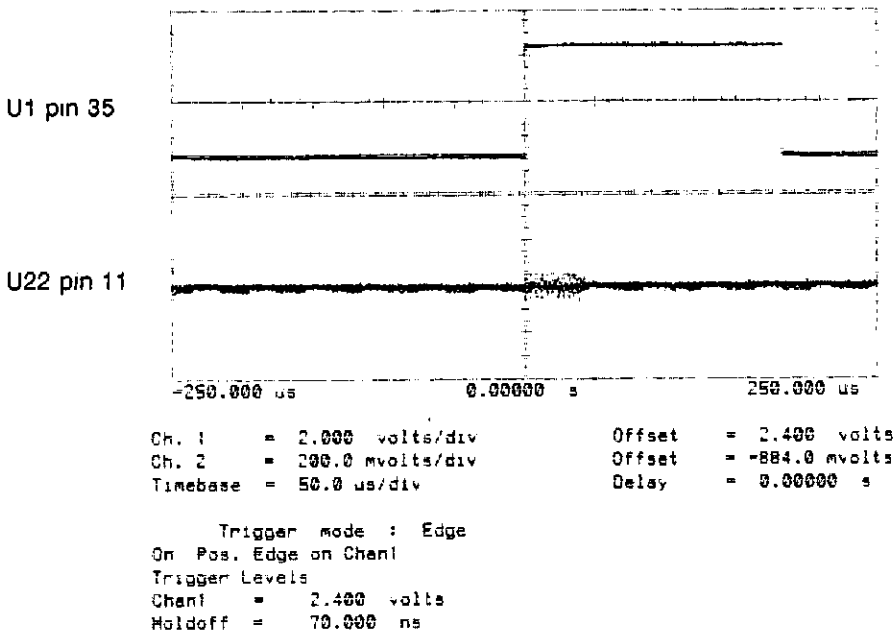


Figure 6D-25. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly.

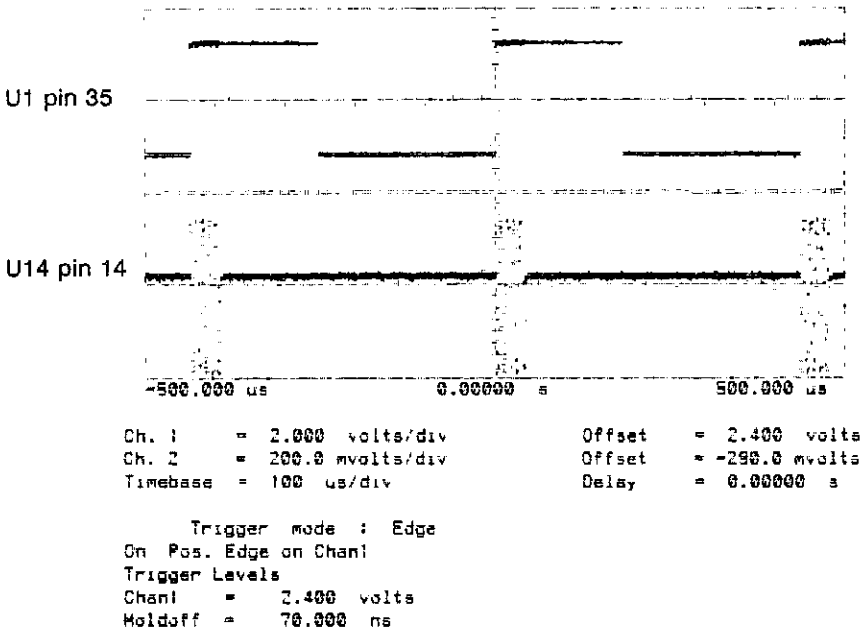


Figure 6D-26. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly.

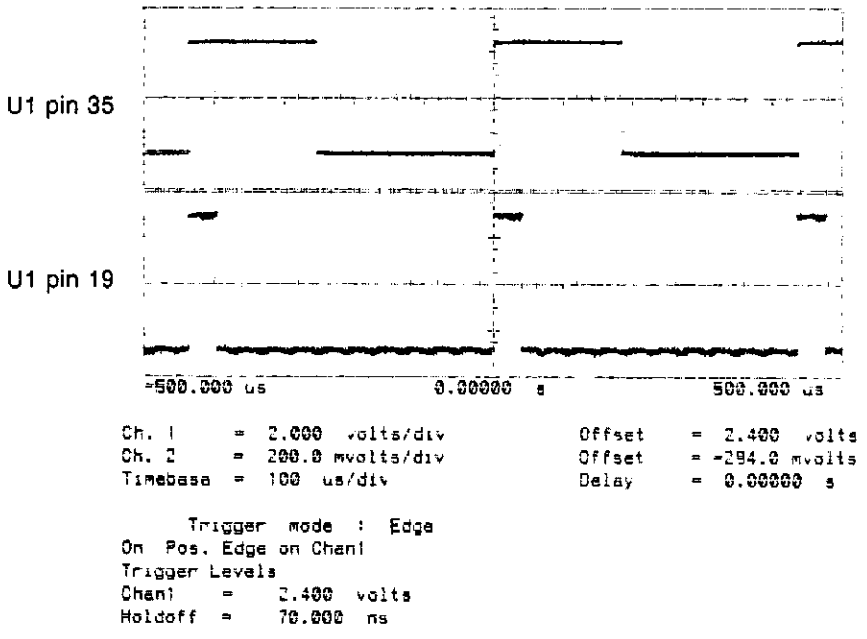


Figure 6D-27. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly.

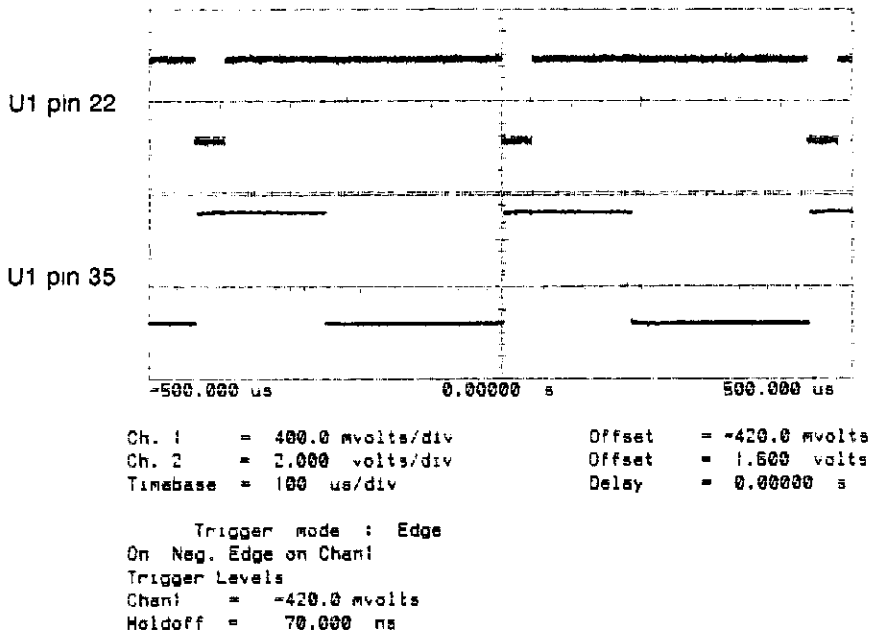


Figure 6D-28. Test Loop 20 Troubleshooting Waveform on the Horizontal Assembly.

LOOP 21 TRIGGER OFF/FREERUN OFF

This loop tests triggers are not generated when either the trigger is disabled and freerun is enabled, or when trigger is enabled and freerun is disabled. If any lower numbered loops fail, troubleshoot them first.

If this loop passes, status lines 1 and 2 should contain zero.

-1 in status line 1 indicates the GO bit turned true while the trigger was disabled and freerun was enabled. There should not be a trigger pulse in this case.

-2 in status line 2 indicates the GO bit turned true while the trigger hybrid was enabled and freerun was disabled. This would mean freerun cannot be turned off.

Initial setup - Identical to loop 20.

Troubleshooting Procedure

Use an oscilloscope to probe the following trigger hybrid inputs from the horizontal control assembly.

Location	Signal	Signal Name
U1 pin 3	2.8 V	Trigger level
U1 pin 33	-.8 V	High frequency reject
U1 pin 32	-.8 V	Sensitivity
U1 pin 22	See figure 6D-29	Enable/disable
U1 pin 24	-.6 V	Freerun on/off
U1 pin 35	0 V	Trigger slope

If any of these signals are bad, perform the extended service umbilical cable test on trigger level input line only. This will determine if the test set is receiving the correct signals from the horizontal control assembly.

Probe U1 pin 19, refer to figure 6D-29. If this signal is bad, replace the trigger hybrid.

U1 pin 19

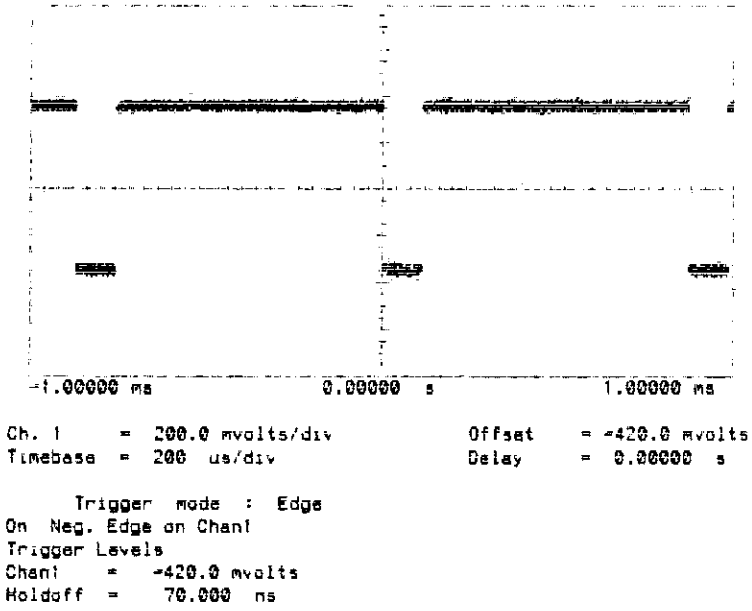


Figure 6D-29. Test Loop 21 Troubleshooting Waveform on the Horizontal Assembly.

LOOP 22 TRIGGER LEVEL (1)

This loop tests if the trigger level can be changed. This is done by toggling the trigger level from +1 V to -1 V and back to +1 V (slope is not important). The trigger is enabled before the level is changed to -1 V which should allow the instrument to trigger. If any loops below 22 fail, troubleshoot them first.

Status line 1 indicates if the instrument triggered.

0 The loop passed.
-1 GO bit turned true while trigger and freerun were disabled.
-2 GO bit turned true without changing the trigger level.
-3 GO bit never turned true when the trigger level changed.

Initial setup - Identical to loop 20.

Troubleshooting Procedure

Perform extended service umbilical cable test on trigger level input line only.

If the umbilical cable test passes, perform the timebase/trigger test.
If the trigger hybrid's output is bad, probe the following points on the horizontal assembly.

Location	Signal	Signal Name
U1 pin 3	See figure 6D-30	Trigger level
U1 pin 33	-.8 V	High frequency reject
U1 pin 32	-.8 V	Sensitivity
U1 pin 22	See figure 6D-30	Enable/disable
U1 pin 24	-.6 V	Freerun on/off
U1 pin 35	0 V	Trigger slope

If the inputs to the trigger hybrid are good, replace the trigger hybrid; otherwise replace the horizontal assembly.

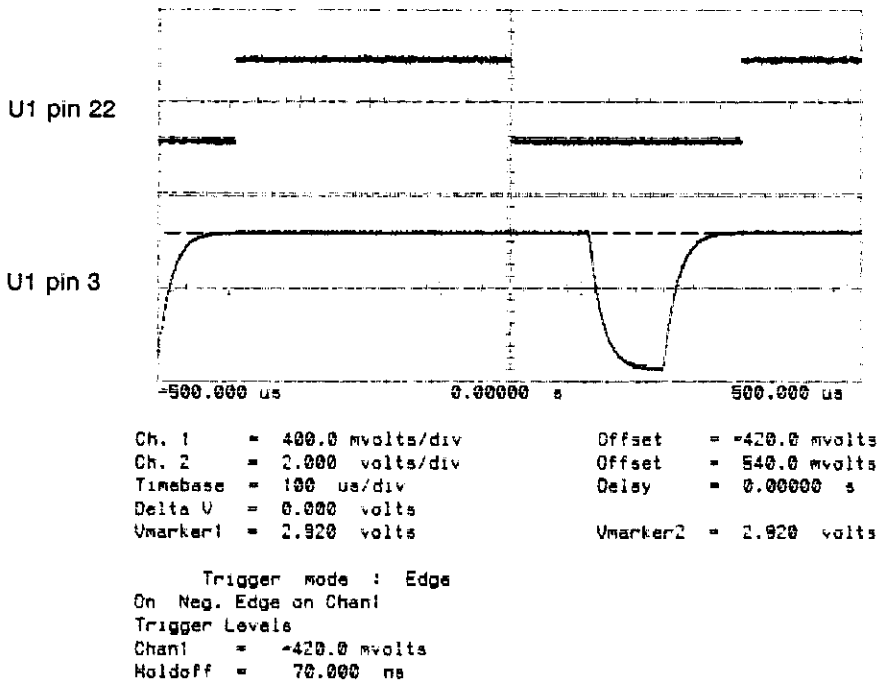


Figure 6D-30. Test Loop 22 Troubleshooting Waveform on the Horizontal Assembly.

LOOP 23 POS/NEG SLOPE

This loop tests that triggers are generated by toggling the Pos/Neg slope line when trigger is enabled and trigger level is toggled. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the following

- 0 Positive level triggering works properly.
- -1 GO bit turned true while trigger was disabled, freerun was off, and slope was positive.
- -2 GO bit turned true before the trigger level was toggled from +1V to -1 V.
- -3 GO bit never turned true by toggling the trigger level from +1 V to -1 V. (slope cannot be set positive)

Status line 2 indicates the following

- 0 Positive level triggering works properly.
- -1 GO bit turned true while trigger was disabled, freerun was off, and slope was negative.
- -2 GO bit turned true before the trigger level was toggled from -1 V to +1V.
- -3 GO bit never turned true by toggling the trigger level from -1 V to +1 V. (slope cannot be set to negative)

Initial setup - Identical to loop 20.

Troubleshooting Procedure

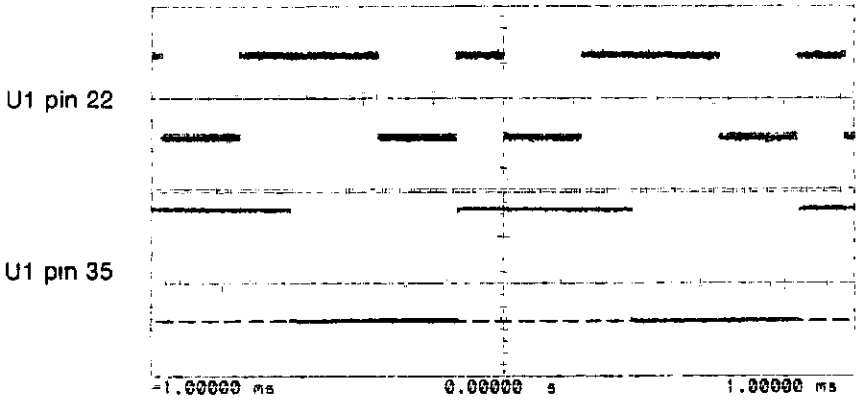
Perform the input umbilical cable extended service test on the trigger slope line.

If the umbilical cable test passes, perform the timebase/trigger test.

If the trigger hybrid's output is bad, probe the following points on the horizontal assembly.

Location	Signal	Signal Name
U1 pin 3	See figure 6D-32	Trigger level
U1 pin 33	-.8 V	High frequency reject
U1 pin 32	-.8 V	Sensitivity
U1 pin 22	See figures 6D-31 and 6D-32	Enable/disable
U1 pin 24	-.6 V	Freerun on/off
U1 pin 35	See figure 6D-31	Trigger slope

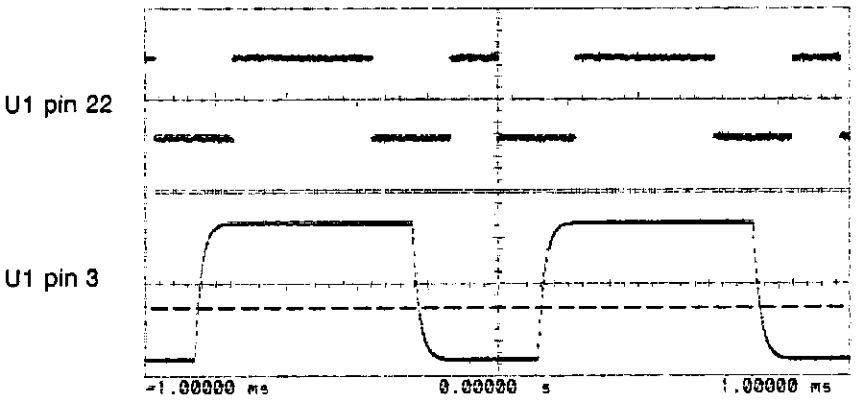
If the inputs to the trigger hybrid are good, replace the trigger hybrid; otherwise replace the horizontal assembly.




```
Ch. 1     =  400.0 mvolts/div          Offset    = -420.0 mvolts
Ch. 2     =  2.000  volts/div          Offset    =  1.600  volts
Timebase  =  200  us/div               Delay     =  0.00000  s
Delta V   =  0.000  volts
Vmarker1  = -20.00 mvolts              Vmarker2  = -20.00 mvolts

      Trigger mode : Edge
On  Neg. Edge on Chan1
Trigger Levels
Chan1     =   -420.0 mvolts
Holdoff   =   3 Events
```

Figure 6D-31. Test Loop 23 Troubleshooting Waveform on the Horizontal Assembly.




```
Ch. 1     =  400.0 mvolts/div          Offset    = -420.0 mvolts
Ch. 2     =  2.000  volts/div          Offset    =  340.0 mvolts
Timebase  =  200  us/div               Delay     =  0.00000  s
Delta V   =  0.000  volts
Vmarker1  = -720.0 mvolts              Vmarker2  = -720.0 mvolts

      Trigger mode : Edge
On  Neg. Edge on Chan1
Trigger Levels
Chan1     =   -420.0 mvolts
Holdoff   =   3 Events
```

Figure 6D-32. Test Loop 23 Troubleshooting Waveform on the Horizontal Assembly.

LOOP 24 TRIGGER LEVEL (2)

This loop tests the trigger offset and trigger hysteresis band. If any lower numbered loops fail, troubleshoot them first.

Initial setup - slope positive, HF reject off, HF sensitivity off (hysteresis at maximum), and trigger level at 500 mV. The trigger level is then decreased in 1 mV increments until a trigger occurs, this is V1. Trigger slope is switched to negative and trigger level set to -500 mV. Trigger level is then increased in 1 mV increments until a trigger occurs, this is V2.
The trigger hysteresis band = V1 - V2. The trigger offset = (V1 + V2) ÷ 2.

Status line 1 indicates the following

0 The Loop passed.
-1 GO bit turned true while trigger was disabled and freerun was off.
-2 GO bit never turned true by changing the trigger level.
-3 Hysteresis offset is out of range.
-4 Hysteresis band is out of range.

Status line 2 indicates the trigger offset range, valid range = 0V ±12 mV.

Status line 3 indicates the trigger hysteresis band, valid range = 20 mV ±12 mV.

Troubleshooting Procedure

If this loop fails, perform the trigger offset and hysteresis adjustments in paragraph 4-17.

Perform the umbilical cable extended service test on the trigger slope line.

If the umbilical cable test passes, perform the timebase/trigger test.

If the trigger hybrid's output is bad, probe the following points on the horizontal assembly.

Location	Signal	Signal Name
U1 pin 3	See figure 6D-33	Trigger level
U1 pin 33	-.8 V	High frequency reject
U1 pin 32	-.8 V	Sensitivity
U1 pin 22	-.8 V	Enable/disable
U1 pin 24	-.6 V	Freerun on/off
U1 pin 35	See figure 6D-33	Trigger slope

If the trigger hybrid inputs are good, replace the trigger hybrid; otherwise replace the horizontal assembly.

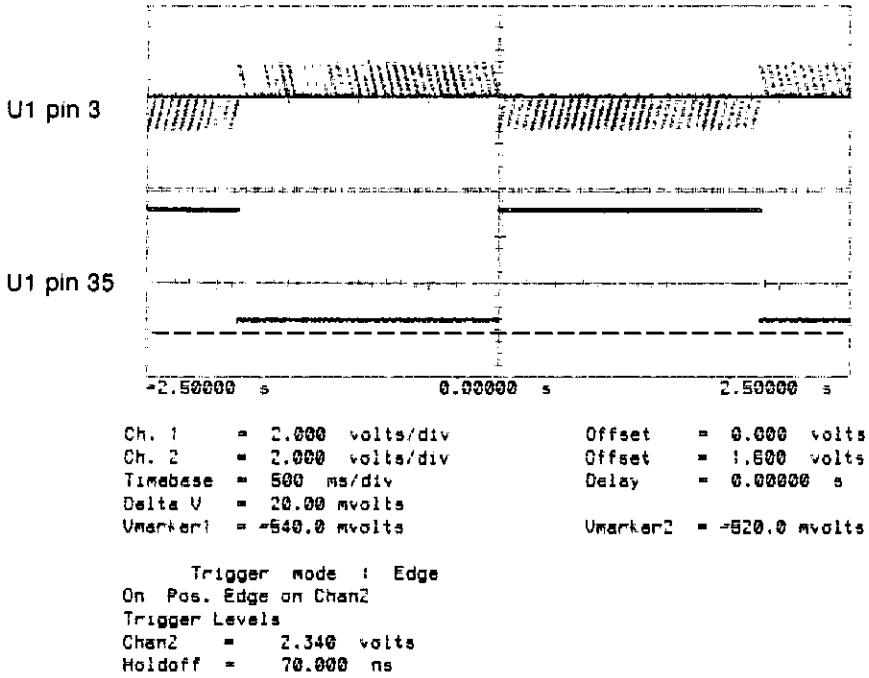


Figure 6D-33. Test Loop 24 Troubleshooting Waveform on the Horizontal Assembly.

LOOP 25 COARSE DELAY TIME

This loop tests the coarse delay timer by timing how long it takes for the GO bit to become true after a trigger pulse occurs at two states. First, when the coarse delay counters are loaded with 4 ns. Second, when the coarse delay counter is loaded with 458.752 μs.

Status line 1 indicates the following;

0 The loop passed.
-1 GO bit turned true while trigger was disabled and freerun was off.
-2 GO bit never turned true when delay = 4 ns.
-3 Difference between short and long delay times is out of range. The valid range is 450 μs to 470 μs.

Status line 2 indicates the following;

-2 GO bit never turned true when delay was set to 458.752 μs.

Status line 3 indicates the time in μs between the trigger occurrence and the GO bit going true for 4 ns of delay.

Status line 4 indicates the time in μ between the trigger occurrence and the GO bit going true for 458.752 μs of delay.

Troubleshooting Procedure

If this test fails, perform the frequency adjustments in paragraph 4-11. Perform the umbilical cable extended service test on the test set's inputs only.

Probe the following signals and refer to figures 6D-34 and 6D-35.

U1 pin 19	Trigger clock	horizontal assembly (if bad, a lower loop will fail)
U8 pin 9	GO bit	horizontal control assembly
U6 pin 2	pin 3 inverted	horizontal control assembly
U8 pin 9	GO bit	horizontal control assembly

If the trigger clock signal is bad, a previous loop should have failed also.

If there is no signal at U8 pin 9 but U6 pins 2 and 3 are good, replace the horizontal control assembly.

If there is no signal at U8 pin 9 and U6 pins 2 and 3 are bad, check the continuity of the umbilical cable and interconnect ribbon cable.

If the cable continuity test passes, probe the following points on the horizontal assembly and refer to figures 6D-36 and 6D-37.

U22 pin 2

U14 pin 14 This is a single shot measurement.
U15 pin 6

If any of these points test faulty, replace the horizontal assembly; otherwise call an HP service center.

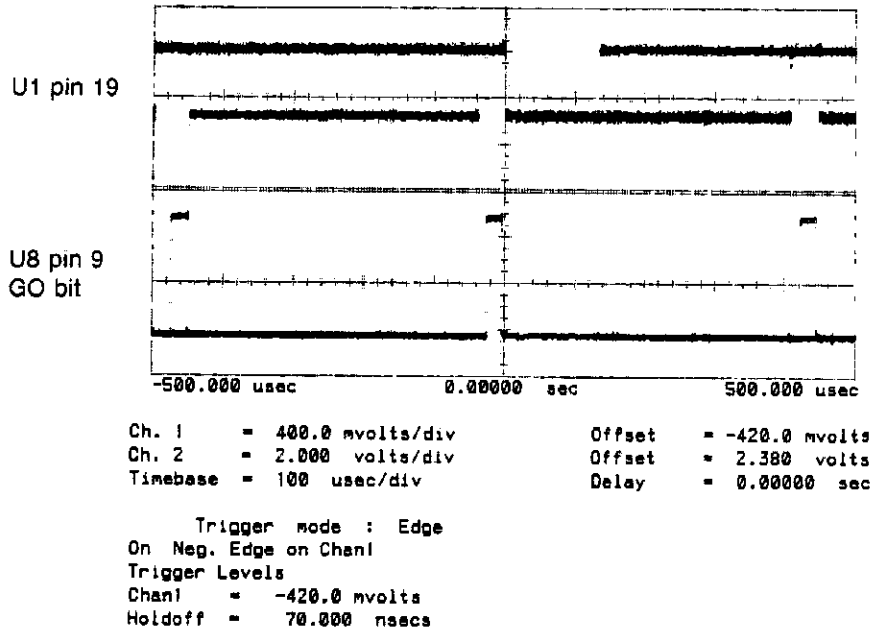


Figure 6D-34. Test Loop 25 Troubleshooting Waveforms on the Horizontal Assembly and on the Horizontal Control Assembly.

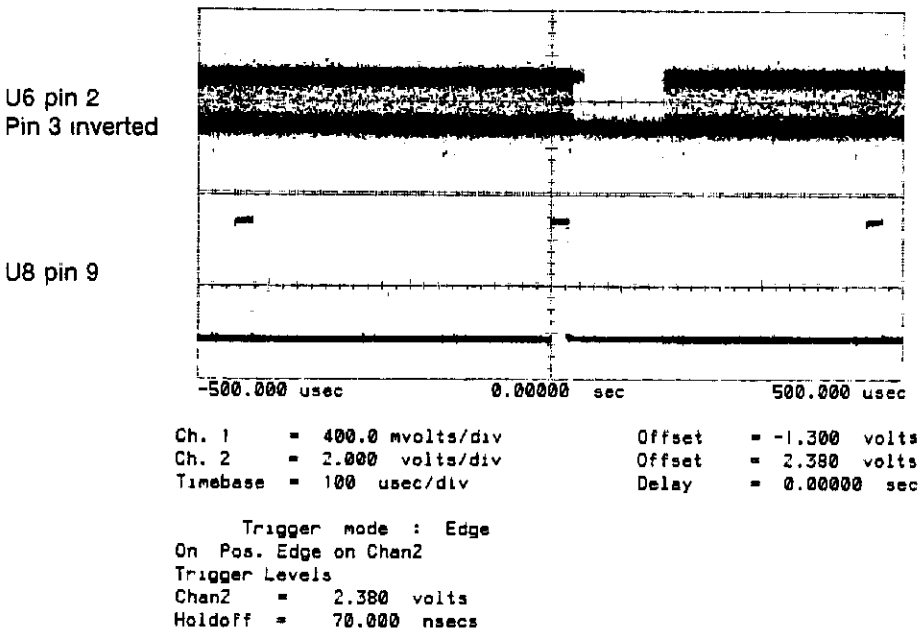


Figure 6D-35. Test Loop 25 Troubleshooting Waveforms on the Horizontal Control Assembly.

U22 pin 2

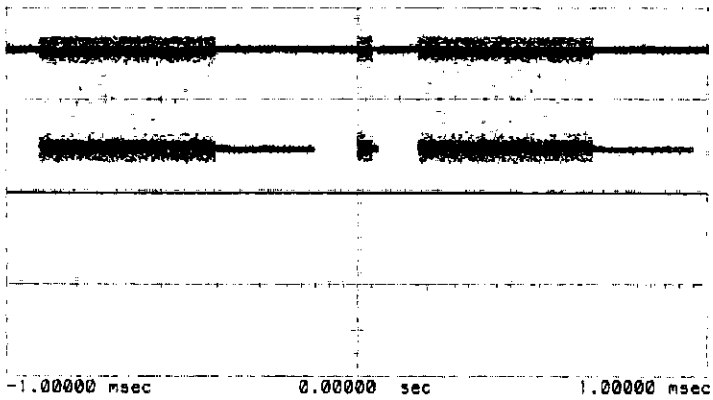


Figure 6D-36. Test Loop 25 Troubleshooting Waveform on the Horizontal Assembly.

U14 pin 14

U15 pin 6

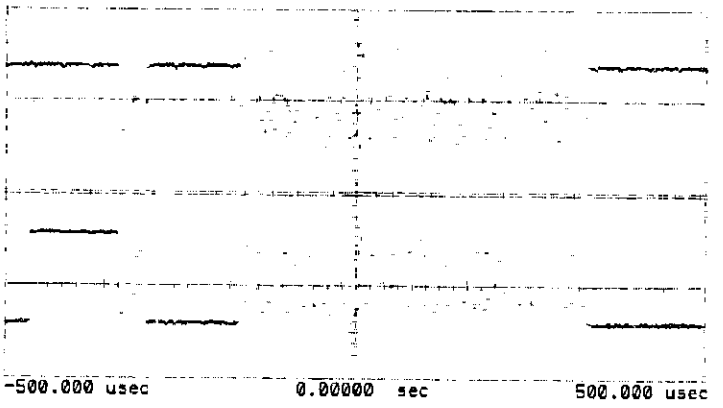


Figure 6D-37. Test Loop 25 Troubleshooting Waveform on the Horizontal Assembly.

LOOP 26 RATE GENERATOR/MULTI-SAMPLE PERIOD

This test checks if the rate generator operates at a particular frequency as expected. The freerun clock is set to 1 KHz. The time between GO bit toggles is approximately 1 ms. It is possible for multiple samples to occur per trigger event at this frequency. The minimum time between samples is 458.752 μs. Therefore, in 1 ms two A/D conversions could occur. Each time a sample is taken, a trigger must start the process. Troubleshoot all lower number loops first.

Status line 1 indicates the following;

-1 GO bit turned true while trigger was disabled and freerun was off.
-2 GO bit turned true while trigger was enabled and freerun was off.
-3 GO bit never turned true.
-4 GO bit never turned true after the first trigger event.
-5 GO bit never turned true after the second trigger event.
-6 Rate generator frequency cannot be calculated.
-7 Rate generator frequency is out of range.

Status line 2 indicates the frequency of the freerun generator, the valid range is 990 Hz to 1010 Hz.

Status line 3 indicates the following.

-6 Sampling period cannot be calculated.
-7 Sampling frequency is out of range.

Status line 4 indicates the period of multi-samples in μs, the valid range is 448 μs to 468 μs.

Troubleshooting Procedure

If the frequency in status 2 in incorrect, perform the extended service input umbilical cable test. The umbilical cable and interconnect ribbon cables could cause this problem. If the test set is not receiving the proper signals and the cables are good, replace the horizontal control assembly.

If status 4 in out of range, probe the following points. Refer to figures 6D-38 through 6D-41.

U3 pin 8	Freerun clock	horizontal assembly
U1 pin 19	Trigger clock	horizontal assembly
U8 pin 9	GO bit	horizontal control assembly
U1 pin 19	Trigger clock	horizontal assembly
U14 pin 14	L250 MHz	horizontal assembly
U1 pin 19		horizontal assembly
U22 pin 2	7.8 MHz	horizontal assembly
U1 pin 19	Trigger clock	horizontal assembly

U3 pin 8 and U1 pin 19 should be good if you are this far in the troubleshooting procedure.

If U8 pin 9 is bad, check for 7.8 MHz at U6 pin 2.
If 7.8 MHz is present at U6 pin 2, replace the horizontal control assembly; otherwise check the continuity of the umbilical cable and the interconnect ribbon cables.
If the cable continuity is good and if U22 pin 2 is bad, replace the horizontal assembly; otherwise call an HP service center.

If U22 pin 2 is bad, replace the horizontal assembly.

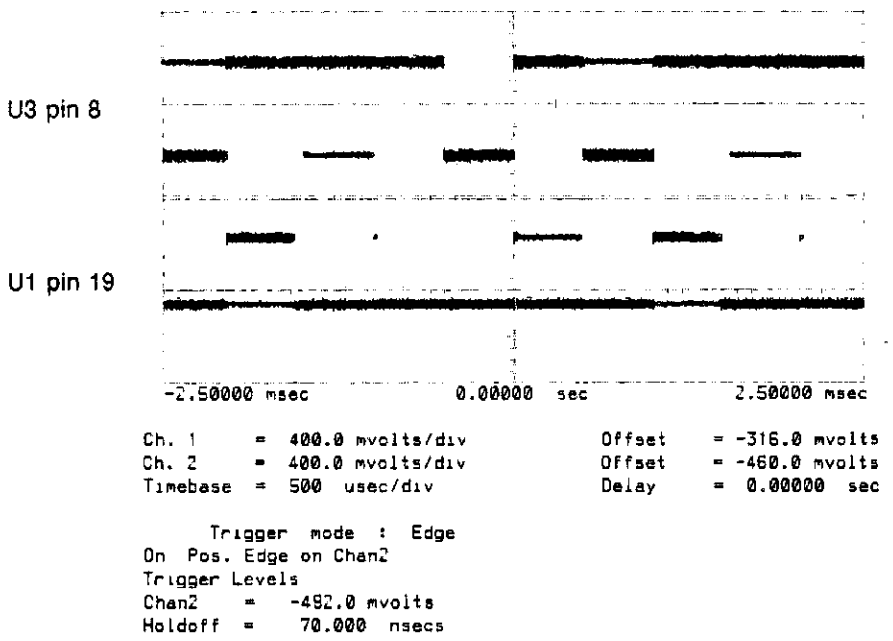


Figure 6D-38. Test Loop 26 Troubleshooting Waveform on the Horizontal Assembly.

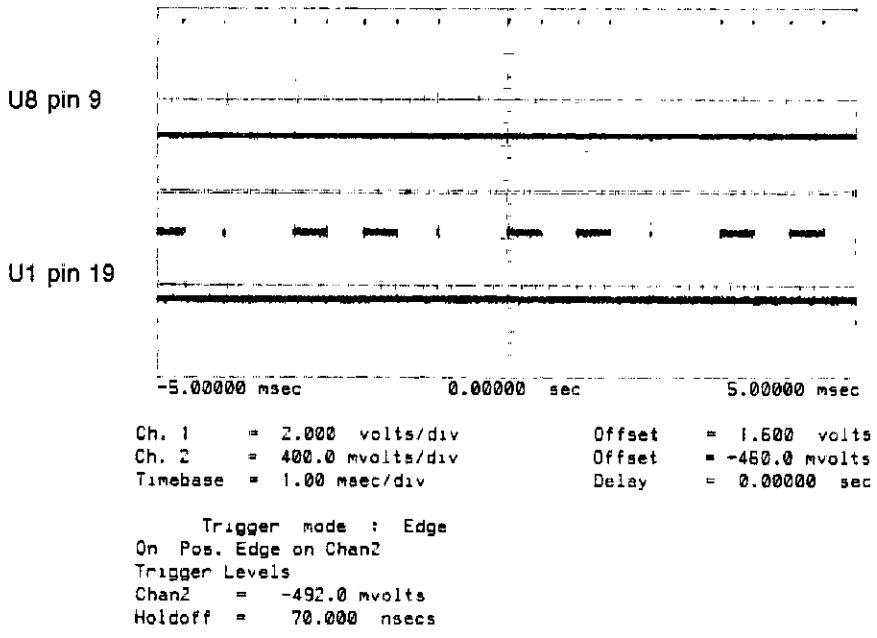


Figure 6D-39. Test Loop 26 Troubleshooting Waveform on the Horizontal Assembly.

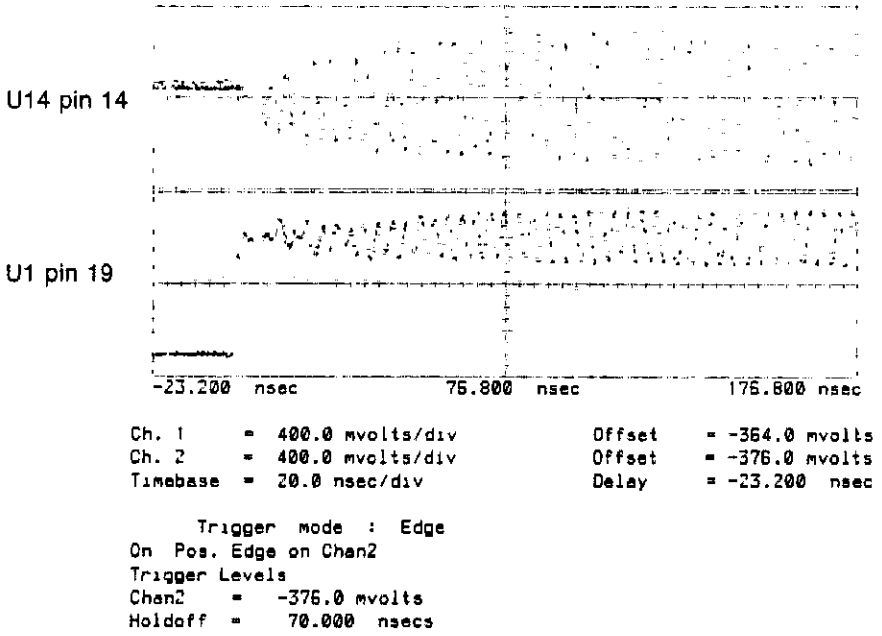


Figure 6D-40. Test Loop 26 Troubleshooting Waveform on the Horizontal Assembly.

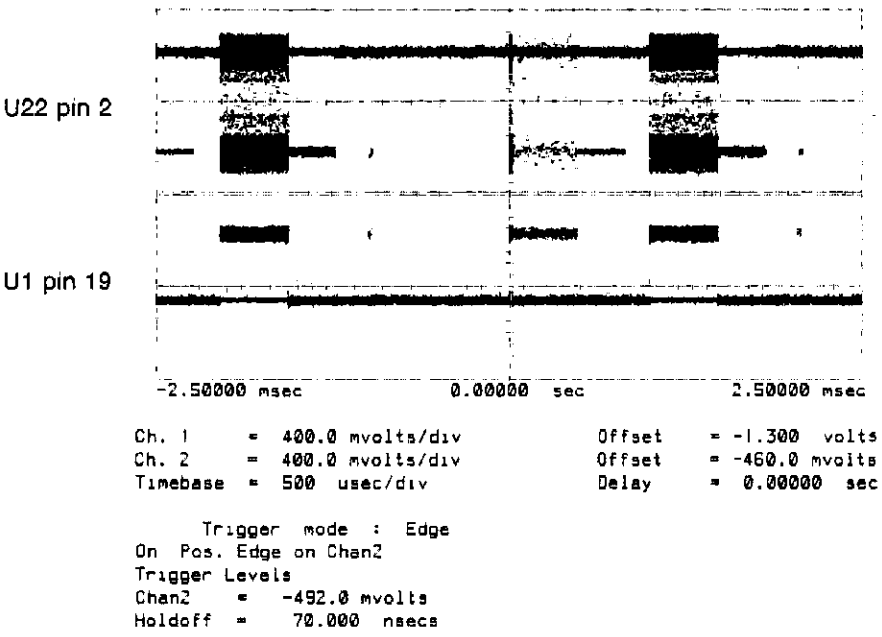


Figure 6D-41. Test loop 26 Troubleshooting Waveform on the Horizontal Assembly.

LOOP 27 HYSTERESIS BAND OFF

This is a reserved test for future enhancements. The present firmware in the HP 54120T ensures that this test always passes.

This loop is similar to loop 24. It checks the trigger hysteresis band and trigger level with the HF sensitivity turned on (hysteresis is at minimum). This loop requires that loops 20-26 pass. If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the following;

- 0 The loop passed.
- -1 GO bit turned true while trigger was disabled and freerun was off.
- -2 GO bit never turned true while changing trigger level.
- -3 Trigger offset is out of range.
- -4 Trigger hysteresis is out of range.

Status line 2 indicates the trigger offset in mV, valid range is 0 V ±12 mV.

Status line 3 indicates the trigger hysteresis band in mV, valid range is -5 mV ±12 mV.

Troubleshooting Procedure

Perform the input umbilical cable extended service test on the HF sense and HF reject lines because the umbilical cable or interconnect ribbon cables could cause this problem. If the test set is not receiving the proper signals and the cables are good, replace the horizontal control assembly.

Probe the following points. If any are bad, replace the horizontal assembly.

U1 pin 3
U1 pin 33
U1 pin 32
U1 pin 24
U1 pin 35
U1 pin 19

If all of these pins are correct except for U1 pin 19, replace the trigger hybrid.

LOOP 28 A/D CONVERSION

This loop measures the time it takes from the reading of channel 3's A/D conversion to the acquisition complete status when acquiring four channels of data. The loop than reads the A/D value on channel 4. If any lower numbered loops fail, troubleshoot them first.

The instrument is setup as follows; trigger disabled, freerun off, sampler off, HF reject off, coarse delay = 1 (minimum delay of 4 ns), fine delay = 0, trigger level = 1 V, slope positive, hysteresis = 0 (maximum), TDR off, rate generator = 500 KHz, channels 1-4 on, bandwidth bias low, offset on all four channels = 0 V, triggers are forced by changing the trigger slope line.

Status line 1 indicates the following;

0	The loop passed.
-1	GO bit is always high while trigger is disabled.
-2	GO bit is always low while forced trigger occurs.
-3	A/D status bit is always busy for channels 1-3 conversions.
-4	A/D status bit is always complete for channel 4's conversion.
-5	A/D status bit is always busy for channel 4's conversion.
-6	Wrong A/D bit pattern from channel 4's conversion.
-7	A/D conversion time took too long (limit is 30 μs).

Status line 2 indicates the channel 4 A/D output bit pattern.
The expected pattern is 111XXXXXXXXXXX0.

Status line 3 indicates the A/D conversion time in μs. The expected time is 20 μs.

Troubleshooting Procedure

Measure the dc voltage at TP1 on the A/D assembly. If it's not approximately 10 V, perform the 10 V reference adjustment paragraph 4-8.

If status line 3 is in error, probe the following points on the A/D assembly. Refer to figures 6D-42 through 6D-46.

U44 pin 1	U42 pin 6
U21 pin 5	U42 pin 8
U21 pin 28	U44 pin 1
U21 pin 6	U42 pin 11
U44 pin 1	
U42 pin 3	

If U44 pin 1 is bad and there are no lower numbered loop failures, call an HP service center.
If any other points are bad, replace the A/D assembly.

If status line 2 is in error, check to see if loops 29-38 fail. If any of these loops did fail, troubleshoot them first; otherwise perform the vertical extended service test on channel 4.

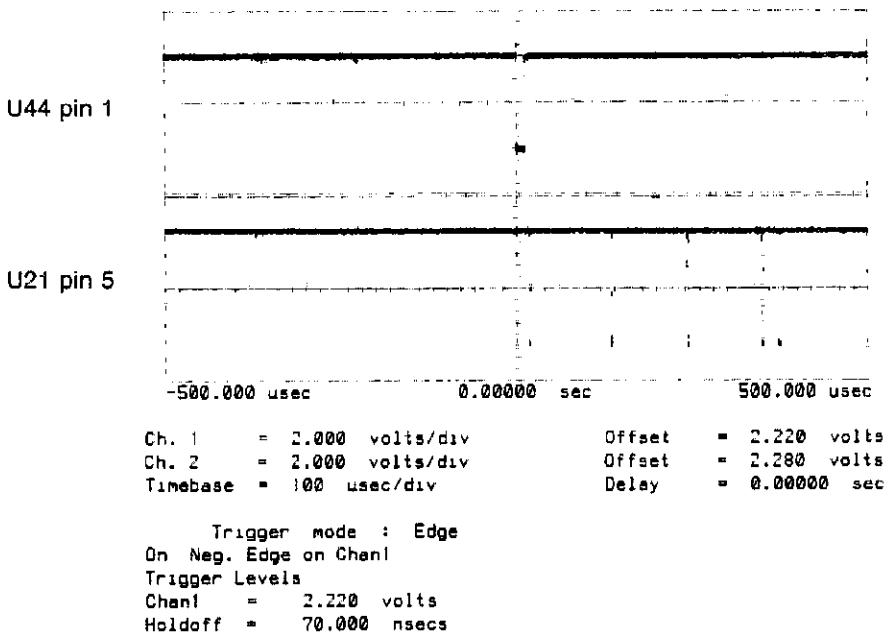


Figure 6D-42. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

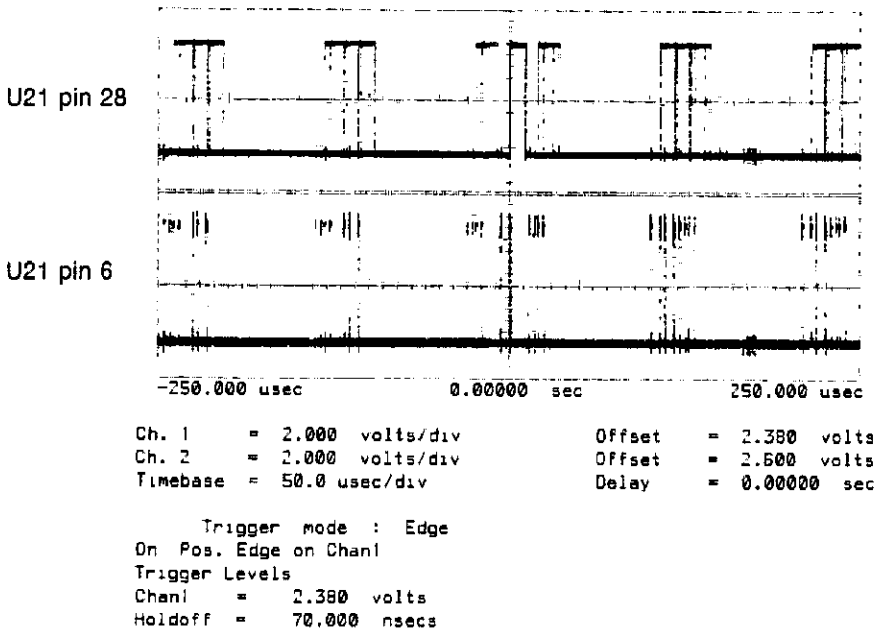


Figure 6D-43. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

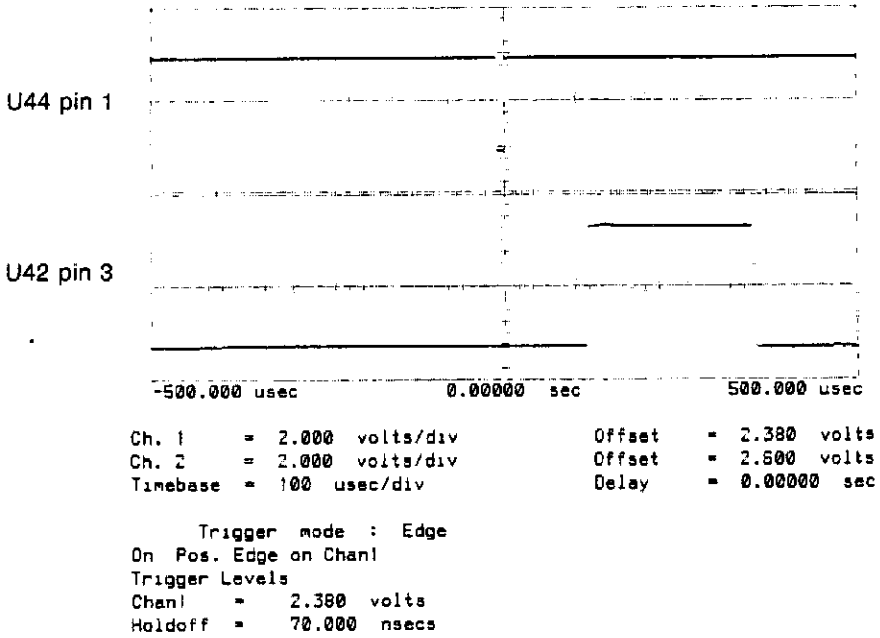


Figure 6D-44. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

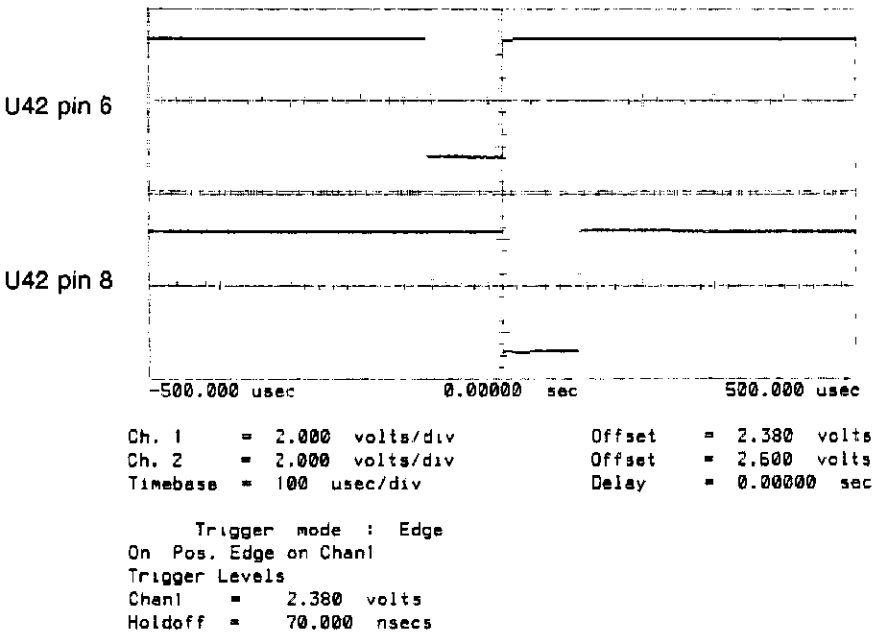


Figure 6D-45. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

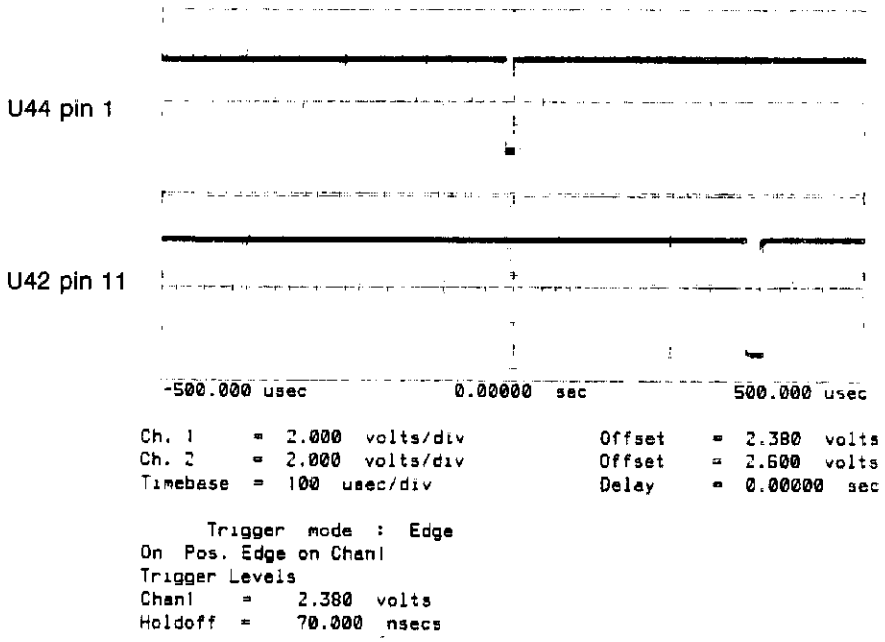


Figure 6D-46. Test Loop 28 Troubleshooting Waveform on the A/D Assembly.

LOOP 29 FEEDTHROUGH

The sampler feedthrough is measured by performing an A/D conversion with the samplers turned off, and then turned on. The difference is sampler feedthrough. Trigger events are forced by changing the trigger slope, this causes a data acquisition process to take place.

The instrument is setup as follows; trigger disabled, freerun off, samplers off, HF reject off, coarse delay = 256 ns, fine delay = 0, trigger level = 1 V, slope positive, hysteresis = 0 (maximum), TDR off, rate generator = 500 KHz, channels are turned on and off one at a time, bandwidth bias low, channel 1 offset = -320 mV, channel 2 offset = -160 mV, channel 3 offset = 160 mV, channel 4 offset = 320 mV.

If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates the A/D output for channel 1 when data can read.

8001H	GO bit turned true while trigger was disabled and freerun was off.
8002H	GO bit never turned true by changing the trigger slope.
8003H	A/D status is always busy.
	The valid range for all A/D values is 800H ±140H.

Status line 2 indicates the A/D output for channel 2 when data can be read.

Status line 3 indicates the A/D output for channel 3 when data can be read.

Status line 4 indicates the A/D output for channel 4 when data can be read.

Troubleshooting Procedure

If status line 1 contains 8001H through 8003H, this should cause lower numbered loops to fail also. Troubleshoot these lower numbered loops first. If lower numbered loops did not fail, call the HP service center

If there are any out of tolerance register failures, refer to table 6D-13, adjustment vs loop failures.

Loops 29 and 30 should be analyzed together. If loop 30 passes but loop 29 fails, replace the vertical assembly.

If only one channel fails, swap samplers to verify that the sampler is not causing the failure.

If swapping samplers does not fix the problem, troubleshoot single channel failures with the vertical extended service test and input umbilical extended service test. Possible failures are: vertical assembly, A/D assembly, ribbon cables, umbilical cable. If loops 31 through 34 or 35 through 38 are also failing, it may be helpful to troubleshoot these loops first.

If all four channels fail, use the pulse flow diagram. If the pulse filter tests pass, replace the A/D assembly.

LOOP 30 DATA ACQUISITION (2)

This loop checks the A/D conversion on each channel with the samplers turned on and no input signals are applied. Each channel is checked 64 times and the results are averaged. Trigger pulses start the data acquisition process. Trigger pulses are forced by toggling the trigger slope line.

The instrument is setup as follows; trigger disabled, freerun off, samplers on, HF reject off, coarse delay = 256 ns, fine delay = 0, trigger level = 1 V, slope positive, hysteresis = 0 (maximum), TDR off, rate generator = 500 KHz, channels 1 through 4 are on, offsets = 0 V, bandwidth bias low.

If any lower numbered loops fail, troubleshoot them first.

Status line 1 indicates channel 1's A/D output.

8001H	GO bit turned true while trigger was disabled and freerun was off.
8002H	GO bit never turned true by changing the trigger slope.
8003H	A/D status is always busy.
	The valid range for all A/D values is 800H ±140H (0 V ±80 mV).

Status line 2 indicates channel 2's A/D output.

Status line 3 indicates channel 3's A/D output.

Status line 4 indicates channel 4's A/D output.

If status line 1 contains 8001H through 8003H, this should cause lower numbered loops to fail also. Troubleshoot these lower numbered loops first. If lower numbered loops do not fail, call the HP service center.

Troubleshooting Procedure

If there are multiple status register failures, refer to table 6D-13, adjustment vs loop failures.

When loop 30 fails but loop 29 passes, check the status registers. If only one status register is out of range, suspect a faulty sampler; otherwise suspect a faulty pulse filter.

Troubleshoot single channel failures with the vertical extended service test and input umbilical extended service test. Possible failures are vertical assembly, A/D assembly, ribbon cables, umbilical cable. If loops 31 through 34 or 35 through 38 are also failing, it may be helpful to troubleshoot these loops first.

If all four channels fail, use the pulse filter extended service test. If the pulse filter test passes, replace the A/D assembly.

LOOP 31 CHANNEL 1 CHECK
LOOP 32 CHANNEL 2 CHECK
LOOP 33 CHANNEL 3 CHECK
LOOP 34 CHANNEL 4 CHECK

All inputs must be disconnected from the test set, this ensures the sampler input to be 0 V. The sampler measures the difference between the input signal and offset. The sampler input is expected to be 0 V, therefore the sampler will read the offset voltage. The offset voltage is set to 0 V. The sampler is turned on and the offset voltage is averaged 64 times. The process is repeated at 250 mV, and -250 mV. The averaged results are compared to the following values.

Status line 1 indicates
.8 ≤ |averaged 250 mV offset voltage minus the averaged 0 V offset voltage | ≤1.2

- 0 The loop passes on the first measurement.
- -1 False trigger occurs when trigger is disabled.
- -2 GO bit always low while forcing triggers.
- -3 A/D status always busy.
- -4 Value out of range (too small)
- -5 Value out of range (too large)

Status line 2 is the result of status line 1 changed to a percentage of 250 mV. The limits are 1 ±.2

Status line 3 indicates the pass/fail of:
.8 ≤ |averaged -250 mV offset voltage minus the averaged 0 V offset voltage| ≤1.2

- 0 The loop passes on the second measurement.
- -1 False trigger occurs when trigger is disabled.
- -2 GO bit always low while forcing triggers.
- -3 A/D status always busy.
- -4 Value out of range (too small)
- -5 Value out of range (too large)

Status line 4 is the result of status line 3 changed to a percentage of 250 mV. The limits are 1 ±.2

Troubleshooting Procedure

If any lower numbered loops fail, troubleshoot them first.

If the value of status lines 1 and 3 are close to passing, perform the sampler bias adjustments (paragraph 4-13), and the offset and gain adjustments (paragraph 4-14).

If all four channels fail and the status registers contain -1, -2, or -3, the trigger loops 21 through 24 should also be failing. If the trigger loops are not failing, call an HP service center.

For single channel failures
Swap samplers to verify that the sampler is not causing the problem.

Perform the A/D extended service test to verify that the offset DAC's are operating correctly.

If the offset DAC's are good and the problem stays in the original channel after swapping samplers, perform the vertical extended service test to determine the faulty module.

LOOP 35 CHANNEL 1 SAMPLER GAIN
LOOP 36 CHANNEL 2 SAMPLER GAIN
LOOP 37 CHANNEL 3 SAMPLER GAIN
LOOP 38 CHANNEL 4 SAMPLER GAIN

All inputs must be disconnected from the test set which causes the sampler input to be 0 V. The sampler measures the difference between the input signal and offset. The sampler input is expected to be 0 V, therefore the sampler will read the offset voltage. The offset voltage is set to 0 V. The sampler is turned on and the offset voltage is averaged 64 times. The process is repeated at 250 mV, and -250 mV. The averaged results are compared to the following values

Status line 1 indicates

$$27\% \leq \left| \frac{\text{Gain at +250 mV at high bandwidth bias mode}}{\text{Gain at +250 mV at high bandwidth bias mode}} \right| \leq 58\%$$

- 0 The loop passes on the first measurement.
- -1 GO bit always high while trigger is disabled.
- -2 GO bit always low while forcing triggers.
- -3 A/D status always busy.
- -4 Value out of range (too small)
- -5 Value out of range (too large)
- -6 Gain at +250 mV low bandwidth mode = 0

Status line 2 indicates the percent of status line 1.

Status line 3 indicates

$$27\% \leq \left| \frac{\text{Gain at -250 mV at high bandwidth bias mode}}{\text{Gain at -250 mV at high bandwidth bias mode}} \right| \leq 58\%$$

- 0 The loop passes on the second measurement.
- -1 GO bit always high while trigger is disabled.
- -2 GO bit always low while forcing triggers.
- -3 A/D status always busy.
- -4 Value out of range (too small)
- -5 Value out of range (too large)
- -6 Gain at -250 mV low bandwidth mode = 0

Status line 4 indicates the percent of status line 3.

Troubleshooting Procedure

If any lower numbered loops fail, troubleshoot them first.

If all four channels fail and the status registers contain -1, -2, or -3, the trigger loops 21 through 24 should also be failing. If the trigger loops are not failing, call an HP service center.

If value of status lines 1 and 3 are close to passing, perform the sampler bias adjustments (paragraph 4-13), and the offset and gain adjustments (paragraph 4-14).

For single channel failures

Swap samplers to verify that the sampler is not causing the problem.

Perform the A/D extended service test to verify that the offset DAC's are operating correctly.

If the offset DAC's are good and the problem stays in the original channel after swapping samplers, perform the vertical extended service test to determine the faulty module.

LOOP 39 TDR

The loop tests the TDR step's low value (V_L) by delaying 1.5 µs from the trigger event and high value (V_H) by delaying 2.5 µs from the trigger event. Freerun clock is the trigger event. V_H and H_L are averaged 64 times. $\Delta V = V_H - V_L$ and should be between 370 mV and 430 mV.

The instrument is setup as follows; trigger disabled, freerun on, sampler on, HF reject off, coarse delay = 1.5 µs and 2.5 µs, fine delay = 0 trigger level = 1, slope positive, hysteresis = 0 (maximum), TDR on, rate generator = 500 KHz, channel 1 on, channels 2-4 off, bandwidth bias low, channel 1 offset = 200 mV.

Note

If there is an SMA short on channel 1's input connector, the SMA short must be removed before this test will pass.

Status line 1 indicates the following;
- -1 False triggers occurred when trigger is disabled.
- -2 Trigger does not occur when sampler is turned on.
- -3 Trigger does not occur when sampler is turned off.
- -4 A/D status bit is always busy.
- -5 ΔV is out of range.

Status line 2 indicates V_H in hex - expected >800H

Status line 3 indicates V_L in hex - expected <800H

Status line 4 indicates ΔV in mV - expected 400 mV.

Troubleshooting Procedure

If lower numbered loops fail, troubleshoot them first.

If status line 1 contains -1, -2, -3, or -4 and no lower numbered loops are also failing, call an HP service center.

Perform TDR adjustments in section 4-15.

Perform the TDR extended service test.

If both channels 1 and 3 fail, perform the TDR system extended service test.
If both channels 1 and 3 still fail, call an HP service center.
If only channel 1 fails, perform the vertical extended service test.

6D-19. EXTENDED SERVICE TESTS

The internal diagnostic loop tests find a very large number of instrument failures and some gross parametric failures. Because of the interaction of many assemblies it may be difficult to troubleshoot the instrument using only the loop tests. Several extended service tests have been developed as an aid in troubleshooting.

The extended service tests are used in two ways. First, when a loop test fails, the troubleshooting information usually refers to one of the extended service tests. Second, with experience the extended service tests may be used without the loops tests for quicker isolation of the problem.

A few of the extended service tests are executed at only some instrument settings. If your instrument is failing at other instrument settings, you may want to adjust the test settings to correlate with your failure.

The extended service test are listed as a procedure with steps. If a step fails, replace the indicated part. If there are no indications on what part to replace, return to the flow diagrams for instructions. If a step passes, continue on with the next step in the procedure.

Figure 6D-47 illustrates the pin locations for the umbilical cable and the ribbon cables. Umbilical cable pins 1-16 correspond with pins 1-16 (respectively) on the ribbon cable connecting to the vertical assembly and A/D assembly. Umbilical cable pins 17-50 correspond with ribbon cable pins 34-1 (respectively) connecting to the horizontal assembly and horizontal control assembly.

Figure 6D-48 illustrates the pin definition of various three pin devices which may require probing.

6D-20. BRIEF DESCRIPTION OF EACH EXTENDED SERVICE TEST

SAMPLER TEST

This is a front panel test which looks for the ability of each sampler to increment and decrement in offset with no signal applied. It also checks if each channel passes the 12.4 GHz bandwidth mode noise specification. If either test fails, a sampler is the first suspected module.

UMBILICAL CABLE TEST

This test checks the signals which interconnect the test set to the mainframe. The input and output lines to the test set are checked, and a test is provided to check the functioning of each line.

UMBILICAL CABLE INPUT TEST

This test checks if the A/D assembly, horizontal control assembly, and umbilical cable are delivering the proper signals to the test set. This is done by exercising various front panel controls on the mainframe and probing points in the test set. This test is similar to the umbilical cable test, but only the input lines to the test set are checked.

SAMPLER INPUT TEST

This test ensures that the input connectors and channel 1's TDR generator are not causing apparent sampler failures. The sampler input connectors are disconnected and the sampler test is performed.

SAMPLER SWAP TEST

This tests swaps a suspected bad sampler with a known good sampler and then performs the sampler test. If the failure follows the suspected bad sampler, then that sampler is actually faulty. If the problem stays with the original channel, swap the samplers back and perform the vertical test to determine the faulty module.

VERTICAL TEST

This test checks if the A/D assembly, vertical assembly, or an interconnecting cable is causing a vertical problem. Various points on the bad channel are compared to the other three channels to help isolate the problem. The four channel paths on the vertical assembly follow separate paths and it would be a very rare problem where more than one channel on the vertical assembly had the same problem (except for multiple faulty samplers).

A/D ASSEMBLY TEST

This test checks two major circuits on the A/D assembly. First, it checks that the A/D assembly is generating outputs for the other assemblies and that the offset DAC circuitry is operating. Second, it checks the analog switch and ADC clocking circuitry. If either of these circuit tests fail, the A/D assembly is suspected as faulty.

PULSE FILTER SYSTEM TEST

This test determines what part of the sample pulse generator circuitry is preventing sample pulses from arriving at the samplers. The suspected faulty components are the pulse filter and horizontal assembly.

TDR TEST

This is a front panel test which determines if the TDR system is working properly. For this test to work, it requires at least one channel of channels 2 through 4 to operate properly. The TDR specifications are checked in channel 1 and the known good channel. If either channel fails, suspect a faulty channel. If both channels fail, suspect a faulty TDR system.

TDR SYSTEM TEST

This test determines which part of the TDR system is faulty. The suspect modules are: TDR step generator, TDR drive circuitry on the horizontal assembly, or TDR delay line.

TRIGGER TEST

This is a quick front panel test is see if the instrument is receiving triggers in both the triggered mode and freerun mode. **The message "Running" on the screen's top left corner does not indicate the instrument is receiving triggers, it indicates the RUN key has been pressed.**

PROBING TRIGGER TEST

This test verifies that the trigger hybrid is functioning properly. External triggers are applied to the instrument and the trigger hybrid's output line is checked. If this test fails, the timebase/trigger test should be run to determine if the trigger hybrid is functioning correctly. If this test passes, the horizontal test should be run to find out why the trigger signal is not being received.

TIMEBASE/TRIGGER TEST

This test verifies that the horizontal assembly is applying the proper signals to the trigger hybrid. If this test passes, the probing trigger test should be run to see if the trigger hybrid is good. If this test fails, the umbilical input test should be run to determine if the horizontal assembly is receiving the correct signals from the mainframe.

HORIZONTAL TEST

This test checks for a timebase fault in either the horizontal assembly, horizontal control assembly, or interconnect cable. The instrument is setup in a known operating state, and the interface between the two boards is probed.

COLOR MONITOR TEST

This test determines if the color monitor is faulty by checking horizontal sync pulses (HSYNC), vertical sync pulses (VSYNC), and color pulses (RGB) at the color monitor's input connector.

COLOR CRT MODULE

It is time consuming to remove a suspected faulty color CRT module from the instrument. This test connects a working color CRT module to the instrument outside the unit without having to remove the suspected faulty monitor. This test requires parts to be used from the 54100 family product support kit.

SOFTWARE TROUBLESHOOTING

Some failures cause the keyboards to lock up or a no display condition to prevent you from entering the troubleshooting menus. This procedure isolates which assembly is causing the problem.

6D-21. SAMPLER TEST

This is a front panel test which looks for the ability of each sampler to increment and decrement in offset with no signal applied. It also checks if each channel passes the 12.4 GHz bandwidth mode noise specification If either test fails, suspect a faulty sampler first. This test is performed on all four channels; however, if only one channel is suspected as faulty, it may be performed on only that channel.

1. Perform one key-down powerup routine.

2. Change display mode to 500 ms persistence, single screen, and grid graticules.
   Turn one channel on and other channels off.
   Set channel which is on to 10 mV/div.
   Change timebase to freerun mode.

3. Use the RPG control to change the channel's offset in a positive direction and a negative direction. If the trace only moves in one direction or not at all, or the dc level drifts, this test fails. Return to the flow diagram for instructions.

4. Press ***Histogram*** menu key.
   Press ***Time/Voltage*** key until ***Voltage*** is highlighted.
   Press ***Window/Acquire/Results*** key until ***Acquire*** is highlighted.
   Set number of samples to 10000.
   Press ***Start Acquiring*** key.
   Press ***Window/Acquire/Results*** key until ***Results*** is highlighted.
   Press ***Sigma*** key.

5. If sigma is > 1 mV, this test fails. Return to the flow diagram for instructions on the failed channel. If the sigma is < 1 mV, this channel passes. Continue with the procedure.

6. Turn channel 1 off and channel 2 on. Set channel 2 to 10 mV/div and repeat steps 3-5 for channel 2.

7. Repeat step 6 for channels 3 and 4.

8. If all the channels pass, this test passes.

6D-22. UMBILICAL CABLE TEST

This test checks the interface between the test set and the mainframe. This is done by exercising various front panel controls on the mainframe and probing points for expected results. This test should be used to verify the umbilical interface test. Probable faulty assemblies are: ribbon cables, umbilical cable, horizontal control assembly, and A/D assembly,

NOTE

Most signals originate at the mainframe, check these signals first. If the mainframe signals are bad the test set cannot be expected to operate properly. If a signal is bad (except for current signals), disconnect the umbilical cable from the signal source and probe the signal again.

1. Perform one key-down powerup routine.
2. Remove top and bottom covers from test set.
3. Start at the top of table 6D-16 and perform each test while probing the test set.
4. If all the probing points test good, then either the vertical assembly or the horizontal assembly is faulty. Return to the flow diagram.
5. Check the continuity of the umbilical cable.
   If the continuity check fails, replace the umbilical cable and return to the flow diagram; otherwise continue with step 6.
6. Check the continuity of the ribbon cable connecting the umbilical cable to the vertical assembly and horizontal assembly in the test set on the lines that failed.
   If the continuity check fails, replace the ribbon cable and return to the flow diagram; otherwise continue with step 7.
7. Check the continuity of the ribbon cable connecting the umbilical cable to the A/D assembly and horizontal control assembly in the mainframe on the lines that failed.
   If the continuity check fails, replace the ribbon cable and return to the flow diagram; otherwise continue with step 8.
8. Replace the board that is a source for the failing signals and return to flow diagram.

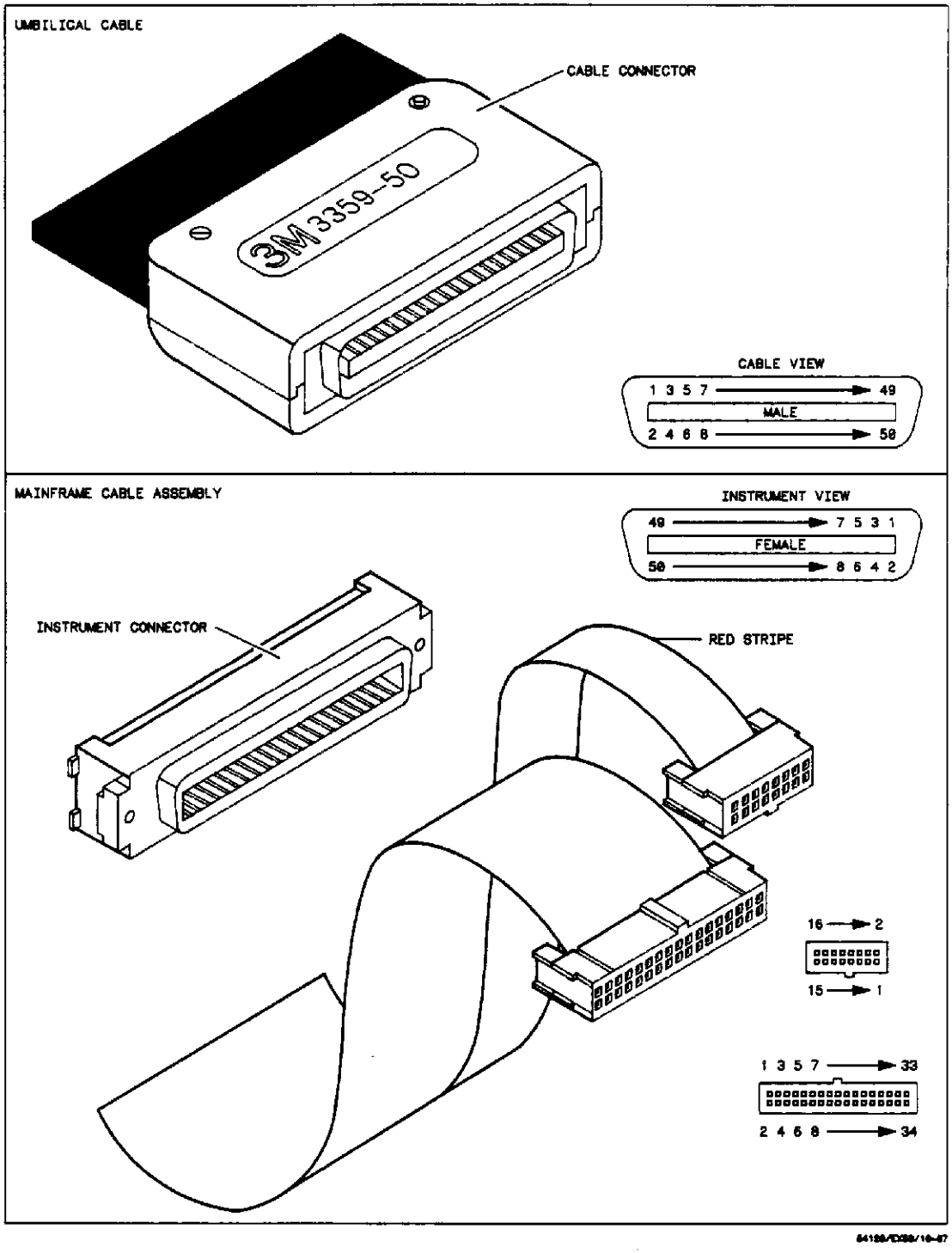


Figure 6D-47. Umbilical Cable and Ribbon Cable Pin Locations.

Table 6D-16. Signal and Pin Description for Umbilical Cable Test.

16 Pin Ribbon Cable	Umbilical Cable Pin No.	Description	Test Set Vert Assy Location	Mainframe A/D Assy Location	Source	Test Description
1	1	Ch 1 offset	R105 & R109*		A/D	**Infit perst, freerun mode. Vary offset from +100 mV to -100 mV, points should vary from +100 mV to -100 mV.
2	2	AGND	TP5	Current Sig		
3	3	Ch 2 offset	R106 & R110*	Current Sig	A/D	Same as channel 1
4	4	AGND	TP5			
5	5	Ch 3 offset	R107 & R111*	Current Sig	A/D	Same as channel 1
6	6	AGND	TP5			
7	7	Ch 4 offset	R108 & R112*	Current Sig	A/D	Same as channel 1
8	8	AGND	TP5			
9	9	AGND	TP5			
10	10	Ch 4 Vert Sig	U28 pin 6	U12 pin 2	Vert.	**Infit perst, freerun mode, offset=+300 mV, probe for fig 6D-49, Vary offset, pulse height should vary
11	11	H/LT	U33 pin 15	U44 pin 1	Vert.	
12	12	Ch 3 Vert Sig	U27 pin 6	U11 pin 2	Vert	Same as channel 4
13	13	-18 V	U36 pin 3	U18 pin 3	A/D***	DMM
14	14	Ch 2 Vert Sig	U26 pin 6	U10 pin 2	Vert	Same as channel 4
15	15	+18 V	U35 pin 2	U17 pin 1	A/D***	DMM
16	16	Ch 1 Vert Sig	U25 pin 6	U9 pin 2	Vert	Same as channel 4

*Measurement is made at the junction of these two resistors.
**Perform a one key-down powerup routine before starting this procedure.
*** Refer to figure 6D-48 for pinouts.

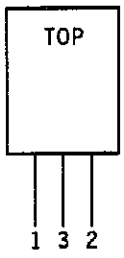


Figure 6D-48. Package Pin Locations.

Table 6D-16. Signal and Pin Description for Umbilical Cable Test (Continued)

34 Pin Ribbon Cable	Umbilical Cable Pin No.	Description	Test Set Horz Assy Location	Mainframe Horz Cntl Location	Source	Test Description
34	17	TDR ON/LOFF	U4 pin 8	U1 pin 10	H.C	**Toggle step on/off, OFF = 0 V, ON = -.8 V
33	18	NC				
32	19	NC				
31	20	AGND				
30	21	AGND				
29	22	AGND				
28	23	Freerun clock	U3 pin 8	U7 pin 10	H.C.	**freerun on, ECL freerun rates
27	24	AGND				
26	25	LEN/RESET	U3 pin 16	U7 pin 2	H.C.	**Trg'd mode, Probe for figure 6D-52
25	26	AGND				
24	27	Slope	U1 pin 35	U1 pin 16	H.C	**Toggle slope, POS = 0 V, NEG = 5 V
23	28	Trig hysteresis	U1 pin 32	U1 pin 15	H.C.	**Toggle HF sense, ON = 0 V, OFF = -.7 V
22	29	Trig level	U1 pin 3	Current Sig	H.C.	**Trg'd mode, Refer to table 6D-18.
21	30	Fine delay	U8 pin 10	Current Sig	H.C.	
20	31	LTC2	U22 pin 11	U3 pin 6	H.C	See fine delay test on next page.
19	32	LTBLOAD	U16 pin 5	U5 pin 4	H.C	This test applies to umbilical pins 33-38 also
18	33	TB4	U16 pin 11	U11 pin 9	H.C	Refer to figures 6D-53 through 6D-57
17	34	TB3	U16 pin 10	U11 pin 11	H.C	**Trg'd mode Probe figures 6D-53 and 6D-54, U16
16	35	TB2	U16 pin 9	U11 pin 14	H.C	pins 9-11 are all high levels until particular delay
15	36	TB1	U16 pin 7	U11 pin 1	H.C	settings are selected. Refer to figure 6D-55. The
14	37	TB0 reset	U15 pin 8	U5 pin 6	H.C	delay settings are approximate. Set delay to 16 ns
13	38	TB0 set	U15 pin 12	U5 pin 10	H.C	and probe for figures 6D-56 and 6D-57
12	39	HF reject	U1 pin 33	U2 pin 9	H.C	**Toggle HF reject, ON = 0 V, OFF = - 7 V
11	40	-18 V	U20 pin 2	U16 pin 3	H.C	DMM*
10	41	-8 V	U26 pin 2	U18 pin 3	H.C	DMM*
9	42	-8 V	U26 pin 2	U18 pin 3	H.C	DMM*
8	43	AGND				
7	44	+18 V	U21 pin 2	U15 pin 1	H.C	DMM*
6	45	AGND				
5	46	+8 V	U11 pin 2	U17 pin 1	H.C	DMM*
4	47	AGND				
3	48	L7.8 MHz	U22 pin 2	U6 pin 3	Horz	**Freerun mode, figures 6D-50 and 6D-51
2	49	7.8 MHz	U22 pin 3	U6 pin 2	Horz	Same as U22 pin 2 except inverted
1	50	AGND				

*Refer to Figure 6D-48 for pinouts.

**Perform one key-down powerup routine.

Fine Delay Test

1. Perform one key-down powerup routine.
2. Set to freerun mode.
3. Change timebase to 10 ps/div.
4. Probe the signal between R140 and R141 on the horizontal assembly. The signal will be noisy and untriggerable with the signal's bottom at 0 V and top at 7 mV.
5. Probe the signals in table 6D-17

Table 6D-17. Fine Delay Test Signals.

Sweep Speed	Signals low level	Signals high level
20 ps/div	0 V	125 mV
50 ps/div	0 V	250 mV
100 ps/div	0 V	500 mV
200 ps/div	0 V	1 V
500 ps/div and above	0 V	2 V

6. If the above signals are good, this test passes.

Table 6D-18. Trigger Level Settings vs Measure Results.

On Screen Trigger Level Value	Measure Value
0 V	0 V
+100 mV	+290 mV
-100 mV	-290 mV
+1 V	+2.9 V
-1 V	-2.9 V

U24 pin 6

U28 pin 6

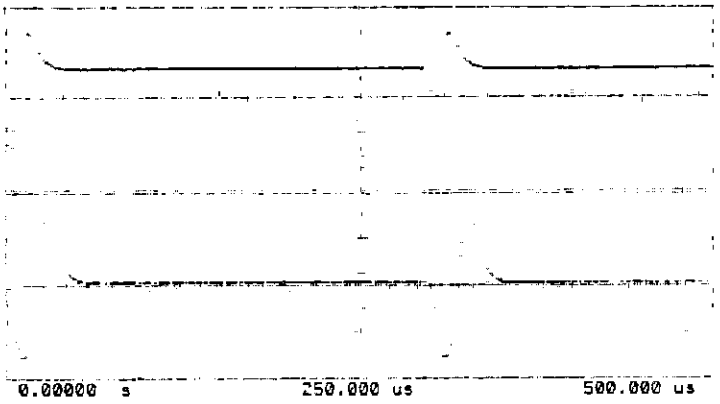


Figure 6D-49. 1KDPU, Infinite Persistence, Single Channel Display, Freerun Channel 4 Offset = +300 mV on the Vertical Assembly.

U22 pin 2

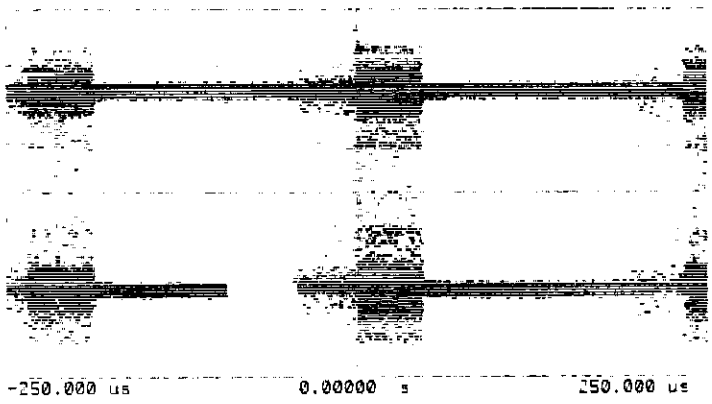


Figure 6D-50. On the Horizontal Assembly.

U22 pin 2

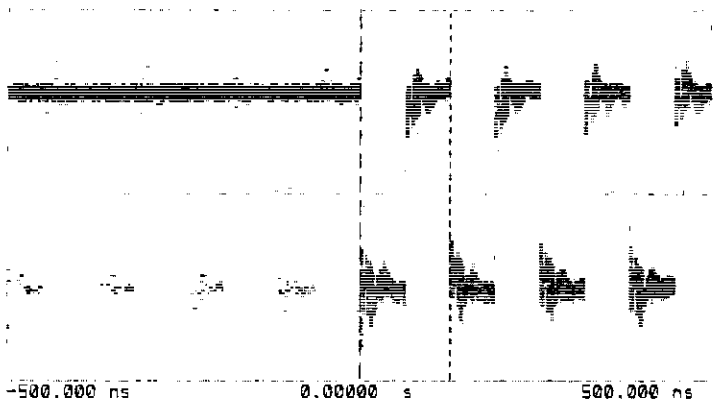


Figure 6D-51. On the Horizontal assembly.

U3 pin 16

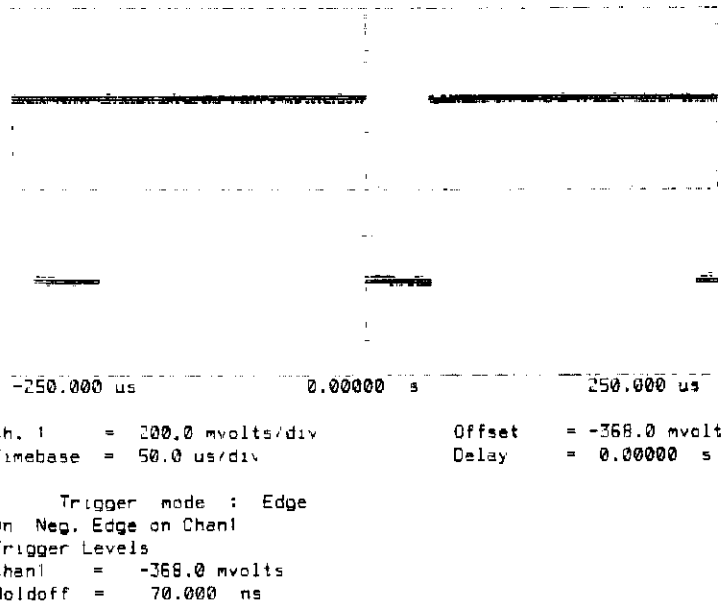
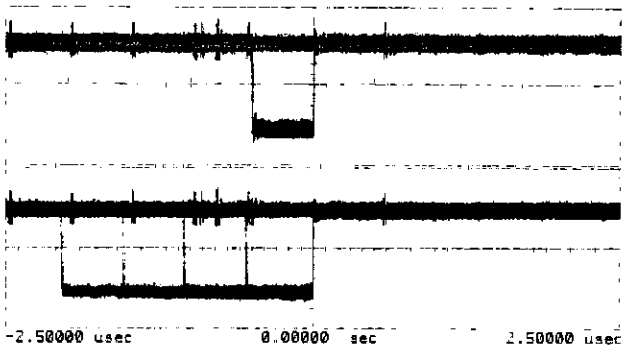


Figure 6D-52. 1KDPU, Freerun, on the Horizontal Assembly.

U16 pin 4

U22 pin 11



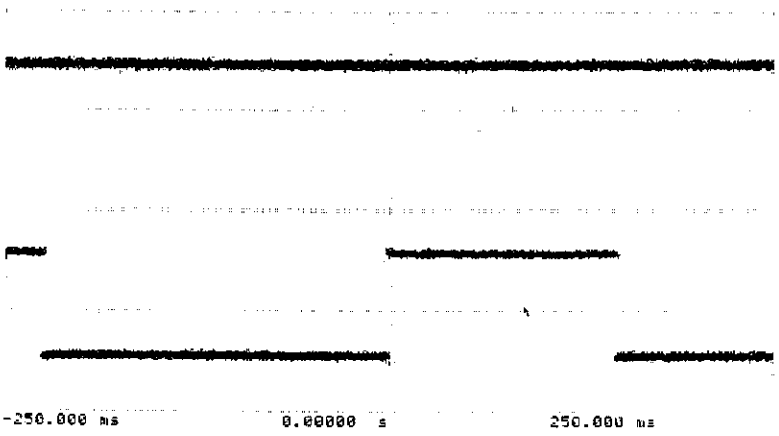

```
Ch. 1     =  400.0 mvolts/div          Offset    = -1.300  volts
Ch 2      =  400.0 mvolts/div          Offset    = -1.300  volts
Timebase  =  500  nsec/div             Delay     =  0.00000  sec

     Trigger mode  :  Pattern
On Pattern [HHXX] When   Entered
Trigger Levels
Chan1     =   -1.300  volts
Chan2     =   -1.300  volts
Holdoff   =    70.000  nsecs
```

Figure 6D-53. 1KDPU, Freerun, on the Horizontal Assembly.

U16 pin 4

U16 pin 7




```
Ch. 1     =  400.0 mvolts/div          Offset    = -1.224  volts
Ch. 2     =  400.0 mvolts/div          Offset    = -1.300  volts
Timebase  =  50.0 ms/div               Delay     =  0.00000  s

     Trigger mode  :  Edge
On  Pos. Edge on Chan2
Trigger Levels
Chan2     =   -1.300  volts
Holdoff   =    70.000  ns
```

Figure 6D-54. On the Horizontal Assembly.

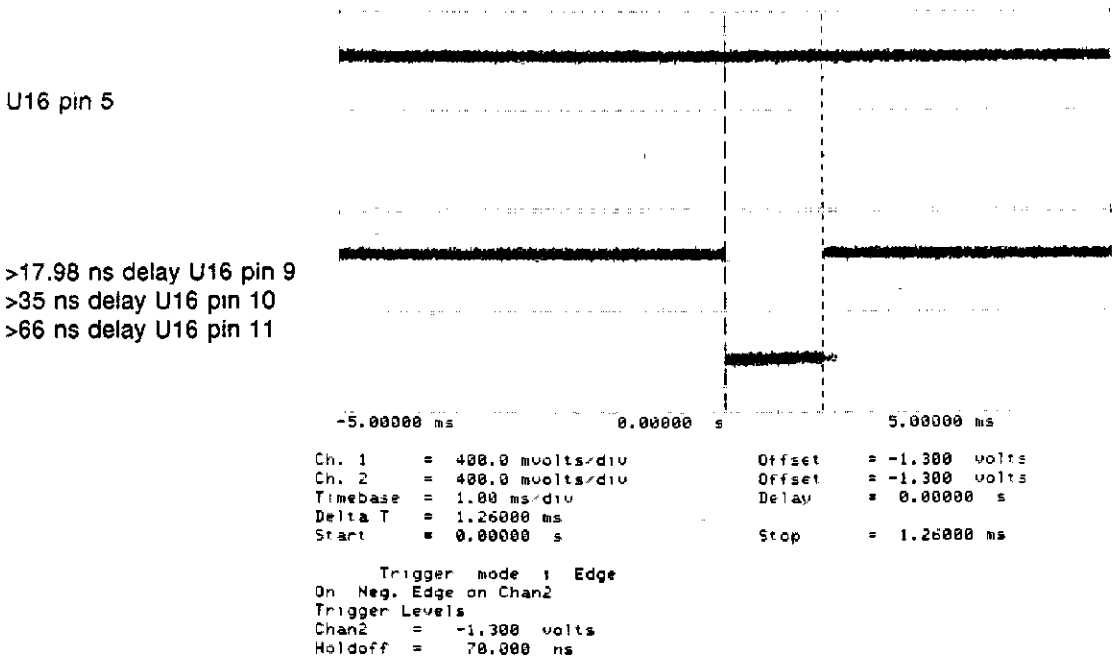


Figure 6D-55. On the Horizontal Assembly.

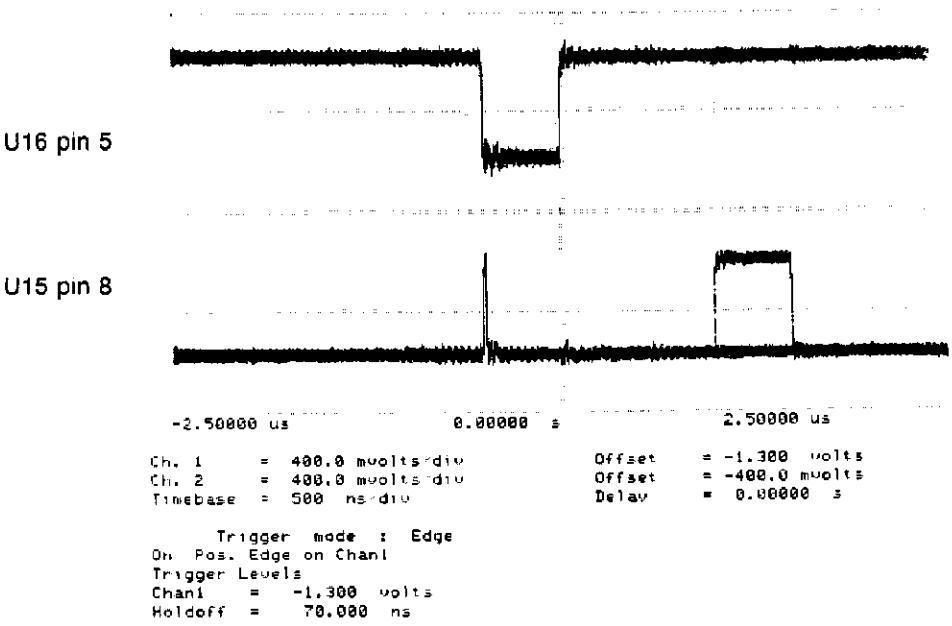


Figure 6D-56. Delay = 16 ns. On the Horizontal Assembly.

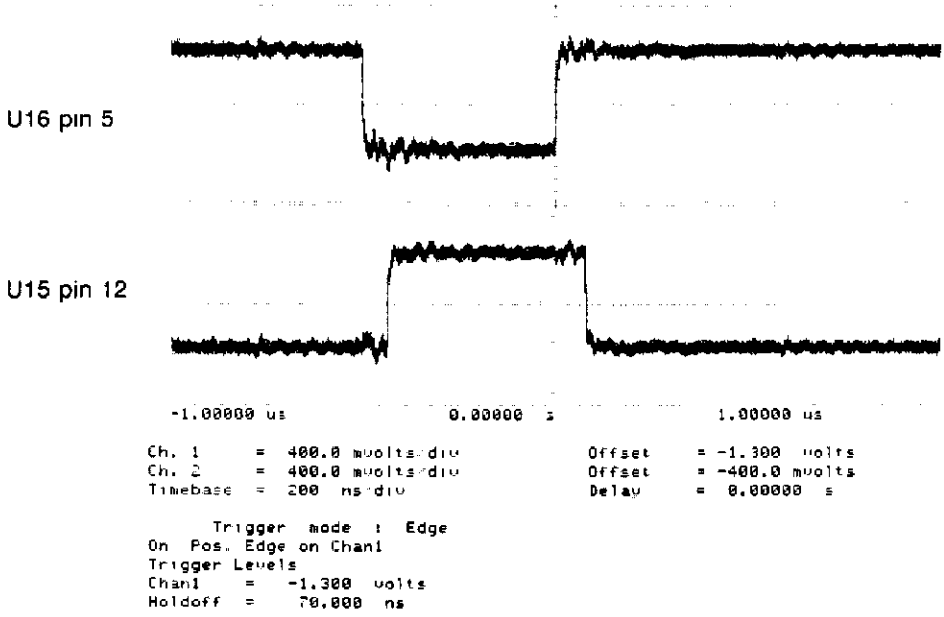


Figure 6D-57. On the Horizontal Assembly.

6D-23. SAMPLER INPUT TEST

This test ensures that each of the channel input connectors and channel 1's TDR generator are not causing apparent sampler failures. The sampler inputs are disconnected and the sampler test is performed.

1. Refer to sampler removal procedure 6A-26 and remove the sampler inputs using a torque wrench at the sampler.
2. Reinstall the sampler.
3. Perform sampler test.
4. Return to flow diagrams.

6D-24. SAMPLER SWAP TEST

This tests swaps a suspected faulty sampler with a known good sampler and then performs the sampler test. If the failure follows the suspected faulty sampler, then that sampler should be replaced. If the problem stays with the original channel, swap the samplers back and ensure the original operating channel is still good. If the channel that was operating before the swap is still good, perform the vertical test on the faulty channel; otherwise, replacement of both samplers, vertical assembly, and pulse filter may be required.

6D-25. VERTICAL TEST

This test checks if the A/D assembly, vertical assembly, or an interconnecting cable is causing a vertical problem. Various probing points on the bad channel are compared to the other three channels to help isolate the problem. The four channel paths on the vertical assembly follow separate paths and it would be a very rare problem where more than one channel on the vertical assembly had the same problem (except for multiple faulty samplers). Usually a multiple channel failure is caused by a faulty trigger hybrid, horizontal control assembly, horizontal assembly, A/D assembly, pulse filter, or pulse filter interconnects.

1. Perform one key-down powerup routine.

2. Change channel under test to the following settings and turn other channels off: display to single screen, persistence to infinite, offset to 320 mV, timebase to freerun.

3. Remove the test set's top and bottom covers.

4. Probe the following points on the vertical assembly. Refer to figures 6D-58 through 6D-62.

Figure	Point No.	Channel 1	Channel 2	Channel 3	Channel 4
6D-58	A	U21 pin 6	U22 pin 6	U23 pin 6	U24 pin 6
	B	U25 pin 6	U26 pin 6	U27 pin 6	U28 pin 6
6D-59	C	U17 pin 6	U18 pin 6	U19 pin 6	U20 pin 6
	D	U25 pin 6	U26 pin 6	U27 pin 6	U28 pin 6
6D-60	E	U13 pin 6	U14 pin 6	U15 pin 6	U16 pin 6
	F	U25 pin 6	U26 pin 6	U27 pin 6	U28 pin 6
6D-61	G	U5 pin 6 - R25	U6 pin 6 - R26	U7 pin 6 - R27	U8 pin 6 - R28
	H	U25 pin 6	U26 pin 6	U27 pin 6	U28 pin 6
6D-62	I	U9 pin 6 - R29	U10 pin 6 - R30	U11 pin 6 - R31	U12 pin 6 - R32
	J	U25 pin 6	U26 pin 6	U27 pin 6	U28 pin 6

5. If points G and I are bad and the sampler has been proven good by swapping it into another channel, then suspect either the pulse filter or semi-rigid cable connecting the pulse filter to the sampler (there is a very slight chance that the vertical assembly may still be at fault). Return to the flow diagram.

6. If any of the above test points are faulty for any of the channels, replace the vertical assembly and return to the flow diagram.

7. If all of the test points are good, then suspect either the A/D assembly, umbilical cable, or ribbon cables connecting to the umbilical cable. Probe the following points on the A/D assembly. If the points on the A/D assembly are not identical to the vertical assembly points, replace either the umbilical cable or the ribbon cables and return to the flow diagram; otherwise replace the A/D assembly and return to the flow diagram. **Adjustments affect the pulse height.**

Channel	Vertical Assembly	A/D Assembly
1	U25 pin 6	U9 pin 2
2	U26 pin 6	U10 pin 2
3	U27 pin 6	U11 pin 2
4	U28 pin 6	U12 pin 2

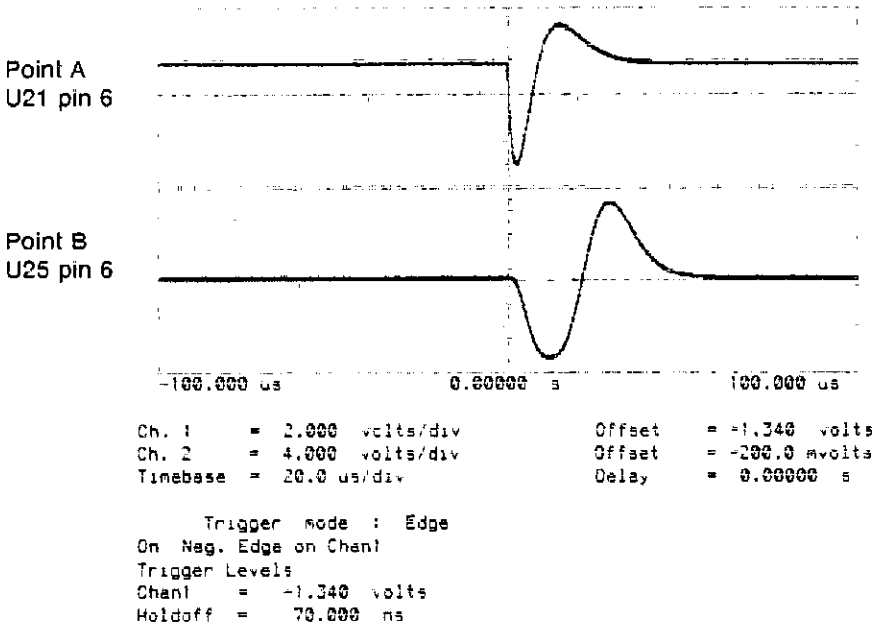


Figure 6D-58. U21 Pin 6 and U25 Pin 6 on the Vertical Assembly.

Point C
U17 pin 6

Point D
U25 pin 6

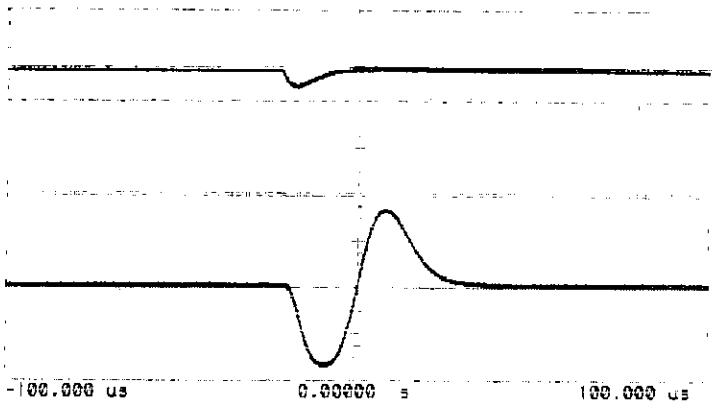


Figure 6D-59. U17 Pin 6 and U25 Pin 6 on the Vertical Assembly.

Point E
U13 pin 6

Point F
U25 pin 6

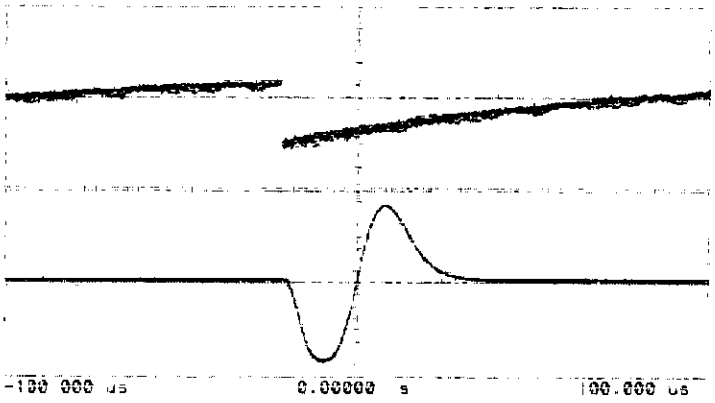


Figure 6D-60. U13 Pin 6 and U25 Pin 6 on the Vertical Assembly.

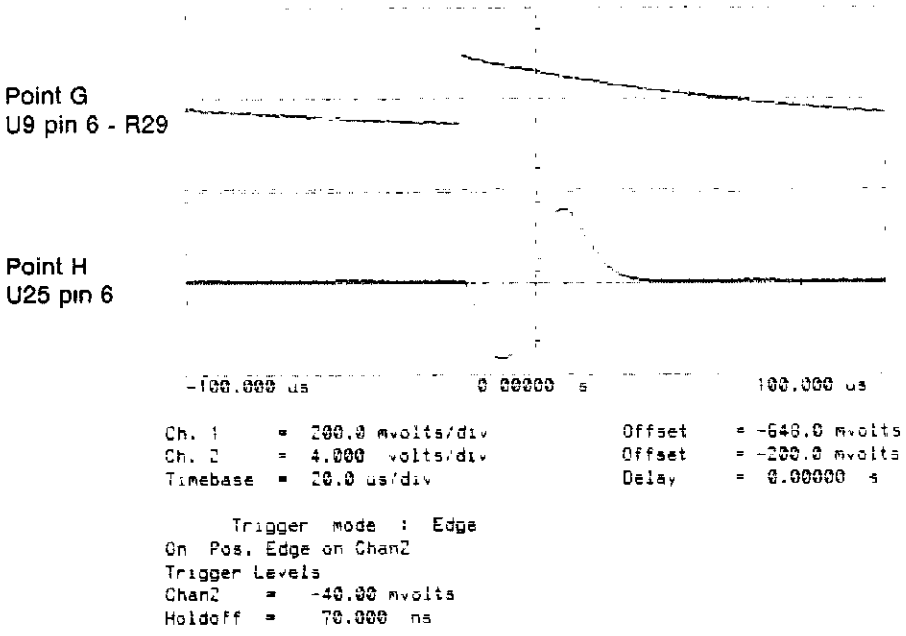


Figure 6D-61. U9 Pin 6 - R29 and U25 Pin 6 on the Vertical Assembly.

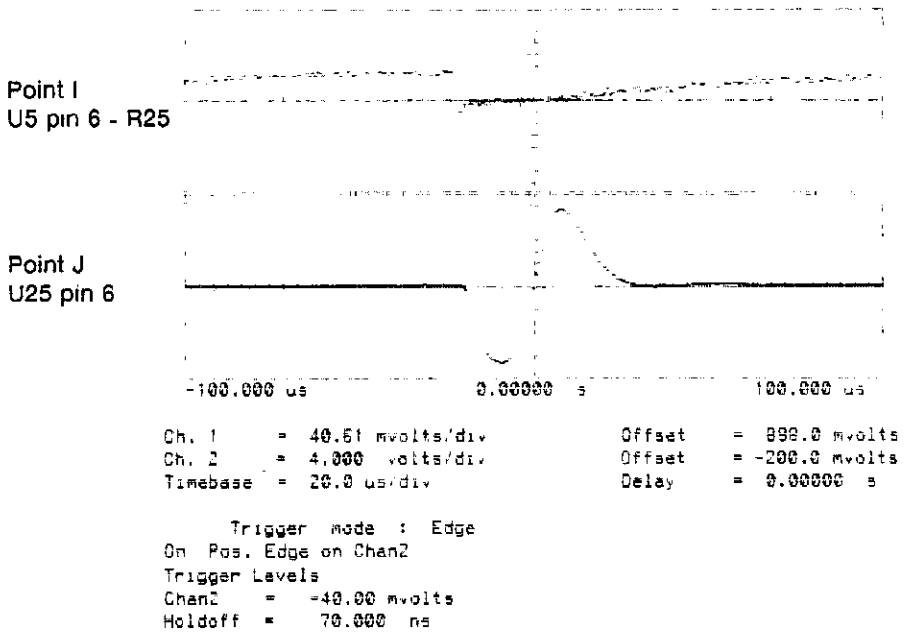


Figure 6D-62. U5 Pin 6 - R25 and U25 Pin 6 on the Vertical Assembly.

6D-26. A/D TEST

This test verifies the operation of three A/D assembly circuits: offset circuitry, analog switch, and clocking circuitry.

1. Remove umbilical cable from mainframe.

2. Perform one key-down powerup routine and change persistence to 300 ms.

3. Adjust each channel's offset in a positive and a negative direction. Probe the following points and verify the dc values vary linearly with changing offset values. When the offset is set to 500 mV and -500 mV the point under test should measure approximately 500 mV and -500 mV respectively.

   A/D - U1 pin 13 for channel 1
   A/D - U2 pin 13 for channel 2
   A/D - U3 pin 13 for channel 3
   A/D - U4 pin 13 for channel 4

   If these points fail, replace the A/D assembly.

4. Reconnect the umbilical cable to the mainframe and perform the umbilical test on the four offset lines going to the test set.

5. If the four offset lines are good, go to step 7

6. If the four offset lines are bad, check the continuity of the umbilical cable.

7. If the umbilical cable is good, perform a one key-down powerup, set to freerun mode, turn all channels on, and probe the following points on the A/D assembly. Refer to figures 6D-63 through 6D-66.

U44 pin 1 U42 pin 3	Infinite persistence
U42 pin 6 U42 pin 8	Infinite persistence
U42 pin 11 U44 pin 1	Infinite persistence
U21 pin 28 U21 pin 6	Single shot may vary depending on position of trigger point.

U44 pin 1

U42 pin 3

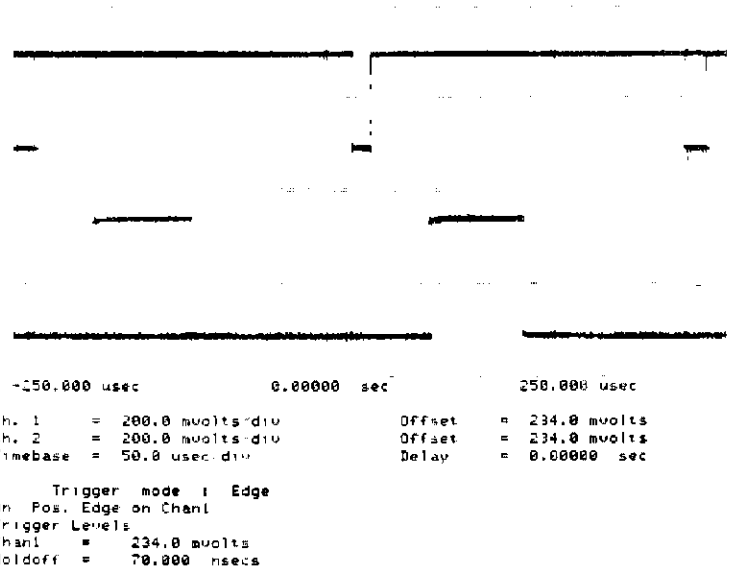


Figure 6D-63. On the A/D Assembly.

U42 pin 6

U42 pin 8

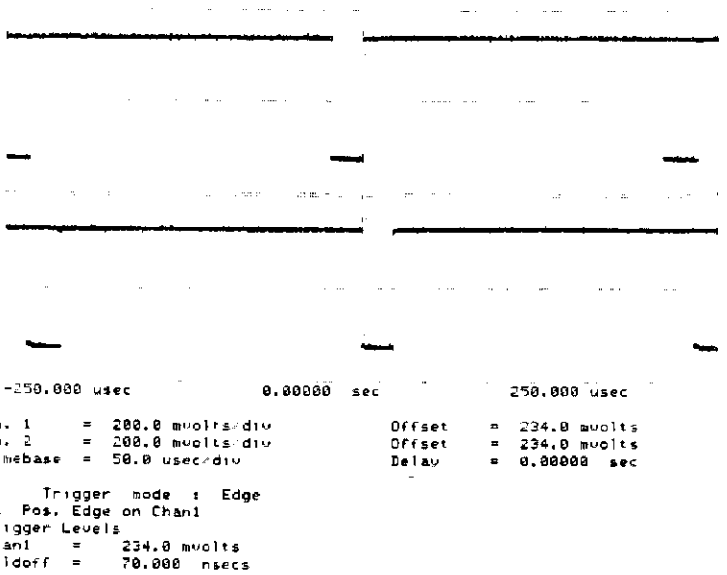


Figure 6D-64. On the A/D Assembly.

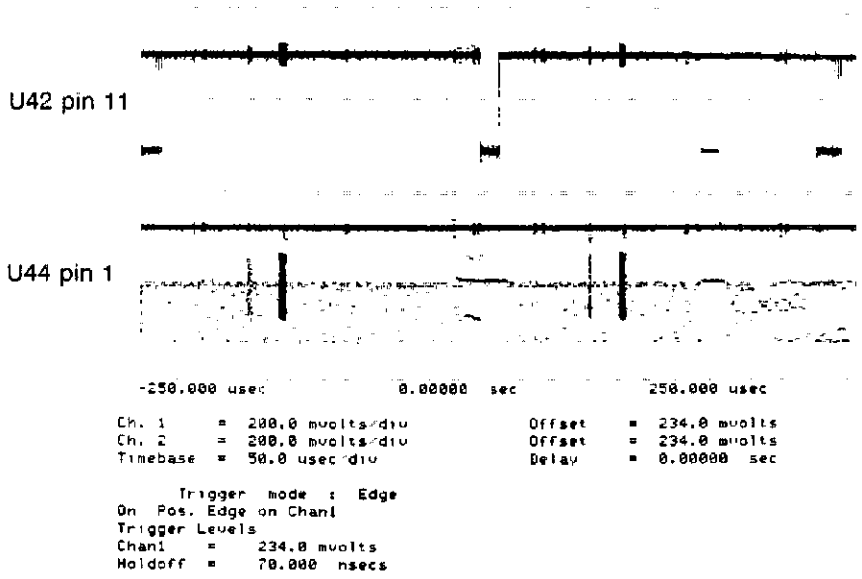


Figure 6D-65. On the A/D Assembly.

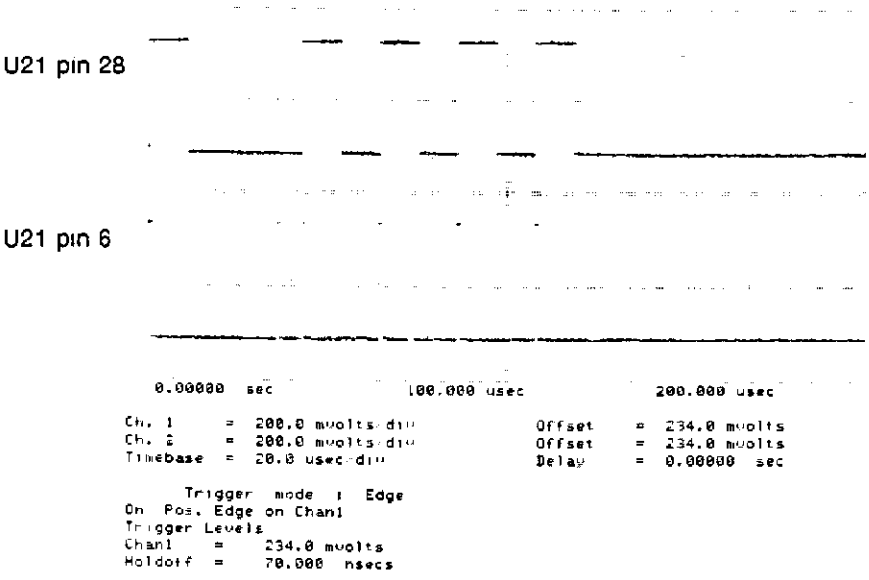


Figure 6D-66. On the A/D Assembly.

6D-27. PULSE FILTER SYSTEM TEST

This test determines if the pulse filter or its bias circuit is faulty.

1. Perform one key-down powerup routine.

2. Probe the following points on the horizontal assembly and compare to figures 6D-67 through 6D-70.

Between L1 and C41 Between collector of Q3 and R66	At 100 ns/div and 2 μs/div
U14 pin 11 Between collector of Q5 and R72	AT 20 ns/div and 50 μs/div

3. Lift the legs of C41 and C88, on the oppsite side of Q3, from the board.

4. Probe the points listed in step 2 above but use figures 6D-71 through 6D-74.

5. If the waveforms in step 2 were bad and the waveforms in step 4 were good, replace the pulse filter; otherwise replace the horizontal assembly.

6. Reinstall the legs of C41 and C88 into the board.

7. Return to the flow diagram.

Between
L1 and C41

Between Collector
of Q3 and R66

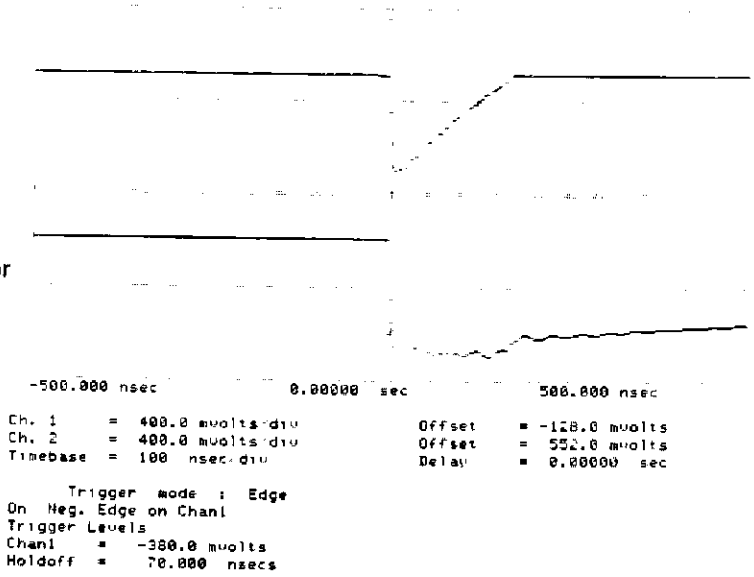


Figure 6D-67. With Pulse Filter Installed in Test Set, on the Horizontal Assembly, 100 ns/div.

U14 pin 11

Between collector
of Q5 and R72

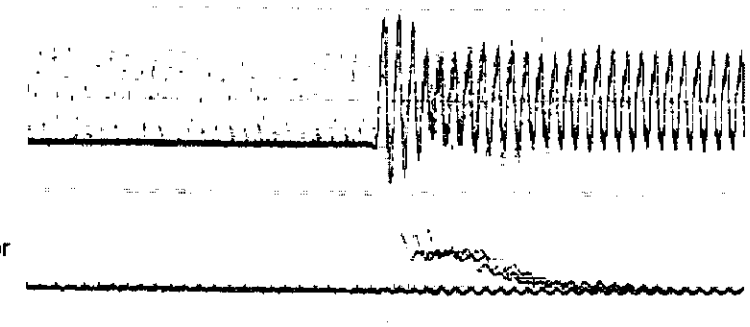


Figure 6D-68. With Pulse Filter Installed in Test Set, on the Horizontal Assembly, 20 ns/div .

Between
L1 and C41

Between collector
of Q3 and R66

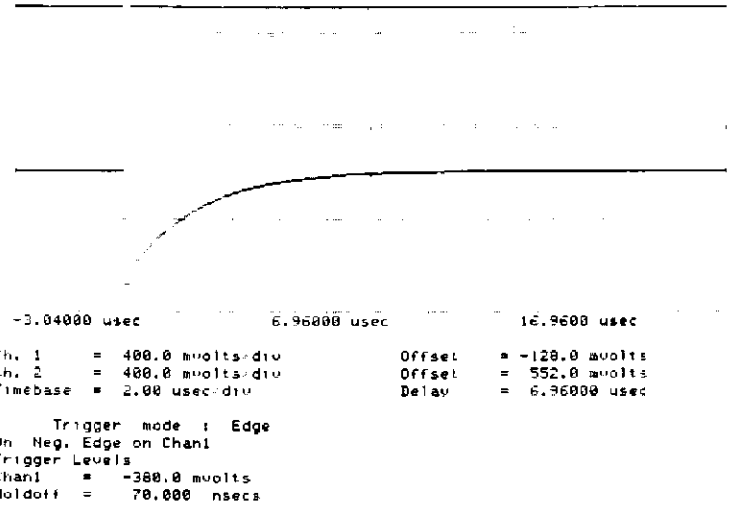


Figure 6D-69. With Pulse Filter Removed from Test Set, on the Horizontal Assembly, 2 µs/div.

U14 pin 11n 5

Between collector
of Q5 and R72

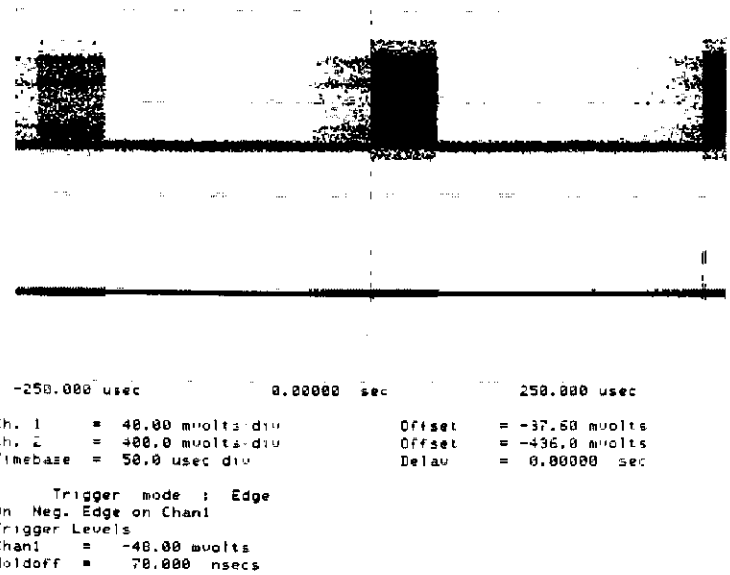


Figure 6D-70. With Pulse Filter Removed from Test Set, on the Horizontal Assembly, 50 µs/div.

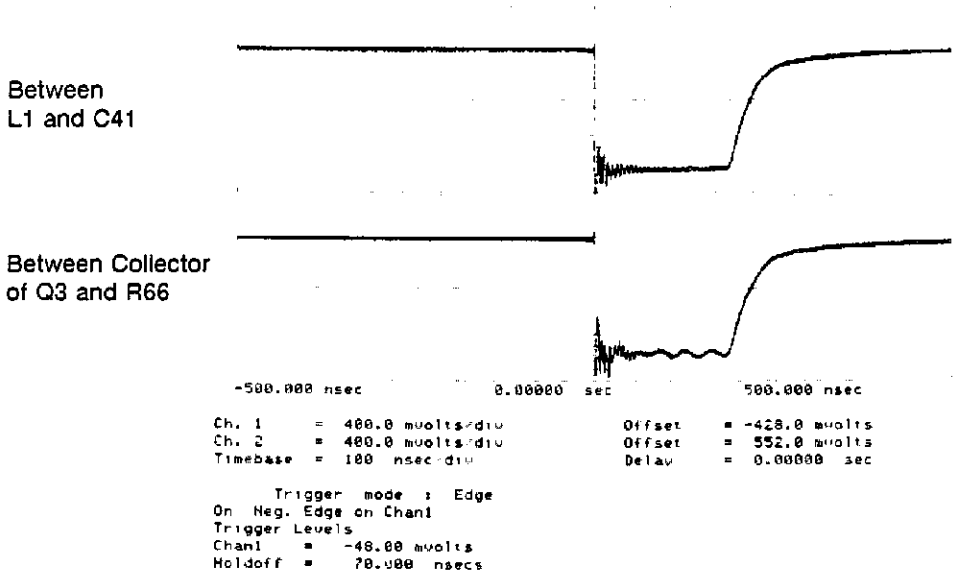


Figure 6D-71. With Pulse Filter Installed in Test Set, on the Horizontal Assembly, 100 ns/div.

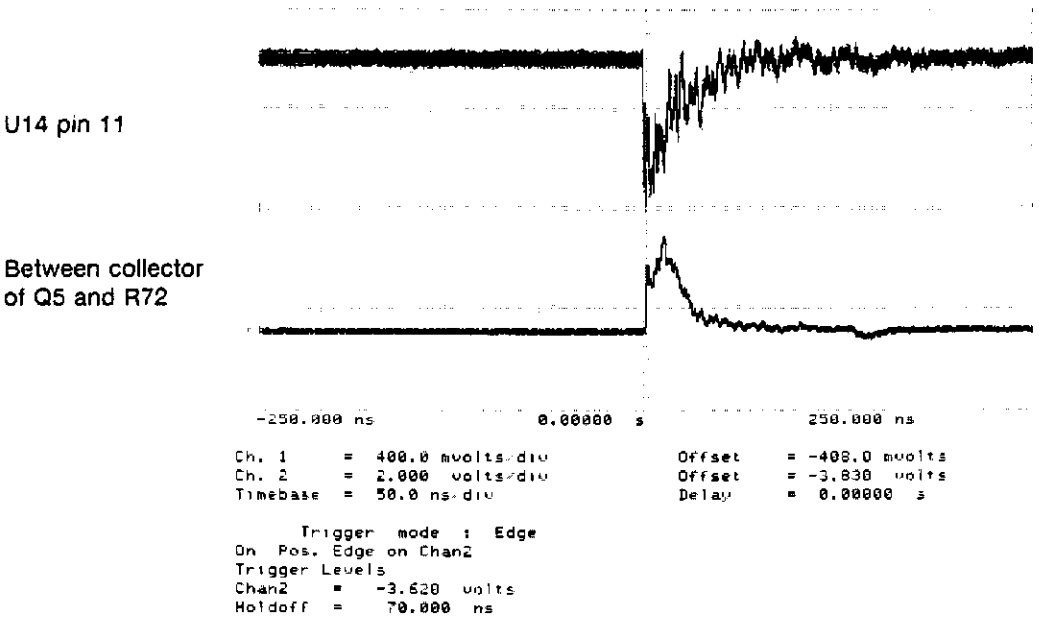


Figure 6D-72. With Pulse Filter Installed in Test Set, on the Horizontal Assembly, 20 ns/div, Trigger Mode Channel 2 Edge.

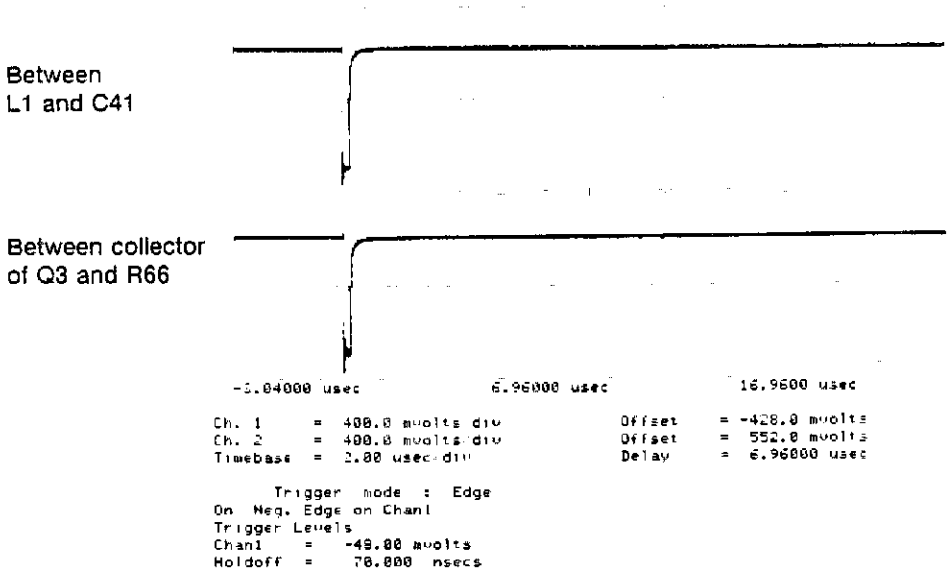


Figure 6D-73. With Pulse Filter Removed from Test Set, on the Horizontal Assembly, 2 µs/div.

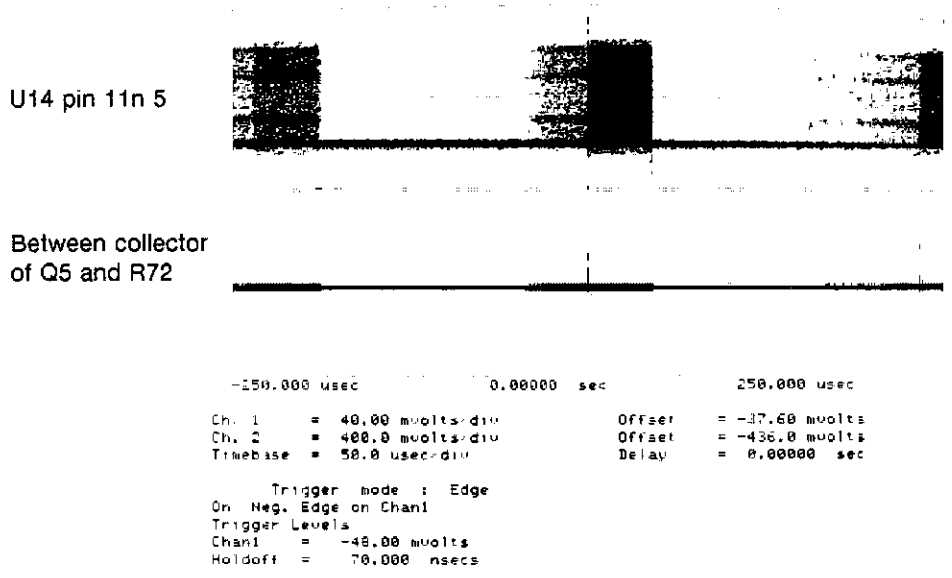


Figure 6D-74. With Pulse Filter Removed from Test Set, on the Horizontal Assembly, 50 µs/div.

6D-28. TDR TEST

This is a front panel test which determines if the TDR system is working properly. For this test to work, it requires at least one good channel other than channel 1. The TDR specifications are checked in channel 1 and the good channel. If either channel fails, suspect a faulty channel. If both channels fail, suspect a faulty TDR system.

1. Perform one key-down powerup routine.

2. Change display to single screen.

3. Press ***Network*** menu key and press ***Reflect/Trans/Cal*** key until ***Cal*** is highlighted. Press ***Preset Reflect Channel*** key.

4. Measure the following pulse parameters on channel 1.

Parameter	**Approximate Expected Results**
Risetime	45 ps
V_{top}	200 mV
V_{bottom}	0 V
Overshoot	3 %
Preshoot	3 %

5. If the measured results are within 100% of the expected results, perform the TDR step generator adjustments, paragraph 4-15, and repeat this procedure's steps 1-4.
   If the measured results are still off, perform vertical adjustment, paragraphs 4-13 and 4-14, and repeat this procedure's steps 1-5.

6. If the measured results are still more than 100% off, than this channel fails.
   Continue with step 7.

7. Connect a semi-rigid S and U cable through an APC 3.5 (f-f) adapter from channel 1 to channel 3.

8. Turn channel 3 on. Press ***Preset Reflect Channel*** key.

9. Change sweep speed to 1 ns/div and channel 1 offset to -500 mV.

10. Measure the following pulse parameters on channel 3.

Parameter	**Approximate Expected Results**
Risetime	60 ps
V_{top}	200 mV
V_{bottom}	0 V
Overshoot	4 %
Preshoot	4 %

11. If the measured results are more than 100% off, this channel fails.

12. Return to the flow diagram.

6D-29. TDR SYSTEM TEST

This test determines which TDR part is faulty: TDR step generator, TDR drive circuitry, or delay line.

1. Perform one key-down powerup routine.
2. Change display to single screen, and turn channels 2-4 off.
3. Press ***Network*** menu key, press ***Reflect/Trans/Cal*** key until ***Cal*** is highlighted, press ***Preset Reflect Channel*** key.
4. If a pulse appears on channel 1, go to step 5; otherwise go to step 8.
5. Perform TDR step adjustments, paragraph 4-15.
6. If the TDR step adjustments do not work properly, replace the TDR generator.

   Repeat the TDR step adjustment. If the adjustments still do not work properly, replace the horizontal assembly.
7. Return to flow diagrams.
8. Remove the test set's top and bottom covers.
9. Probe the following points. If they are good, the TDR system is probably good. If they are bad, the timebase or trigger system is bad; return to the flow diagram.

   U4 pin 6 Figure 6D-75
   U4 pin 8

   Junction of
   R173-R31 Figure 6D-76
   U4 pin 4
10. Disconnect TDR delay line (W15) from horizontal assembly.
11. Probe the following points. If they are good, replace the TDR step generator; otherwise replace the horizontal assembly.

    U4 pin 6 Figure 6D-77
    U4 pin 8

    Junction of
    R173-R3 Figure 6D-78
    U4 pin 4

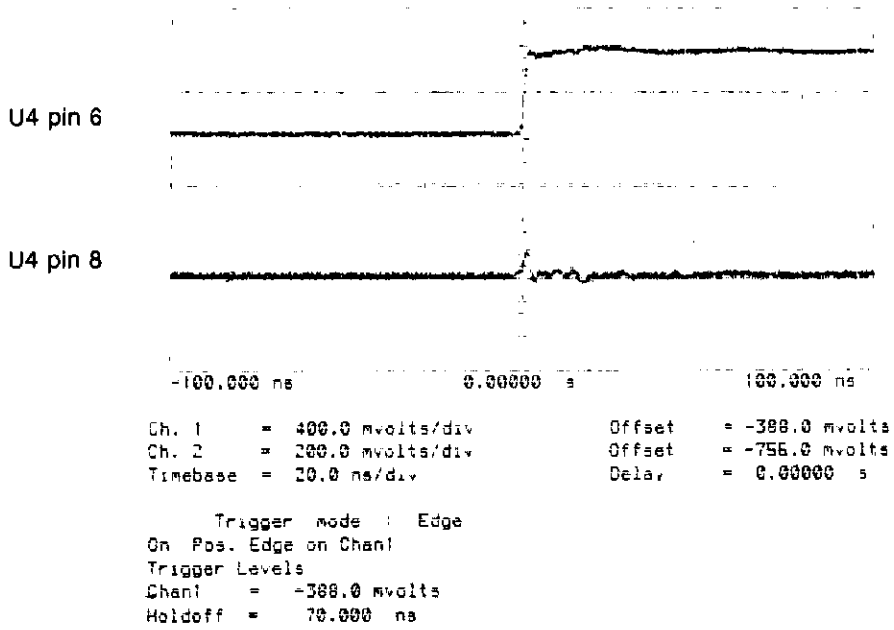


Figure 6D-75. On the Horizontal Assembly.

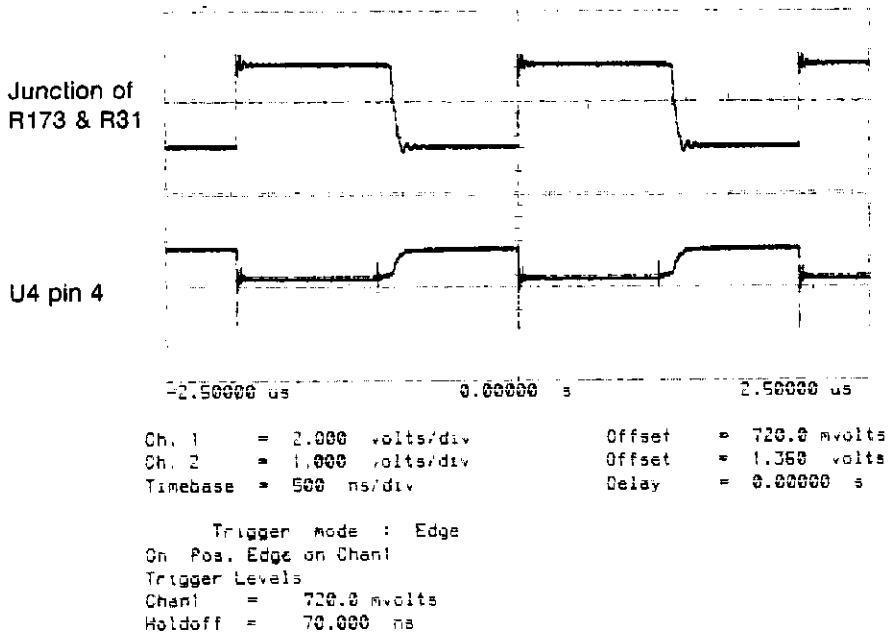


Figure 6D-76. On the Horizontal Assembly.

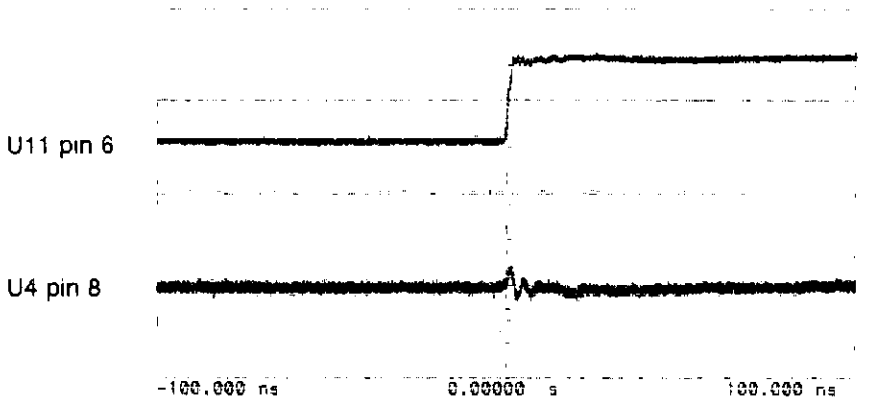


Figure 6D-77. On the Horizontal Assembly.

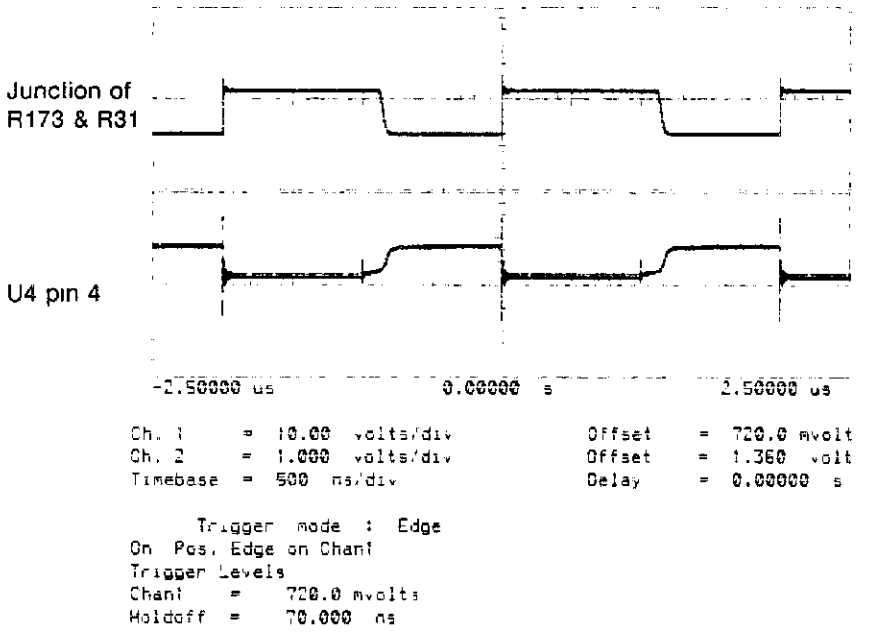


Figure 6D-78. On the Horizontal Assembly.

6D-30. TRIGGER TEST

This is a quick front panel test to see if the instrument is receiving triggers in both the triggered and freerun modes. The message "Running" on the screen's top left corner **DOES NOT** indicate the instrument is receiving triggers, it indicates the RUN key has been pressed.

1. Apply a 100 KHz sine wave with an amplitude of 100 mV and offset of 0 V to the external trigger input and press the ***Autoscale*** key.
2. Change to trg'd mode and 0 V trigger level, average mode with 2048 averages.
3. Press ***Clear Display*** key.
4. If the number of averages increases, the instrument is receiving triggers in the trg'd mode.
5. Remove the signal from the external trigger input and attach an SMA short to the external trigger input.
6. Change the timebase mode to freerun and press the ***Clear Display*** key.
7. If the number of averages increases, the freerun mode is operational.

6D-31. PROBING TRIGGER TEST

This test verifies the trigger hybrid is functioning properly. External triggers are applied to the instrument and the trigger hybrid's output lines are checked. If this test fails, the timebase/trigger test should be performed to determine if the trigger hybrid is functioning properly. If this test passes, the horizontal test should be performed to find out why the trigger signal is not being received.

1. Remove the test set's top and bottom covers.

2. Apply a 20 MHz sine wave with an amplitude of 300 mV and an offset of 0 V to a power splitter. Connect the power splitter to channel 1 and to the external trigger input.

3. Perform a one key-down powerup routine.
   Press the ***Autoscale*** key.
   Change display persistence to 300 ms, trigger mode to trg'd.

4. Probe U1 pin 19 and expand the timebase to see the edge with high resolution. When trying to determine if this is a good signal, look for a clear stable trigger. If there are many misplaced dots to the edge's left or right side, or if there appears to be two edges, then the signal is faulty. The jitter test should be executed to determine if the quantity of misplaced dots are within specification.

5. Change the applied signal to 500 MHz. Probe U1 pin 19 Use the same criteria as step 4 to determine if the trigger is operating correctly.

6. If steps 4 and 5 are good, then the trigger circuit's normal triggered mode is good.

7. Remove the signal from the oscilloscope.
   Change the timebase mode to freerun and set freerun rate to 500 KHz.

8. Probe U1 pin 19 checking for stable signals.
   Change the freerun rate to each range possible and verify the trigger event rate is correct and the output is stable as defined in step 4.
   If all the trigger event rates are correct, the trigger circuit's freerun mode is good.

9. If both the triggered and freerun modes are correct, this test passes; otherwise it fails.

10. Return to the flow diagram.

6D-32. TIMEBASE/TRIGGER TEST

This test verifies the horizontal assembly is applying the proper signals to the trigger hybrid. If this test passes, the probing trigger test should be run to see if the trigger hybrid is good. If this test fails, the umbilical input test should be run to determine the faulty module.

1. Perform one key-down powerup routine. Perform the umbilical input test for the following points: freerun clock, trig LEN/RESET, trigger slope, trigger hysteresis, and trigger level. If the above points are good proceed to step 3; otherwise this test fails and return to the flow diagrams.

2. Perform the umbilical input test for the following points. Refer to figure 6D-79.

In place of	Probe on trigger hybrid
U3 pin 16	U1 pin 22 (level shifted)
U3 pin 8	U1 pin 24 (less gain)

4. If these points are good, the trigger hybrid is receiving good signals and this test passes. Return to the flow diagrams.

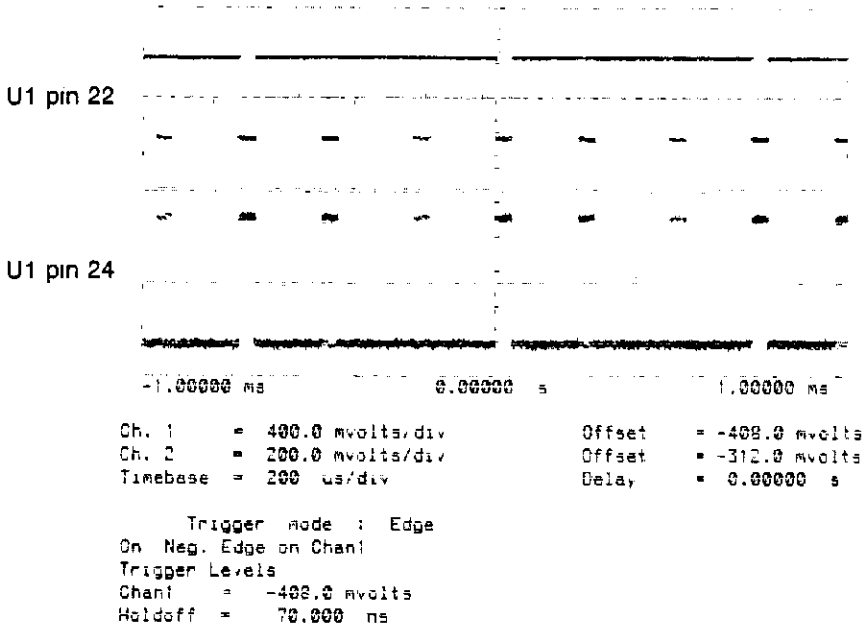


Figure 6D-79. On the Horizontal Assembly.

6D-33. HORIZONTAL TEST

This test checks for a timebase fault in either the horizontal assembly, horizontal control assembly, or interconnect cable. The instrument is setup in a known operating state, and the interface between the two boards is probed.

1. Perform one key-down powerup routine.

2. Probe the points indicated on figures 6D-80 through 6D-87. If either U22 pin 11 or U3 pin 8 is bad, replace the horizontal control assembly. If J5 pin 11 is bad, go to the pulse filter troubleshooting flow diagram. If any of the remaining points are bad, replace the horizontal assembly.

U14 pin 4

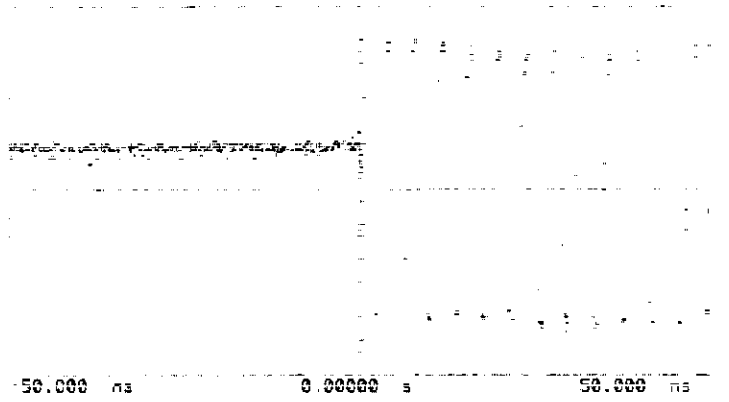


Figure 6D-80. On the Horizontal Assembly, 1KDPU, Trg'd Mode.

U15 pin 6

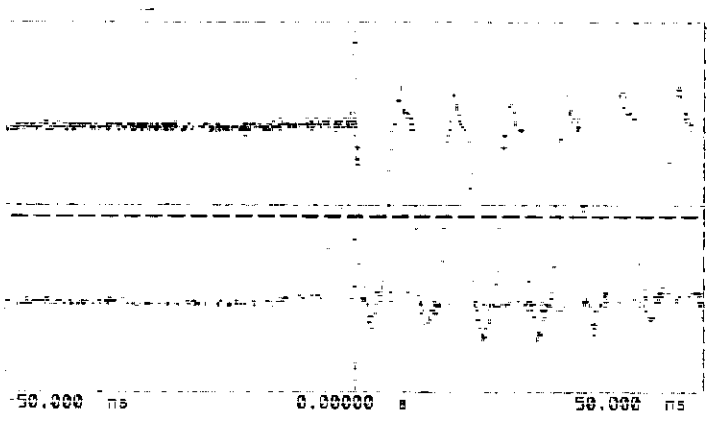
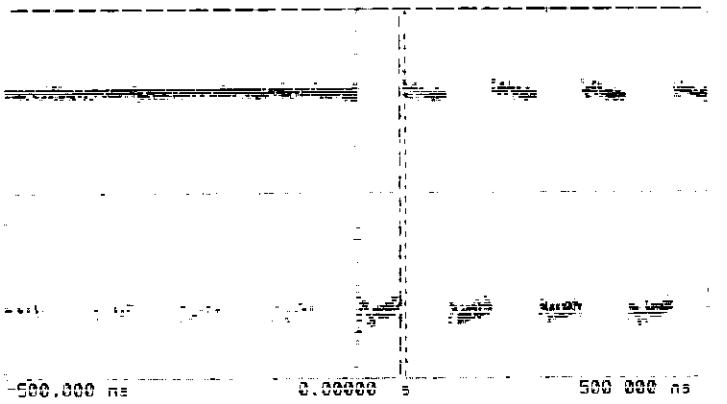


Figure 6D-81. On the Horizontal Assembly.

U16 pin 14



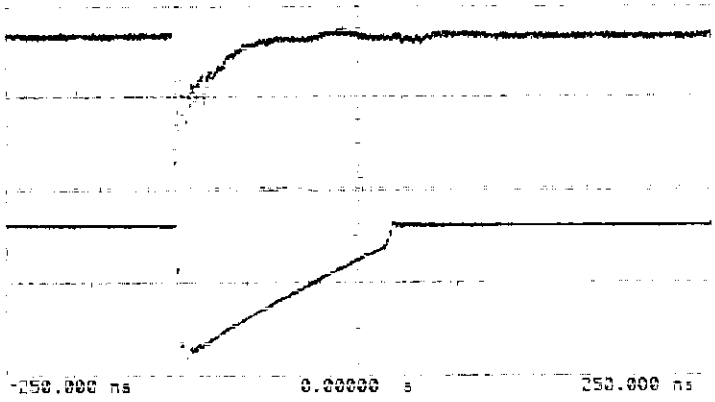

```
Ch. 1      =  200.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  100  ns/div               Delay      =  0.00000  s
Delta T    =  0.000   ns
Start      =  60.500  ns                Stop       =  60.500  ns
Delta V    =  0.000  volts
Vmarker1   = -412.0 mvolts              Vmarker2   = -412.0 mvolts

      Trigger mode : Edge
On  Neg. Edge on Chan1
Trigger Levels
Chan1     =    -1.300  volts
Holdoff   =    70.000  ns
```

Figure 6D-82. On the Horizontal Assembly.

U14 pin 11

J5 pin 1
or between
L1 & C41




```
Ch. 1      =  400.0 mvolts/div          Offset     = -544.0 mvolts
Ch. 2      =  4.000  volts/div          Offset     = -3.000  volts
Timebase   =  50.0 ns/div               Delay      =  0.00000  s

      Trigger mode : Edge
On  Pos. Edge on Chan2
Trigger Levels
Chan2     =    -2.180  volts
Holdoff   =    70.000  ns
```

Figure 6D-83. On the Horizontal Assembly.

U14 pin 11

U22 pin 11

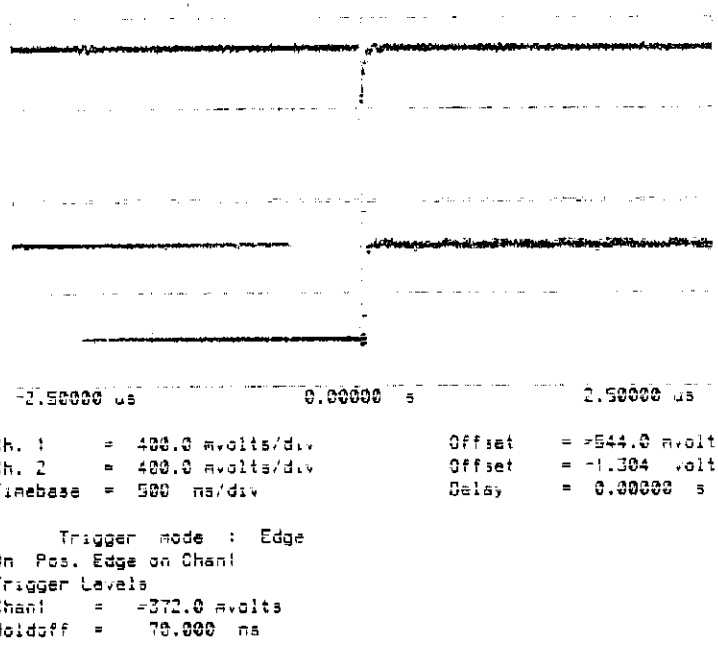


Figure 6D-84. On the Horizontal Assembly.

U14 pin 11

U22 pin 7

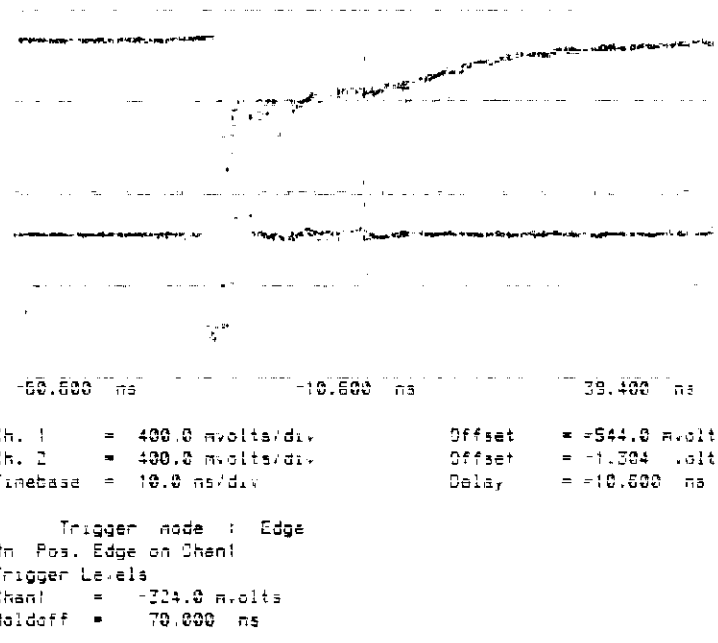
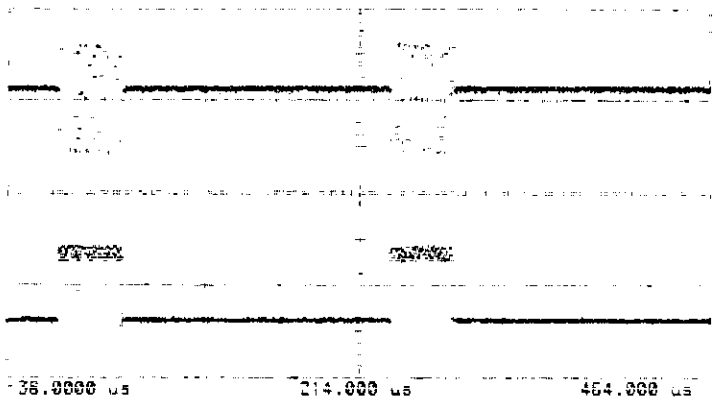


Figure 6D-85. On the Horizontal Assembly.

U14 pin 14

U1 pin 19



-36.0000 us 214.000 us 464.000 us

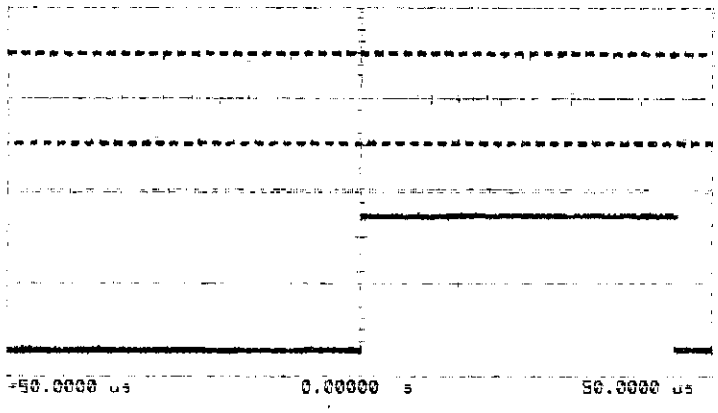
Ch. 1 = 400.0 mvolts/div Offset = 304.0 mvolts
Ch. 2 = 400.0 mvolts/div Offset = -276.0 mvolts
Timebase = 50.0 us/div Delay = -36.0000 us

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = -280.0 mvolts
Holdoff = 70.000 ns

Figure 6D-86. On the Horizontal Assembly.

U3 pin 8

U1 pin 19



-50.0000 us 0.00000 s 50.0000 us

Ch. 1 = 400.0 mvolts/div Offset = -368.0 mvolts
Ch. 2 = 200.0 mvolts/div Offset = -280.0 mvolts
Timebase = 10.0 us/div Delay = 0.00000 s

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = -280.0 mvolts
Holdoff = 70.000 ns

Figure 6D-87. On the Horizontal Assembly.

6D-34. COLOR MONITOR TEST

This test determines if the color monitor is faulty by checking horizontal sync pulses (HSYNC), vertical sync pulses (VSYNC), and color pulses (RGB) at the color monitor's input connector.

1. Turn mainframe's power switch to STBY.

2. Remove the mainframe's top and bottom covers.

3. Turn the mainframe's power switch to ON.
   Check the +120 V at the module power connector. Refer to figure 6D-88.
   The correct voltage should be between +118 V and +122 V.
   If the +120 V supply is incorrect, refer to the power supply troubleshooting procedure.

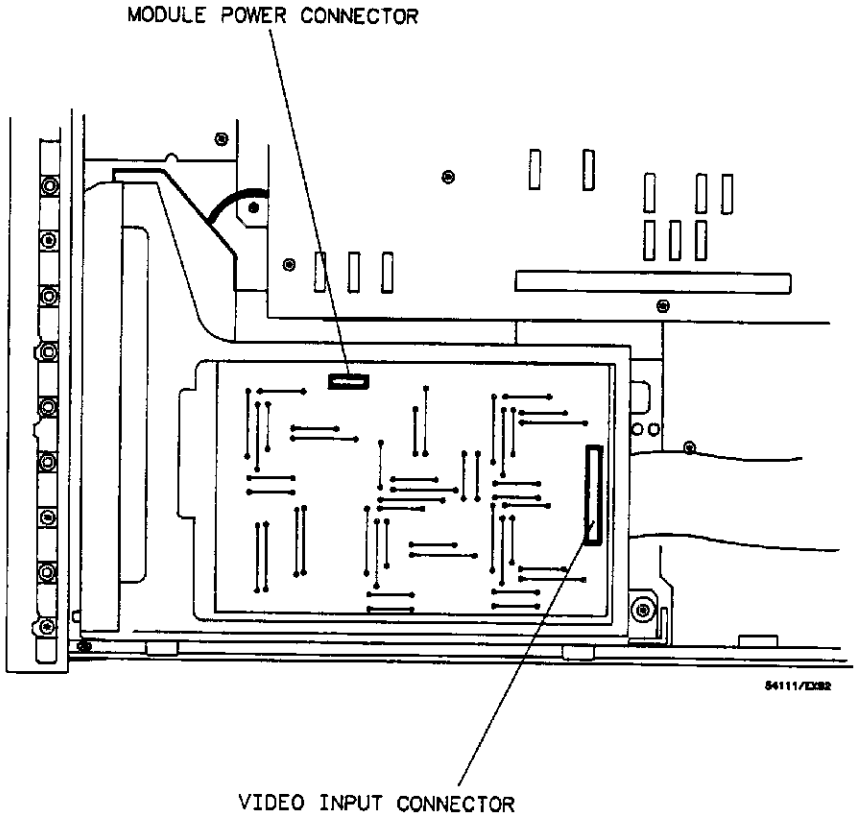


Figure 6D-88. Color CRT Module Input Connections.

4. Move the clear plastic shield on the bottom of color CRT module by pushing it rearward until it clears the front frame. Hinge the clear plastic shield away from the board.

5. Connect 10:1 divider probes to monitor oscilloscope.
   Connect channel 1 to vertical sync test point, pin 3 of video input connector.
   Connect channel 2 to horizontal sync test point, pin 7 of video input connector.
   The vertical and horizontal sync pulses are TTL levels and should resemble figure 6D-89.

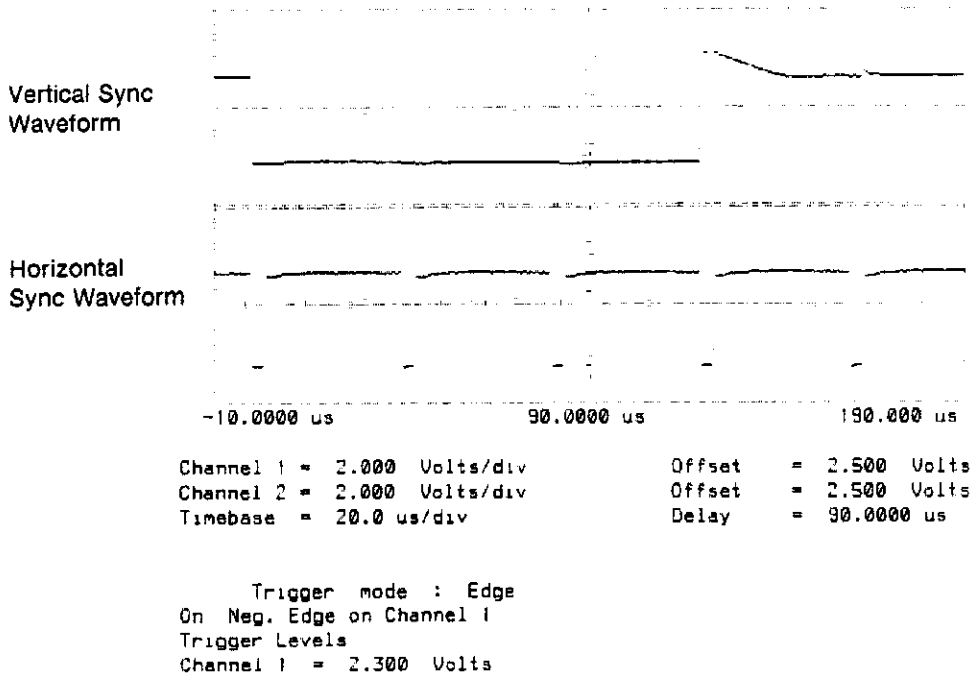
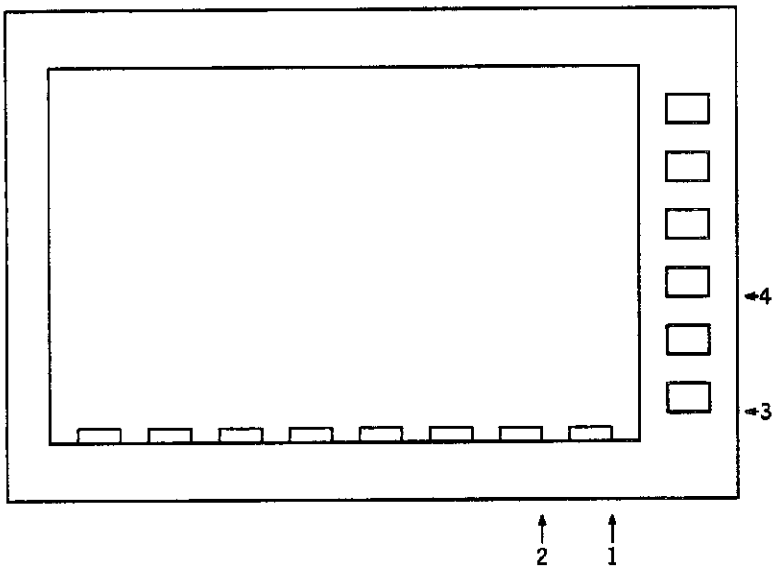


Figure 6D-89. Vertical and Horizontal Sync. Waveforms.

7. Before checking the video waveforms, try to get a known display on screen. If the display is operating, press ***more***, ***Utility***, ***CRT Setup Menu***, and ***Color Purity*** keys.
This will place a white raster on screen which means all video signals will be at maximum levels.

   If there is no display, try to get the same signals by pressing the following softkeys.
   IN BOTTOM ROW PRESS:
   1. Key at extreme right.
   2. Key second from right.

   IN VERTICAL COLUMN PRESS:
   3. Key at bottom.
   4. Key third from bottom.



8. Probe the following points. The video signals have a 0 V baseline and will vary in amplitude from 0 V to approximately 600 mV, depending on the characteristics of the colors displayed.

Video Signal	**Video Input Connector**
red	21
green	29
blue	37

9. The video signals can be loaded down by the color CRT module's input circuits. If the video signals were bad in step 8, disconnect the cable from the video input connector and recheck the signals on the color display assembly.

Video Signal	**J2 on Display Assembly**
red	14
green	18
blue	22
Sync Signals	**On display assembly**
Vert. sync	V.Sync TP
Horz. sync	H.Sync TP

10. If the video signals are now good, replace the color CRT module.

6D-35. COLOR CRT MODULE TESTING

It is time consuming to remove a suspected faulty color CRT module from the instrument. This test connects a good color CRT module outside the instrument without having to remove the suspected faulty monitor. This requires the use of parts from the HP 54100 family product support kit.

WARNING

Chassis ground on the color CRT module will be disconnected from the chassis ground of the instrument. This will leave the color CRT module chassis ground floating. Therefore, use an alligator clip lead to connect the monitor's chassis ground to the instrument's chassis ground.

1. Turn mainframe's power switch to STBY and remove power cable.
2. Remove mainframe's top and bottom covers.
3. Disconnect color CRT module power cable from primary power supply.
4. Connect a replacement power cable (54110-61601) from the product support kit to the primary power supply.
5. On instrument's bottom side, disconnect the wide ribbon cable from the suspected faulty color CRT module and extend it away from the instrument.
6. Place the known good color CRT module next to the instrument.
7. Connect the wide ribbon cable to the working color CRT module.
8. On the working color CRT module's bottom PC board is a connector labeled B-4, connect the power cable (from step 4) to this connector.
9. On the working color CRT module's bottom PC board is a connector labeled B-2, connect a display control cable from the product support kit to this connector.
10. Connect the CRT brightness control from the product support kit to the other end of the display control cable.
11. Reconnect the power cord and turn the instrument on.
12. If the display is now operational, the suspected faulty color CRT module in the instrument is bad.

6D-36. SOFTWARE TROUBLESHOOTING

Some failures cause the keyboards to lock up and prevent you from entering the troubleshooting menus. This procedure isolates which assembly is causing the problem. After the problem is repaired, return to the flow diagram.

1. Perform two key-down powerup routine.

2. Turn mainframe's power switch to STBY and remove the horizontal and A/D assemblies from the mainframe. Remove the ribbon cables from the assemblies.

3. Turn mainframe on. If there is a graphics pattern (core troubleshooting pattern) repeated displayed, go to step 4; otherwise go to step 10.

4. Turn mainframe's power switch to STBY and install the horizontal control assembly in the mainframe. Do not connect the ribbon cable.

5. Turn the mainframe's power switch to ON. If the core troubleshooting pattern is displayed on screen and the keyboards and display are still functional, go to step 6; otherwise replace the horizontal control assembly and return to flow diagram.

6. Turn the instrument's power switch to STBY and install the A/D assembly in the mainframe. Do not connect the ribbon cable.

7. Turn mainframe on. If the keyboards and display are still functional, go to step 8; otherwise replace the A/D assembly and return to flow diagrams.

8. Turn the mainframe's power switch to STBY and connect the ribbon cable to the horizontal control assembly only.

9. Turn mainframe on. If the keyboards and display are still functional, go to step 9; otherwise continue with step 8's instructions.
   Disconnect umbilical cable from test set. If display and keyboards are still functional, replace the horizontal assembly in the test set and return to the flow diagram.
   Disconnect umbilical cable from the mainframe. If the display and keyboards are still functional replace the umbilical cable and return to the flow diagram; otherwise replace the ribbon cable.

10. Turn the mainframe's power switch to STBY and connect the ribbon cable to the A/D assembly only.

11. Turn mainframe on. If the keyboards and display are still functional, go to step 9; otherwise continue with step 9's instructions.
    Disconnect umbilical cable from test set. If display and keyboards are still functional, replace the vertical assembly in the test set and return to the flow diagram.
    Disconnect umbilical cable from the mainframe. If the display and keyboards are still functional replace the umbilical cable and return to the flow diagram; otherwise replace the ribbon cable.

12. Replace the following assemblies in order and check the core troubleshooting pattern each time: CPU assembly, display assembly, I/O.

13. Return to flow diagram.

Appendix A Table of Contents

Chapter 1 General Information

Chapter 2 Accessory Kit Devices

Chapter 3 Making Accurate Measurements

Chapter 4 Making Good Connections

A1 General Information

Safety and Handling Precautions

Precautions that apply generally to Hewlett-Packard equipment, including the HP 54007A Accessory Kit, are explained in the Safety Considerations page. The devices in the kit, however, are not mechanically, electrically, or chemically hazardous, so no special safety precautions are necessary.

Extreme care must be taken in handling and storing these devices to protect them from mechanical damage. This is especially true in making connections, in order to avoid damaging the connectors and to avoid damaging the HP 54120T oscilloscope by electrostatic discharge (ESD) A detailed discussion of connection procedures appears later in this manual

The devices in the HP 54007A Accessory Kit have very precise mechanical tolerances, some on the order of one ten-thousandth of an inch (a few microns). Therefore, rough handling of any kind must be avoided. Do not permit any of the devices to fall on any hard surface or come in contact with dirt, oils, or abrasives The connectors must be clean and undamaged to ensure an accurate calibration.

The foam-lined storage case in which you receive the accessory kit is the best place to store the devices Never store any of the devices loose, in a desk drawer, or place them contact-end down on a table top The lid of the storage case is detachable and allows convenient storage, even in a shallow desk drawer.

Incoming Inspection

The foam-lined storage case provides enough protection for the accessory kit during shipping. If the case arrives in good condition, the devices are probably in good condition. If the case or devices appear to have been damaged, set aside the accessory kit and all packaging materials, contact the nearest Hewlett-Packard sales/support office listed inside the back cover of this manual.

Hewlett-Packard will arrange for repair or replacement of incomplete or damaged shipments without waiting for a settlement from the transportation company.

Enclosed is an entire parts list with illustrations to identify all devices in this kit. See Table A2-1 to verify that your shipment is complete

Equipment Required But Not Supplied

If you will be using SMA connectors in your calibrations or test setups, a precision connector gauge for measuring the contact pin locations of SMA connectors, as well as for connecting 3.5 mm precision connectors, is recommended. Please read the caution about SMA connectors (see Chapter 3, "Device Specifications"). Precision connector gauges for SMA connectors are available from Maury Microwave Corporation.

A few tools are required to make safe and repeatable connections with either the precision 3.5 mm connectors or SMA connectors.

- Torque wrench (optional) capable of 8 lb-in (90 N-cm) to install precision 3.5 mm devices to each other and the front panel connectors (HP part number 1250-1863, CD 7).
- Torque wrench (optional) preset to 5 lb-in for mating SMA connectors to precision 3.5 mm connectors (HP part number 8710-1582).

All precision 3.5 mm connectors must be visually inspected before use and cleaned (or replaced) as needed. The following equipment is required for cleaning

- An illuminated, 4-power magnifying glass for visual inspection of the connectors. The exact power of the glass is not critical, but the type of illumination is. Ordinary room lighting, or oblique lighting from a desk lamp casts shadows that can easily mask the small defects you are trying to see. Therefore, make sure that the magnifying glass has built-in lighting and provides axial, shadowless illumination. Illuminating magnifying glasses are available from most equipment suppliers. Hewlett-Packard does not sell or recommend any particular model

- Compressed air in a pressurized can, HP part number 92193Y, can be used to blow dust and lint from the connectors. Any source of clean, dry, low-pressure air can be used if it has an effective oil-vapor filter and condensation trap placed just before the air outlet hose.

When using compressed air from a pressurized can, hold the can upright. If the can is tilted or inverted, the liquid propellant sprays out with the air. The propellant evaporates instantly on the connector surface and causes the connector to become too cold for the calibration to continue. If this happens, you must wait until thermal equilibrium is re-established within the allowable temperature range before continuing the calibration. Permanent connector damage from the propellant is unlikely.

- Liquid Freon (trichlorotrifluoroethane), HP part number 8500-1914, CD 7, is the only cleaning solvent recommended by Hewlett-Packard for cleaning 3.5 mm connectors. Several types of liquid Freon exist, so make sure that the kind you use contains only trichlorotrifluoroethane. Some other types contain harmful compounds which can damage precision connectors. A liquid is preferred over spray because the liquid can be applied sparingly and selectively. If a spray must be used, spray the cleaning swab only, not the connector.

Do not use any solvents other than liquid Freon. They can leave residues that react destructively with the metal plating on the connectors, or erode essential plastic dielectric supports. Along with your supply of solvent, keep a microscope slide or a similar piece of clear glass to check the solvent periodically for contamination.

- Plastic foam swabs, HP part number 9300-0468 CD 1, are used along with liquid Freon to clean the connector surfaces. These swabs resemble common swabs, but have lint-free plastic foam tips.

Replaceable Parts

To order an HP part, list the description, HP part number with check digit (CD), and the quantity desired. Send your order to the nearest Hewlett-Packard sales/service office.

See Table A2-1 for individual Hewlett-Packard part numbers of all components in the HP 54007A Accessory Kit.

A2 Accessory Kit Devices

Introduction

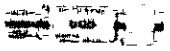
This chapter describes and explains the uses of the components of the HP 54007A Accessory Kit. All precautions apply to the uses covered in this chapter.

Table A2-1. Parts List for HP 54007A Accessory Kit

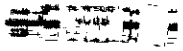
Part Number	CD	Description	Qty Per
11667B	8	Power Splitter, APC-3.5 (f)	1
1250-1748	7	Adapter, APC-3.5 (m-m)	1
1250-1869	3	7.5 cm Airline, APC-3.5 (f)	1
1250-2127	8	Coaxial Short, APC-3.5 (f)	1
1250-2128	9	Coaxial Short, APC-3.5 (m)	1
33340C 006	2	6 dB Attenuator, APC-3.5 (f-m)	1
33340C 040	2	40 dB Attenuator, APC-3.5 (f-m)	1
54007-29301	0	Foam liner, accessory kit	1
54007-61601	1	6 cm Semi-rigid L, SMA (m-m)	2
54007-61602	2	3 cm Semi-rigid L, SMA (m-m)	1
54007-85501	0	Box, Walnut	1
54007-90901	5	Operating Note-Accessory Kit	1
8120-4941	0	17 in. Coaxial Cable Assy, APC-3.5 (f-f)	1
8120-4942	1	17 in. Coaxial Cable Assy, APC-3.5 (f-m)	1
909D	4	50 ohm Termination, APC-3.5 (m)	1
909D 011	4	50 ohm Termination, APC-3.5 (f)	1

1250-2128, CD 9,
Coaxial Short (m)

1250-2127, CD 8;
Coaxial Short (f)



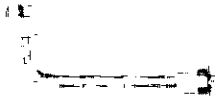
HP 33340C, CD 2;
6 dB Attenuator (f-m)



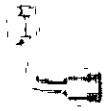
HP 33340C, CD 2;
40 dB Attenuator (f-m)

HP 909D, CD 4;
50 Ω Terminator (m)

HP 909D, CD 4;
50 Ω Terminator (f)



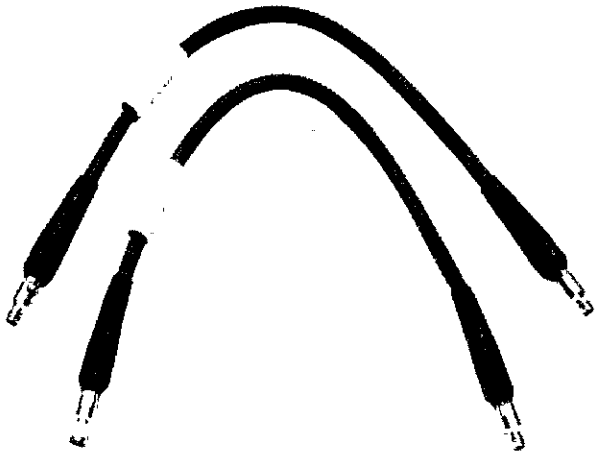
54007-61601, CD 1;
6 cm Semi-Rigid L (m-m)



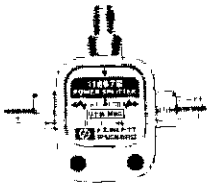
54007-61602, CD 2;
3 cm Semi-Rigid L (m-m)

1250-1876, (not included in HP 54007A) 15 cm Beadless Airline

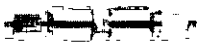
1250-1869, CD 3, 7.5 cm Beadless Airline



8120-4941, CD 0; 17 in. Coaxial Cable Assembly (f-f)
8120-4942, CD 1; 17 in. Coaxial Cable Assembly (f-m)



HP 11667B, CD 8,
Power Splitter (f)



1250-1748, CD 7,
Adapter (m-m)

7.5 cm Beadless Airline

A 7.5 cm beadless airline has been included in the HP 54007A Accessory Kit for use in discontinuity separation and isolation. This device, although not a perfect termination, can improve and reduce reflections, increase the round-trip time of reflections, or isolate perturbations in the circuit.

The airline is a known 50 Ω load and is a good reference. Due to this fact, the primary uses are as follows:

1. The primary use of the 7.5 cm beadless airline is to separate perturbations. If you place a known load between perturbations you can spatially separate known perturbations from those in the device-under-test and evaluate each individually

2. The airline can be used as a precision 50 Ω load during reflection calibrations. Place the airline at the reference plane and increase the timebase until the end of the airline is offscreen (to the right). This yields a 50 Ω reference dependent only on the mechanical dimensions of the airline.

3. By placing the airline on the HP 54121A test set, the device-under-test can be separated from the incident edge. This is convenient for viewing data that is close to the incident edge, plus you can see the 50 Ω reference more clearly in relation to the device-under-test.

Connecting the 7.5 cm beadless airline is a very sensitive procedure. More care must be taken than for normal connections. First verify that the center conductor is properly oriented when installed; the male end of the center conductor should be at the end of the outer conductor with the connector nut.

CAUTION

Wear a grounded wrist strap and discharge static electricity by grasping the outer shell of the test port briefly before you begin making the connection. When connecting the airline, you are touching exposed center conductors that are connected to the internal circuits of the HP 54120T oscilloscope.

The airline is small, and the center and outer conductors are almost the same length, so connecting the center conductor at the same time as the outer conductor is difficult. But, it is also difficult to slide the outer conductor over the center conductor without risking damage to the inner surface of the outer conductor. Therefore, check the center conductors to see if they have mated after the outer conductors have been loosely connected. Pressing gently on the end of the center conductor with a plastic rod will usually mate the conductors.

Connect the airline as follows:

1. Retract the connector nut on the airline fully. Put the center conductor into the airline and verify that the female end of the center conductor emerges from the female end of the outer conductor. This end will be connected to the test set.

2. Hold the airline and center conductor, bring both the airline and center conductor to the test port connector. Carefully align and mate the center conductors. Then make a preliminary connection by fastening the test set connector nut finger tight. In handling the center conductor, use lint-free gloves or finger cots.

3. When the preliminary connection has been made, verify that the center conductors have mated by pressing gently on the end of the center conductor with a plastic rod.

4. Connect the termination device to the opposite end of the airline. Carefully align and mate the center conductor of the device with the center conductor of the airline. Then make a preliminary connection of the terminating device and the airline by fastening connector nut finger tight.

Now make the final connections:

5. Start at the test port with the counter-rotation technique (see Figures A4-9 and A4-10) to eliminate air wedges from this connection. After counter-rotation, retighten the connection finger tight and use a torque wrench to make the final connection. Support the airline when making connections to avoid applying lateral or vertical (bending) force.

6. Tighten the connection of the termination device or adapter on the airline with the counter-rotation technique. You will have to hold the airline firmly to prevent loosening the test port connection. After counter-rotation, retighten the connection finger tight and use the 3.5 mm connector torque wrench to make the final connection.

Disconnect the airline by reversing the above procedure.

15 cm Beadless Airline

The 15 cm airline is not included in the HP 54007A Accessory Kit. This device will enhance testing lines and reading reflections by extending the time before they are returned and displayed. The time extension is significant. It will allow you to take measurements without the fear of a known perturbation in the circuit. The 15 cm beadless airline gives greater separation between a known perturbation and perturbations of the device-under-test.

Connection procedures are the same as for the 7 5 cm airline.

The HP 54007A storage box has been designed to accommodate the 15 cm beadless airline.

Model 909D 50 Ω Terminator

The HP 909D is a precision, low-reflection load for terminating 50 Ω coaxial systems in their characteristic impedance. When trying to normalize out gross perturbations the precision 50 Ω becomes more important. The HP 909D is used to improve the quality of precision reflection measurements and normalize the HP 54120T to precision specifications.

The HP 909D comes with the rugged APC-3.5 connector for measurement repeatability even after hundreds of connections.

The performance is specified to 26.5 GHz. Based on limited tests the expected SWR at 34 GHz is in the range of 1.3, and the HP 909D will operate to 39 GHz before higher mode resonances have any significant effect

Impedance stability with both time and temperature, a key parameter for precision terminations, is achieved by using tantalum nitride on sapphire thin film technology.

Maintenance

The HP 909D is used for precise measurements so it must be kept in top operating condition. Hewlett-Packard recommends that the connector be inspected periodically and cleaned if necessary. It is also recommended that the HP 909D be verified annually or after 1000 connections.

Specifications

Frequency Range. dc to 26.5 GHz
Impedance: 50 Ω
SWR: 1.02, dc-3 GHz
1.036, 3-6 GHz
1.12, 6-26.5 GHz
(At 26.5 GHz the typical SWR is 1.1. Statistically, 90% of the terminators produced will meet this performance).
Power Rating: 2W ave @ 20° C derated to 1 W ave. at 75° C
100 W peak (10 μs max. pulse width) @ 20° C
Connector APC-3.5 male; Opt.. 011, APC-3.5 female.
Dimensions: 23 mm x 4 mm diameter (0.91 in x 0.16 in diameter).

Environment

In a non-operating environment the terminator should be stored in a clean, dry place. The following environmental limitations apply to both storage and shipment (unless stated otherwise in the Data Sheet).

a. Temperature: -55 to $^{+}75^{\circ}$ C
b. Humidity: < 95% relative @ $^{+}40^{\circ}$ C
c. Altitude: < 15,300 metres (50,000 ft)

The operating environment of the instrument should be within the following limitations (unless stated otherwise in the Data Sheet).

a. Temperature: 0 to $^{+}55^{\circ}$ C
b. Humidity: < 95% relative at $^{+}40^{\circ}$ C
c. Altitude: < 4500 meters (15,000 ft)

CAUTION

Storage or operation of the instrument in an environment other than that specified may cause damage to the instrument and may void the warranty.

Coaxial Attenuators

The HP 33340C coaxial fixed attenuator offers broad frequency coverage, low SWR and small size. The attenuator is available in nominal attenuation values of 3, 6, 10, 20, 30 and 40 dB. It is fully tested to meet specifications at all frequencies and over most of the frequency band. It will typically perform much better than specified.

The HP 33340C attenuator is included in this kit in the 6 dB and 40 dB values.

Applications

One of the main applications is to reduce the power to critical microwave circuits to avoid possible damage. Another application is to "pad" badly matched devices, such as mixers in order to minimize SWR. Use of the HP 33340C will not only protect your instrument, it also increases the input signal range.

Specifications

Frequency range: HP 33340C dc - 26.5 GHz

Attenuation Accuracy:	6 dB	40 dB
HP 33340C		
dc-18.0 GHz	0.6 dB	1.0 dB
dc-26.5 GHz	0.6 dB	1.3 dB

SWR:	6 dB	40 dB
HP 33340C		
dc-8 GHz	1.10	1.10
8-12.4 GHz	1.15	1.15
12.4-26.5 GHz	1.27	1.25

Attenuation Range:	6 dB	40 dB	20 dB
HP 33340C			
	5.0	100	10

Temperature, stability: HP 33340C 0.0002 dB/dB/° C
Maximum input power: 2W ave @ 20° C derated to 1W ave at 75° C,
100 W peak
Power sensitivity: 0.001 dB/w
Connectors 33340C, APC-3.5 (m,f)
Weight: HP 33340C, 8.5 g (0.3 oz)

Environmental

Temperature, non-operating: -55 to $^{+}85^{\circ}$
Temperature, operating: -40 to $^{+}75^{\circ}$
Altitude, non-operating: 50,000 feet
Altitude, operating: 15,000 feet
Humidity: cycling 5 days, 40° C at 95% RH with condensation
Vibration: 7 G's 5-2000 Hz
Shock: 500 G's, 1.8 ms in six directions.
EMC: radiated interference is within Mil Std. 461 method RE02, VDE 0871 and CISPR Publication 11

Coaxial Short

The coaxial short is a precision, low-inductance device that will give an accurate representation of frequency information of reflected energy. It can provide a precision reference point for TDNA calibration as a time reference. It can be used to determine a baseline reference (voltage) for absolute ground.

The short is used in calibration of dielectric and velocity constants because it has a precision time offset of 21.17 ps and can be either deducted out of measurements, or more commonly, the offset is < 1% and has no bearing on the measurement.

Both male and female shorts have the same electrical length.

Test Port Return Cables

The 17 in. test port return cables are used in performance verifications (see *HP 54120T 20 GHz Digitizing Oscilloscope Service Manual.*) They are included in the HP 54007A Accessory kit for low loss network measurements. And they are flexible for hard-to-access areas. The lengths are matched so that the reflection path length equals the transmission path length and both measurements can be made in the same timebase setting. The flexible cables are not precision impedance devices.

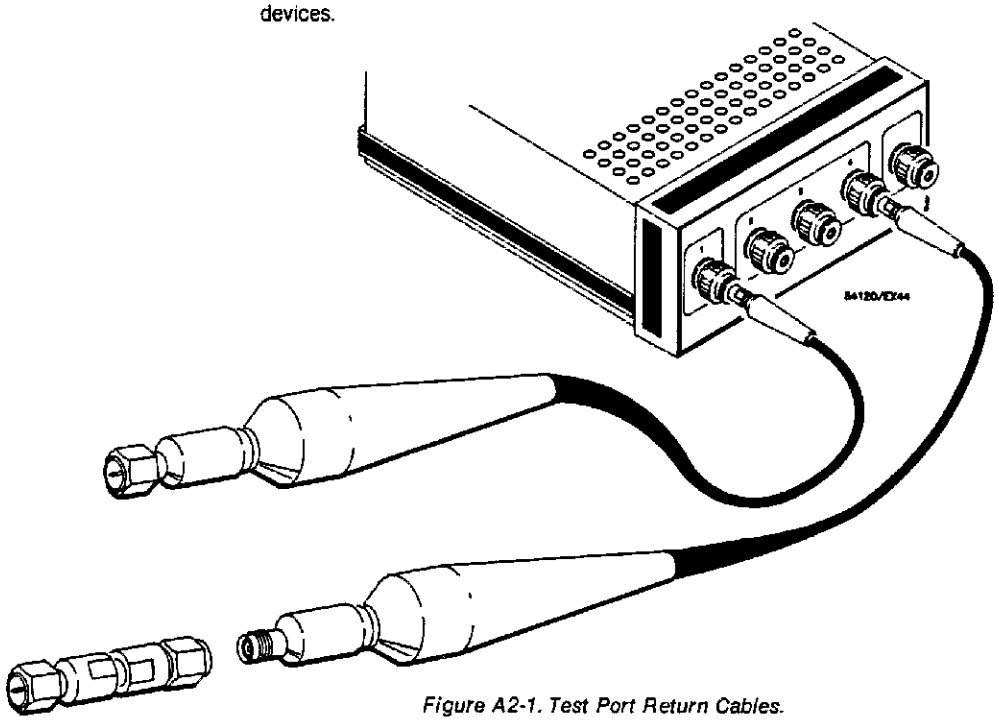


Figure A2-1. Test Port Return Cables.

The cables included in the accessory kit have female-to-female and male-to-female end connectors. The male and female ends of the two cables allow direct connection for calibrating the transmission path. This implies that the device under test should be equipped with male and female connectors (see Adapter (m-m)).

Characteristics

Impedance 50 Ω
Capacitance: 26 pF/ft (85.3 pF/metre)
Time delay: 1.2 ns/ft (3.9 ns/metre)
Velocity of Propagation: 85% of C
Dielectric Constant: 1.4
Jacket Withstand: 1.0 kV
Dielectric Withstand: 1.0 kV
Center Conductor: 15 AWG solid
Minimum Bend Radius: 25 mm (1 Inch)

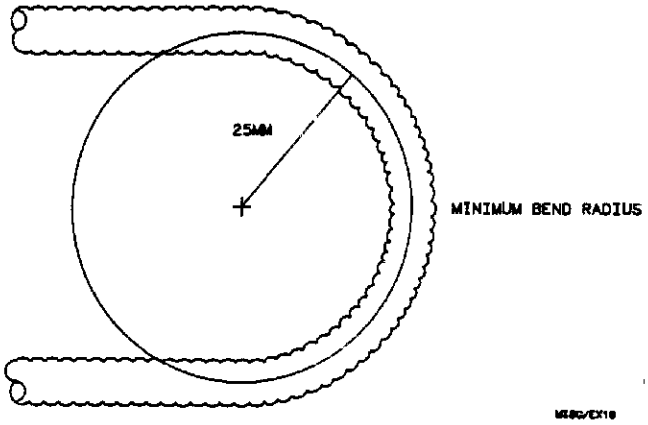


Figure A2-2. Minimum Bend Radius.

To prolong the life of these cables, minimize repeated bending to a tight radius. Do not exceed the 25 mm radius specification

VSWR

2-4 GHz < 1.15
4-8 GHz < 1.25
8-18 GHz < 1.30
18-26.5 GHz < 1.35

Insertion Loss

0-4 GHz < 0.36 dB
4-8 GHz < 0.50 dB
8-12 GHz < 0.60 dB
12-16 GHz < 0.72 dB
16-18 GHz < 0.80 dB
18-26.5 GHz < 1.0 dB

Note

VSWR and Insertion loss are typically 10% better than characterized.

Adapter (m-m)

The m-m Adapter is a precision APC-3.5 device used to change connector sex. Many situations will arise when both ends to be connected are female. Placing a m-m Adapter will not change the circuit characteristics other than the electrical length The electrical length is approximately 137 ps and the mechanical length is 41 mm. These dimensions are approximate and should be verified before any critical measurements are made.

If, when using the test port return cables, the input has two female connections, this adapter can be connected to the device-under-test. This hook-up will add 137 ps to your measurement.

Semi-Rigid L Connectors

The semi-rigid "L" connectors are used to create network connections and access different channels or functions simultaneously This allows you to view the trigger signal, attenuate the TDR signal, or connect and configure any way you desire (see Figures A2-2 and A2-3).

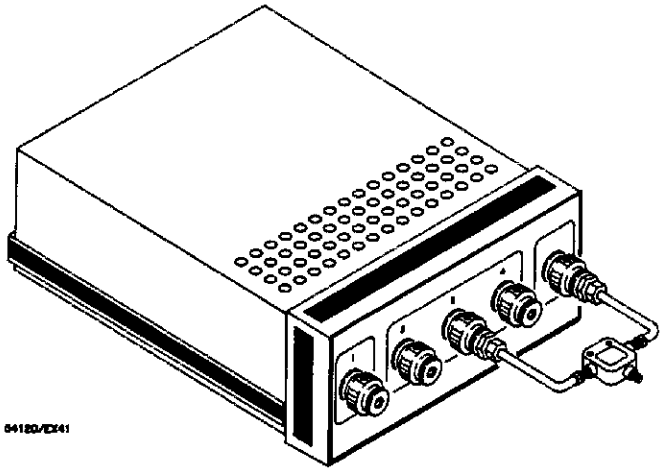


Figure A2-3. Viewing the Trigger Signal.

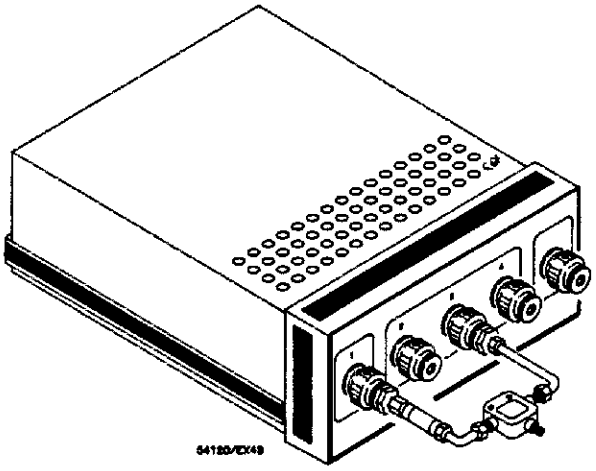


Figure A2-4. Attenuating the TDR Signal.

Power Splitter

This section contains operating and service information for the HP 11667B power splitter (see in Figure A4-4). It explains how the operator checks this device and describes the one performance test required to test tracking between the output arms.

Description

The HP 11667B is a two-resistor power splitter used in oscilloscope measurement systems that have one output arm for triggering the HP 54120T oscilloscope. The power splitter is useful for making attenuated TDR measurements.

Safety Considerations

Do not apply more than +27 dBm RF CW power to the HP 11667B, or the power splitter may be damaged.

Specifications

These are performance standards or limits against which the instrument may be tested.

Frequency Range: dc to 26.5 GHz
Maximum Input Power: +27 dBm (0.5W)

	dc to 18.0 GHz	dc to 26.5 GHz
Input SWR:	1.22	1.29
Equivalent Output SWR: (leveling or ratio measurement)	1.22	1.22
Output Tracking: (between output arms)	0.25 dB	0.40 dB

Connectors: Precision 3.5 mm (f) on all ports
Dimensions: 47 mm X 40 mm X 10 mm (1.85 in x 0.39 in)
Shipping Weight: 0.14 kg (4.94 oz)

Supplemental Characteristics

These are not specifications, but typical characteristics included as additional information for the user.

	Frequency (GHz)	
	dc to 18.0	dc to 26 5
Phase Tracking (between output arms)	1.5°	2.5°
Output Tracking	0.25 dB	0.40 dB

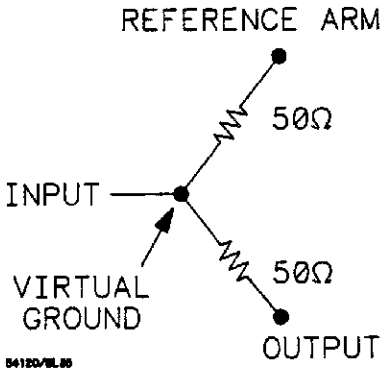


Figure A2-5. HP11667B Schematic.

Connections

Follow all handling precautions discussed in chapter A4 and maintain all device specifications while handling, connecting, or disconnecting the power splitter

Operating Environment

Temperature, 0 to 55° C (32 to 131° F)
Humidity, Up to 95% relative
Altitude, Up to 4,572 metres (15,000 feet)

Storage and Shipment

Temperature, -40 to +75° C (-40 to +167° F)
Humidity, Up to 95% relative
Altitude, Up to 7,620 metres (25,000 feet)

Protect the HP 11667B from temperature extremes that could introduce internal condensation.

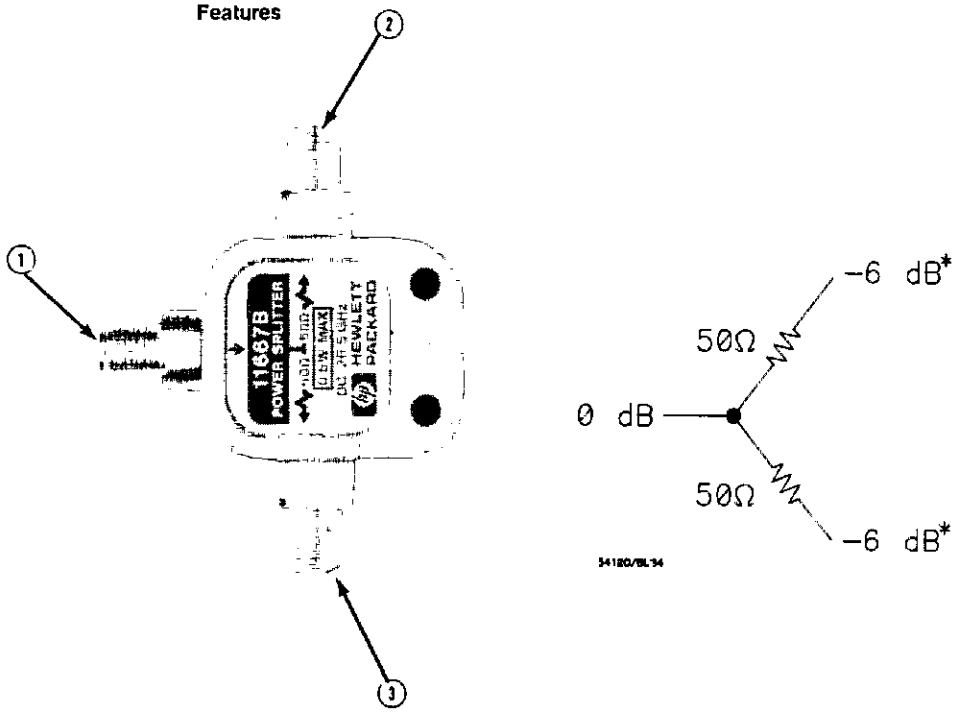


Figure A2-6. Power splitter.

1. Input port for incoming signal

2. 3 Output ports used as exit ports Output signal is 6 dB down in power from input signal. Either port may be used as test or reference port since power is equal in both ports.

* Typical in 50 Ω system at dc Loss typically increases 0 05 dB/GHz

A3 Making Accurate Measurements

Introduction

This chapter acquaints you with the operating conditions and procedures necessary to use the devices properly. Familiarize yourself with this information before trying any measurements.

Hewlett-Packard guarantees that the performance of your calibration devices will equal or exceed the listed specifications. Certain operating procedures must be followed if these specifications are to be met and maintained, due to the precision of the devices and to the performance capabilities of the HP 54120T oscilloscope.

The performance of the TDNA calibration devices described in Device Specifications are the performance values guaranteed by Hewlett-Packard. Characteristics are typical, or nominal, values

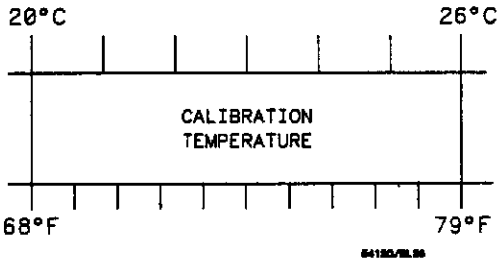
Operating Conditions and Procedures

Temperature, wear of the precision 3.5 mm connectors, and operator skill can all significantly affect the accuracy and repeatability of microwave measurements.

Temperature

Temperature of the calibration devices is critical because the dimensions of the devices (electrical characteristics) change with temperature. Figure A3-1 illustrates the allowable environmental conditions for using the HP 54007A kit. These conditions must be met if accurate measurements are to be obtained.

Note that the operating temperature during calibration and actual device measurements must be 20-26° C (68-79° F). During device measurements, the operating temperature must be within ±1° C (1.8° F) of the temperature during calibration. Thus, if the calibration was done at 22° C (71.6° F) the operating temperature must be 21-23° (69.8-73.4° F). If the work area is subject to temperature fluctuations, you might want to record the temperature at which the calibration is made, to assure repeatability and accuracy.



Operating temperature during actual measurements must be within ± 1° C (±1.8° F) of the calibration temperature.

Storage temperature: **Min -40° C (-40° F)**
Max +65° C (+149° F)

Relative humidity: 20-80% (30° C maximum wet bulb) during operation, 5-95% during storage; non-condensing at all times.

Barometric pressure (expressed as altitude): <4500 metres (15,000 ft) during operation, <15,000 during storage.

Figure A3-1. Allowable Temperature, Humidity, Pressure.

The temperature of the calibration devices and all connectors must be stable before use. Devices kept with the oscilloscope are usually at a stable temperature and can be used immediately. Devices that have been moved from one location to another should be allowed to reach the same temperature as the oscilloscope

Heat Source Your fingers are also a heat source. Normal body temperature is 37° C (98.6° F). You should avoid unnecessary handling of the devices during use. Some devices have a plastic jacket over the connector body to provide thermal insulation during handling. Barometric pressure and relative humidity also affect device performance, although less than temperature. Air exists between the inner and outer conductors of these devices (air-dielectric devices), and the dielectric constant of air depends on pressure and humidity (see Figure A3-2)

Wear Connector wear will eventually degrade performance. The calibration devices, which are typically used only a few times each day, should have a very long life However, because the connectors often undergo many connections a day, they wear rapidly. Therefore, it is essential that all connectors on the HP 54120T oscilloscope test set be inspected regularly, both visually (with a magnifying glass) and mechanically (with a connector gage), and replaced as necessary. Procedures for visual and mechanical inspection are given in the next section of this manual. For test sets used in high-volume work, it is best to place an adapter on both the input and the output ports. It is easier and cheaper to replace a worn adapter than a worn test set connector.

Skill Operator skill in making good connections is essential. The mechanical tolerances of the precision 3 5 mm connectors used in the HP 54007A kit are two or three times better than the tolerances in regular 3.5 mm connectors. Slight errors in operator technique that would go unnoticed with regular connectors often appear with precision connectors in the calibration kit. Incorrect operator technique can often result in lack of repeatability. Carefully study and practice the connection procedures that are explained later in this manual until your calibration measurements are consistently repeatable.

Device Specifications

Electrical specifications depend upon several mechanical conditions. A 3.5 mm connector is a precision connector dedicated to very specific tolerances. SMA connectors are not precision mechanical devices. They are not designed for repeated connections and disconnections and are very susceptible to mechanical wear. They are often found, upon assembly, to be out of specification. This makes them potentially destructive to any precision 3.5 mm connectors with which they might be mated.

CAUTION

Use extreme caution when mating SMA connectors with 3.5 mm precision connectors. Prevent accidental damage due to worn or out-of-specification SMA connectors. Such connectors can destroy a precision 3.5 mm connector, even on the first connection.

Hewlett-Packard recommends that you keep three points clearly in mind when you mate SMA and precision 3.5 mm connectors.

SMA Inspect

1 Before mating an SMA connector (even a brand new one) with a precision 3.5 mm connector, carefully inspect the SMA connector, both visually and mechanically with a precision connector gauge designed to measure SMA connectors A male SMA connector pin that is too long can smash or break the delicate fingers on the precision 3.5 mm female connector. Gauging SMA connectors is the most important step you can take to prevent damaging your equipment.

Alignment

2 Be careful with alignment Push the two connectors together with the male contact pin precisely concentric with the female. Do not overtighten or rotate either center conductor Turn only the outer nut of the male connector and use a torque wrench (5 lb.in., 60 N-cm) for the final connection Note that this torque is less than that when mating precision 3.5 mm connectors with each other. A torque wrench suitable for SMA connectors preset to 5 lb.in is available (HP part number 8710-1582, CD 0)

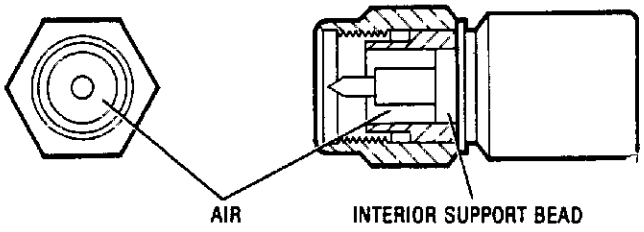
Install an adapter on the test set if many connections and disconnections will be made. Then, if accidental damage does occur, the adapter is all that needs to be replaced. It is easier and cheaper to replace a damaged adapter than an entire test set connector.

SMA connectors can then be mated with precision 3.5 mm connectors without difficulty or fear of expensive and time-consuming repairs.

Mismatch

3. Significant structural and dimensional differences exist between these two types of connectors. Precision 3.5 mm connectors, also known as APC-3.5 connectors, are air-dielectric devices. Only air exists between the center and outer conductors. The male or female center conductor is supported by a plastic "bead" within the connector. In SMA connectors, a plastic dielectric supports the entire length of the center conductor. In addition, the diameter of both the center and outer conductors of an SMA differ from that of a precision 3.5 mm connector.

Precision 3.5 mm Connector



SMA Connector

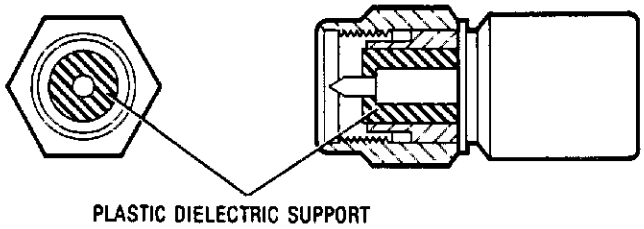


Figure A3-2. SMA and Precision 3.5 mm Connectors.

When an SMA connector is mated with a precision 3.5 mm connector, the connection exhibits a continuity mismatch (SWR), typically about 1.10 at 20 GHz. This mismatch is less than when two SMA connectors are mated, but still higher than when precision 3.5 mm connectors are mated. Keep this fact in mind when making measurements on SMA and precision 3.5 mm coupled junctions.

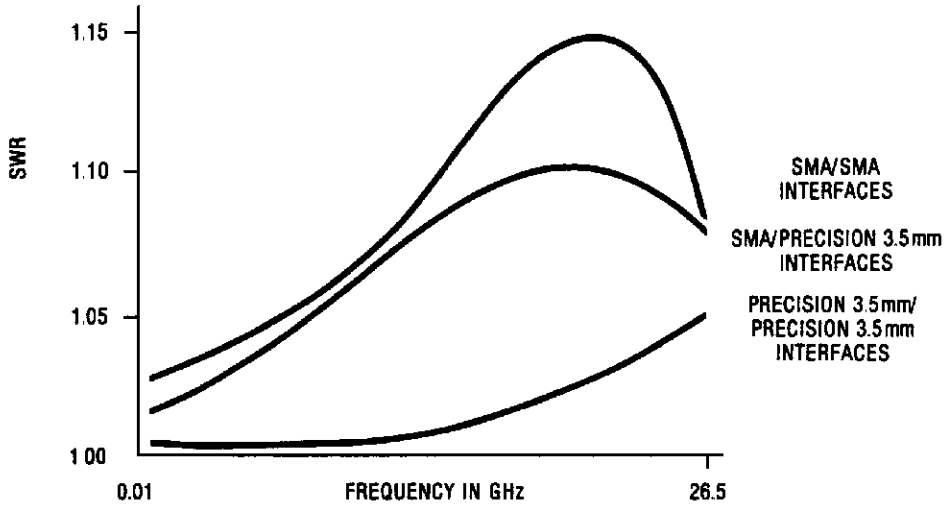


Figure A3-3. Typical SWR of SMA and Precision 3.5 mm Connectors.

A4 Making Good Connections

Introduction

This chapter explains the operating procedures which must be followed to obtain an accurate TDNA calibration

Accuracy requires that 3.5 mm precision connectors be used, however, SMA connectors can be used if special care is taken when mating the two, and all connectors are undamaged and clean. Before each use, the mechanical dimensions of all connectors must be checked with a connector gauge to make sure that the center conductors are positioned correctly All connections must be made for consistent and repeatable mechanical (and therefore electrical) contact between the connector mating surfaces

Carefully study and practice all procedures in this chapter until you can successfully perform them repeatedly. Accuracy and repeatability are critical for good microwave measurements. Note that the device connection procedures differ in several important ways from traditional procedures used in the microwave industry. Hewlett-Packard procedures have been developed through careful experimentation.

Handling Precision 3.5 mm Connectors

Precision 3.5 mm connectors must be handled carefully if accurate calibrations and measurements are to be obtained.

- Store the devices in the foam-lined storage case when not in use.
- Avoid bumping or scratching any part of the mating surfaces.
- Be careful to align the center connectors. Check the alignment carefully before tightening the connector nuts

- Use a torque wrench for all final connections in order to avoid overtightening.

- Support the devices being used in order to avoid vertical or lateral force on any connectors. This precaution is critical when using the airline, 6 cm "L", or cables.

When disconnecting devices:

- Do not rock or bend any connections.

- Pull the connector straight out without unscrewing or twisting.

- Before storage, screw the connector nut all the way out to help protect the surfaces, and use the plastic caps provided. These plastic caps can be taken off easily by unscrewing, rather than pulling.

CAUTION

Do not use a damaged or defective connector. It will damage any good connector to which it is attached. Throw the connector away or have it repaired.

A connector is bad if it fails either the visual or mechanical examinations or when an experienced operator cannot make repeatable connections. The time and expense involved in replacing test set connectors warrants considerable caution when any connector might be less than perfect.

If any doubts exist about a connector, call your Hewlett-Packard representative. HP field offices offer limited professional advice and have access to the factory for information.

Visual Inspection and Cleaning

Always begin a calibration with a careful visual inspection of the connectors, including the test set connectors to make sure they are clean and undamaged.

CAUTION

Make sure that you and your equipment are grounded before touching any center conductor so you won't cause static electricity and create a potential for electrostatic discharge. When using or cleaning connectors on the test set, be aware that you are touching exposed center connectors that are connected directly to the internal circuits of the oscilloscope. Touching the center conductor, especially with a wiping or brushing motion, can cause an electrostatic discharge (ESD) and severely damage these sensitive circuits.

Visual Inspection

Use an illuminated, 4-power magnifying glass (see Figure A4-1) for visual inspection.

1. Before you begin, make sure you and any equipment you are using are grounded to prevent electrostatic discharge.
2. Examine the connectors first for obvious problems, such as deformed threads, contamination, or corrosion
3. Next concentrate on the mating surfaces of each connector. Look for scratches, rounded shoulders, misalignment, or any other signs of wear or damage.
4. Make sure that the surfaces are clean, free of dust and solvent residues.

Dirt or damage visible with a 4-power magnifying glass can cause degraded electrical performance and possible connector damage. All connectors should be repaired or discarded immediately

Cleaning Cleaning the connectors is seldom necessary. Dust or dirt on the connector surfaces can be brushed or wiped away gently with a plastic foam swab or low-pressure, clean, compressed air. Be sure that you and all of your cleaning equipment are grounded to avoid electrostatic discharge.

If necessary, liquid Freon (trichlorotrifluoroethane), HP part number 8500-1914 CD 7, is the only cleaning solvent recommended by Hewlett-Packard for cleaning 3.5 mm connectors. Several types of liquid Freon exist, so make sure that the kind you use contains only trichlorotrifluoroethane. Some other types contain harmful compounds which can damage precision 3.5 mm connectors. Using the solvent in liquid is preferred because the liquid can be applied sparingly and selectively. If spray must be used, spray the cleaning swab only, not the connector. Use a microscope slide, or similar piece of clear glass to check the solvent periodically for contamination (see Figure A4-1).

CAUTION

Do not, under any circumstances, use abrasives (not even pencil eraser) or any solvent other than trichlorotrifluoroethane. Residue can be left behind that can damage the metal connector surfaces and the plastic conductor supports.

When you are satisfied that all the connectors are clean and undamaged, you can proceed to the mechanical inspection of connector dimensions.

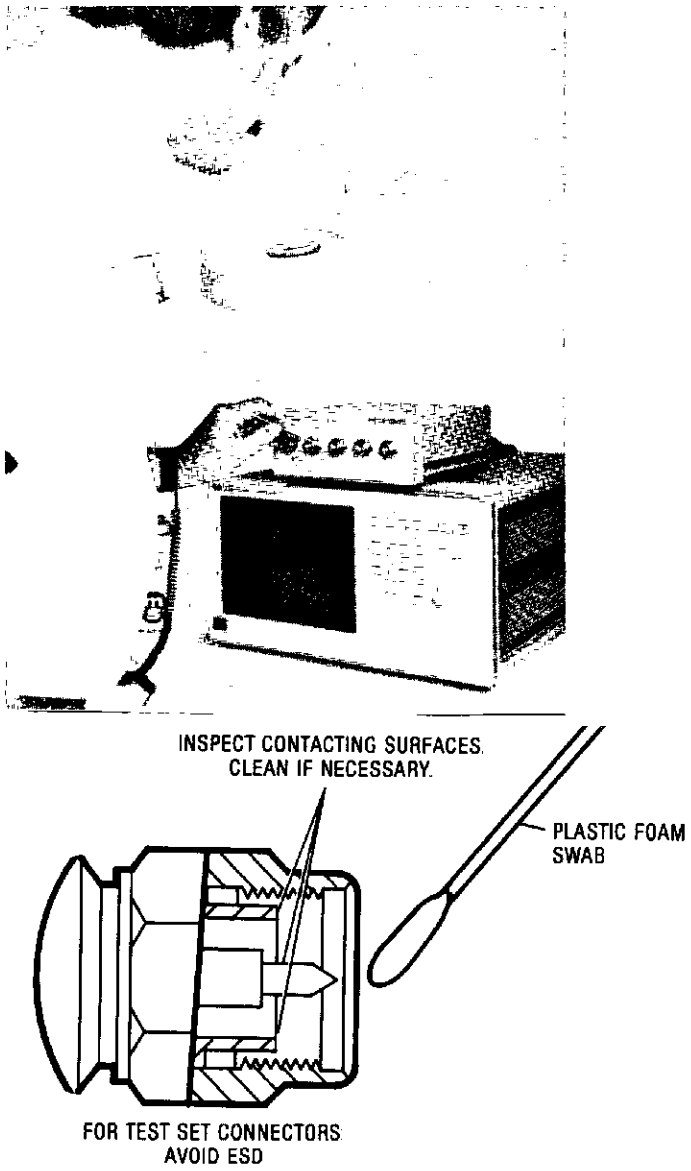


Figure A4-1. Visual Inspection of Precision 3.5 mm Connectors.

Figure A4-2 Checking Cleaning Solvent for Contamination.

Mechanical Inspection

Mechanical inspection of the connectors is the next step. This inspection consists of using the appropriate male or female precision 3.5 mm connector gauge to check the mechanical dimensions of all connectors, including those on the test set. The purpose of doing this is to make sure that perfect mating will occur between the connector surfaces. Perfect mating assures a good electrical match and is very important mechanically to avoid damaging the connectors themselves, especially on the oscilloscope.

Center Conductor

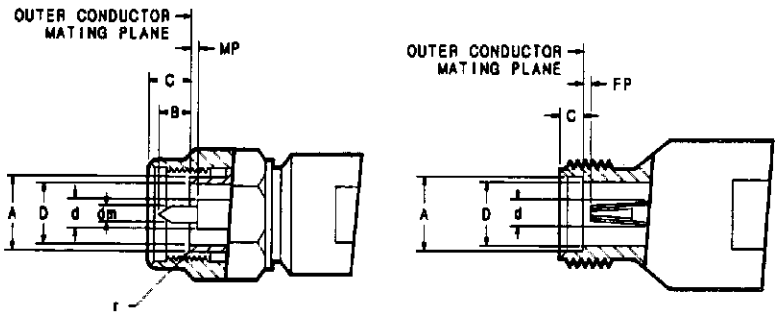
The critical dimension to be measured is the recession of the center conductor. This dimension is shown as MP and FP in Figure A4-3. No protrusion of the shoulder of the center conductor is allowable on any connector. The maximum allowable recession of the center conductor shoulder is 0.003 in. (0.08 mm) on all connectors, except those on the test sets.

On the test set connectors, not only is no protrusion allowable, the shoulder of the center conductor must be recessed at least 0.0002 in. (0.005 mm). The maximum allowable recession of the center conductor shoulder on the test set connectors is 0.0021 in. (0.056 mm).

Outer Conductor

If any contact protrudes beyond the outer conductor mating plane, the contact is out of tolerance and must be replaced. If the center conductor is not recessed at least 0.0002 in. (0.005 mm), it is out of tolerance and must be replaced. In both cases the out-of-tolerance connector will permanently damage any connector attached to it. Destructive electrical interference will also result due to buckling of the female contact fingers. This is often noticeable as a power hole several dB deep occurring at about 22 GHz.

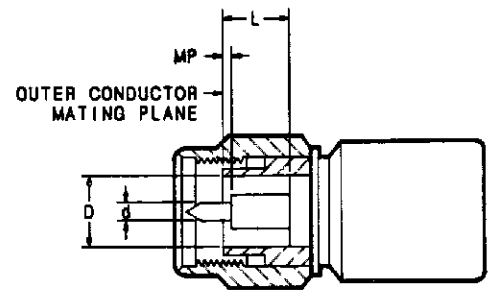
If any contact is recessed too far behind the outer conductor mating plane (>0.0021 in. >0.056 mm, except in test sets), poor electrical contact will result, causing high electrical reflections. Careful gauging of all connectors will help prevent this condition.

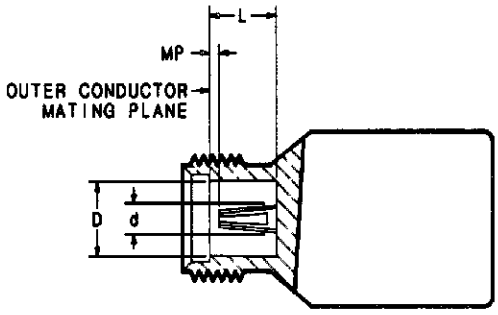


D = inside diameter of the outer conductor
d = diameter of male/female center connector
A = outside diameter of outer conductor at the mating plane
r = corner relief for male connector
B = protrusion of the male contact pin tip beyond the outer conductor mating plane
C = recession of the outer conductor mating plane behind outer face of connector
MP = recession of male contact pin shoulder behind outer conductor mating plane
FP = recession of face of female connector behind outer conductor mating plane
d_m = diameter of tip of male contact pin

Male Connectors	Female Connectors	Male Connectors	Female Connectors
$D=\underset{3.500\pm0.013\text{mm}}{0.1378\pm0.0005\text{in}}$	$D=\underset{3.500\pm0.013\text{mm}}{0.1378\pm0.0005\text{in}}$	$B=\underset{2.16^{+0.13}_{-0.38}\text{mm}}{0.085^{+0.005}_{-0.015}\text{in}}$	N/A
$d=\underset{1.519\pm0.008\text{mm}}{0.0598\pm0.0003\text{in}}$	$d=\underset{1.519\pm0.008\text{mm}}{0.0598\pm0.0003\text{in}}$	$C=\underset{3.05\pm0.38\text{mm}}{0.120\pm0.015\text{in}}$	$C=\underset{1.93\pm0.05\text{mm}}{0.076\pm0.002\text{in}}$
$A=\underset{4.580^{+0.00}_{+0.15}\text{mm}}{0.1803^{+0.000}_{-0.002}\text{in}}$	$A=\underset{4.590^{+0.05}_{-0.00}\text{mm}}{0.1807^{+0.002}_{-0.000}\text{in}}$	$MP=0.000^{+0.003}_{-0.000}\text{in}=0.000^{+0.08}_{-0.00}\text{mm}$	$FP=0.000^{+0.003}_{-0.000}\text{in}=0.000^{+0.08}_{-0.00}\text{mm}$
$r\leq\underset{0.08\text{ mm}}{0.003\text{ in}}$	$r\leq\underset{0.08\text{ mm}}{0.003\text{in}}$	$d_m=\underset{0.94^{+0.00}_{-0.03}\text{mm}}{0.037^{+0.000}_{-0.001}\text{in}}$	N/A

Figure A4-3. Mechanical Dimensions of Connector Faces.





D = inside diameter of outer conductor	=	0.1378±0.0003in 3.500±0.008mm
d = diameter of center conductor	=	0.0598±0.0002in 1.519±0.005mm
M.P. **FP** = recession of center conductor shoulder	=	0.000 +0.000/−0.003in 0.00 +0.00/−0.08mm
L = length of outer conductor	=	0.197 ± 0.001in 0.00 ± 0.000mm

C = concentricity of contact is governed by mating connector: typically <0.003 FIM (TIR)

Figure A4-4. Mechanical Dimensions of the Short Circuit.

Before using the connector gauge to measure the connectors, visually inspect the end of the gauge and the calibration block in the same way that you inspected the connectors. Dirty or damaged gauge facings can cause dirty or damaged connectors Two connector gauges (Figure A4-5) are available from Hewlett-Packard, one for each connector type, male and female. A single gauge calibration block is used to zero both gauges; one end protrudes for zeroing the male connector gauge. The part number for both gauges, as well as the calibration block is 1250-1862.

Figures A4-6 to A4-8 show how to use the connector gauges. Zero the gauge with the calibration block (see Figure A4-6) It is recommended that you zero both gauges first, then measure each of the terminations and/or adapters that will be used. Then, as the last step, measure the test set connectors

Figures A4-7 and A4-8 show how to measure precision 3.5 mm connectors. Note that a plus (+) reading on the gauge indicates recession of the center conductor and a minus (-) reading indicates protrusion. Since no protrusion of either connector is allowable, readings for connectors within the allowable range will be on the plus (+) scale of the gauge. Also note that the allowable tolerance range for the test set connectors is different from the range for other connectors. Both ranges are shown in Figures A4-7 and A4-8. Before measuring test set connectors, be sure that the RF power to the test set is off and that you and your equipment are grounded to prevent electrostatic discharge.

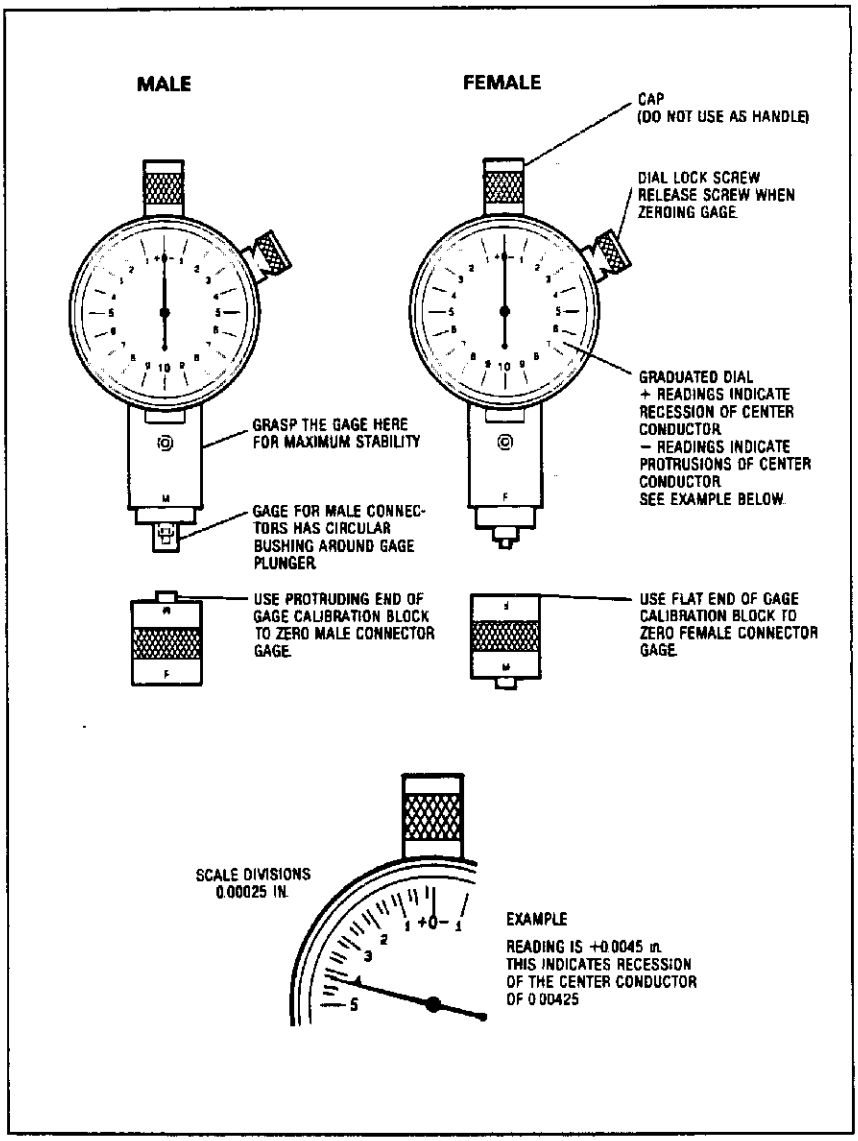


Figure A4-5. Precision 3.5 mm Connector Gauges.

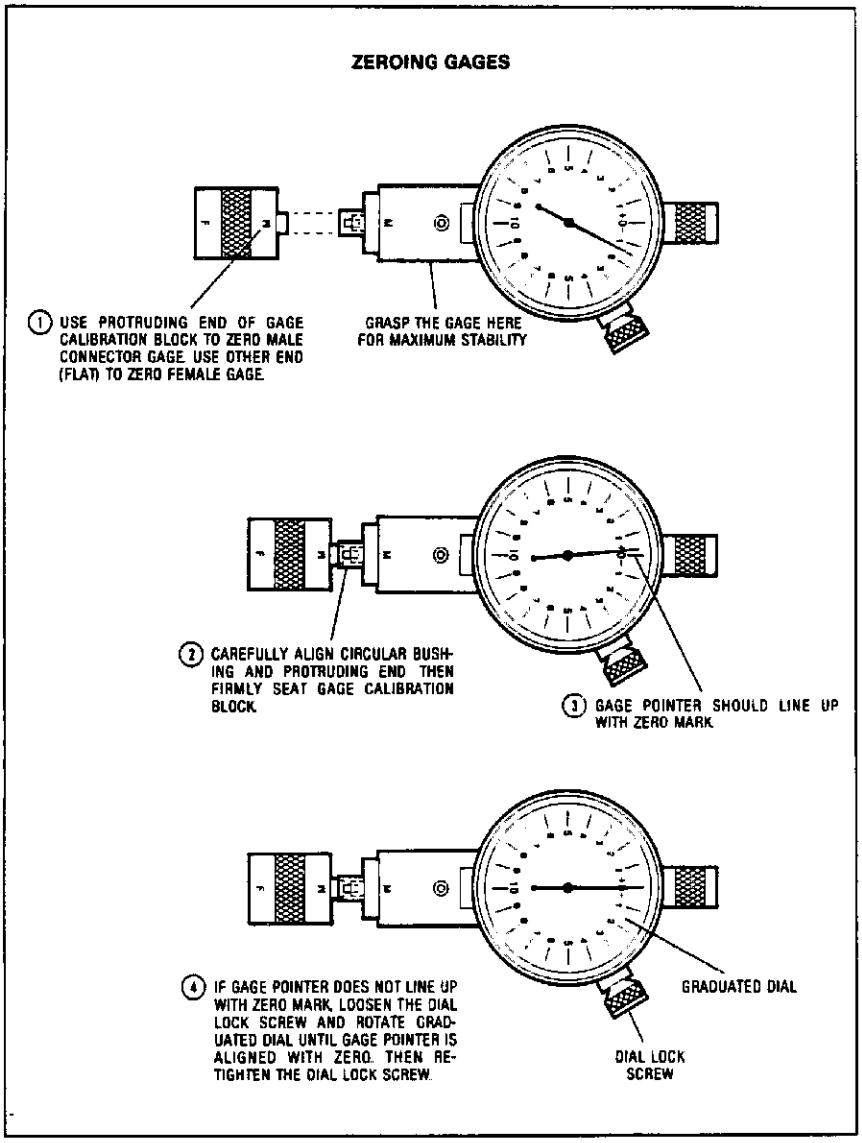


Figure A4-6 Zeroing Precision 3.5 mm Connector Gauges

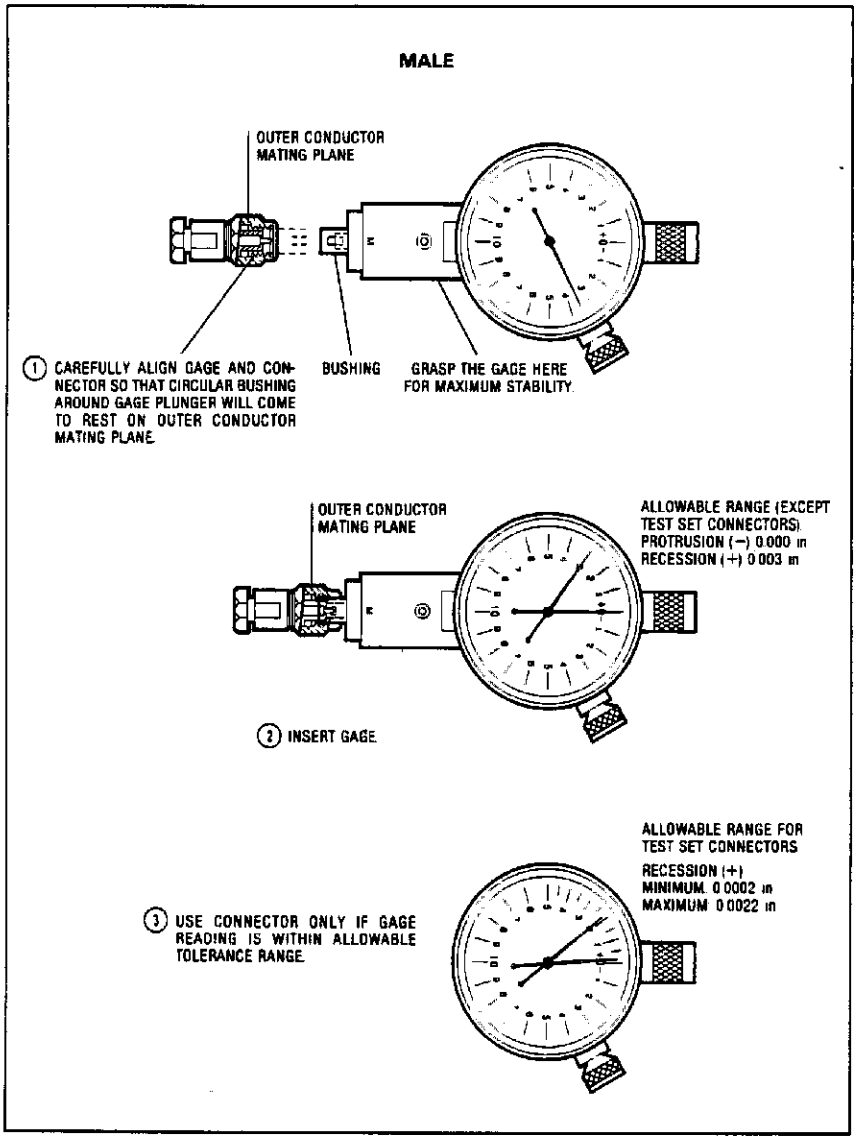


Figure A4-7. Measuring Precision 3.5 mm Male Connectors.

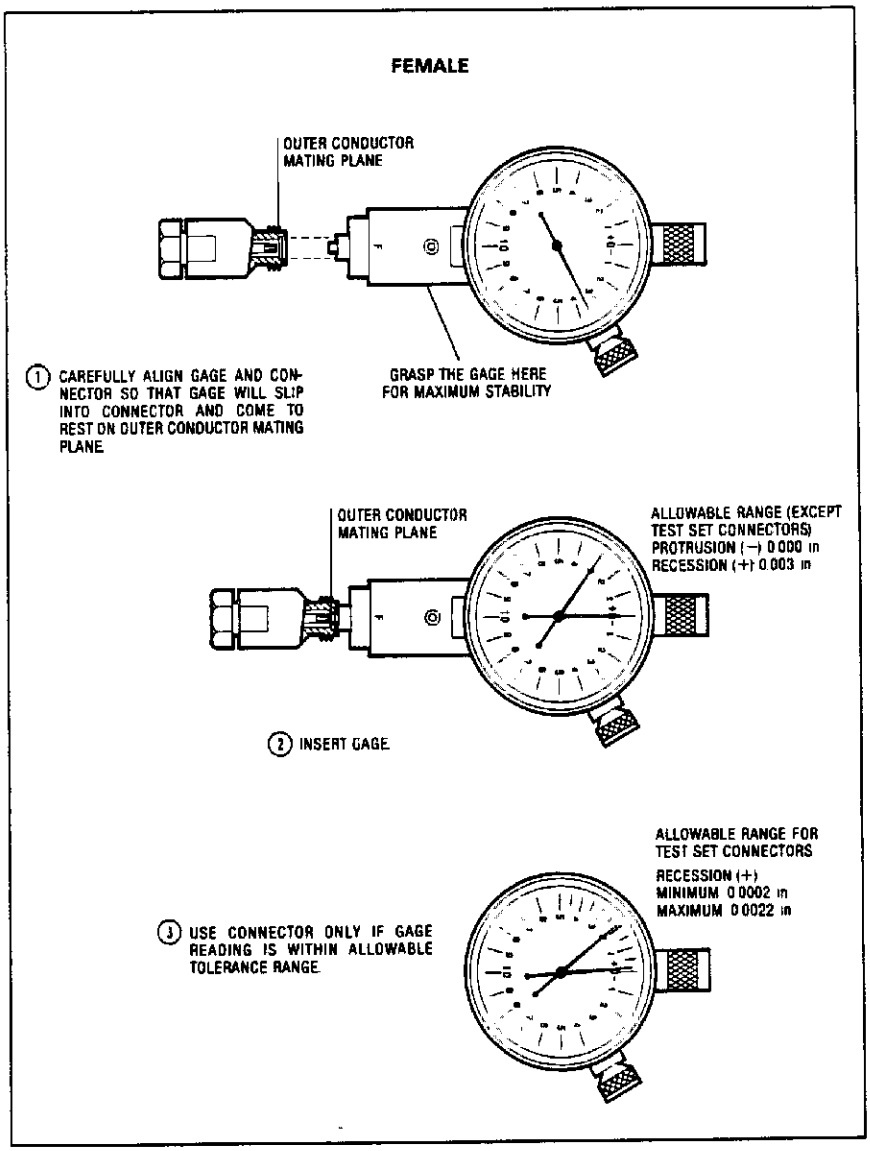


Figure A4-8. Measuring Precision 3.5 mm Female Connectors.

Connecting the Devices

Figures A4-9 and A4-10 illustrate the Hewlett-Packard recommended procedures for making connections with the calibration devices. Notice that these recommended procedures differ from traditional procedures used in the microwave industry, especially the counter-rotation technique and procedure for connecting the airline.

The counter-rotation technique, recommended here, involves a slight rotation of the termination or adapter just before the final tightening of the connector nut. This eliminates the very small air wedge between the outer conductors that frequently occurs when the body is held stationary during tightening, as it is in the traditional procedure. The HP 54120T will detect the reflections caused by such small wedges

The counter-rotation technique does not harm the connectors. The gold plating on the outer conductor surface will become burnished in time. This is normal, and as long as the surface remains smooth, the connector is still good. After much use the gold plating may eventually wear through and expose the beryllium-copper substratum. This too is normal, and if it is smooth the connector is still good, although the beryllium-copper surface may oxidize if the connector is used infrequently.

If the burnished surface is rough, scratched, rippled, or has other irregularities, too much tightening force is being used. If the roughness is severe, the connector is ruined and should not be used.

CAUTION

Damage can result if SMA connectors are overtightened to precision 3.5 mm connectors. Use a torque wrench designed for SMA connectors, set to a 5 lb.in. (60 N/cm) A torque wrench suitable for SMA connectors is available, HP part number 8710-1582.

Counter-Rotation Technique

The recommended Hewlett-Packard counter-rotation technique is for precision 3.5 mm connectors. Before making any connections to the test set, ground yourself with a grounded wrist strap. Also, it is good practice to grasp the outer shell of the test port before you make any connections to the test set in order to discharge any static electricity on your body. This is the most effective single safeguard to prevent ESD damage to your instruments.

Connect 3.5 mm devices by the following procedure (see Figures A4-9 and A4-10):

1. If the device has a retractable connector nut, fully retract the nut before mating the connectors. Carefully align the male and female contact pins and slide the connectors straight together until the center and the two outer conductors meet. Be careful not to twist or bend the contact pins. You should feel a slight resistance as the connectors mate.

2. Make the preliminary connection by attaching the connector nut of the male connector to the female. Support the body of the device and turn the connector nut until the mating surfaces make light contact. Do not overtighten. All you want is a connection of the outer conductors with gentle contact at all points of both mating surfaces.

3. When you are satisfied with this preliminary connection, use the following counter-rotation technique to eliminate air wedges between the mating planes (see Figure A4-9). If the calibration device is male, hold the connector nut firmly. Very slowly rotate the body of the device about 10-20° counterclockwise. Note that this slight rotation or backwiping is sufficient. Greater rotation does not improve electrical performance and increases wear on the connector surfaces.

If the calibration device is female (the connector nut is on the test set), very slowly rotate both the connector nut and the body of the device clockwise 10-20° (counterclockwise rotation will loosen the connection).

Light, smooth frictional resistance felt during the counter-rotation indicates you have made the preliminary connection correctly and that the counter-rotation technique has been successful. Roughness felt during counter-rotation indicates either that the connectors are damaged or that there is roughness in the connector nut/thread contact. Inspect both connectors again before proceeding, to make sure that the roughness is due to roughness in the connector nut interface rather than on the connector mating planes.

4. Tighten the connector nut finger tight, allowing the device to turn with the nut if it tends to do so. A small rotation of the body of the device at this point is acceptable and tends to occur naturally.

5. Use a torque wrench to make the final connection. Use of the torque wrench assures the final connection will be tight enough for optimum electrical performance, but not so tight as to distort or damage the connectors (see page A1-2).

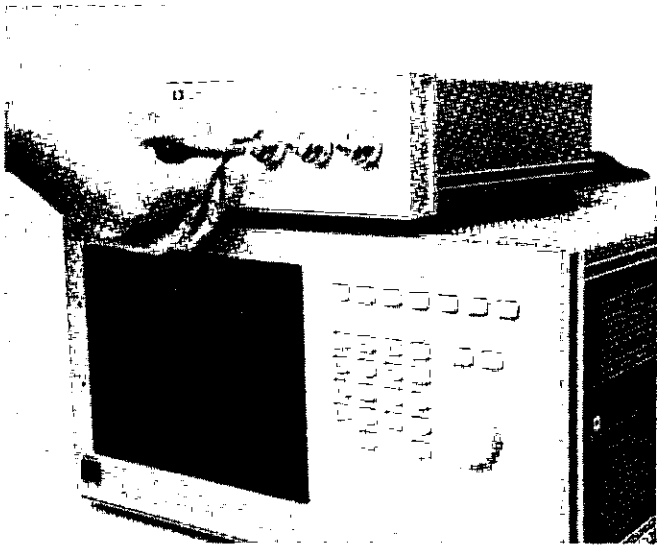
To disconnect, follow this procedure:

1. Loosen the connector nut on the male connector with the torque wrench. Leave the connection finger tight.

2. While supporting the calibration device, gently unfasten the connectors and pull the calibration device straight out of the test port connector. Do not twist either the center conductor or the outer conductor housing or exert lateral or vertical (bending) force on the connection.

Note that some precision 3.5 mm female connector fingers are very tight and can pull the center pin of their mates out past specifications as they are disconnected. If such a male pin is inserted into a female connector it can cause considerable damage by pushing the female center conductor back too far. Be aware of this possibility and re-check all connectors before mating them again.

1 Retract connector nut fully. Align contact pins and mate center conductors



2. Make preliminary connection: Tighten connector nut until mating surfaces make light contact. Support devices at all times.

3. Use counter-rotation technique Hold connector nut stationary. Rotate device body 10 to 20 degrees counterclockwise

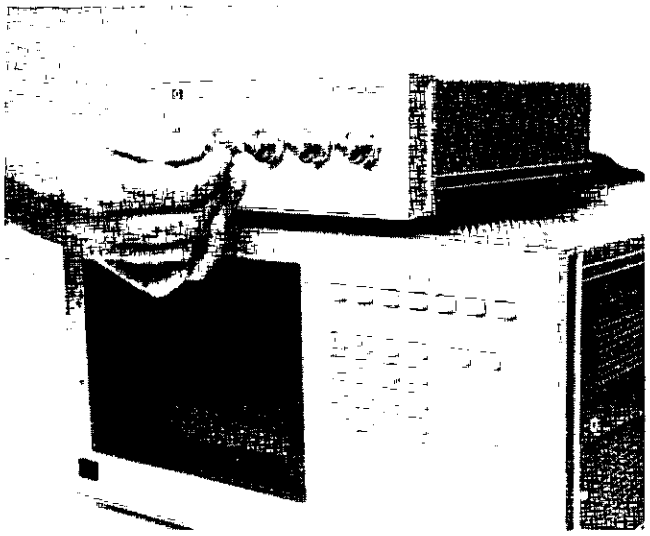


Figure A4-9. Counter-rotation Technique.

4. Tighten connector nut finger tight. Some rotation of the device body is acceptable. Use torque wrench to make final connection.

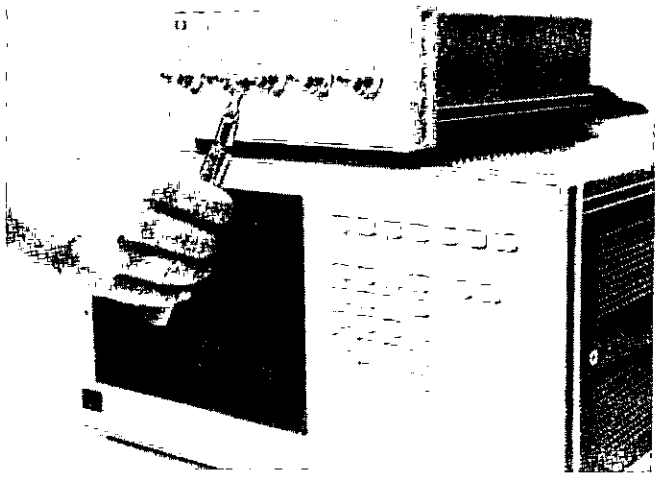


Figure A4-10. Counter-rotation Technique.

APPENDIX B

B-1. MANUAL BACKDATING

This appendix backdates the HP 54120T Service Manual to serial prefix numbers which are previous to the the serial prefix numbers on the manual's title page. **DO NOT** use this information for ordering replacable parts. Old part numbers are usually obsoleted and directly replaced by current part numbers. Refer to the Replaceable Parts portion, Section 5, of this manual to obtain the current part numbers when ordering replaceable parts.

Serial Prefix Number 2714A for the HP 54121A Four Channel Test Set

The HP 54121A contained the following assemblies:

A1 Assembly 54120-66505 or exchange assembly 54120-69505
A2 Assembly 54120-66504 or exchange assembly 54120-69504

Both of the above assemblies were obsoleted and are directly replaced by assemblies listed in the Replaceable Parts portion of this manual.