Errata

Title & Document Type: 3497A Installation and Service Manual

Manual Part Number: 03497-90020

Revision Date: December 1982

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

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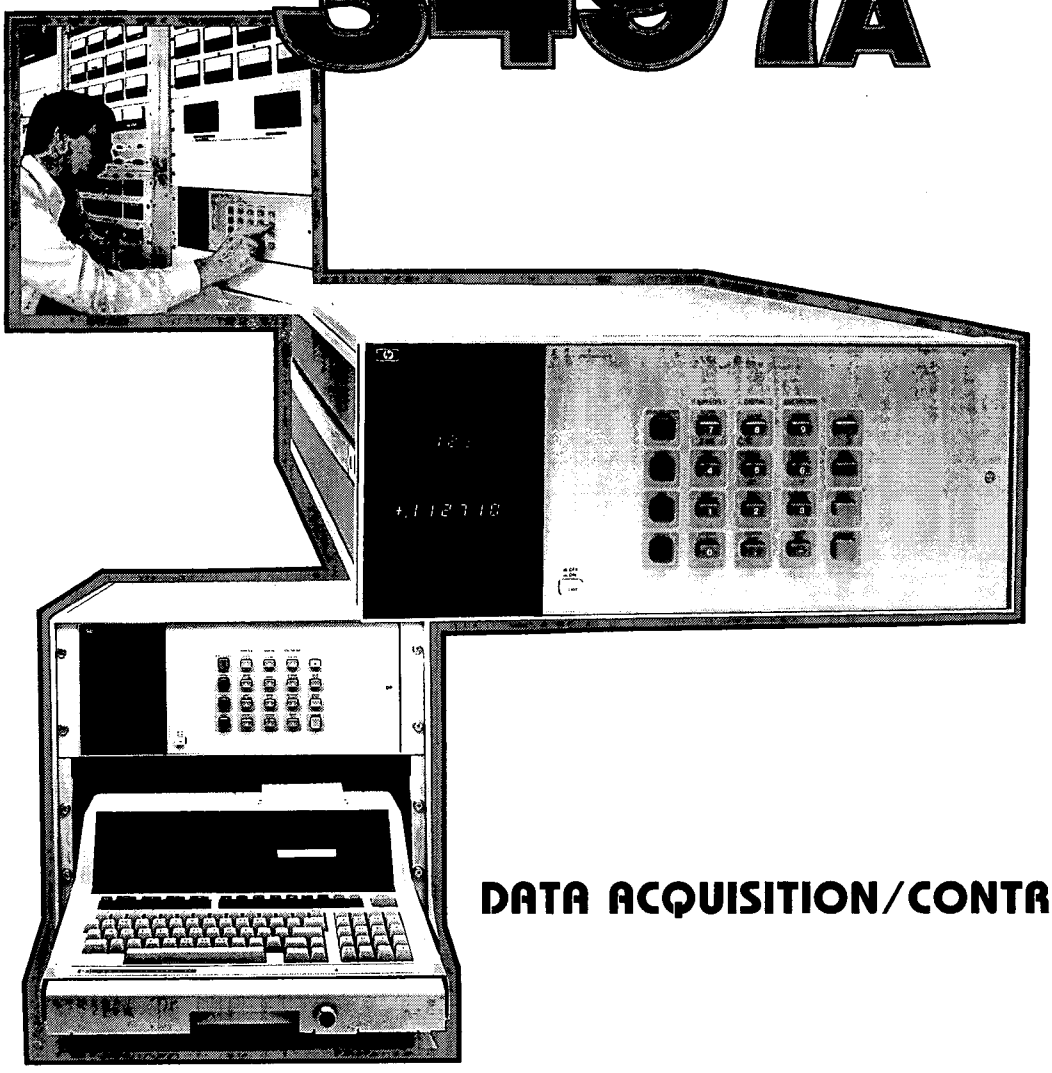
Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

Agilent Technologies

INSTALLATION AND SERVICE MANUAL

HEWLETT PACKARD

3497A



DATA ACQUISITION/CONTROL UNIT

HEWLETT PACKARD

INSTALLATION AND SERVICE MANUAL

MODEL 3497A
DATA ACQUISITION/CONTROL UNIT

Serial Number

This manual applies to instruments with serial number prefixes 22221A and greater.

WARNING

The information in this manual is for the use of Service Trained Personnel. To avoid electrical shock, do not perform any procedures in the manual, install or reconfigure the instrument, or do any servicing to the 3497A and its options, unless you are qualified to do so.

Manual Part Number 03497-90020

Microfiche Part Number 03497-90070

P.O. Box 301, Loveland, Colorado 80537 U.S.A.

Printed: December 1982

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment [,except that in the case of certain components listed in Section I of this manual, the warranty shall be for the specified period] . During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by -hp-. Buyer shall prepay shipping charges to -hp- and -hp- shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to -hp- from another country.

Hewlett-Packard warrants that its software and firmware designated by -hp- for use with an instrument will execute its programming instructions when properly installed on that instrument. Hewlett-Packard does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

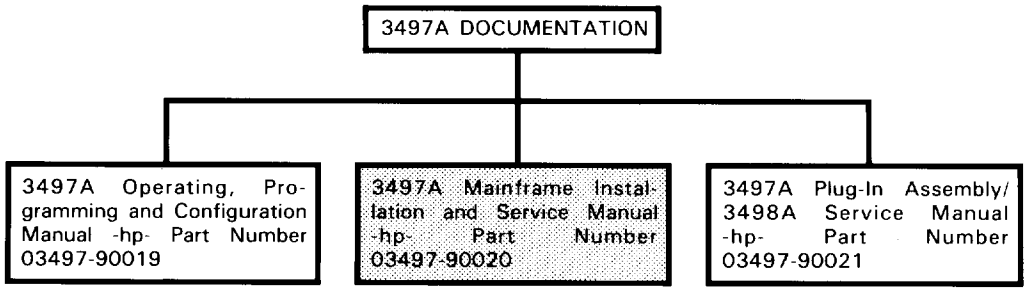
3497A DOCUMENTATION

This chart shows the manuals that are included in 3497A documentation. There are three types of 3497A manuals, as shown below. Each manual is enclosed in a separate three-ring binder.

The Operating, Programming and Configuration (OPC) Manual contains operating, programming and configuration information for the 3497A, for its plug-in assemblies (Options 010 through 140) and for the 3498A Extender.

The 3497A Mainframe Installation and Service (I&S) Manual contains installation and service information for the 3497A mainframe and the optional DVM.

The Plug-In Assembly Service Manual contains service information for all plug-in assemblies (except Option 140 which has no user service) and for the 3498A Extender.



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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.

GROUND THE INSTRUMENT

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

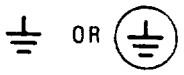
Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SAFETY SYMBOLS

General Definitions of Safety Symbols Used On Equipment or In Manuals.

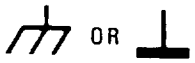
Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which,if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

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SECTION I
GENERAL INFORMATION

WARNING

The information in this manual is for the use of Service Trained Personnel. To avoid electrical shock, do not perform any procedures in the manual, install or reconfigure the instrument, or do any servicing to the 3497A and its options, unless you are qualified to do so.

1-1. INTRODUCTION

1-2. The 3497A Installation and Service Manual has information to install, reconfigure, and service the mainframe of the 3497A Data Acquisition/Control Unit. This includes information for the standard mainframe (HP-IB), Serial I/O mainframe (Option 232), front panel, and voltmeter option (Option 001). If you need information for other options (e.g. Counter, Strain Gage, etc.), refer to the appropriate option manual. This manual is designed for the use of Service Trained Personnel only.

NOTE

The 3497A Installation and Service Manual applies only for the 3497A's standard (HP-IB) and Serial I/O mainframes, front panel, and voltmeter option. For other options, refer to the appropriate option manual.

1-3. HOW TO USE THE MANUAL

1-4. The manual is divided into eight different sections plus three appendices with each section responsible for certain information. For example, Section II has installation information, Section V has the parts listing, Section VIII has service information, etc. The sections are as follows:

1-5. Section I - General Information

1-6. A short description of the manual and introduction to the 3497A is given in this section. The section also lists instrument options and accessories. The specification table is not included; it is in Section IV of the manual.

1-7. Section II - Installation

1-8. This section explains how the 3497A is prepared for use and includes power requirements, line voltage selection, etc. The section also explains how to connect the scanner for remote operation (both HP-IB and Serial I/O).

1-9. Section III - Instrument Control

1-10. The 3497A can be locally or remotely controlled, which is explained in Section III. Local control is performed from the front panel and remote control is over the HP-IB or Serial I/O bus.

1-11. Section IV - Performance Test and Adjustment

1-12. The 3497A's complete performance tests and adjustment procedures are in this section. The required equipment table and specification table are also included in Section IV.

1-13. Section V - Replaceable Parts

1-14. Section V lists the replaceable parts for the mainframe, front panel, and voltmeter option. Pictures and illustrations of chassis and mechanical parts are also included.

1-15. Section VI - Backdating

1-16. This section has information for adapting the manual for 3497A's with serial number prefixes different than shown on the title page.

1-17. Section VII - Theory Of Operation

1-18. The complete theory of operation for the 3497A's mainframe, front panel, and voltmeter is in this section.

1-19. Section VIII - Service

1-20. This section has troubleshooting procedures, schematics, and other applicable service and maintenance items for the 3497A. Troubleshooting procedures, schematics, and block diagrams are given in service groups. Included in Section VIII are also procedures to select the appropriate service groups.

1-21. APPENDIX

1-22. The manual has three appendices: Appendix A, B, and C. The appendices give a short description of the Hewlett-Packard Interface Bus, Serial I/O, and other applicable information.

1-23. 3497A DESCRIPTION

1-24. The following paragraphs give a description of the different sections and options of the 3497A to which this manual applies.

1-25. Mainframe

1-26. The mainframe of the 3497A provides the interfacing, power supplies, and support structure for optional plug-in cards and assemblies. It is also the interfacing means between the 3498A Extender and a controller. A block diagram representation of the mainframe is in Figure 1-1.

1-27. The outguard controller circuitry of the mainframe controls the digital communication between the HP-IB or Serial I/O, front panel, rear panel ports, inguard circuitry (via the crossguard), timer/pacer, and the outguard option cards. The outguard controller can have either HP-IB circuitry or Serial I/O circuitry. It cannot have both at the same time. The HP-IB circuitry permits communication between the 3497A and an HP-IB compatible computer or controller. The Serial I/O circuitry permits communication with a computer in a bit serial format, either directly or over telephone lines using asynchronous full duplex modems.

1-28. Front Panel

1-29. Local control is accomplished by using the 3497A's standard front panel. This front panel has an alphanumeric keyboard for programming the scanner and a display for showing measurement results, status, etc. The front panel also has an audible and programmable alarm (beeper), which turns on if an illegal entry is made from the keyboard. The front panel does not affect the remote control capabilities of the 3497A.

1-30. If only remote control is desired (i.e., no local control), the standard front panel can be replaced by an optional front panel (Option 260). The optional panel has only an On/Off switch and power On indicator. Since it has no keyboard and display, all programming and display of readings is performed remotely by a computer or controller.

1-31. Voltmeter Option

1-32. The voltmeter option (Option 001), if installed, is part of the inguard circuitry. The voltmeter gives the 3497A dc voltage measurement capabilities which, along with a programmable current source (which is part of the voltmeter card), can be used for resistance measurements. The voltmeter is fully programmable either locally from the front panel, or remotely over the HP-IB or Serial I/O bus.

1-33. INSTRUMENT AND MANUAL IDENTIFICATION

1-34. Instrument Identification is by a serial number located on the 3497A's rear panel. Hewlett-Packard uses a two-part serial number, with the first part (prefix) identifying a series of instruments and the second part (suffix) identifying a particular instrument within a series. An alpha character between the prefix and suffix identifies the country in which the 3497A was manufactured (A is for the U.S.A., G is for Germany,etc.).

1-35. OPTIONS

1-36. The available options for the 3497A are rack mounting options and functional options (e.g., plug-in options like the Counter, Strain Gage, etc.). The rack mounting options are listed in Table 1-1 and the functional options with corresponding field installable kits are listed in Table 1-2. Another option is Option 910. This option supplies an extra set of manuals.

Table 1-1. Rack Mounting Options

3497A Option	-hp- P/N	Description
907	5061-0090	Front Handle Kit
908	5061-0078	Rack Flange Kit
909	5061-0084	Rack Flange and Handle Kit

Table 1-2. Option/Functional Area Cross Reference

3497A Option	Field Installable Kit	Functional Area
Standard	NA	3497A mainframe with realtime clock, front panel keyboard and display, and HP-IB interface
Opt. 001	44420A	5½ digit voltmeter and current source
Opt. 010	44421A	20 channel relay multiplexer assembly
Opt. 020	44422A	Relay multiplexer assembly with thermocouple compensation
Opt. 050	44425A	16 channel digital/interrupt assembly
Opt. 060	44426A	100KHz reciprocal counter assembly
Opt. 070	44427A	120 ohm strain gage/bridge assembly
Opt. 071	44427B	350 ohm strain gage/bridge assembly
Opt. 110	44428A	16 channel actuator/digital output assembly
Opt. 115	44431A	8 channel high voltage actuator assembly
Opt. 120	44429A	Dual output zero to ± 10V D to A converter
Opt. 130	44430A	Dual output zero to 20 milliamps/4 to 20 milliamp D to A converter
Opt. 140	44432A	Breadboard card
Opt. 230	NA	Clock format is M:D:H:M:S
Opt. 231	NA	Clock format is D:M:H:M:S
Opt. 232	NA	Serial I/O (RS232) interface replaces HP-IB interface
Opt. 260	NA	Delete 3497A keyboard and display (i.e., standard front panel)
Opt. 298	NA	Add a 3498A Extender

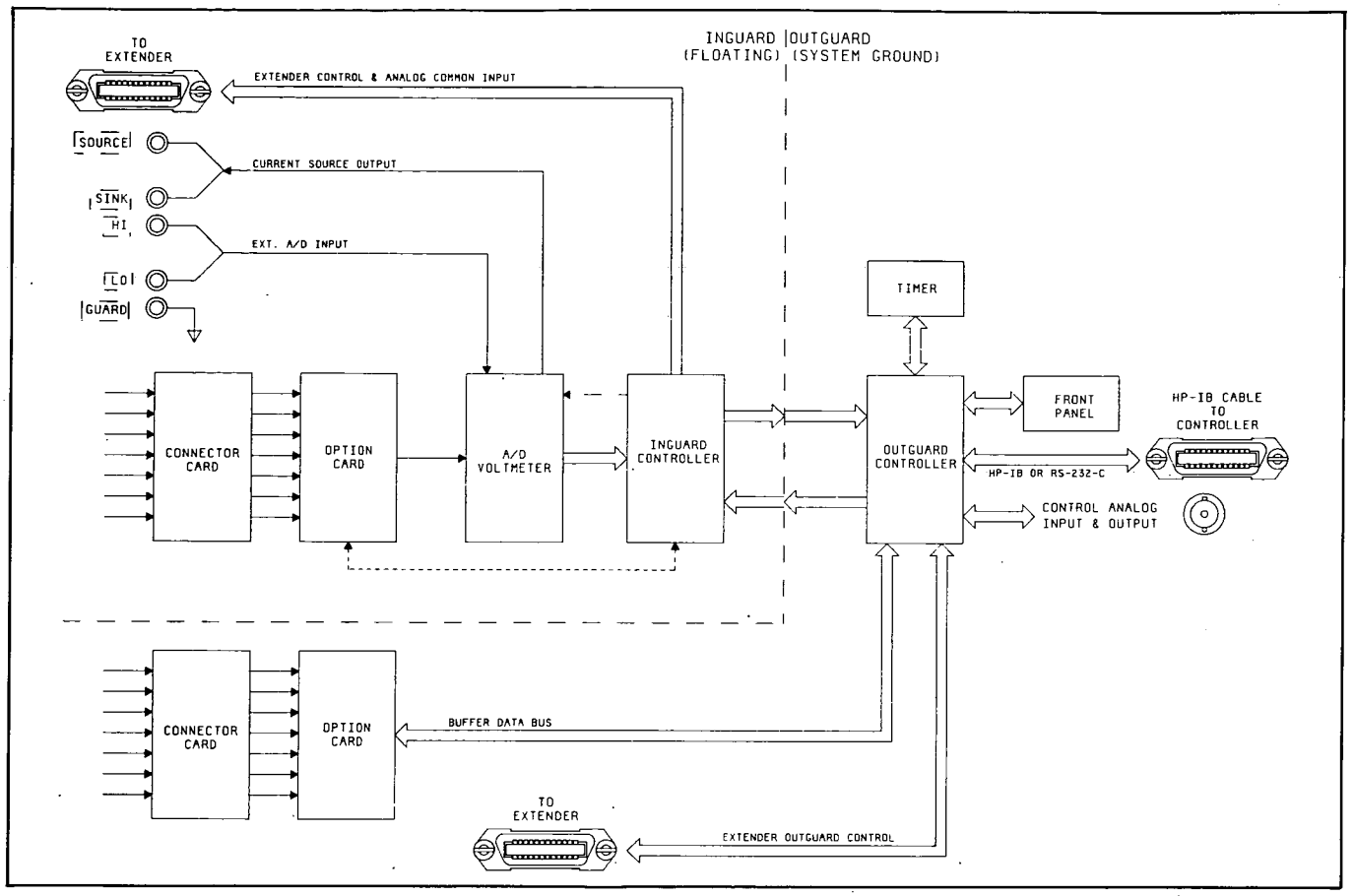


Figure 1-1. Mainframe Block Diagram

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. This section of the manual has the necessary information and instructions to install and interface the 3497A Data Acquisition/Control Unit. Included are initial inspection procedures, power requirements, environmental information, and instructions for repacking the instrument for shipment. Other information includes the operation and configuration of the battery back-up circuitry which is used to keep the 3497A's real time clock (part of the timer/pacer circuitry) operational when ac power is removed. The information in this section is for Service Trained Personnel.

2-3. The information in this section is for both the HP-IB and Serial I/O mainframes, front panel, and voltmeter option. For installation instructions of other options, refer to the applicable Installation and Service Manuals of the options.

WARNING

The information in this manual is for the use of Service Trained Personnel. To avoid electrical shock, do not perform any procedures in the manual or do any servicing to the 3497A and its options, unless you are qualified to do so.

2-4. INITIAL INSPECTION

2-5. The 3497A was carefully inspected both mechanically and electrically before shipment. It should be free of scratches and in perfect electrical order upon receipt. To confirm this, the instrument should be inspected for physical damage incurred during transit. If the instrument was damaged in transit, file a claim with the carrier. If there is any damage or if the unit does not operate correctly, see the warranty statement at the beginning of this manual.

2-6. SAFETY CONSIDERATIONS

2-7. It is imperative that only service trained personnel be allowed access to devices within the cabinet enclosure of the 3497A. Under any circumstances, be aware of the following safety information.

WARNING

Only personnel with a knowledge of electronic circuitry should install, reconfigure, or service the instrument.

WARNING

Voltages as high as 357 volts may be present within the protective safety covers and cabinet enclosures of the 3497A. These voltages may be accessible on exposed chassis parts once the safety cover has been removed. LETHAL voltages may be present even though the instrument is disconnected from the ac power source. BEFORE handling or servicing any of the plug-in option cards, make certain that all sources of external power are either turned off or disconnected.

2-8. If the Serial I/O option is installed (see paragraph 2-56 to configure the option), the following additional cautions and warnings must also be considered.

a. Since the Serial I/O option is designed for use with modems and computers that are RS-232C or RS-449/423 compatible, more than one manufacturer may supply components to make up a system. Some manufacturers might use a grounding technique that could cause electrical shock hazards to exist when an RS-232C device is interfaced. The safety considerations are meant to make the user aware of this type of condition, in order that the necessary precautions to prevent electrical shock are taken.

b. The 50-pin male connector on the cable supplied with the Serial I/O option, has a metal housing which is internally connected to the cable shield. The other end of the cable has an RS-232C connector with pin 1 also connected to the cable shield. Standard RS-232C defines pin 1 as "Protective Ground" and the pin will most likely be connected to the chassis of the device being interfaced (computer or modem). Make sure the device being interfaced has an earth ground chassis. This insures that the exposed metal housing on the 3497A connector will not be at some hazardous voltage level.

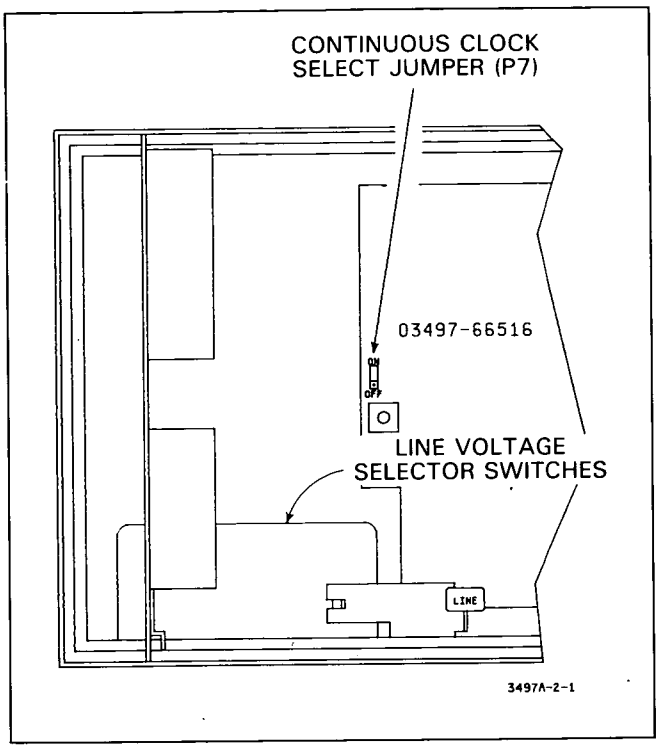


Figure 2-1. Line Voltage Switches and Clock Backup Mode Select Jumper

c. Standard RS-449/423 does not specify protective ground or safety ground as an interchange circuit. Therefore, when RS-449/423 equipment is used and bonding of the equipment chassis' is required, a separate conductor should be used which conforms to the appropriate national or local electrical code. In all cases, any device being interfaced should have an earth grounded chassis.

2-9. BATTERY BACKUP FOR REAL TIME CLOCK

2-10. The 3497A mainframe includes a real time clock which is part of the timer/pacer circuitry. As long as the 3497A is turned on with ac power connected, the clock is kept operational by the instrument's power supplies. If ac power is removed, a 6V lead-acid battery (inside the 3497A mainframe) is used to backup the clock (i.e., the clock is kept operational by the battery). The only functions backed up are the time of day and elapsed time; other clock functions are not backed up. The battery backup operation can be selected for two different modes: Mode 1 and Mode 2.

2-11. Mode 1. In Mode 1, the battery keeps the real time clock operational when ac power is disconnected and the Power Line switch is in the ON position. Battery backup does not operate when the Power Line switch is in the OFF position. Mode 1 is selected when the Continuous Clock Select Jumper (jumper plug P7) is in the "OFF" position. Jumper plug P7 is located on the power supply board behind the front panel as shown in Figure 2-1. The 3497A is set to Mode 1 when shipped from the factory.

2-12. Mode 2. In this mode, the battery keeps the real time clock operational when ac power is disconnected and the Power Line switch is either in the ON or OFF position. The mode is selected by placing the Continuous Clock Select Jumper (P7) in the "ON" position.

2-13. Battery. The battery, if fully charged, supplies power to the clock for at least 24 hours. Normally, the battery is always charged whenever the instrument is operating on ac line power. If the battery is completely discharged, 14 to 16 hours may be required to fully charge the battery.

2-14. POWER REQUIREMENTS

2-15. Line Power

2-16. The 3497A can be operated from any power source supplying 100V, 120V, 220V, or 240V (-10% to +5%), 48Hz to 66Hz single phase. Power consumption is 150VA.

2-17. Line Voltage and Fuse Selection

2-18. The line voltage is selected by switches located on a subpanel behind the front panel, as shown in Figure 2-1. Figure 2-2 provides information for line voltage and fuse selection. Make sure the line voltage select switches are in the correct position and the correct fuse is installed (see next paragraph), before applying ac power to the instrument.

2-19. The fuse is changed at the fuse holder located on the right rear panel of the instrument (as viewed from the back). To remove the fuse, insert the blade of a small flat blade screwdriver into the slot of the fuse holder cap. Push the cap in and then turn the screwdriver counterclockwise. The cap will pop out and can then be removed with the fuse.

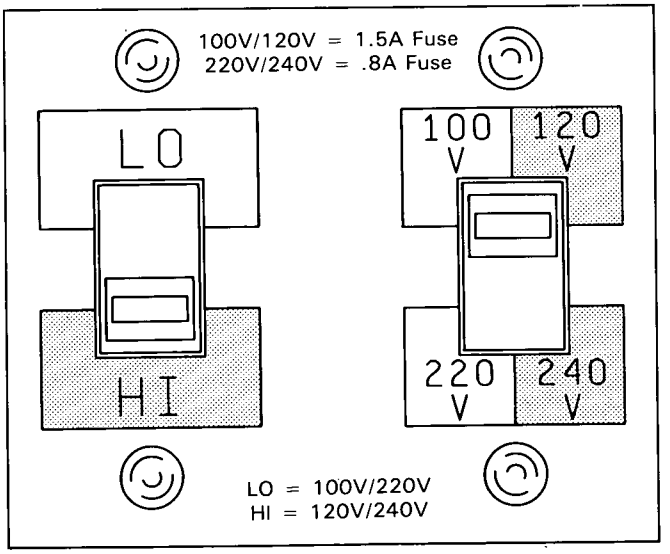


Figure 2-2. Line Voltage Selection

CAUTION

Always make sure that ac line power is disconnected before removing and installing the fuse.

2-20. Power Cable and Grounding Requirements

2-21. To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the instrument panel and cabinet be grounded. The 3497A is equipped with a three-conductor power cord which, when plugged into an appropriate receptacle, grounds the instrument cabinet. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to Figure 2-3 for the available power cable and plug configuration and appropriate -hp- part numbers.

2-22. INSTRUMENT INSTALLATION

2-23. The 3497A is shipped with plastic feet and tilt stand in place, ready for use as a bench instrument. The plastic feet are shaped so that the 3497A can be mounted on top of other -hp- instruments. When operating the instrument, choose a location that provides at least three inches of clearance at the rear and at least one inch at each side. Failure to provide adequate clearance will result in excessive internal temperature increases, reducing instrument reliability. The clearances provided by the plastic feet in bench stacking and the filler strip in rack mounting allow air passage across the top and bottom cabinet surfaces.

2-24. Option 908 (Rack Mount Kit) enables the 3497A to be mounted in an equipment cabinet. The rack mount for the 3497A is an EIA standard width of 19 inches. Installation instructions are included with the Rack Mount Kit. Option 908 may be ordered from the nearest -hp- Sales and Service Office under -hp- Part Number 5061-0078.

2-25. PLUG-IN OPTION INSTALLATION

2-26. Since there are a total of five slots in the 3497A mainframe (marked 0 to 4), a total of five plug-in options can be installed in the instrument. The installation procedure is as follows:

a. Turn the 3497A off and remove the power line cable from the instrument.

b. Remove the rear panel safety cover by removing the two screws that hold it in place.

c. Locate the option to be installed. Each option has an option card (i.e., printed circuit board) and a terminal card. Make sure the terminal card is plugged into the option card.

d. Locate the finger ring on the terminal card and make sure it is turned to the left (i.e., counterclockwise

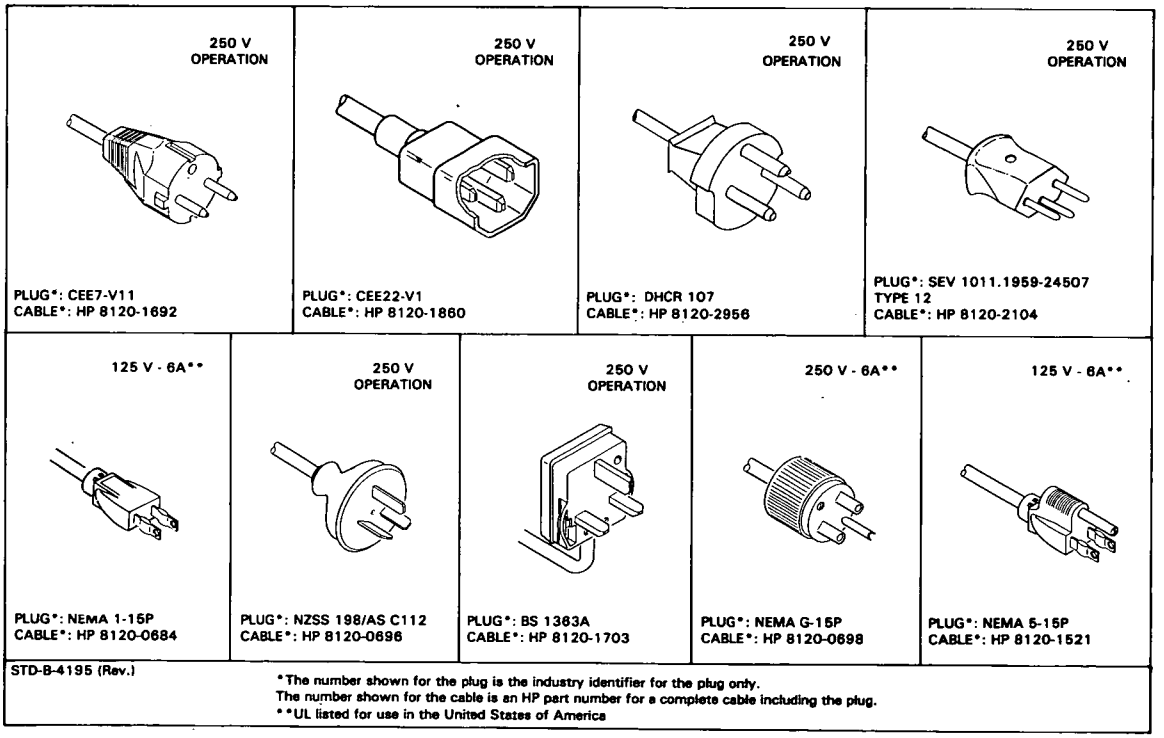


Figure 2-3. Power Cables

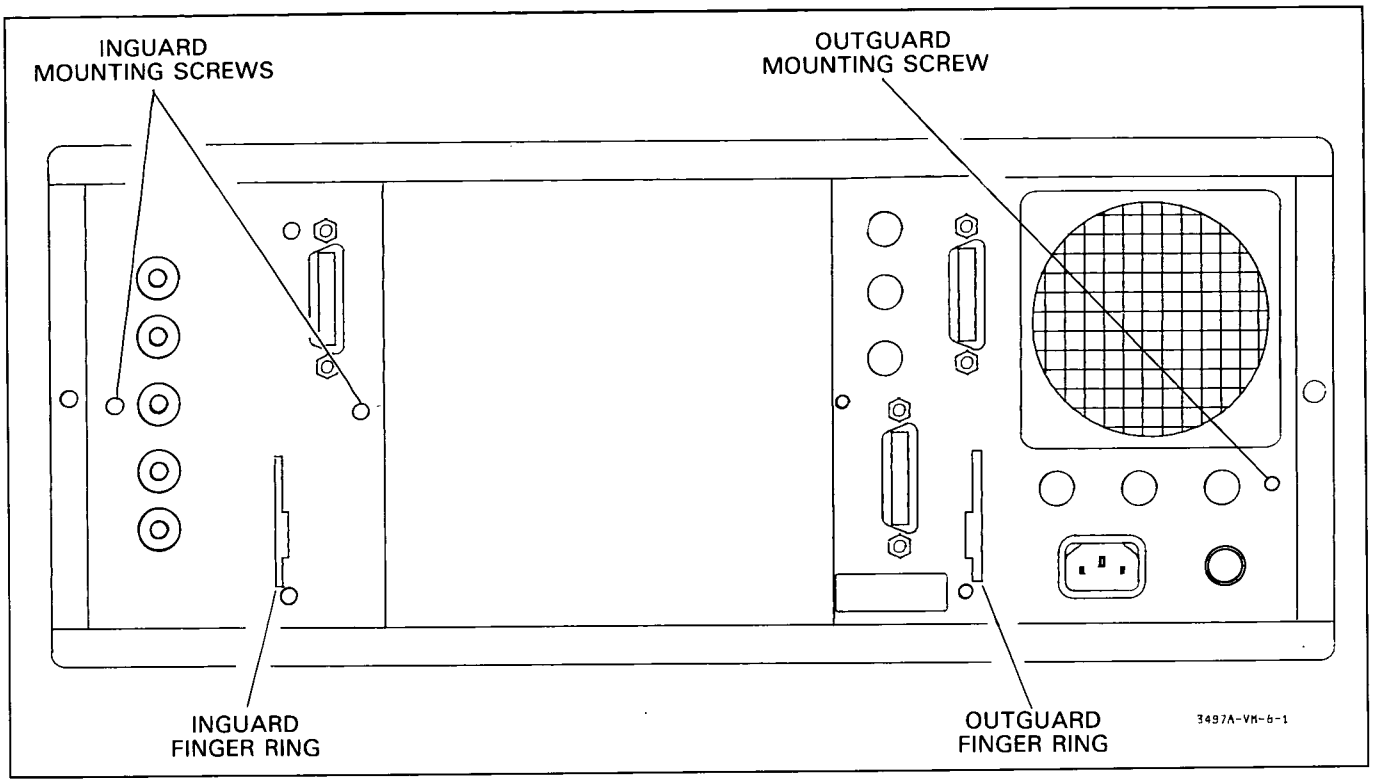


Figure 2-4. Outguard and Inguard Mounting Screws and Finger Rings

in the unlocked) position. The ring should be in the horizontal position.

e. Determine into which slot the option is to be installed (slot 0, 1, 2, 3, or 4) and locate the arrow next to the slot number. Align the option card (printed circuit board) with the arrow and then push the option into the slot until it seats firmly in the motherboard socket.

f. Turn the finger ring on the terminal card to the right until the ring is at a 45 degree angle to lock the option in place. The option is now installed.

2-27. OUTGUARD LOGIC BOARD REMOVAL AND INSTALLATION

2-28. Removal and installation of the HP-IB or Serial I/O outguard logic board is required if the boards are to be reconfigured. For example, the boards need to be removed to change the HP-IB address (see paragraph 2-41), the speed, word length, etc. (see paragraph 2-72 through 2-88), or the internal clock configuration. The removal and installation procedures are in the following paragraphs. Since the outguard logic board may need to be removed for troubleshooting purposes, the following procedures are repeated in Section VIII of this manual.

2-29. Outguard Logic Board Removal

2-30. The following procedures can be used to remove the outguard logic board (HP-IB or Serial I/O).

WARNING

To avoid personal injury and/or equipment damage, read and understand the safety considerations in paragraph 2-6 before any cable is connected to any device interfaced with the 3497A.

a. Turn the 3497A off and remove the power line cable from the instrument.

b. Remove the rear panel safety cover by removing the two screws that hold it in place.

c. Locate the screw on the outguard rear panel that holds the logic board in place (see Figure 2-4). Loosen the screw but do not remove it. It is held in place by a rubber grommet.

d. Use the built-in finger ring, shown in Figure 2-4, to pull the board from the motherboard slot connector. The board can be completely removed from the

mainframe or pulled out only far enough to gain access to the switches. The board must be completely removed to reconfigure the clock.

e. To reconfigure the HP-IB controller, refer to paragraph 2-41 and to reconfigure the Serial I/O controller, refer to paragraph 2-56. To reconfigure the clock, refer to paragraph 2-91.

2-31. Outguard Logic Board Installation

2-32. To install the outguard logic board, do the following:

a. Make sure the 3497A is turned off and the power line cable is removed from the instrument.

b. Locate the arrow marked "CONTROLLER TIMER" and align the outguard logic printed circuit board with the corresponding slot. Then push the board into the slot until it sets firmly in the motherboard socket.

c. Locate the rear panel mounting screw, shown in Figure 2-4, and tighten the screw.

d. Reinstall the rear panel safety cover. The 3497A is now ready for use.

2-33. INGUARD CONTROLLER (AND VOLTMETER OPTION) REMOVAL AND INSTALLATION

2-34. If the voltmeter option is installed in the instrument, the option's printed circuit board is physically and electrically connected to the inguard controller board. If the voltmeter option is not installed, only the inguard controller board is installed in the instrument. The voltmeter option is normally installed at the factory, but is also available as a field installable option. The following procedures show how to remove the inguard controller board, how to install the voltmeter option, and how to install the inguard controller board. Similar procedures are in Section VIII of this manual.

2-35. Inguard Controller Board Removal Procedure

2-36. Do this procedure to remove the inguard controller board. This procedure must also be performed to install the voltmeter option. Do the following:

a. Turn the 3497A off and remove the power line cable from the instrument.

b. Remove the rear panel safety cover by removing the two screws that hold it in place. Then remove the rear cover bracket by removing the screws that hold the bracket in place.

c. Locate the two screws on the inguard rear panel that hold the inguard controller board in place (see Figure 2-4). Loosen the screws but do not remove them. They are held in place by a rubber grommet.

d. Use the built-in finger ring, shown in Figure 2-4, to pull the controller board from the motherboard slot connector. This completes the procedure to remove the inguard controller board. To reinstall the board, go to paragraph 2-39. To install the voltmeter option, continue with the next paragraph.

2-37. Voltmeter Option Installation Procedure

2-38. Use this procedure to install the voltmeter board on the inguard controller board. Do the following:

a. Obtain the voltmeter option printed circuit board. While looking at the board, locate the two sets of red and black twisted pair cables attached to the board. One twisted pair is soldered to the board and the other pair is plugged into the board using female plug-in terminals.

b. Locate the red and black twisted pair soldered to the board and connect it (with its female plug-in terminals) to the non-component side of the inguard controller board, as shown in Figure 2-5.

c. Place the voltmeter printed circuit board, component side out, in position over the inguard controller mounting frame, as shown in Figure 2-5. Secure the board with one machine screw (-hp- Part Number: 0515-0271), as shown in Figure 2-6.

d. Locate the other red and black twisted pair plugged into the voltmeter board. Wrap the red wire around the binding post of the CURRENT SOURCE HI Terminal and wrap the black wire around the binding post of the CURRENT SOURCE LO Terminal, as shown in Figure 2-7. Using a low wattage (25 Watt) soldering iron, solder the red and black wires to their respective terminals.

e. Carefully attach the ribbon cable edge connector to the inguard controller board.

f. Place the metal shield in position over the voltmeter board and secure it with four machine bolts (-hp- Part No: 0515-0212), as shown in Figure 2-8.

g. Locate the A/D Jumper (blue jumper plug, J3) on the inguard controller board shown in Figure 2-9. Place the jumper in the "A/D" position, as shown in the figure. Continue with the next paragraph to reinstall the Inguard Controller Board.

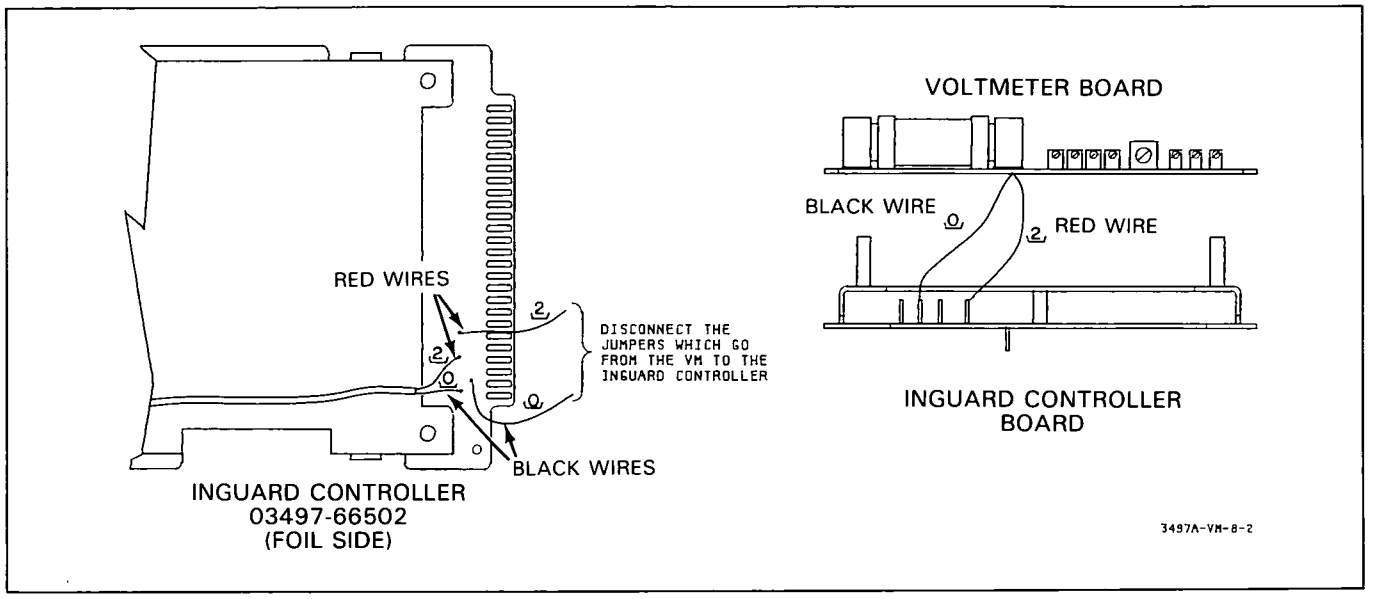


Figure 2-5. Inguard Controller Board with Voltmeter

2-39. Inguard Controller Board Installation

2-40. Do the following procedure.

a. Make sure the 3497A is turned off and the power line cable is removed from the instrument.

b. Locate the arrow marked "INGUARD CONTROLLER" and align the inguard controller printed circuit board into the corresponding slot. With the inguard controller board aligned, the voltmeter board should also be aligned with the "A/D OPTION" arrow. Then push the board into the slot until it sets firmly in the motherboard socket.

c. Locate the rear panel mounting screws, shown in Figure 2-4, and tighten the screws.

d. Reinstall the rear panel safety cover. If the voltmeter option board was installed, perform the voltmeter performance tests in Section IV of this manual. The 3497A is now ready for use.

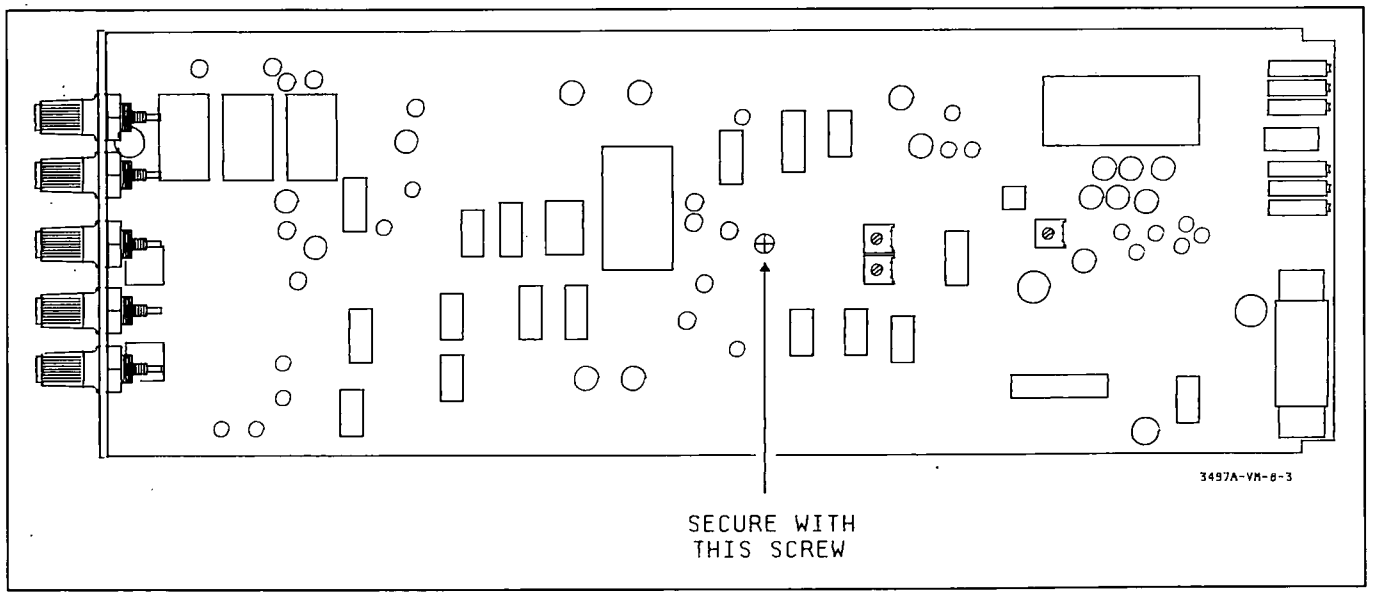


Figure 2-6. Mounting Voltmeter on Inguard Controller

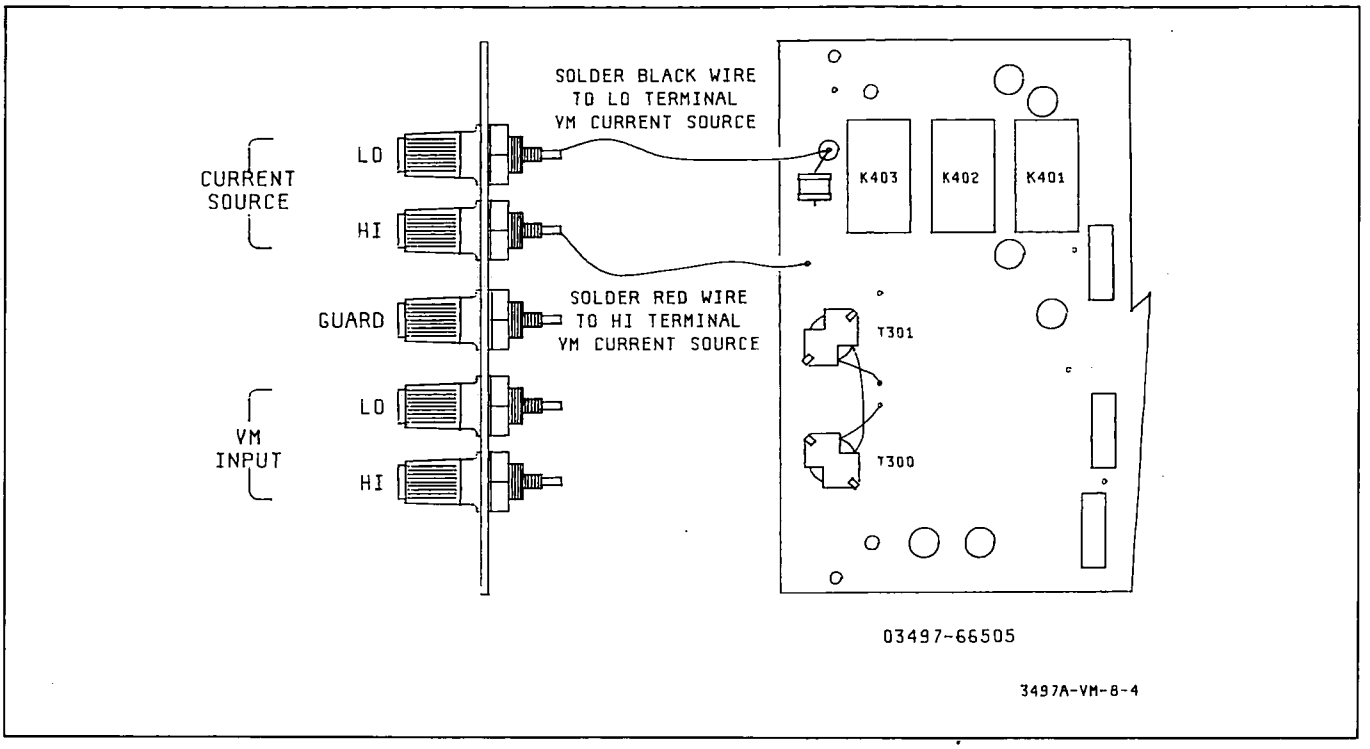


Figure 2-7. Voltmeter Connection

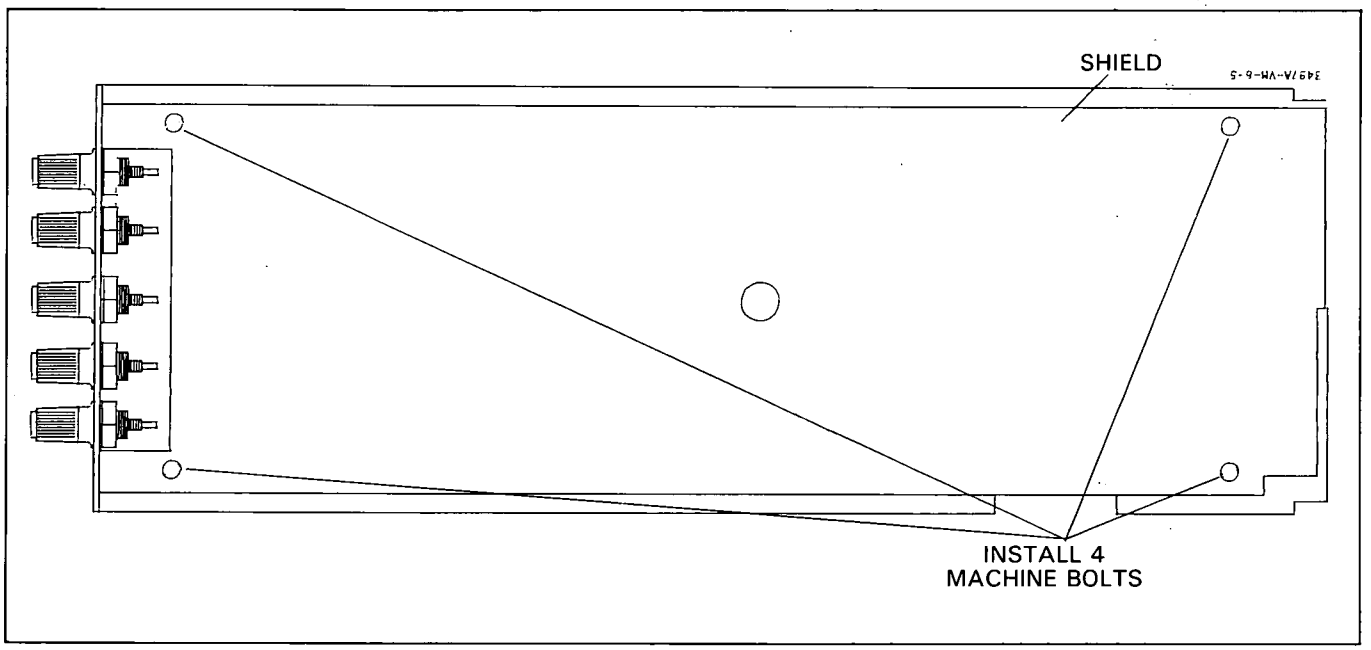


Figure 2-8. Voltmeter Installation

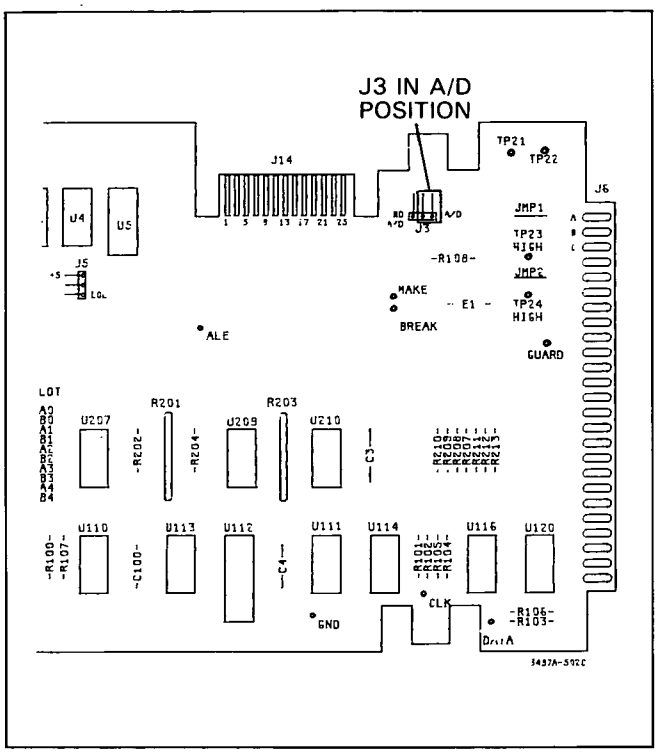


Figure 2-9. A/D Jumper Configuration

2-41. HP-IB SYSTEM CONNECTION AND CONFIGURATION

2-42. The following paragraphs have information on how to connect the 3497A to the Hewlett-Packard Interface Bus (HP-IB), how to set the HP-IB Address, and other related information. The paragraphs apply to 3497A's with HP-IB capabilities only. For the Serial I/O connection and other applicable information, refer to paragraph 2-56.

NOTE

HP-IB is Hewlett-Packard's implementation of IEEE Std. 488-1978, "Standard Digital Interface For Programmable Instrumentation".

2-43. HP-IB Connection

2-44. The 3497A is connected to the HP-IB by the 3497A's rear panel HP-IB connector using an interface cable. A typical HP-IB System interconnection is illustrated in Figure 2-10.

2-45. A total of 15 HP-IB compatible instruments can be connected to the Bus. The required cables have identical "piggy-back" connectors on both ends so that several cables can be connected to a single source. A good rule to follow is not to stack more than two cables on any one connector. If the stack is loo long, any force on the stack can produce enough leverage to break the connector. Since the 3497A uses all the HP-IB lines, any damaged connector pins may affect the HP-IB operation. Also, be sure that each connector is firmly screwed in place to keep it from working loose during normal use. The HP-IB Connector is represented in Figure 2-11.

2-46. Cable Restrictions

2-47. Various lengths of HP-IB cables can be ordered, as an accessory, from Hewlett-Packard. The cable lengths are 1, 2, or 4 meters and are listed in Section I of this manual with corresponding accessory numbers. For correct HP-IB performance, certain cable length restrictions should be followed. These restrictions are as follows and

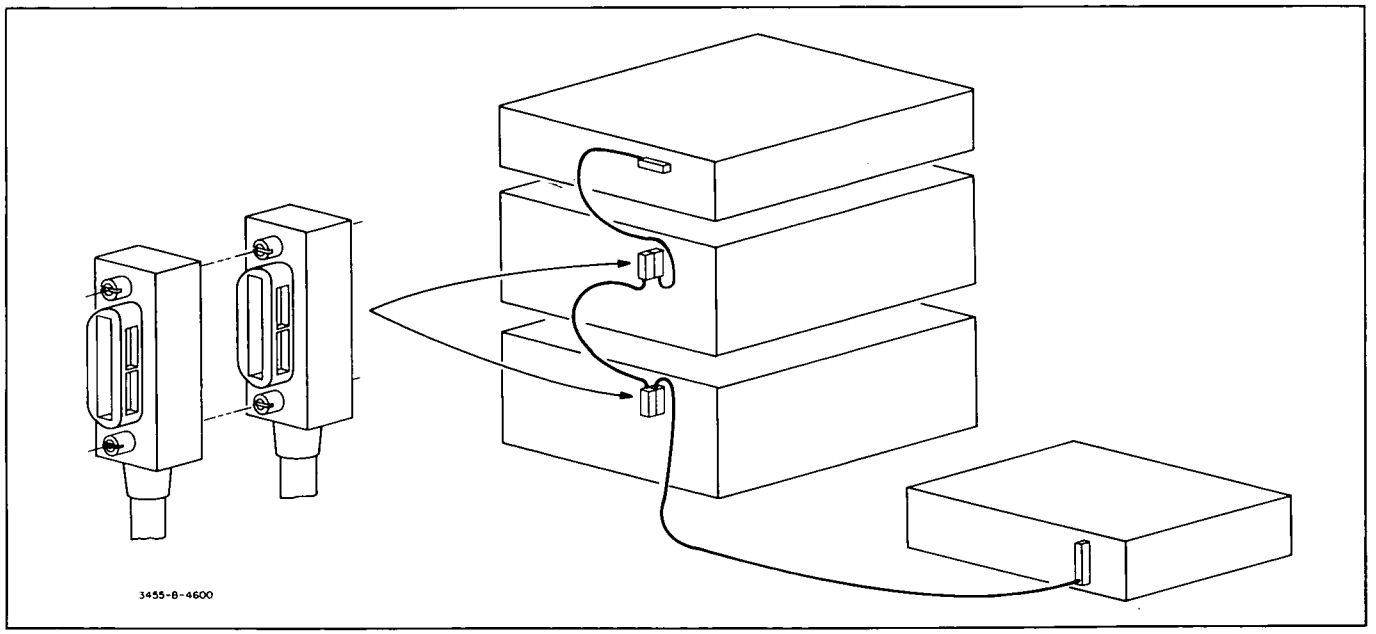


Figure 2-10. Typical HP-IB System Interconnection

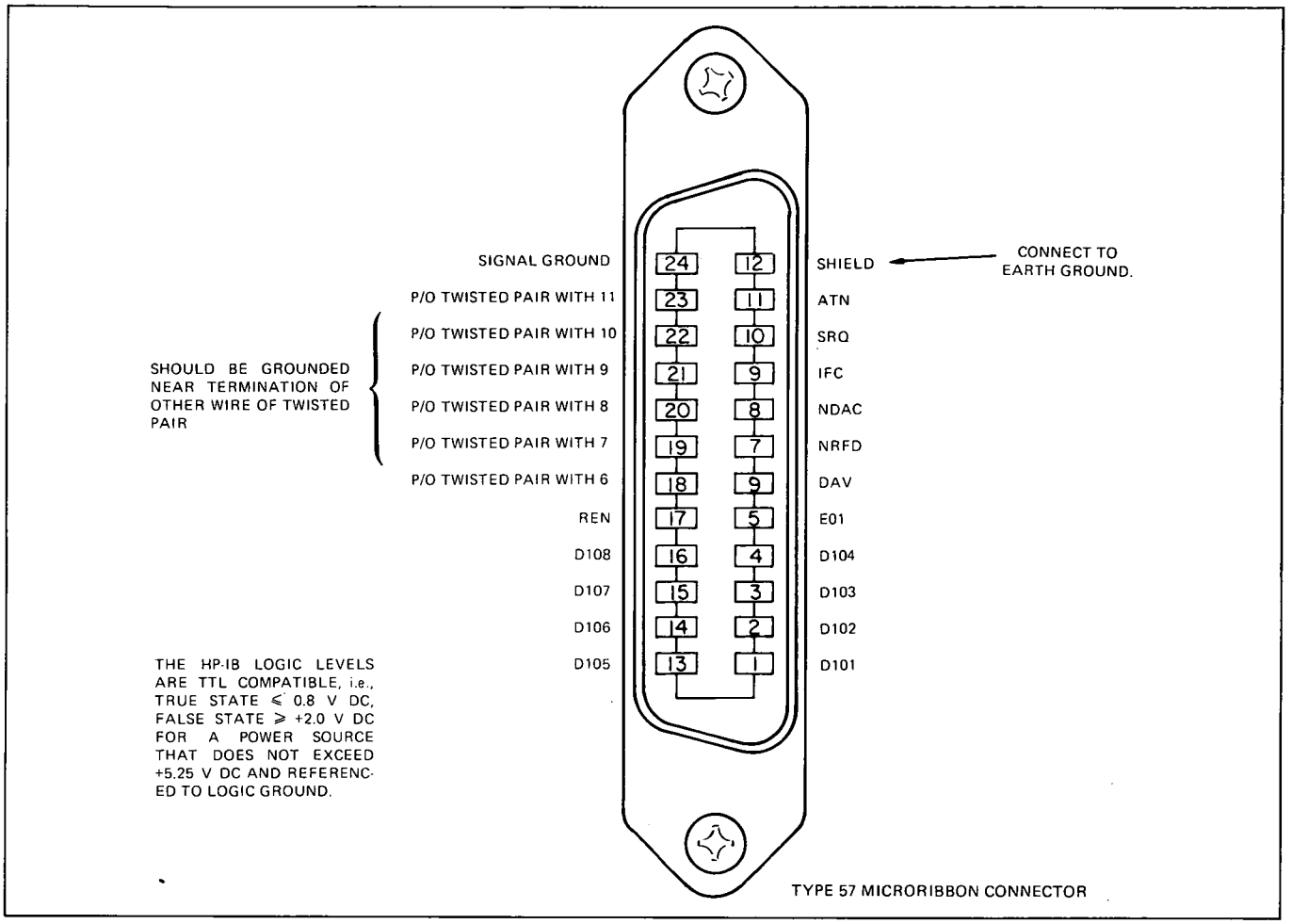


Figure 2-11. HP-IB Connector

should be kept in mind when connecting the 3497A to the HP-IB.

a. The total cable length for the system must be less than or equal to 20 meters (65 feet).

b. The total cable length must be less than or equal to 2 meters (6 feet) times the total number of devices connected to the HP-IB.

2-48. HP-IB Address Selection

2-49. 3497A Address. Each instrument on the HP-IB has a unique "talk" and "listen" address. The address of the 3497A is set by its Bus Address Switch. The Bus Address Switch is a seven section "DIP" switch located on the outguard logic board (board is behind the right rear panel of the instrument). Since the switch is on the outguard logic board, the board must be removed to change the 3497A's address setting. A procedure to remove the board is in paragraph 2-27.

2-50. The five switches labeled A1 through A5 in Table 2-1 are used to set the address. The other two switches are used to set the 3497A to the Talk-Only Mode (see paragraph 2-52) and the Power-On SRQ feature (see paragraph 2-54). For more information on the Talk-Only mode and Power-On SRQ, refer to Section III of this manual or the 3497A Operating, Programming, and Configuration Manual.

2-51. The 3497A normally leaves the factory with an address setting of decimal "09". The corresponding ASCII codes for the listen address is ")" and for the talk address is "I". The 3497A may be left at its factory setting or may be set to any alternate address setting, as shown in Table 2-1. The table also shows the instrument's address switch, factory address setting, and location of the switch on the outguard logic board.

2-52. Talk-Only Mode

2-53. The 3497A's Talk-Only mode is used to provide measurement data to another device, like a printer, without an HP-IB controller or computer. The mode is selected by setting the sixth switch of the Address Switch to the "1" (ON) position, as shown in Table 2-1. Refer to Section III of this manual or the 3497A Operating,

Programming, and Configuration Manual for more information.

2-54. Power-On SRQ

2-55. The 3497A's Power-On SRQ feature, when enabled, allows the instrument to output a Require Service message after the instrument is turned on. The feature is selected by setting the seventh switch of the Address Switch (labeled "SRQ ON" on the outguard board) to the "1" (ON) position, as shown in Table 2-1. Refer to Section III of this manual or the 3497A Operating, Programming, and Configuration Manual for more information.

2-56. SERIAL I/O OPTION CONNECTION AND CONFIGURATIONS

2-57. The 3497A, if the Serial I/O option is installed, is compatible with the Electronic Industries Association (EIA) standards RS-232C and RS-449 with RS-423 electrical subset. The CCITT (Comite Consultatif International Telephonique et Telegraphique; an international consultive body) standards V.24 and V.10 closely resemble RS-232C and RS-423 respectively, although they are not identical. Since the Serial I/O option does not use all of the interchange circuits defined by the standards (both EIA and CCITT), the respective EIA and CCITT standards can be considered equivalent from a 3497A operating standpoint.

2-58. EIA RS-232C (CCITT V.24)

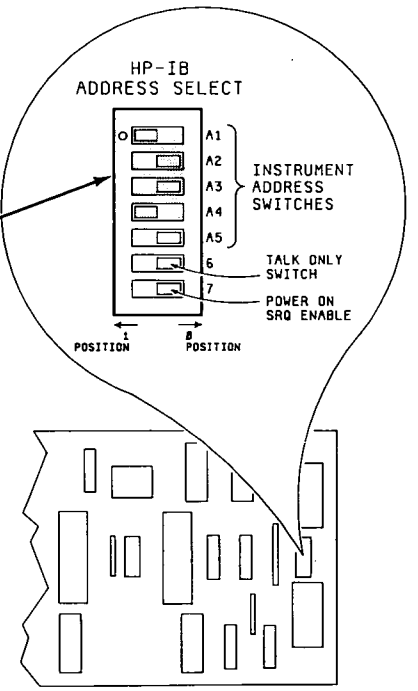
2-59. RS-232C specifies a 25-pin connector but does not define a particular type. The connector on one end of the cable supplied with the Serial I/O option has become the industry de facto standard. Standard RS-232C specifies that 22 of the pins will have dedicated assignments for the data, control and timing circuits, and leaves three pins unassigned. The electrical requirements are specified for synchronous or asynchronous (used by the 3497A) operation within its operating range of 0 to 20,000 bits per second (bps). For more information on RS-232C, refer to Appendix B of this manual.

2-60. EIA RS-449/423 (CCITT V.10)

2-61. RS-449 designates a 37-pin connector and encompasses two standards for the voltage requirements, RS-422 and RS-423. RS-423 is implemented by the 3497A and specifies the electrical characteristics for unbalanced voltage digital interface circuits. RS-423 and RS-232C

Table 2-1. HP-IB Address Selection

ASCII Code Character		Address Switches					5-bit Decimal Code
Listen	Talk	A5	A4	A3	A2	A1	
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
-	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	\	1	1	1	0	0	28
=	]	1	1	1	0	1	29
> °	~	1	1	1	1	0	30



have overlapping parameters permitting interoperation between the two types of devices. Performance will be limited by the RS-232C device. RS-422 is not RS232C compatible and is not implemented. For more information on RS-449/423, refer to Appendix B of this manual.

2-62. RS-232C or RS-449/423 Lines Required

2-63. The lines required for operation depend on the type of connection made. When the 3497A is interfaced directly to a computer (i.e., without a modem), the lines listed in Table 2-2 are required. When communicating with a computer or controller through a modem, the lines listed in Table 2-3 are required. The tables list both the RS-232C and equivalent RS-449/423 lines.

Table 2-2. Required Lines when Directly Connected to a Controller

RS-232C Line	RS-449/423 Line
Transmitted Data	Send Data
	Ground for Send Data
Received Data	Received Data
	Ground for Received Data
Signal Ground	Signal Ground

Table 2-3. Required Lines when Connected to a Modem

RS-232C Line	RS-449/423 Line
Transmitted Data	Send Data
	Ground for Send Data
Received Data	Received Data
	Ground for Received Data
Signal Ground	Signal Ground
Data Terminal Ready	Terminal Ready
	Ground for Terminal Ready
Data Carrier Detect	Receiver Ready
	Ground for Receiver Ready
Request to Send	Request to Send
	Ground for Request to Send
Clear to Send	Clear to Send
	Ground for Clear to Send
Data Set Ready	Data Mode
	Ground for Data Mode

2-64. System Configurations

2-65. The 3497A can be operated in a system in one of two ways:

a. Directly connected to a computer via RS-232C or RS-449/423.

b. Connected to an asynchonous full duplex modem, via RS-232C or RS-449/423, for remote site operation using dedicated or switched telephone lines.

Typical system configurations are shown in Figure 2-12.

2-66. Cable Requirements and Length Restrictions

2-67. The 3497A (if the Serial I/O option is installed) is supplied with a cable (-hp- Part No. 13222-60001) that has a 50-pin connector on one end and an RS-232C connector on the other end. The 50-pin connector plugs into the serial I/O connector on the rear panel. The RS-232C connector plugs either into a modem or computer.

2-68. RS-232C limits cable length to 50 feet (15.24 meters). The most important consideration is that the load capacitance at the interface point cannot exceed 2500pF. Longer cables are sometimes successfully used when the total load capacitance does not exceed 2500pF. A detrimental effect of excessive load capacitance is that it increases the rise and fall times of digital signals on the lines.

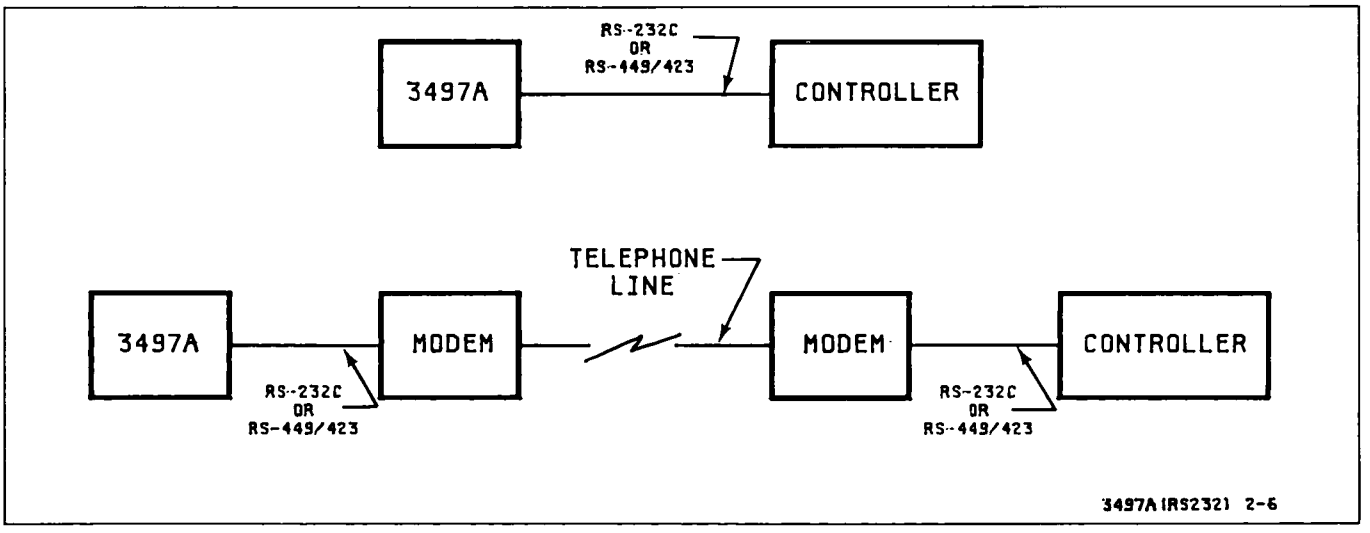


Figure 2-12. System Configurations

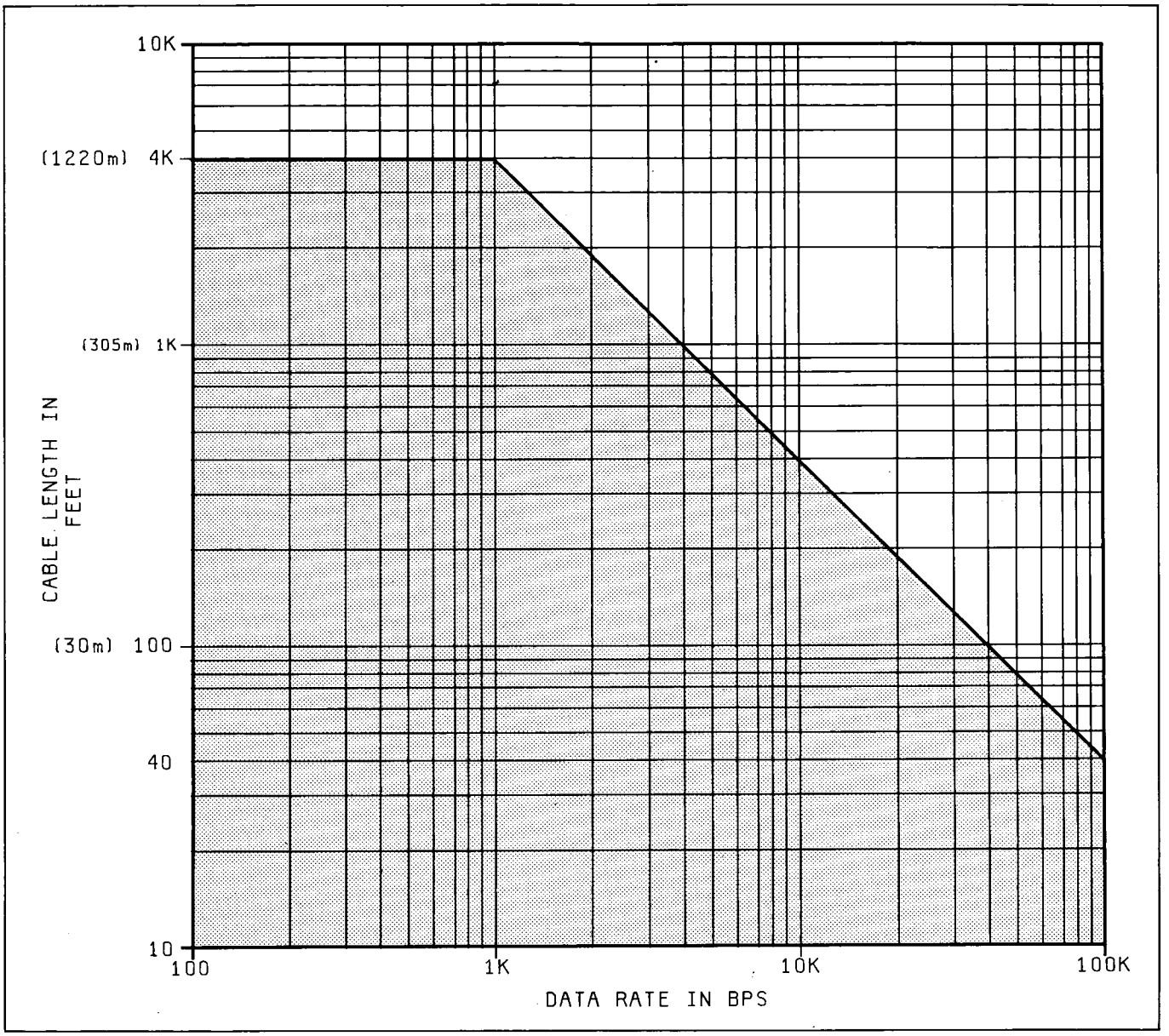


Figure 2-13. RS-449/423 Cable Length Restrictions

2-69. The cable length limits imposed by RS-449/423 depend on the speed of operation as shown in Figure 2-13. For example, with a cable length of 4000 feet (1200 meters), the maximum speed is 1000 bps. Figure 2-13 is based on calculations and emperical data using twisted pair telephone cables with a shunt capacitance of 16 pF per foot, a source impedance of 50 ohms, a 12 volt peak to peak source signal, and allowing a maximum near-end crosstalk of one volt peak. The source signal rise time at modulation rates below 900 bps is 100μS and above 900 bps is .1 bit time. Figure 2-13 does not account for cable imbalance or common mode noise beyond 4V (sum of ground potential difference, greater offset voltage and externally induced noise).

2-70. Interchange Circuits Required

2-71. The required RS-232C or RS-449/423 interchange circuits depend on the system configuration used (see Figure 2-12). These circuits were given in Tables 2-2 and 2-3. Make sure that all of the required lines are assigned properly in the connector which will be plugged onto the 3497A cable connector. Sometimes these assignments are altered to meet special applications. The 3497A assumes that the lines are assigned according to the respective standard used.

2-72. Configuration Switch Settings

2-73. General. The Serial I/O option is equipped with configuration switches that are preset at the factory to implement the following:

300 bits per second (bps)
DC1 Handshake "OFF"
7-bit ASCII with odd parity
Direct connect to a controller
RS-232C operation

2-74. Although the configuration switches are located on the outguard logic board, some of the switch settings can be read without removing the board. This is done by doing a system reset or system clear (see Section III of this manual for more information), or by turning the 3497A off and on again while watching the instrument's display. The first number in the display will be either a 0, 1, 2, or 3, dependent on how word length and parity is specified. The codes are as follows.

0 - 8-bit ASCII with odd parity
1 - 8-bit ASCII with no parity bit sent
2 - 7-bit ASCII with odd parity
3 - 7-bit ASCII with no parity bit sent

2-75. The second group of numbers indicates the selected speed of operation. For example, 19,200 bps would be displayed as 19.2, 9600 bps as 9.6, and so on. The status of the DC1, modem/controller, and RS-232C/RS-449 switches are not displayed. To read these switches, the outguard logic board must be removed. The procedure to remove the board is described in paragraph 2-27. Before going to the removal procedure, read the safety precautions in paragraph 2-6.

2-76. Configuration Switches. The configuration switches on the outguard logic board (S1 and S2) are preset at the factory. Switch S1 is used to configure the following:

Speed of operation in bits per second (bps)
On/Off state of the DC1 Handshake
7 or 8-bit ASCII with parity specifier
Connect to a modem or to a computer

Switch S2 is used to configure the following:

RS-232C
or
RS-449/423

2-77. Any of the factory settings can be verified or changed by removing the outguard logic board (refer to paragraph 2-27 for the removal procedure). The following paragraphs give the appropriate switch setting instructions for the configuration switches.

2-78. Speed of Operation Switches. Switch segments 1, 2, and 3 of switch S1 are preset at the factory for 300 bps as follows:

Switch segment 1 set to "0"
Switch segment 2 set to "1"
Switch segment 3 set to "1"

2-79. Refer to figure 2-14 to determine the location and possible configurations of switch segments 1 through 3. Note that the "0" and "1" positions are not labeled on the outguard logic board. Make sure you are looking at the switches correctly by orienting the board as shown in Figure 2-14. A "0" is set when a switch is positioned to the right and a "1" is set when positioned to the left.

2-80. To change the speed of operation, refer to the table in Figure 2-14. Choose the desired speed and change the switches accordingly. For example, if you wish to operate at 19,200 bps, set switch segments 1, 2, and 3 to "0" (right position).

2-81. DC1 Handshake Switch. Switch segment 4 of S1 is preset to "0" at the factory to disable the DC1 handshake (see Section III for information on DC1 handshake). To enable the DC1 handshake, set switch segment 4 to "1" (left position). Since the "0" and "1" positions are not labeled on the outguard board, orient the switch as shown in Figure 2-15.

2-82. Word Length and Parity Switches. Switch segment 5 and 6 of S1 are preset at the factory for 7-bit ASCII with odd parity, as follows:

Switch segment 5 set to "0"
Switch segment 6 set to "1"

2-83. Refer to figure 2-16 to determine the location and possible configurations of switch segments 5 and 6. Note that the "0" and "1" positions are not labeled on the outguard board. Make sure you are looking at the switches correctly by orienting the board, as shown in Figure 2-16. A "0" is set when a switch is positioned to the right and a "1" is set when positioned to the left.

2-84. To change the word length and/or parity, refer to the table in Figure 2-16. Choose one of four possible selections and then set the switch segments accordingly. For example, if you wish to select 8-bit ASCII with odd parity, set switch segment 5 and 6 to "0" (right position).

2-85. Controller and MODEM Switch. Switch segment 7 of S1 is preset to "0" at the factory. This is the correct setting when the 3497A is directly connected to a controller. When using a modem, set switch segment 7 to "1" (left position). Since the "0" and "1" positions are not labeled on the controller board, make sure the switch is oriented as shown in Figure 2-17.

2-86. RS-232C and RS-449/423 Switches. Switch segments 2, 3, 4, and 5 of switch S2 are preset at the factory to "0", which is the setting for RS-232C.

2-87. Refer to figure 2-18 to determine the location and possible configurations of switch segments 2 through 5. Note that switch segment 1 is not used and may be in either position. Also note that the "0" and "1" positions are not labeled on the outguard board. Make sure you are looking at the switches correctly by orienting the board as shown in Figure 2-18. A "0" is set when a switch is positioned to the right and a "1" is set when positioned to the left.

2-88. To change the operation for RS-449/423, refer to Figure 2-18 and move switch segments 2, 3, 4, and 5 to "1" (left position). Note that all of the switch segments are set either to "0" or "1", dependent on which serial standard (RS-232C or RS-449/423) is used.

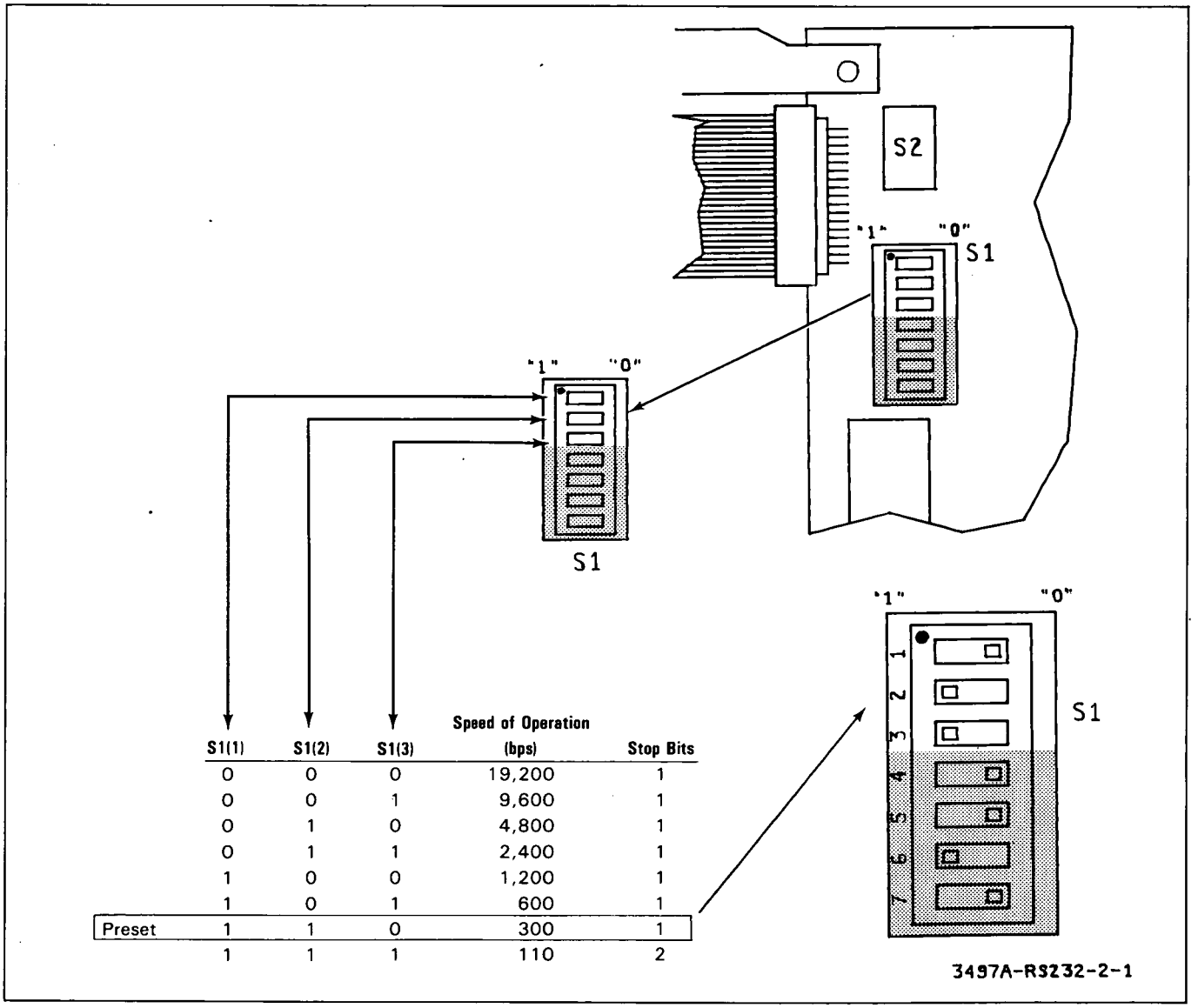
2-89. System Installation Procedure

2-90. Once the 3497A has been set-up for the desired configuration, use the following procedure to install the instrument in a system.

a. Locate the serial cable and plug it into the female connector on the 3497A rear panel. Then snap the two wire clips into place to secure it.

b. Connect the serial cable (RS-232C or RS-449/423) to the computer or the modem, dependent on system configuration used.

c. Plug the 3497A power cord into an ac power source and turn the instrument on. The 3497A is now ready for use.



	S1(1)	S1(2)	S1(3)	Speed of Operation (bps)	Stop Bits
	0	0	0	19,200	1
	0	0	1	9,600	1
	0	1	0	4,800	1
	0	1	1	2,400	1
	1	0	0	1,200	1
	1	0	1	600	1
Preset	1	1	0	300	1
	1	1	1	110	2

Figure 2-14. Serial I/O Speed of Operation Switches

2-91. 3497A INTERNAL CLOCK CONFIGURATION

2-92. Dependent on which option is selected, the 3497A's internal clock can be configured for an American Date Format (Month:Day:Hours:Minutes:Seconds) or a European Date Format (Day:Month:Hours:Minutes:Seconds). Option 230 is the American format and option 231 is the European format. The European format is selected by installing a jumper on the timer/pacer board. The American format is selected when the jumper is removed. The following paragraph has a procedure to reconfigure the clock.

2-93. Since the timer/pacer sits "piggyback" on the outguard logic board, the outguard board must be removed to reconfigure the timer/pacer board. Do the outguard logic board removal procedure in paragraph 2-29 before doing the following:

a. Refer to Figure 2-19. With the outguard logic board removed, locate and remove the timer/pacer board mounting screw on the outguard logic board. Remove the screw, as shown in Figure 2-19.

b. Locate the timer/pacer board on the non-component side of the outguard logic board. Remove the timer/pacer board.

c. Refer to Figure 2-20 and locate the clock configuration jumper on the timer/pacer board. If the American date format (Option 230, M:D:H:M:S) is desired, remove the jumper. If the European date format (Option 231, D:M:H:M:S) is desired, install and solder the jumper into the appropriate holes.

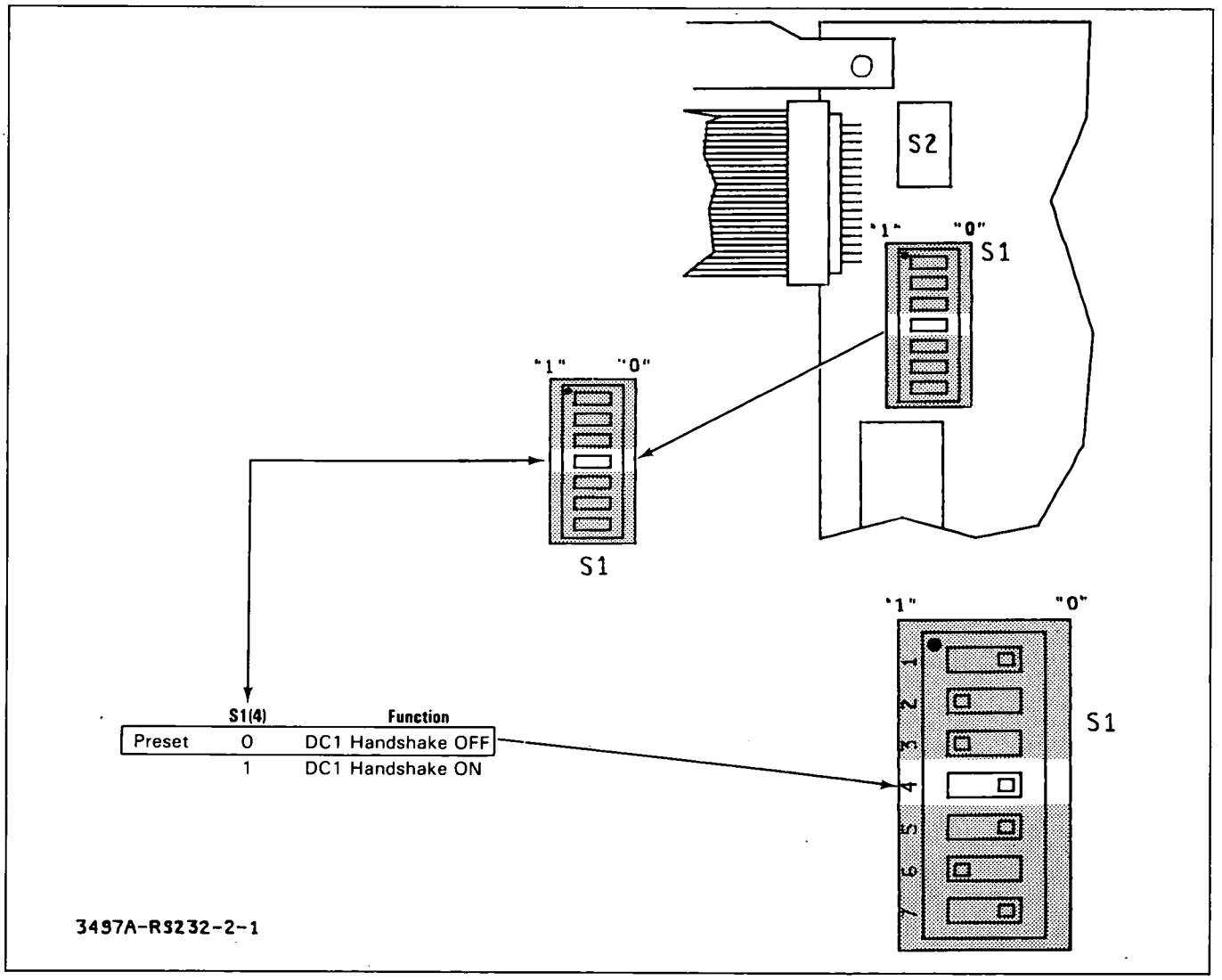


Figure 2-15. Serial I/O DC1 Handshake Switch

d. Once the clock is correctly configured, reinstall the timer/pacer board onto the outguard logic board. Then reinstall the mounting screw.

e. Go to paragraph 2-31 to reinstall the outguard logic board.

2-94. STORAGE AND SHIPMENT

WARNING

The 3497A is not intended for outdoor use. Do not expose it to rain or excess moisture.

2-95. Environmental Requirements

2-96. The instrument may be stored or shipped in environments within the following limits:

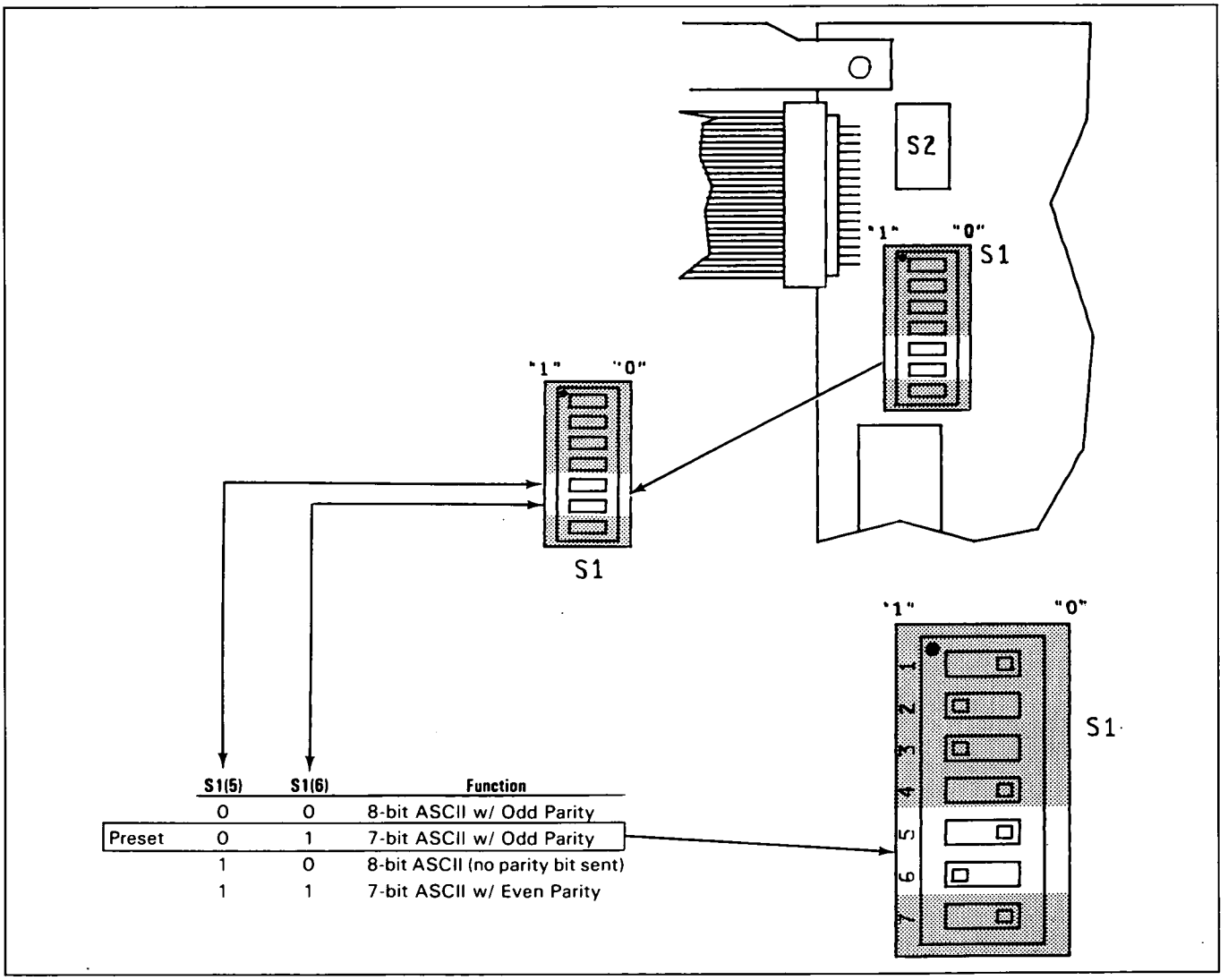
Temperature.....-40V°C to +75°C
Humidity.....Up to 95% at 40°C

The instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-97. Packaging

2-98. Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for service, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to insure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-99. Other Packaging. The following general instructions should be used for repacking with commercially available materials.



	S1(5)	S1(6)	Function
	0	0	8-bit ASCII w/ Odd Parity
Preset	0	1	7-bit ASCII w/ Odd Parity
	1	0	8-bit ASCII (no parity bit sent)
	1	1	7-bit ASCII w/ Even Parity

Figure 2-16. Serial I/O Word Length and Parity Switches

a. Wrap the instrument in heavy paper or anti-static plastic. If the instrument is being returned to Hewlett-Packard for service, attach a tag indicating the type of service required, return address, model number, and full serial number.

b. Use a strong shipping container. A double-wall carton made of 350 pound test material may be adequate.

c. Use a layer of shock-absorbing material 70mm to 100mm (3 to 4 inch) thick around all sides of the instrument, to provide firm cushioning and prevent movement inside the container. Protect the control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to insure careful handling.

f. In any correspondence with Hewlett-Packard, refer to the instrument by model number and full serial number.

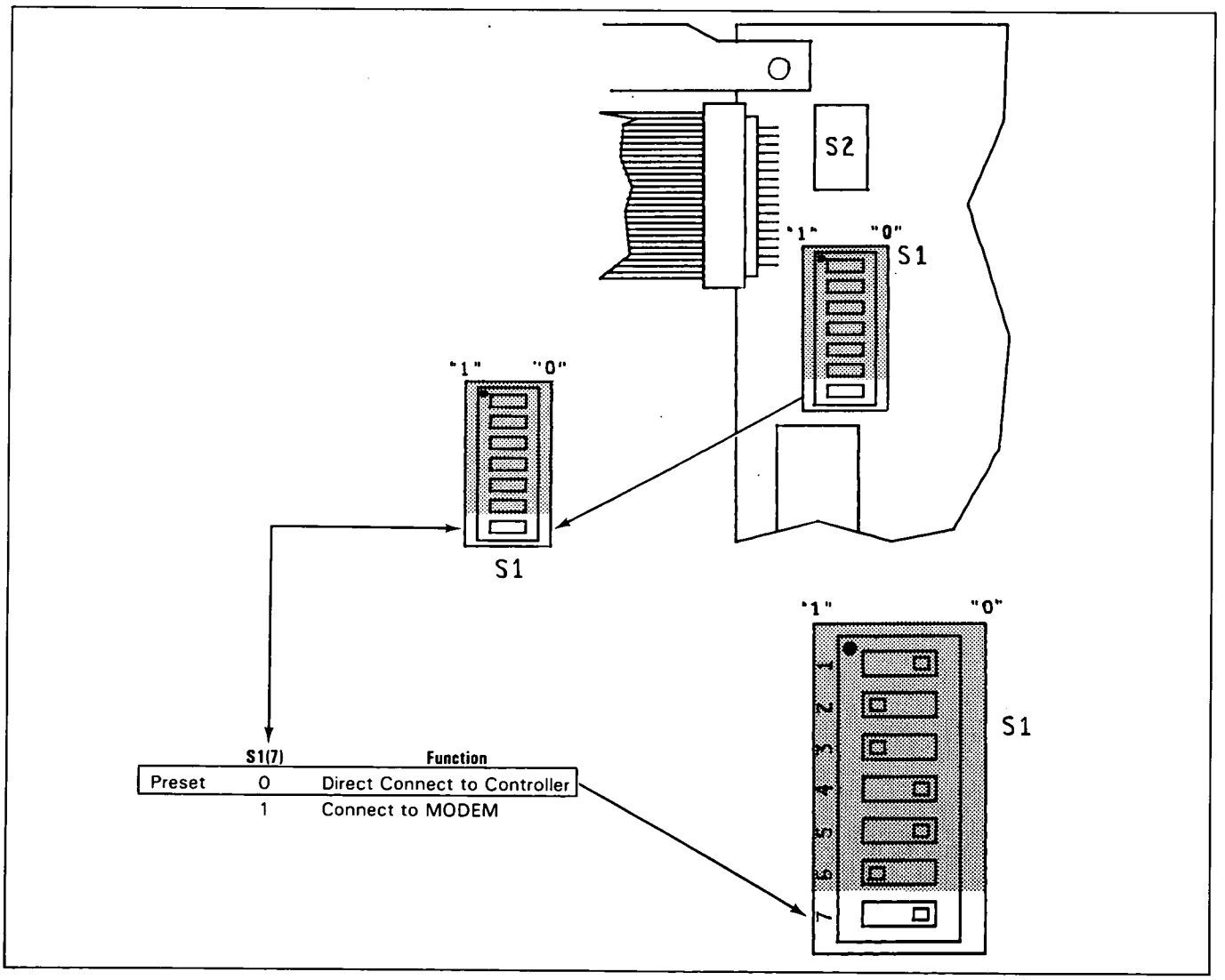


Figure 2-17. Serial I/O Controller/MODEM Switch

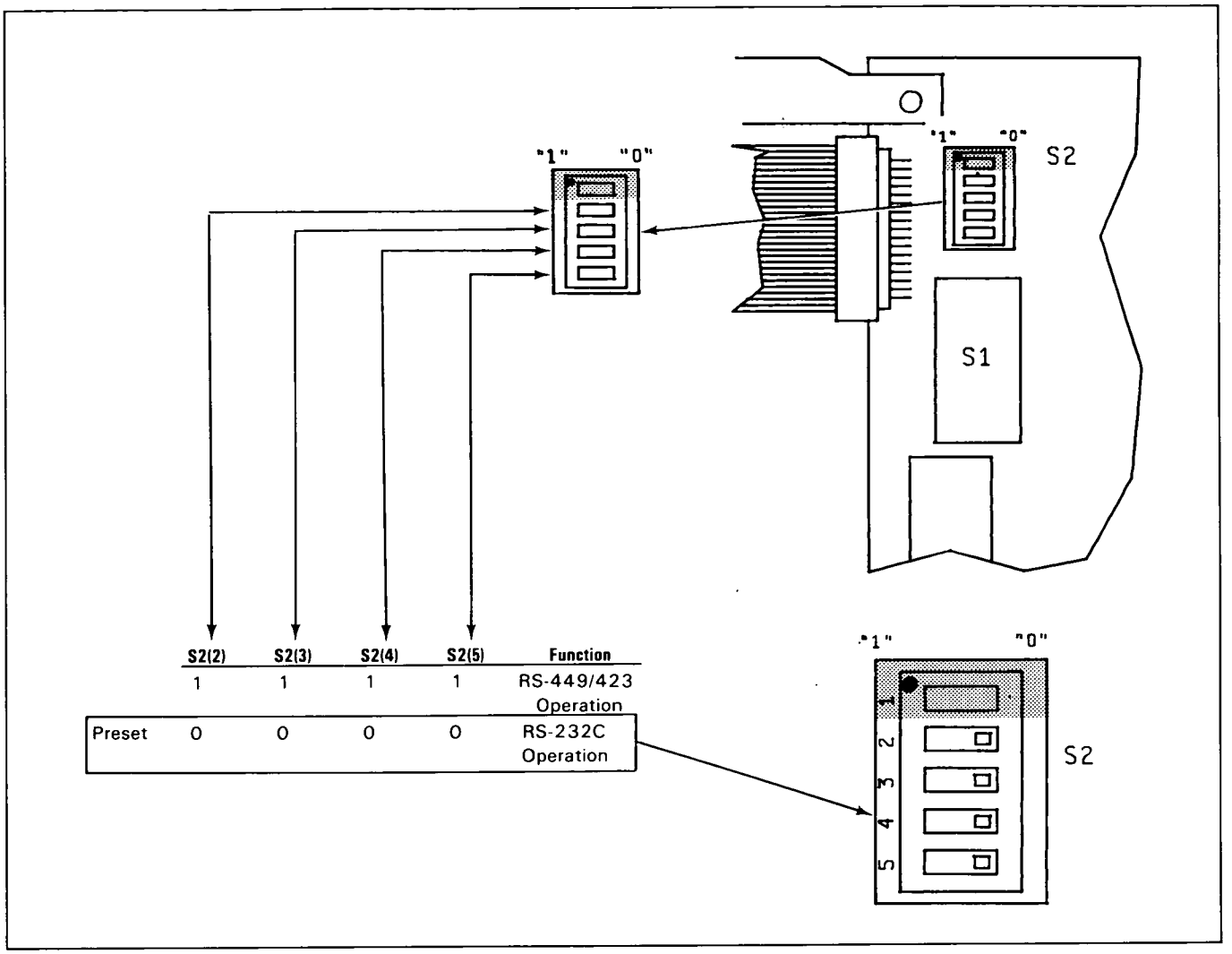


Figure 2-18. RS-232C and RS-449/423 Switches

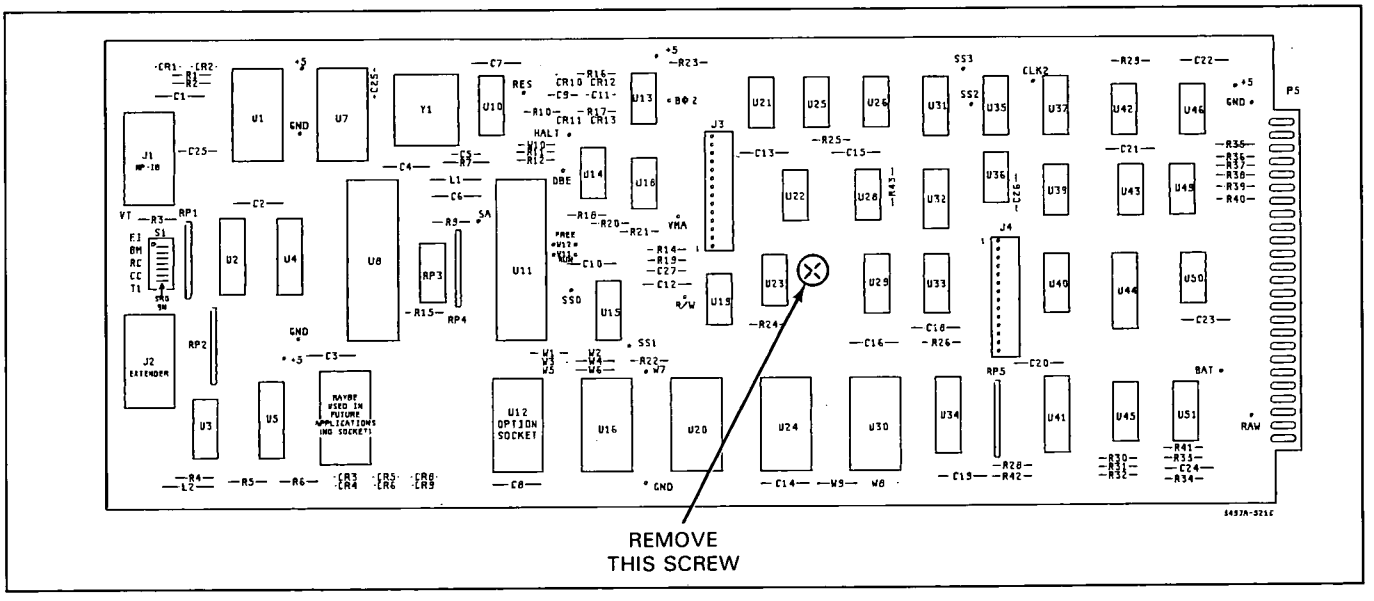


Figure 2-19. Timer/Pacer Board Mounting Screw

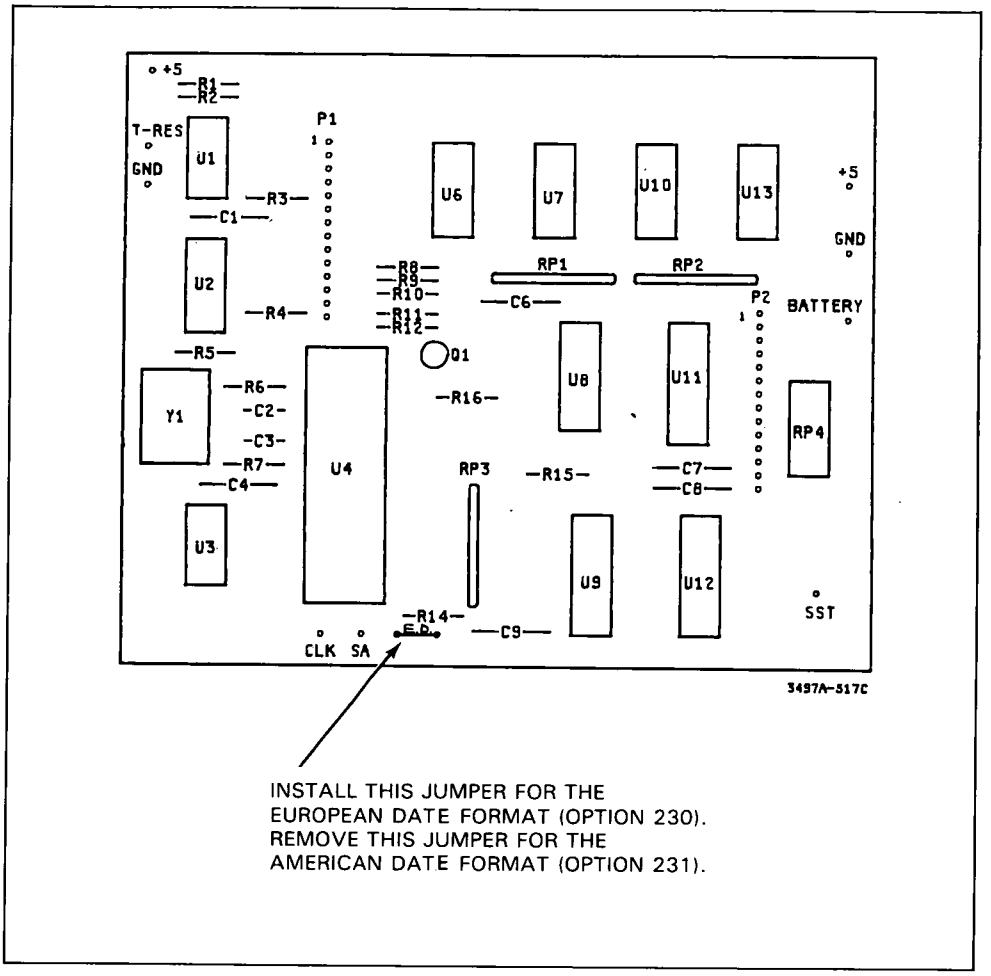


Figure 2-20. Clock Configuration Jumper

SECTION III
INSTRUMENT CONTROL

3-1. INTRODUCTION

3-2. This section of the manual contains information on how to control the 3497A mainframe using the standard front panel and over the HP-IB or Serial I/O bus. The information is an abbreviated description on controlling the instrument and is written for a Service Trained Person, rather than an operator. For more complete control information, refer to the 3497A Operating, Programming, and Configuration Manual.

3-3. Section III is separated into the following areas.

Mainframe General Information - paragraph 3-5
Front Panel Control (Standard Front Panel) - paragraph 3-16
Remote Control (HP-IB)- paragraph 3-20
Remote Control (Serial I/O) - paragraph 3-48

Front Panel Control is only possible if the standard front panel is installed. If the optional front panel (Option 260) is installed, no local control is possible. Instrument control using the HP-IB is only possible for the standard mainframe and control using the Serial I/O bus is only possible if the Serial I/O option (Option 232) is installed.

NOTE

HP-IB is Hewlett-Packard's implementation of IEEE Std. 488-1978, "Standard Digital Interface For Programmable Instrumentation" and ANSI MC.1.1.

3-4. The control information in the following paragraphs also includes information on controlling the voltmeter option (Option 001). The information only applies to instruments which have the voltmeter option installed. Ignore the information if the option is not installed.

3-5. MAINFRAME GENERAL INFORMATION

3-6. AC Power Requirements

3-7. Before connecting ac power to the 3497A, make sure the power source matches the requirments of the instrument (see line voltage switches behind the front panel). If the instrument is incompatible with the power source, refer to Section II of this manual for power requirement modification.

3-8. Turn-On and Reset

3-9. When the 3497A is first turned on, it goes through a Self-Test routine. This routine is used to check some of the mainframe circuitry (including front panel and timer/pacer assemblies). During the Self-Test routine, the display will show "3497A". After it goes through the routine and the test passes, either the reading from the voltmeter option is displayed or, if the option is not installed, dashes (----) are displayed.

3-10. If a failure is noted in the mainframe outguard circuitry, either "1" or "3" is displayed. A "1" shows that there is a crossguard failure and a "3" shows a timer/pacer failure. If any of these failures are noted, go to Section VIII for troubleshooting.

3-11. The Reset feature is used to return the 3497A back to the turn-on state without turning the instrument off and on. This is accomplished when the RESET button is pressed.

3-12. Self-Test

3-13. This test is similar to the one performed at turn-on. The major difference is that it has to be selected from either the front panel or over the HP-IB or Serial I/O bus. This test checks the voltmeter circuitry in addition to the outguard circuitry.

3-14. The Self-Test is enabled by either pressing the SELF TEST button on the standard front panel (if installed) or by sending program code "ST1" over the HP-IB (see paragraph 3-26) or the Serial I/O bus (see paragraph 3-52). The test is disabled by pressing the SELF TEST button a second time, by pressing the RESET button, or by sending program code "ST0" (if in remote) over the HP-IB or Serial I/O bus.

3-15. When the Self-Test is enabled and it passes, all of the front panel LEDs will turn on (if the standard front panel is installed). This will remain on as long as the test is enabled and shows that the test passes. This can also be checked remotely by reading the 3497A output. An output of "8E8" shows that the test passed. If any tests fail, a number is displayed which corresponds to the failing test. A "1" shows a crossguard failure, a "2" shows an A/D converter failure, and a "3" shows a timer/pacer failure. If any of these failures are noted, go to Section VIII for troubleshooting.

3-16. FRONT PANEL CONTROL (STANDARD FRONT PANEL)

3-17. All mainframe functions (except for some remote operations), can be controlled and selected from the standard front panel. If the optional front panel is installed (Option 260), no front panel control is available.

3-18. Refer to the 3497A front panel and note that most of the pushbuttons select either a function (e.g., Self-Test, Reset, etc.), a number from 0 to 9, a "," or a "-". In addition to these buttons, there is also a blue button. This button is the shift button and is used to reconfigure the numbered buttons and the "," and "-" buttons. When the blue button is pressed, the blue lettering below the buttons are the new configurations. The blue letters are used to select certain functions and operating modes of the 3497A. For example, the letter "T" selects the timer function, the letter "V" the dc voltmeter function, etc. The letters are also used to remotely program the instrument to those functions and modes. Once the appropriate letters and numbers are selected by pressing the corresponding buttons, press the EXECUTE button and the 3497A will then be configured to the new selected range and mode.

3-19. All of the letters, numbers, and the corresponding instrument functions and operating modes are listed in Table 3-1. The table is repeated in the 3497A Operating, Programming, and Configuration Manual. An example on how to select a function using the buttons follows this paragraph. In the example, the 10V range of the 3497A's DC Voltmeter (i.e., the voltmeter option) is selected. Do the following:

a. Press Blue Button. The blue lettering below the buttons is now valid for the number, ",", and "-" buttons.

b. Press "," Button. This button corresponds to the letter "V" which selects the DC voltmeter function. If the "0" button is pressed, the letter "T" is selected which selects the timer function. When the button is pressed, the front panel display will go blank.

c. Press "2" Button. This button corresponds to the letter "R" which selects the range mode of the voltmeter. Once this button is pressed, the number, ",", and "-" buttons go back to their normal configuration. The blue lettering no longer applies.

d. Press "3" Button. The numbers are now selected when a number button is pressed. Since number "3" button now selects the 10V Range, this button is pressed. If the number "2" button is pressed, the 1V Range is selected. When the "3" button is pressed, the number 3 will be displayed on the front panel display.

e. Press EXECUTE Button. The voltmeter is now set to the 10V Range.

3-20. REMOTE CONTROL (HP-IB)

3-21. General

3-22. All of the mainframe and voltmeter functions, ranges, and operating modes can be selected using the HP-IB. In addition, the clock, voltmeter readings, self-test results, and other mainframe and option outputs can be read using the HP-IB. Other remote functions include the Require Service operations. The following paragraphs give some information on how to remotely program and read the 3497A when using the HP-IB, and also information on the Require Service operation. For more complete remote information, refer to the 3497A Operating, Programming, and Configuration Manual.

3-23. A general description of the HP-IB is in Appendix A of this manual. Read the description if you are not familiar with the HP-IB. This information will be helpful when reading the following paragraphs.

3-24. 3497A HP-IB Addressing

3-25. HP-IB requires that a device on the HP-IB has a unique "listen" and "talk" address. The address for the 3497A is selected using the instrument's address switch, which is located on the main logic board. The 3497A's address is decimal "9". Refer to Section II of this manual for information on possible address codes and how to select the codes.

3-26. Setup of the 3497A Using the HP-IB

3-27. The 3497A mainframe, voltmeter option, and plug-in options are setup and configured using program codes. These codes are listed in Table 3-1, which also shows the functions of the different codes. The codes can also be noted on the standard front panel. For example, look at the SELF TEST pushbutton on the front panel and note that the "S" and "T" letters of the words SELF TEST are underlined. These letters are the program codes (with a "1" added) which are used to remotely select the self-test mode. It looks like this: "ST1". The "ST" selects the mode and the "1" turns it on. Besides the self-test function, other functions and operating modes also use the underlined letters on the front panel. An example on how to remotely send program codes using the Model HP-85A Computer is as follows:

```
OUTPUT 709 ;"ST1"
```

3-28. When the program codes are sent to the 3497A, the following sequence takes place.

a. The HP-IB remote (REN) line is enabled. This places the 3497A and all other devices on the HP-IB in remote. When this happens, the 3497A's "REMOTE" light will turn on, if it was previously off.

Table 3-1. 3497A Commands

ANALOG

AC chan#,chan#,... chan# = 0 to 999	ANALOG CLOSE. Closes 1 to 4 channels (one per decade) of analog assemblies.
AEn, n = 0 to 2 AE0 = EXT INCR OFF AE1 = EXT INCR ON AE2 = FAST SCAN	ANALOG EXTERNAL INCREMENT. Enables or disables the EXT INCR port. In FAST SCAN (AE2), multiframe BBM Sync is ignored. In AE1, external pulse into EXT INCR port increments channel closed to next channel.
AF chan# chan# = 0 to 999	ANALOG FIRST CHANNEL. Selects first channel to be closed in an analog sequence but does not close channel.
AI chan# chan# = 0 to 999	ANALOG INPUT. Closes channel and triggers DVM to take a measurement.
AL chan# chan# = 0 to 999	ANALOG LAST CHANNEL. Selects last channel to be closed in an analog sequence but does not close channel.
AO slot#,chan#,value slot# = 0 to 89 chan# = 0 or 1 value = 0 to ±10238 (VDAC) 0 to 10238 (IDAC)	ANALOG OUTPUT. Sets the output voltage level for the VDAC and output current level for the IDAC. VDAC output is −10.2375V to +10.2375V in 2.5 mV increments. IDAC output is 0−20 mA (5μA increments) or 4−20 mA (4 μA increments).
AR	ANALOG RESET. Opens analog assembly channels in 3497A and 3498A and sets VF1, VT1, VR5, VW0, VS0, AE0, AF0 and AL999.
AS	ANALOG STEP. Performs software channel advance from the presently closed channel to next channel. Repeating the command sequences channels from AF to AL and back to AF. If AF < AL, channels increment. If AF > AL, channels decrement.
AV chan# chan# = 0 to 999	ANALOG VIEWED CHANNEL. Dedicates display to channel selected but does not close channel and does not affect other 3497A operations. Display is updated when channel closed and measurement taken.

Table 3-1. 3497A Commands (Cont'd)

COUNTER

CE slot#,n
slot# = 0 to 4; n = 0 to 2 0 = No interrupts enabled 1 = Interrupt on measurement complete 2 = Interrupt on overflow

COUNTER ENABLE INTERRUPTS.

Enables counter to send an interrupt to 3497A when specified interrupt condition occurs. If 3497A is set for Digital Interrupt, interrupt is sent to controller.

CF slot#,n
slot# = 0 to 89; n = 0 to 6 0 = Counter Stop 1 = Count Up 2 = Count Down 3 = Avg 1000 Periods 4 = Avg 100 Periods 5 = Measure 1 Period 6 = Measure 1 Period

COUNTER FUNCTION.

Sets mode of operation for the counter and starts the function. CT command MUST be set before CF command is executed. For n = 3 to 6, CT slot#, 1 and 2 set period measurements and CT slot#, 3 and 4 set pulse width measurements.

CR slot#,n
slot# = 0 to 89; n = 1 to 3 1 = Read without wait 2 = Read with wait 3 = Read continuously

COUNTER READ.

Allows the results of counter measurements to be read in one of three ways.

CS slot#,value
slot# = 0 to 89 value = 0 to 999999

COUNTER SET.

Sets the start point (0 to 999999) for the Count Up or Count Down functions. Also sets number of pulses in Pulse Output mode (start point value = twice the number of pulses output).

CT slot#,n
slot# = 0 to 89; n = 1 to 4 1 = Rising/Rising Edges 2 = Falling/Falling Edges 3 = Rising/Falling Edges 4 = Falling/Rising Edges

COUNTER TRIGGER.

Selects edge of input signal on which to trigger counter. For Count Up or Count Down, CT slot#, 1 and 3 perform same function as do CT slot#, 2 and 4.

Table 3-1. 3497A Commands (Cont'd)

DIGITAL

DC slot#,chan#,chan#,... slot# = 0 to 89 chan# = 0 to 15	DIGITAL CLOSE. For Option 110 assembly, command connects NO contact to common. For Option 115 assembly, command closes channel relays. Channels not specified remain in previous state.
DE slot#,value slot# = 0 to 4 value = 0 to 377 (Octal)	DIGITAL INTERRUPT ENABLE. Enables the Option 050 assembly to send an interrupt to the 3497A when channel bits selected by the command are set true (by external input to the assembly).
DI slot# slot# = 0 to 4	DIGITAL INTERRUPT STATUS. Used to determine interrupt status of bits 0 – 7 in the Option 050 assembly. Also used to determine cause of interrupt from the Option 060 assembly.
DL slot# slot# = 0 to 89	DIGITAL LOAD. For Option 050 assembly, returns octal value (0 – 177777) of contents of 16 input channels. For Option 110 assembly, returns octal value (0 – 177777) of condition of 16 output channels. For Option 115 assembly, returns octal value (0 – 377) of condition of 8 channel relays.
DO slot#,chan#,chan#.... slot# = 0 to 89 chan# = 0 to 15	DIGITAL OPEN. For Option 110 assembly, connects NC contact to common for channels specified. For Option 115 assembly, opens relays in channels specified. Relays in channels not specified remain in previous state.
DR slot# slot# = 0 to 89	DIGITAL READ. For HP-IB, DR returns same information as DL command, except that readings are continuously updated. For Serial Data, with SO1 in effect returns continuously updated readings. With SO0 in effect, returns one reading per command.
DS slot# slot# = 0 to 4 value = 0 to 377 (Octal)	DIGITAL INTERRUPT SENSE. Sets edge transition sense which will cause channel 0 – 7 bits to be set in an Option 050 assembly. Polarity sense set by octal value. Polarity sense 1 = chan bit set by low-to-high transition.
DV slot# slot# = 0 to 89	DIGITAL VIEWED SLOT. Dedicates the front panel display to slot specified. To exit this mode, use DV without slot specifier.
DW slot#,value slot# = 0 to 89 value = 0 to 177777 (octal)	DIGITAL WRITE. For Option 110 assembly, connects NO or NC contact to common as specified by octal value. For Option 115 assembly, opens or closes relays as specified by octal value. All chans of assy in slot addressed are affected by DW command.

Table 3-1. 3497A Commands (Cont'd)

SYSTEM

SA	SYSTEM ALARM. Initiates an audible alarm (BEEP).
SC [Serial Data]	SYSTEM CLEAR. For Serial Data operation, the SC command is similar to BREAK message, except that SC does not clear the command buffer or return the 3497A to local mode. SC clears system errors but does not reset VF2, VF3 or clear voltmeter storage.
SDn SD0 = Display OFF SD1 = Display ON	SYSTEM DISPLAY. SD0 turns off the 6-digit display and CHANNEL lights for faster reading rates. With SD0, only data entered with SVn command affects display.
SEn [HP-IB] n = 0 to 377 (octal)	SERVICE REQUEST ENABLE. SE sets the SRQ mask bits which enables 3497A to send an interrupt to the controller when specified system conditions occur.
SEn [Serial Data] n = 0 to 377 (octal)	SERVICE REQUEST ENABLE. SE sets the interrupt mask bits which enables 3497A to send an interrupt to the controller when specified system conditions occur.
SI	SYSTEM INITIALIZE. Sets the digital assemblies and the DVM to initial conditions but does not affect the analog assemblies.
SLn [Serial Data] SL0 = Keyboard Enabled SL1 = Keyboard Disabled	SYSTEM LOCK. Used to disable the front panel keys so that commands can't be entered from the front panel. With SL1, 3497A can't be returned to local mode unless SL0 is sent or power is turned off.
SOn [HP-IB] SO0 = Output immed. SO1 = Output reading on controller request	SYSTEM OUTPUT WAIT. When SO1 in effect, two modes to return data to controller. With VS0, 3497A takes measurement and waits for controller request to transfer data. With VS1 or VS2, 3497A takes n readings (as set by VNn) and waits for controller request to transfer.
SOn [Serial Data] SO0 = Cont output SO1 = One output/comd	SYSTEM SINGLE/CONTINUOUS OUTPUT. SO1 enables 3497A to send a single reading/command for commands which normally return continuous data, such as ST, VT1, DR slot#, TD and CR slot#,3.
SR slot#,n slot# = 0 to 89; n = 0 to 7 SR slot#,0 = Read sig SR slot#,0–7 = Read register [Option 140]	SYSTEM READ. Use SR slot#,0 to determine type of assembly in slot (except analog assemblies). Use SR slot#, 0 through 7 to read register n in slot addressed (Option 140 only).

Table 3-1. 3497A Commands (Cont'd)

SR [Serial Data]	STATUS REGISTER READ. The SR command returns a six-bit octal value of the status register true bits.
STn ST0 = Self Test OFF ST1 = Self Test ON	SELF-TEST ST1 causes 3497A to perform internal self-test. 8E8 returned if self-test passes.
SVn n = ±999999	SYSTEM VIEW. When the display is turned off by an SD0 command, the SV command writes data specified by n to the display.
SW slot#,register#,data slot# = 0 to 89 register# = 0 to 7 data = 0 to 377	SYSTEM WRITE. Use SW to write data to any assembly directly controlled by the main processor (i.e. digital assemblies).
TIMER	
TA HH MM SS Hours = 0 to 24 Minutes = 0 to 59 Seconds = 0 to 59	TIME ALARM (SET). Sets 3497A timer. If SRQ mask (HP-IB) or interrupt mask (Serial Data) has been set for time alarm, interrupt sent to controller when time on real-time clock matches time set by TA.
TD MMDDHHMMSS or TD DDMMHHMMSS	TIME OF DAY (SET). Sets 3497A real-time clock to programmed time.
TD	TIME OF DAY (READ). Reads time of day from real-time clock. Data returned has format MM:DD:HH:MM:SS or (European) DD:MM:HH:MM:SS.
TEn TE0 = RESET TE1 = HALT TE2 = START	ELAPSED TIME (CONTROL). Use TEn to monitor elapsed time from start of an operation. Use the TE command (without a number) to read time elapsed since TE2 command received.
TE	ELAPSED TIME (READ). Use TE to read elapsed time (1 sec increments) since elapsed timer control started by TE2 command. Data returned has format DDDDDD sec.
TI HH MM SS	TIME INTERVAL. Use TIn to generate pulses from TIMER port with periods from 1 sec to 24 hr. If SRQ or interrupt mask set, 3497A sends interrupt for every pulse output.
TOn n = 0 to 9999	TIME OUTPUT. Use TOn to generate pulses from TIMER port with periods from 100 μsec to 0.9999 sec (in 100 μsec increments). Period output is n x 100 μsec. Interrupt not available with TOn command.

Table 3-1. 3497A Commands (Cont'd)

VOLTMETER

VAn VA0 = Autozero OFF VA1 = Autozero ON	VOLTMETER AUTOZERO. With autozero on, DVM takes measurement between each reading. With autozero off, DVM makes autozero measurement before first reading and when DVM switched to new range.
VCn n = 0 to 3 0 = OFF 1 = 10 μA 2 = 100 μA 3 = 10 mA	VOLTMETER CURRENT SOURCE RANGE. Programs output of DVM current source to 1 of 3 values: 10 μA, 100 μA or 10 mA.
VDn n = 3 to 5 3 = 3 1/2 digits 4 = 4 1/2 digits 5 = 5 1/2 digits	VOLTMETER DISPLAY. Selects number of digits to be displayed on front panel and sets voltmeter integration time. Max reading rate for 60 Hz operation is 300 readings/sec (Autozero OFF). Max rate for 50 Hz is 250 readings/sec.
VFn n = 1 to 3 1 = ASCII 2 = Packed BCD 3 = Time, ASCII, Chan#	VOLTMETER FORMAT. Selects the output format for transmission of data over the bus, when voltmeter storage is off (VSO).
VNn n = 1 to 999	VOLTMETER NUMBER READINGS/TRIGGER. Sets number of readings taken per trigger pulse input. Readings are taken sequentially and output over the bus in format set by VFn.
VRn n = 1 to 5 1 = 0.1V 2 = 1.0V 3 = 10 V 4 = 100V 5 = Autorange	VOLTMETER RANGE. Sets range of DVM. Maximum overrange capability for each range is 120% of full-scale. In autorange, DVM upranges at 120% of full-scale and downranges at 11% of full-scale.
VSn n = 0 to 2 0 = Storage OFF 1 = Store in ASCII 2 = Packed BCD	VOLTMETER STORAGE. Store up to 60 readings in ASCII (50 for Serial Data) or up to 100 readings in Packed BCD (85 in Serial Data). Use VS without number to transfer readings to controller.
VTn n = 1 to 4 1 = Internal 2 = External 3 = Software 4 = Hold	VOLTMETER TRIGGER. Set one of four trigger modes. In internal, DVM automatically takes another reading when present one completed. In external, trigger signal input to EXT TRIG port causes DVM to take n readings/trigger (as set by VNn). In software, command causes DVM to trigger and take n readings as set by VNn. In hold, DVM pauses and does not take measurements.
VWn n = 0 to 999999	VOLTMETER WAIT. Causes the DVM to wait n x 100 μsec between each reading. Maximum wait time is 99.9999 sec.

b. The unlisten command "?" is sent to all devices on the HP-IB.

c. The computer "talk" address, "U", is sent over the HP-IB to designate the computer as the Talker.

d. The 3497A "listen" address, ")", is sent to designate the 3497A as the Listener. When this happens, the 3497A's "LISTEN" light will turn on, if it was previously off.

e. After the 3497A is set to listen, program code "ST1" is now sent to the instrument.

f. A carriage return (CR), line feed (LF), and End or Identify (EOI) statement are sent to the 3497A. This completes the sequence.

The program sequence looks like this:

"?U)","ST1" CR LF (and EOI)

3-29. Reading the 3497A's Output Using the HP-IB

3-30. Various 3497A outputs can be read using the HP-IB. These include the dc voltmeter readings, time of day, self-test results, and outputs from the plug-in options. An example on how to read the 3497A output using the Model HP-85A Computer is as follows:

ENTER 709 ; A

3-31. When the 3497A output is read, the following sequence takes place.

a. The HP-IB remote (REN) line is enabled. This places the 3497A and all other devices on the HP-IB in remote. When this happens, the 3497A's "REMOTE" light will turn on, if it was previously off.

b. The unlisten command "?" is sent to all devices on the HP-IB.

c. The computer "listen" address, "5", is sent over the HP-IB to designate the computer as the Listener.

d. The 3497A "talk" address, "I", is sent to designate the 3497A as the Talker. When this happens, the 3497A's "TALK" light will turn on.

e. After the 3497A is set to talk, it will output its data (i.e., voltmeter reading, time of day, etc.). This data is stored into variable "A" by the computer.

f. The carriage return (CR) and line feed (LF) statements are then sent to the computer. This completes the sequence.

The sequence looks like this:

"?5I",DATA CR LF

3-32. Require Service

3-33. The 3497A can output a Require Service message under certain conditions. To output the message, the 3497A's SRQ Mask must first be set. The only exception is the Power-On SRQ function (see paragraph 3-36) which is set using part of the 3497A's address switch. Once the SRQ Mask is set and the instrument requires service, the Require Service Message is output. When the message is output, the front panel SRQ light will then turn on. The 3497A is then normally polled (i.e., Serial Poll performed) by the computer. When the computer polls the 3497A, the 3497A outputs a status byte message. The high and low levels (i.e., output state) of this message depends on what bits in the SRQ Register are set (true) and not set (not true). The bits set (true) in the SRQ Register results from the condition that caused the Require Service Message. The following paragraphs have information on the SRQ Register, how to setup the SRQ Mask, and the Power-On SRQ function.

3-34. SRQ Register. The SRQ Register is shown in Figure 3-1. Each bit in the register, when true, shows the reason why the Require Service Message is output. The true bits are cleared (i.e., set untrue) when the 3497A is polled.

3-35. Setting the SRQ Mask. The SRQ Mask is set by sending program code "SExx" where "SE" enables the mask and "xx" is the octal code of the bits in the SRQ Register that are to be set. For example, to set the Time Interrupt bit in the SRQ Mask, send program code "SE10". If more than one bit is to be set, use the octal number of all the bits which are to be set. For example, to set the Time Interrupt bit and the Time Alarm bit, send program code "SE14".

3-36. Power-On SRQ Function. The Power-On SRQ Function, when enabled, outputs a Require Service Message when power is applied to the 3497A (with the instrument turned on). This can be used to determine if a power failure has occured while the instrument was operating. Unlike the other bits in the SRQ Register, the Power-On SRQ bit is set by the address switch (see Section II of this manual on how to set the switch).

3-37. Talk-Only Mode

3-38. This mode is used to transfer data (dc voltmeter readings) to another HP-IB device without using a controller. This feature is selected by the address switch (see Section II of this manual on how to set the switch). When the feature is selected, the dc voltmeter reading is output over the HP-IB each time the voltmeter is triggered.

MAN SRQ	SRQ	PON SRQ	MSG NOT EXEC	TIME INTERV	TIME ALARM	DIG INT	DRS
b7	b6	b5	b4	b3	b2	b1	b0
MSD			2nd MSD			LSD	

Bit	Function	Definition
b7	MAN SRQ	Bit set when front panel button is pressed
b6	SRQ	SRQ bit set when 3497A requires service (Require Service Message output)
b5	PON SRQ	Bit set when 3497A turned on after power failure
b4	MSG NOT EXEC	Bit set when incorrect syntax is sent to the 3497A
b3	TIME INTERV	Bit set when time interval is completed
b2	TIME ALARM	Bit set when the set time alarm is reached by the internal clock
b1	DIG INT	Developed by the Digital Plug-In Option(s) (see option manual)
b0	DRS	Bit set when voltmeter is ready to output data (i.e., reading)

Figure 3-1. SRQ Register

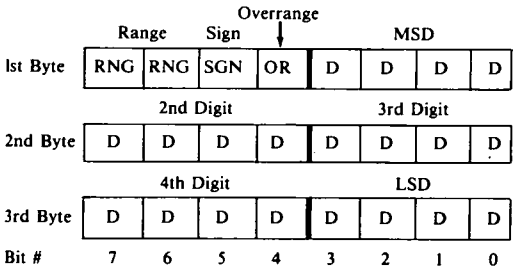
3-39. Output Format

3-40. The voltmeter readings can be output over the HP-IB in two different formats: ASCII and Packed. The following paragraphs explain the two different output formats. Other outputs, like the Time of Day, are only output in the ASCII Format.

3-41. ASCII Format. The dc voltmeter's output in the ASCII Format is normally selected when the 3497A is turned on or reset. It can also be selected by sending program code "VF1". The output, when in the ASCII Format, consists of 13 bytes and looks like this:

±D.DDDDD±D CR EOI LF

3-42. Packed Format. The dc voltmeter's output in the Packed Format is selected by sending program code "VF2". The output consists of 3 bytes and looks like this:



MSD-LSD are in BDC

Range	Sign
00 = .1V	1 = −(minus)
01 = 1V	0 = +(plus)
10 = 10V	
11 = 100V	Overrange
	1 or 0

199999 indicates overload

±.DDDDDD + D

Decimal point is assumed to be left of overrange digit. Range bits determine range (e.g. for 11 = 100V, move decimal three(11) places to right).

NOTE

A program to unpack the output of the 3497A in the Packed Format is in the 3497A Operating, Programming, and Configuration Manual.

3-43. Other HP-IB Operations

3-44. The following paragraphs explain the response of the 3497A when certain HP-IB messages are sent.

3-45. Trigger Message. When the Trigger Message is sent to the 3497A, two actions take place. The dc voltmeter is triggered (if the voltmeter option is installed) and the next channel on the analog plug-in option is selected (if an option is installed).

3-46. Clear Message. This message, when sent, sets the 3497A to the turn-on state.

3-47. Local Lockout. All the front panel pushbuttons, including the LOCAL button, have no effect when this message is sent.

3-48. REMOTE CONTROL (SERIAL I/O)

3-49. General

3-50. All of the mainframe and voltmeter functions, ranges, and operating modes can be selected over the Serial I/O bus. In addition, the clock, voltmeter readings, self-test results, and other mainframe and option outputs can be read over the bus. Other remote functions include the Interrupt Mask and Status Register operations. The following paragraphs give some information on how to remotely program and read the 3497A using the Serial I/O bus. For more complete remote information, refer to the 3497A Operating, Programming, and Configuration Manual.

3-51. A general description of the Serial I/O bus is in Appendix B of this manual. Read the description if you are not familiar with the bus. This information will be helpful when reading the following paragraphs.

3-52. Setup of the 3497A Using the Serial I/O Bus

3-53. The 3497A mainframe, voltmeter option, and plug-in options are setup and configured using program codes (or commands). These codes are listed Table 3-1, which also shows the functions of the different codes. The codes can also be noted on the standard front panel. For example, look at the SELF TEST pushbutton on the front panel and note that the "S" and "T" letters of the words SELF TEST are underlined. These letters are the program codes (with a "1" added) which are used to remotely select the self-test mode. It looks like this: "ST1". The "ST" selects the self-test function and the "1" turns it on. Other functions and operating modes also use the underlined letters on the front panel. An example on how to remotely send program codes using the Model HP-85A Computer is as follows:

```
OUTPUT 10 USING "K" ;"ST1"
```

3-54. When the program code is sent to the 3497A, the computer then sends a Carriage Return (CR). This tells the 3497A that all of the data has been sent. Unlike HP-IB, the Serial I/O bus requires that no Line Feed (LF) is sent. This is deleted by the "#,K" symbols in the output statement of the HP-85A.

3-55. Reading the 3497A's Output Using the Serial I/O Bus

3-56. Various 3497A outputs can be read using the Serial I/O Bus. These include the dc voltmeter readings, time of day, self-test results, and outputs from the plug-in options. An example on how to read the 3497A output using the Model HP-85A Computer is as follows:

```
ENTER 10 USING "#,K" ; A
```

3-57. When the 3497A output is read, its output is stored into variable "A". Since the computer normally requires a Line Feed (LF) and since no Line Feed is sent by the 3497A, the "#,K" symbols are used so that the computer will only recognize the Carriage Return (CR) and not the Line Feed.

3-58. Implementing DC1

3-59. DC1 should only be used in situations where the computer is not capable of receiving data from the 3497A at any time. If DC1 is to be implemented, refer to Section II of this manual to configure the the switch for this function. With DC1 enabled, the 3497A will not send any data requested until it receives the DC1. To send DC1 using the HP-85A, send the following:

```
OUTPUT 10 USING "#,K" ; CHR$(17)
```

3-60. Interrupt Mask

3-61. The Interrupt Mask is set by sending program code "SExxx" where "SE" enables the mask and "xxx" is the octal code of the bits in the mask that are to be set. For example, to set the Time Interrupt bit in the mask, send program code "SE110". Octal number "10" sets the Time Interrupt bit and octal number "100" sets the SRQ Enable bit. The Interrupt Mask is shown in Figure 3-2. The eight bits in the mask is a replica of the first eight bits in the Status Register (see paragraph 3-63).

3-62. When a bit is set in the Interrupt Mask and the resultant condition appears, an interrupt is sent to the computer via the break message. The transmitting line is then held in the space condition for about 20mS.

3-63. Status Register

3-64. The Status Register is updated as events occur and is completely independent of the Interrupt Mask. The Status Register is read using program code "SR". To read the register, first send code "SR" and then read the 3497A immediately. This is represented as follows:

```
OUTPUT 10 USING "#,K" ;"SR"
ENTER 10 USING "#,K" ; A
```

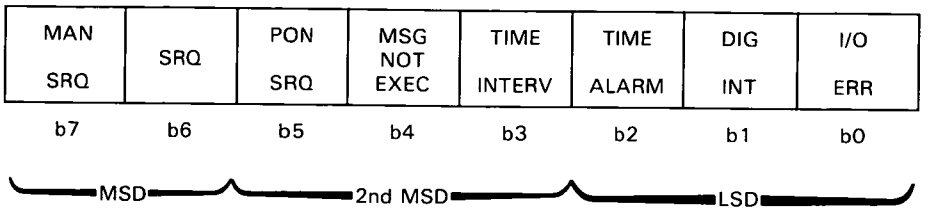
3-65. The first eight bits (bits 0 through 7) is a replica of the eight bits in the Interrupt Mask (see paragraph 3-60). An "SR" program code (or command), however, causes six octal digits to be returned with leading zeroes suppressed. The Status Register and the bit assignments are given in Figure 3-3.

3-66. Voltmeter Output Format

3-67. The voltmeter readings can be output over the Serial I/O bus in two different formats: ASCII and Packed. The dc voltmeter's output in the ASCII Format is normally selected when the 3497A is turned on or reset. It can also be selected by sending program code "VF1". The output, when in the ASCII Format, consists of 13 bytes and looks like this:

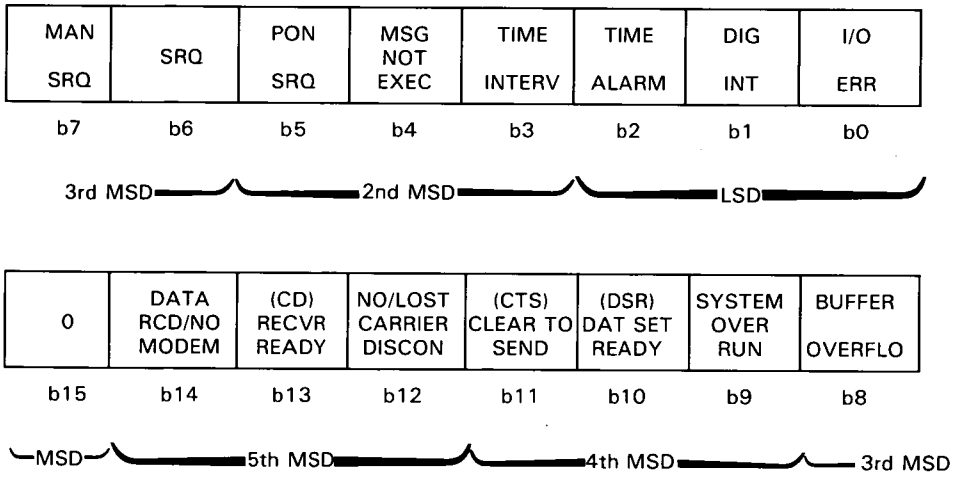
```
±D.DDDDD±D CR
```

In the Packed Format, the readings are output using three bytes. The bytes are the same as used with the Packed Format that is used with the HP-IB operation (see paragraph 3-42).



Bit	Function	Definition
b7	MAN SRQ	Activated from the front panel
b6	SRQ	SRQ enable which enables a break when an interrupt causing event occurs
b5	PON SRQ	Enables a break if the 3498A Extender experiences a power loss
b4	MSG NOT EXEC	Enables a break if syntax is wrong, voltmeter storage buffer is full, etc.
b3	TIME INTERV	Enables a break when a specific time interval has elapsed
b2	TIME ALARM	Enables a break if a time alarm match occurs
b1	DIG INT	Digital Plug-In options are enabled to develop an interrupt
b0	I/O ERR	Bit set when parity, overrun, or framing error occurs

Figure 3-2. Interrupt Mask



Bit	Function	Definition
b0	I/O ERR	Bit set when parity, overrun, or framing error occurs
b1	DIG INT	Developed by the Digital Plug-In Option(s) (see option manual)
b2	TIME ALARM	Bit set when the set alarm time is reached by the internal clock
b3	TIME INTERV	Bit set when time interval is completed
b4	MSG NOT EXEC	Bit set when incorrect syntax is sent to the 3497A
b5	PON SRQ	Bit set when 3497A turned on after power failure
b6	SRQ	SRQ bit set when an interrupt causing event occurs
b7	MAN SRQ	Bit set when front panel button is pressed
b8	BUFFER OVERFLO	Bit set if command string exceeds 42 characters
b9	SYSTEM OVERRUN	Bit set if a command is received while 3497A is busy with other command
b10	DATA SET READY	Bit set when the modem turns on its handshake line
b11	CLEAR TO SEND	When bit is set this modem line is on
b12	NO OR LOST CARRIER	Bit set if a modem connect sequence fails the 20 second time-out
B13	DATA CARRIER DETECT	When bit is set this modem line is on
b14	DATA RCD/NO MODEM	Data received when modem is not connected
b15	0	Always 0

Figure 3-3. Status Register

SECTION IV
PERFORMANCE TEST AND ADJUSTMENT

4-1. INTRODUCTION

4-2. This section of the manual has the 3497A's performance verification checks, performance tests, adjustment procedures, and specifications for both the standard (HP-IB) and Option 232 (Serial I/O) mainframes. The performance verification checks determine if the mainframes and the standard front panel are operational. The performance tests are used to check the voltmeter option against the published specifications. The adjustment procedures are used to calibrate the instrument to the published specifications and to do the necessary adjustments after troubleshooting the instrument.

4-3. Since the same equipment is used to adjust (i.e., calibrate) and check the performance of the voltmeter option, the adjustment procedures are combined with the performance test procedures. The procedures are set up in such a way that the tests can be ignored, if so desired. A separate performance test is, however, given for the voltmeter option.

4-4. INSTRUMENT SPECIFICATIONS

4-5. Specifications are the performance characteristics of the instrument which are certified. These specifications, listed in Table 4-1, are the performance standards or limits against which the 3497A can be tested. Table 4-1 also lists some supplemental characteristics of the 3497A that should be considered as additional information only.

4-6. Any changes in the specifications due to manufacturing changes, design, or traceability to the National Bureau of Standards will be covered in a manual change supplement or revised manual. The specifications listed here supercede any previously published.

4-7. Specification Breakdown

4-8. The 3497A's specifications are grouped according to instrument function (e.g., DC Volts and DC Current Functions of the voltmeter option). Within each group there may be one, two, or three main sets of specifications: the 24 hour, 90 day, and 1 year limits. The limits to which the instrument conforms depends on when the instrument was last calibrated and the instrument function. The 24 hour limits should only be used if the instrument was calibrated within the last 24 hours, otherwise the 90 day or 1 year limits apply.

4-9. For the voltmeter option only, each set of specifications includes an accuracy specification for each voltage and current range. They are specified as a percentage of the reading and an add-on of a certain number of counts. For example, the 24 hour full scale DC Volts Function accuracy on the 10V Range (in the 5 Digit Display Mode) is:

$$\pm .002\% \text{ of reading} + 1 \text{ count}$$

giving a full scale accuracy of $\pm .002\%$ or (2 count) plus 1 count (or .001%), which is a total of 3 counts (or $\pm .003\%$). (This is only true at full scale and changes at 1/10 scale; see next paragraph.)

4-10. The number of counts changes the accuracy of the voltmeter option at 1/10 scale. For example, the percentage (same function, range, and digit mode) at 1/10 scale is still .002%. However, the number of counts (1) is .01% at 1/10 scale. This gives a total of .012% rather than .003%.

4-11. EQUIPMENT REQUIRED

4-12. All required test equipment for the performance verification checks, performance tests, adjustment procedures, and troubleshooting procedures are listed in Table 4-2 (Recommended Test Equipment). The equipment used for the individual tests and adjustment procedures are also listed at the beginning of each procedure. The equipment required for troubleshooting are listed in the troubleshooting procedures (in Section VIII of this manual). If any of the recommended equipment is not available, use substitute equipment. A short description of the required equipment and the critical specifications necessary to do the test and adjustment procedures is in the following paragraphs. This information may be helpful in choosing substitute equipment.

4-13. Mainframe Performance Verification Check (HP-IB)

4-14. Desktop Computer. The recommended computer to do the checks is as follows:

a. A Model HP-85A Desktop Computer with an 82937A I/O Interface Card and I/O ROM (-hp- Part No. 00085-15003). If a different computer is used, refer to the block diagram description of the test procedure (in Figure 4-4) to write the test program.

b. An -hp- Model 5328A Counter (includes Options 11 and 41) with HP-IB capabilities and 10nS resolution.

4-15. Mainframe Performance Verification Check (Serial I/O)

TABLE 4-1. SPECIFICATIONS

STANDARD (HP-IB) MAINFRAME SPECIFICATIONS

CLOCK:

Format:

Option 230:
U.S. Month:Day:Hours:Minutes:Seconds

Option 231:
European Day:Month:Hours:Minutes:Seconds

Modes:

Function	Maximum Time	Resolution	Accuracy	Outputs
Real Time	1 year	1 second	±(.005% of Time + 0.1 seconds)	HP-IB SRQ
Time Alarm	24 hours	1 second	±(.005% of Time +0.1 seconds)	HP-IB SRQ
Time Interval	24 hours	1 second	±(.005% of Time +0.1 seconds)	HP-IB SRQ TTL Pulse
Elapsed Time	10^6 seconds	1 second	±(.005% of Time +0.1 seconds)	N/A
Timer Output	1 second	100 μseconds	±.02% of Time	TTL Pulse

Power Failure Protection:

Battery backup for 24 hours for all functions except TIMER OUTPUT.

OUTPUTS:

Time Output:

Mode	Accuracy	Pulse Width
Time Interval	±(.005% of Time + 0.1 seconds)	50 μseconds ± 10%
Timer Output	±(.02% of Time)	16 μseconds ± 10%

ENVIRONMENTAL:

Warm Up Time: 1 hour

Operating Temperature: 0°C to +55°C

Non-operating Temperature: −40°C to +75°C

Humidity: 95% at 40°C, except as noted.

Shock: 30G, 11 Msec half sine wave on each of six sides.

Vibration: 10 Hz to 55 Hz to 0.010 inch peak-to-peak excursion.

Operating Power: Switch selection of 100/120/220/240 ±10% 48-66Hz, less than 150 VA.

Physical Parameters:

Size: 428.6 mm (16.87 inches) wide
520.7 mm (20.5 inches) deep
190.5 (7.5 inches) high

Net Weight: 20.4 Kg (45 lbs.)
(Maximum, with assemblies in all slots.)

Shipping Weight: 26.3 Kg (58 lbs.)

Table 4-1. Specifications (Cont'd)

SERIAL I/O OPTION (OPTION 232) SPECIFICATIONS

These specifications are particular to the 3497A Option 232 operating at 60 Hz line frequency. For 50 Hz operation, multiply rates by 5/6. Such specifications are as common to both the standard HP-IB 3497A and Option 232 are found in the 3497A Data Sheet publication 5952-8886.

BPS RATE VS. DISTANCE

RS232C (V.24) recommends a maximum cable length of 50 feet or less than 2500 pf total load capacitance.
The distance specifications for RS432 (V.10) are:

BPS	110	300	600	1200
Distance	1200 m	1200 m	1200 m	900 m
	4000 ft	4000 ft	4000 ft	3000 ft

BPS	2400	4800	9600	19200
Distance	600 m	300 m	120 m	60 m
	2000 ft	1000 ft	400 ft	200 ft

MAXIMUM READING RATE FOR 85 READINGS

Packed mode, display off, reading storage on, single trigger burst, fixed channel

#Digits	Auto Zero On	Auto Zero Off
3½	205	300
4½	125	205
5½	26	50

BPS VS READING RATE

Readings transferred directly into the computer. Packed mode, display off, internal trigger, fixed range.

Auto Zero Off	300	1200	9600	19200
3½	10	38	190	210
4½	10	38	130	175
5½	10	30	45	45

Auto Zero On	300	1200	9600	19200
3½	10	38	140	160
4½	10	38	100	110
5½	10	20	25	25

ASCII mode, display off, internal trigger.

Auto Zero Off	300	1200	9600	19200
3½	3	10	65	100
4½	3	10	60	86
5½	3	10	30	38

Auto Zero On	300	1200	9600	19200
3½	3	10	60	90
4½	3	10	50	70
5½	3	8	20	22

Minimum analog switching time for sequential scanning: 280 channels/s (ch/s)

Minimum analog switching time for random scanning 10 Channels or less: 125 channel/s (ch/s)

>10 Channels

BPS	300	1200	9600	19200
Switching Rate ch/s	7	26	83	95

Minimum analog switching and reading time for sequential scanning:

BPS	300	1200	9600	19200
Switching Rate ch/s	10	40	120	130

Minimum analog switching and reading time for random scanning 10 channels or less:

BPS	300	1200	9600	19200
Switching Rate ch/s	5	18	60	65

<10 Channels

BPS	300	1200	9600	19200
Switching Rate ch/s	7	13	25	27

Interrupt response. The length of time for BREAK to be sent to the computer after an interrupt occurs: 150 ms. Includes HP-85A response time.

D to A output response vs BPS. The length of time required to respond to a change in the output of the D to A card after the commands for change are received by the 3497A.

BPS	300	1200	9600	19200
Switching Rate ms	500	175	100	100

Handshakes: ENQuire/ACKnowledge and DC1

Error Checking: Even, odd, or no parity. On detection of a parity error, the status register sets a bit for parity error.

OUTPUT DATA FORMAT

The 3497 has the ability to send data in ASCII or packed BCD. The output format for ASCII is:

Volt Measurement	±DD.DDDDDE±DOR
Voltmeter Format 3	DD:DD:DD:DD:DDCR±D.DDDDDE±D,±DDDCR (Time of day / reading / channel)
Time of Day	DD:DD:DD:DD:DDCR
Elapsed Time	DDDDDDDDDDCR (1st 4 digits are 0)
Digital Read or Digital Load	OOOOOOCR (0-177777 Octal)
Digital Interrupt	OOOOOOCR (last thre digits are 0-377 Octal)
Counter Totalize	DDDDDDCR
Counter Period	D.DDDDDDE±DCR (Sec)
System Read	OOOOOOCR (last three digits are 0-377 Octal)

NOTE: D = Decimal Digit
O = Octal Digit
0 = Zeros
E = Exponent

The packed BCD is used only for voltage measurements.

Table 4-1. Specifications (Cont'd)

3497 OPTION 001 DC VOLTMETER - CURRENT SOURCE SPECIFICATIONS

DC Voltage.

Input Characterisitcs:

At 25°C <60% relative humidity.

Input Capacitance:

.1V to 10V ranges	$>10^{10}$ ohms
100V range	10 Mohms ± .5%

Input Capacitance:

HI to LO	<120pf at 1MHz
LO to GUARD	2700pf
GUARD to Chassis	2500pf
Unguarded Chassis	20pf

Isolation, 3497 & Voltmeter:

	25°C, <85%R.H. 40°C, <60%R.H.	40°C, <95%R.H.
HI to LO	$>10^{10}$	$>10^{9}$
LO to GUARD	$>10^{8}$	$>10^{7}$
Guard to Chassis	$>10^{8}$	$>10^{7}$

Resolution:

Range	Maximum Reading (5 Digit)	5 Digit Resolution	4 Digit Resolution	3 Digit Resolution
0.1V	.119999	1μV	10μV	100μV
1.0V	1.19999	10μV	100μV	1mV
10.0V	11.9999	100μV	1mV	10mV
100.0V	119.999	1mV	10mV	100mV

Maximum input voltage between any terminals or from any terminal to the chassis (rack or bench mount):

170 Volts peak

Measurement Accuracy:

(% of reading ± number of counts, Auto-zero on)

24 hours: 23°C ± 1°C

Range	5 Digit Display	4 Digit Display	3 Digit Display
0.1V	0.003 + 3	0.01 + 1	0.1 + 1
1.0V	0.002 + 1	0.01 + 1	0.1 + 1
10.0V	0.002 + 1	0.01 + 1	0.1 + 1
100.0V	0.002 + 1	0.01 + 1	0.1 + 1

90 day: 23°C ± 5°C

Range	5 Digit Display	4 Digit Display	3 Digit Display
0.1V	0.007 + 3	0.01 + 1	0.1 + 1
1.0V	0.006 + 1	0.01 + 1	0.1 + 1
10.0V	0.006 + 1	0.01 + 1	0.1 + 1
100.0V	0.006 + 1	0.01 + 1	0.1 + 1

1 year: 23°C ± 5°C

Range	5 Digit Display	4 Digit Display	3 Digit Display
0.1V	0.015 + 3	0.02 + 1	0.1 + 1
1.0V	0.015 + 1	0.02 + 1	0.1 + 1
10.0V	0.015 + 1	0.02 + 1	0.1 + 1
100.0V	0.015 + 1	0.02 + 1	0.1 + 1

For Auto-zero off, in stable environment (± 1°C) add:

Range	5 Digit Display
0.01V	+10 counts
1.0V	+ 1 count
10.0V	+ 1 count
100.0V	+ 1 count

Reading Rate:

	Auto-zero on	Auto zero off
5 digit display (1)	25 R/S	50 R/S
4 digit display(.1)	100 R/S	200 R/S
3 digit display (.01)	150 R/S	300 R/S

integration periods in power line cycles (PLC) .1 = 16.7ms for 60Hz. 1 = 20.0ms for 50Hz. Maximum reading rate shown is for 60 Hz power line only. For 50Hz reading rate, multiply readings per second by 5/6.

Temperature coefficient:

(% of reading ± no. of counts)/°C to 55°C. 5 digit display.

Range	0.1V	1.0V	10.0V	100.0V
Temp. Coeff.	.00025 + .15	.0002 + .02	.0002 + .01	.00025 + .03

Normal and Effective Common Mode Rejection (1 Kohm, unblanced).

Integration Period	AC (50Hz, 60Hz ± .09%) NMR (dB)	ECMR (dB)	DC ECMR (dB)
<1~	0	90	120
1~	60	150	120

DC CURRENT SOURCE.

24 hour, 23°C ± 1°C

Range	% of error
10μA	.0125%
100μA	.0125%
1.0mA	.0125%

90 day, 23°C ± 5°C

10μA	.025%
100μA	.025%
1.0mA	.025%

1 year, 23°C ± °C

10μA	.032%
100μA	.032%
1.0mA	.032%

Temperature Coefficient:

10μA	.0025%°C
100μA	.0025%°C
1.0mA	.0025%°C

Table 4-2. Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model	Use*
Desktop Computer	HP-IB Capability	-hp- Model HP-85A	MSPT
Serial I/O Interface	Use with HP-85A	-hp- No. 82939A	SPT
I/O Interface Card	Use with HP-85A	-hp- No. 82937A	MPT
I/O ROM	Use with HP-85A	-hp- No. 00085-15003	MSPT
Counter	HP-IB Compatible Resolution: 10nS	-hp- Model 5328A (Opt 041)	MPT
DC Standard	Voltage: .1V to 100V Accuracy: ±.005%	Systron Donner Model 107	VPAT
DC Transfer Standard	Voltage: 1V, 10V, 1.018V, 1.019V Accuracy: ±5ppm Stability: ±.001% (30 Day)	Fluke Model 731B	VPA
Reference Divider	Division Ratio Accuracy: ±.001% Output Voltage Range: .1V to 100V	Fluke Model 750A	VPA
DC Null Voltmeter	Voltage Range: 1μV to 10V	Keithley Model 155	VPA
Resistance Standard	Resistance: 10K ohm Accuracy: ±.001%	Guildline Model 9330/10K or 9330A/10K	VPA
	Resistance: 100K ohm Accuracy: ±.001%	Guildline Model 9330/100K or 9330A/100K	
Digital Voltmeter	Voltage Range: 100μV to 100V	-hp- Model 3456A	MSVAT
Bus System Analyzer	HP-IB Capability	-hp- Model 59401A	MT
Oscilloscope	Bandwidth: DC to 100MHz	-hp- Model 1741A	MSVT
Signature Analyzer	N/A	-hp- Model 5004A	MST

*M = Mainframe (Standard) P = Performance Test
S = Mainframe (Serial I/O) A = Adjustment
V = Voltmeter Option T = Troubleshooting

4-16. Desktop Computer. The recommended computer is a Model HP-85A Desktop Computer with an 82939A Serial I/O Interface Card equipped with the standard female connector and I/O ROM (Part No. 00085-15003). If a different computer is used, refer to the block diagram description of the test procedure (in Figure 4-6) to write the test program.

4-17. Mainframe Adjustments (Battery Charger and Thermocouple)

4-18. A Digital Voltmeter or Digital Multimeter (DVM or DMM) with 4 digit display capabilities is required to do the adjustment. Although any meter with 4 digit capabilities can be used, the -hp- Model 3456A is recommended since it is also used in some troubleshooting procedures.

4-19. Voltmeter Option Performance Test and Adjustment

4-20. The voltmeter option has two different performance tests and adjustment procedures, one is for the voltmeter circuitry (DC Volts Test and Adjustment) and the other is for the current source (Current Source Test and Adjustment). The following lists the required equipment for the tests.

4-21. DC Volts Test and Adjustment. For the DC Volts Test and Adjustment, a DC Transfer Standard is required which is calibrated to a 1.017V, 1.018V, or 1.019V standard cell. The standard cell's accuracy should be calibrated by, and traceable to, the National Bureau of Standards (NBS). The standard should be adjusted shortly before testing the voltmeter option card. It is also recommended to leave the Transfer Standard in a controlled environment where the ambient temperature is within one or two degrees of the temperature in which it was calibrated. The option should also be tested in this environment. Once the Transfer Standard is calibrated, use it in conjunction with the recommended reference divider to test and calibrate the dc voltmeter part of the option. The following lists the test equipment and critical specifications.

a. DC Transfer Standard. The DC Transfer Standard chosen for the DC Volts Test and Adjustment is the Fluke Model 731B DC Reference Standard. The critical requirements are as follows:

1. Required output voltage is 1.018V or 1.019V. A transfer standard with 1.017V capability can also be used.

2. Additional required output voltages are 1V and 10V.

3. Accuracy requirement is at least ±5ppm (±.0005%).

4. Stability is better than ±10ppm (±.001%) for 30 days.

b. DC Standard. The recommended DC Standard is the Systron Donner Model M107 Precision Voltage Source. The critical requirements are as follows:

1. Output from 10mV to 100V.

2. Within ±.005% full scale accuracy.

3. Short term stability better than .0002% per hour.

c. Reference Divider. The recommended reference divider is the Fluke Model 750A Reference Divider. The critical specifications are as follows:

1. Output voltage range from .1V to 100V.

2. Division accuracy better than ±.001%.

4-22. DC Current Test and Adjustment. A 10K ohm and a 100K ohm Standard Resistor is required for the DC Current Test and Adjustment Procedures. The recommended resistors are the Guildline Model 9330/10K or 9330A/10K for the 10K ohm resistor and 9330/100K or 9330A/100K for the 100K ohm resistor. An accuracy of ±.001% or better is required. If the standard resistors are not available, use substitutes that meet the critical requirements. If a substitute is not available, a calibrated decade resistor with 10K ohm and 100K ohm settings may be used. The correction factors on the decade resistor's calibration chart must be algebraically added to the 3497A reading to achieve the required accuracy.

4-23. Voltmeter Test Using the Optional Front Panel. The Voltmeter Performance Tests and Adjustment procedures use the 3497A's standard front panel to setup the option and to read the results. If the optional front panel (Option 260) is installed, use the recommended desktop computer to remotely set-up and read the voltmeter option. The required equipment is the Model HP-85A with I/O ROM (-hp- Part No. 00085-15003) and the 82937A I/O Interface Card (for the HP-IB mainframe) or the 82939A Serial I/O Interface Card (for the Serial I/O option). Refer to paragraph 4-73 on how to remotely set-up the voltmeter option using the computer.

4-24. TEST CARDS

4-25. Performance Test Cards are provided at the end of this section and they may be used to record the 3497A voltmeter option's performance. No test cards are required for the mainframe and front panel tests. It is recommended to fill out the cards and refer to them while doing the test. The test limits and set-up information are printed on the cards for easy reference. Since this information is printed on the cards, the cards can be used as abbreviated test procedures, if you are familiar with the test procedures. The cards can also be used as a permanent record and may be reproduced without written permission from Hewlett-Packard.

4-26. PERFORMANCE TEST CYCLE

4-27. A periodic performance test is recommended for the 3497A voltmeter option card. This should be done as part of an incoming inspection test and at 24 hour, 90 day, or 1 year intervals, dependent on your environmental condition and accuracy requirements. The mainframes and front panel do not require a periodic performance test, but should be tested if a malfunction is suspected.

4-28. TEST FAILURE

4-29. If the 3497A fails any performance verification checks or performance tests, do the necessary adjustments or repairs to make the instrument operational. Make only the adjustments or repairs dependent on what test fails. For example, if only the 10V Range of the voltmeter option fails, calibrate only that range.

4-30. INSTRUMENT SET-UP

4-31. Instrument set-up is specified in each test and adjustment procedure.

4-32. INSTRUMENT WARM-UP

4-33. The 3497A must be warmed up at least 1 hour before doing any of the performance tests and adjustments.

4-34. TEST CONSIDERATION

4-35. Because the 3497A's voltmeter option is able to make highly accurate dc volts measurements, certain requirements have to be met. For example, the DC Standard that is used to test and adjust the 3497A's voltmeter should be good enough so that its errors do not introduce any significant uncertainties in the Performance Tests and Adjustments. A standard which is ten times better than the 3497A's voltmeter option nearly eliminates the uncertainties. Since standards with these accuracies are not readily available, use the recommended DC Volts Standard. Make sure the standard has been calibrated to its 24 hour specifications and will be used within 24 hours after calibration, before testing and calibrating the 3497A voltmeter.

4-36. Ambiguous Region

4-37. Since the available test equipment is not an order of magnitude better than the 3497A, it is important to be aware of the uncertainties or "ambiguities". The uncertainties between the standard and voltmeter create an Ambiguous Region, as shown in Figure 4-1. The region gets bigger when the voltmeter limits are tighter and/or the standard's specifications are less accurate. The best test is when you know your standard's actual limits.

4-38. PERFORMANCE VERIFICATION CHECKS

4-39. The performance verification checks are made to make sure that the mainframes (either HP-IB or Serial I/O) and front panel are operational. The front panel test is included with both mainframe checks, but can be ignored if the standard front panel is deleted. The checks are as follows:

Mainframe Check (HP-IB) - paragraph 4-40
Mainframe Check (Serial I/O) - paragraph 4-51

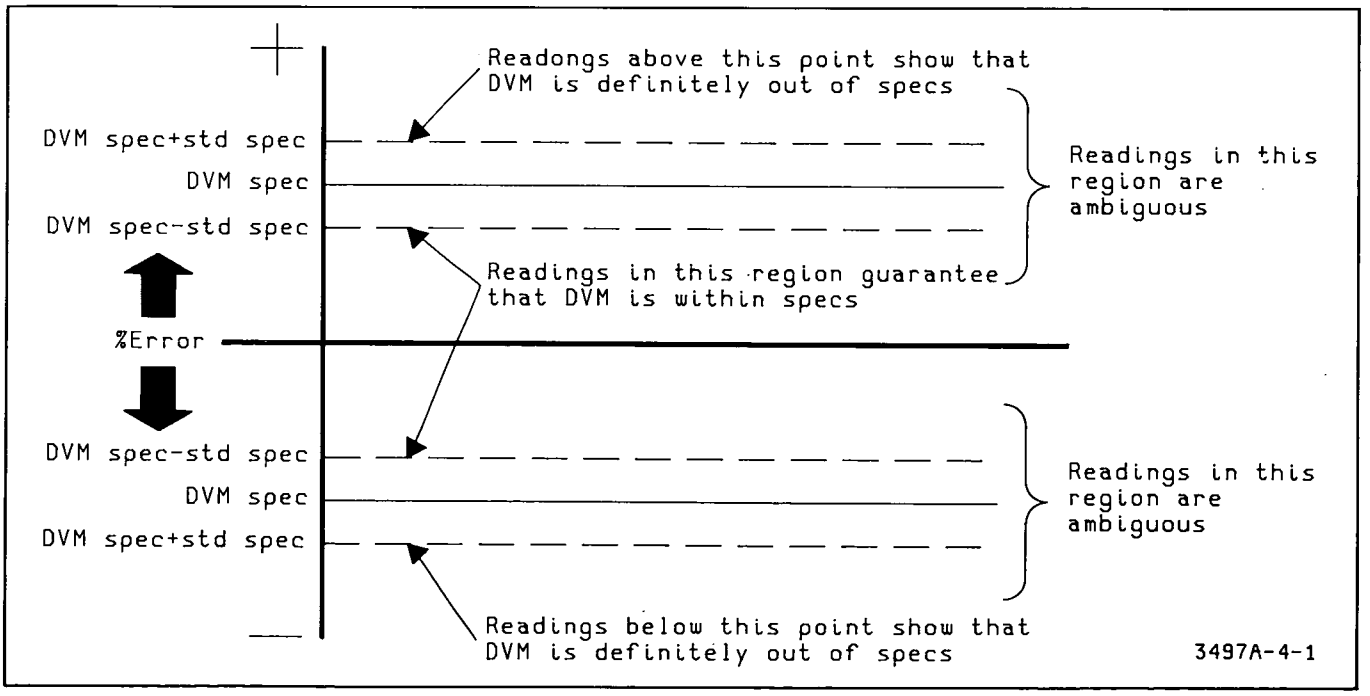


Figure 4-1. Ambiguous Regions

4-40. Mainframe Check (HP-IB)

4-41. Do the mainframe test only for the standard (HP-IB) 3497A. If the Serial I/O option is installed, go to paragraph 4-51 for the test procedure. The mainframe check includes the following:

Self-Test and Front Panel
Battery Backup and Power-On SRQ
SRQ Tests
Timer Tests

The tests are performed remotely using the Model HP-85A Desktop Computer and Model 5328A (Options 11 and 41) Counter. Each test is in a subroutine which can be individually selected, if so desired. A description of each test is in the following paragraphs.

4-42. Self-Test and Front Panel Test. The 3497A Self-Test is used to check some of the instrument's operating circuitry. Once the test is completed, the results are transferred to the computer. When the Self-Test is enabled, all the front panel display indicators are on and part of the front panel operation is then checked.

4-43. The test starts when the computer sends the Self-Test command (program code ST1) to the 3497A. Program execution is then held for one second while the test takes place. The test results are then read by the computer. If the results are 8E8 (formatted to 800000000 by the Model HP-85A), the test passes and the self-test check is completed. If other results are noted, like 1E1 (10), 2E2 (200), or 3E3 (3000), the test program goes to a subroutine to determine what failed. The failure is then printed out on the computer printer and, since the 3497A should be repaired before continuing with the performance verification check, the complete performance check is aborted. Failure codes 1E1, 2E2, and 3E3 show Crossguard, Voltmeter, and Timer errors, respectively.

4-44. Battery Backup and Power-On SRQ Test. The Battery Backup Test is performed to make sure that the 3497A's internal battery keeps the instrument clock operational, when line power is removed. The Power-On SRQ Tests make sure that the Require Service message is output after power is applied to the instrument. Both tests are performed by the same subroutine since power has to be cycled on the 3497A to do the tests.

4-45. In the Battery Backup Test, the instrument clock is set to 23:00 hours by the computer. This is done by sending program code "TD0000230000". The instrument is then turned off and on. The clock is checked by the computer to make sure it is not reset to zero, indicating that the clock was operational with line power off.

4-46. After checking the clock, the computer checks and makes sure the SRQ line is true and that the Power-On SRQ bit (part of the Require Service message) is set. If these conditions are true, the Power-On SRQ test passes.

To do the Battery Backup and Power-On SRQ tests, the Continuous Clock jumper and the Power-On SRQ switch (which is part of the HP-IB Address Switch) have to be in the ON position.

NOTE

Make sure the Continuous Clock Jumper and Power-On SRQ Switch are in the ON position, when doing the Battery Backup and Power-On SRQ tests. The 3497A is shipped from the factory with both jumper and switch in the OFF position (see Section II of this manual).

4-47. SRQ Tests. These tests verify that the Time Alarm SRQ, Time Interval SRQ, and Message Not Executed SRQ operate. If any of these SRQ conditions occur, the computer is interrupted and it goes to a subroutine. In the subroutine, it is determined what bit of the Require Service Message is true. From that information it is then determined if the SRQ test passes. The tests are explained as follows:

a. Message Not Executed SRQ. This test checks whether or not the 3497A can send an interrupt, when it receives an invalid syntax statement (i.e., incorrect program codes or a message that the 3497A cannot execute). The test starts by setting the Message Not Executed bit in the service request register mask true. Next, "WRONG SYNTAX" is sent to the 3497A. The instrument should "beep", set the appropriate SRQ bit, and should interrupt the computer. The computer then goes to a subroutine to determine if the correct bit is true. If the bit is true, the test passes and the next two tests are selected. If the bit is not true or the computer is not interrupted, the test fails.

b. Time Alarm and Time Interval SRQ. These tests make sure that an interrupt occurs when the Time Alarm turns on and after a certain time interval. The program starts by setting the Time Alarm and Time Interval bits in the service request register mask. Next, the 3497A clock is set to zero. At this time, the Time Alarm is also set to turn on 15 seconds after setting the clock and the Time Interval is set to 10 seconds. The computer then goes into a time loop. After 15 seconds are completed, the 3497A should interrupt the computer, indicating that the SRQ line is true. The computer then goes to a subroutine to determine if the time alarm SRQ bit is true. If the correct bit is true, the computer then goes back to the time loop. If the bit is not true, the test fails and the computer continues with the next test. If the computer does not get interrupted, the test also fails and the time loop continues. After the computer is interrupted by the Time Alarm interrupt, the computer is interrupted again about 10 seconds after the Time Alarm interrupt. The same takes place for Time Interval as was done for Time Alarm (i.e., if the correct SRQ bits are not set or the computer does not get interrupted, the test fails).

4-48. Timer Tests. Two tests are performed for the Timer Tests: Time Interval and Timer Output. The tests are as follows:

a. Time Interval. This test checks to see if the pulses output at the 3497A's rear panel meet the specified limits, when the Time Interval Mode is selected. By sending program code "TI1", the Time Interval mode is selected and the resultant output pulses will have a time interval of 1 second. A counter is used to measure the time. It then transfers the time information to the computer which makes sure the specified limits are met. If they are not, the test fails and the 3497A requires service (go to Section VIII of this manual).

b. Timer Output. This test is similar to the Time Interval Test. The only difference is that the output pulses have a time interval of 100μS, instead of 1S. This mode is selected by sending program code "TO1".

4-49. Equipment. The required equipment for the test is as follows:

Desktop Computer (-hp- Model HP-85A)
I/O Interface Card (-hp- 82937A)
I/O ROM (-hp- Part No. 00085-15003)
2 ea. HP-IB Cables (-hp- 10631A)
HP-IB Compatible Counter (-hp- Model 5328A, Options 011 and 041).

4-50. Test Procedure. The mainframe is tested automatically using the program in Figure 4-2. It is required to leave the 3497A address to the factory preset setting when running the test. If a different computer or counter is used, refer to the test block diagram description in Figure 4-4 to write your own program. The test program is written in such a way that individual tests can be selected, if so desired, instead of the complete test. Do the following:

a. Make sure that all test equipment and the 3497A are turned off.

b. With the Desktop Computer turned off, install the I/O ROM and I/O Interface Card into the computer.

c. Refer to Figure 4-3. Connect one HP-IB cable from the computer to the counter and connect another cable from the counter to the 3497A.

d. Using a coax cable with BNC connectors, connect the 3497A TIMER output port (on the rear panel) to Input A of the counter.

e. Turn all of the equipment on and make sure the counter is set to HP-IB address "10" and the 3497A to address "09" (factory address setting).

f. Make sure the equipment has been operating long enough to meet specifications. The 3497A requires at least a one hour warm-up time.

g. Load the Performance Test Program into the computer.

h. Press RUN on the computer and the test will start. Make sure the requests displayed by the computer are performed.

4-51. Mainframe Check (Serial I/O)

4-52. Do this test only if the 3497A Serial I/O option (Option 232) is installed. If the option is not installed, go to the mainframe test procedure, in paragraph 4-40, for the standard 3497A. The Serial I/O mainframe test is as follows:

Self-Test and Front Panel
Battery Backup
Power-On SRQ
Message Not Executed SRQ
Time Interrupt

The tests are performed remotely using the Model HP-85A Desktop Computer. A description of the tests is in the following paragraphs.

4-53. Self-Test and Front Panel Test. The 3497A Self-Test is used to check some of the instrument's operating circuitry. Once the test is completed, the results are transferred to the computer. When the Self-Test is enabled, all the front panel indicators are on and part of the front panel is then checked.

4-54. The test starts when the computer sends the Self-Test command (program code ST1) to the 3497A. Program execution is then held for one second while the test takes place. The test results are then read by the computer. If the results are 8E8 (formatted 800000000 by the Model HP-85A), the test passes and the self-test check is completed. If other results are noted, like 1E1 (10), 2E2 (200), or 3E3 (3000), the test program goes to a subroutine to determine what failed. The failure is then printed out on the computer printer. Failure codes 1E1, 2E2, and 3E3 indicate Crossguard, Voltmeter, and Timer errors, respectively.

4-55. Battery Backup Test. The Battery Backup test is used to verify whether the 3497A's internal battery keeps the instrument clock operational, when power is removed. The instrument clock is set to 23:00 hours by the computer which is done by sending program code "TD0000230000". The instrument is then turned off and on. The clock is checked by the computer to make sure it is not reset to zero, indicating that the clock was operational with power off.

```
 10 ! 3497A PERFORMANCE TEST
 20 ! STANDARD MAINFAME
 30 DIM A$[20],B$[20]
 40 CLEAR
 50 RESET 7
 60 ! COUNTER IS ADDRESS 10
 70 ! 3497A IS ADDRESS 09
 80 BEEP
 90 DISP "Enter Date";
100 INPUT A$
110 CLEAR
120 DISP "Enter 3497A Serial Num
    ber";
130 INPUT B$
140 CLEAR
150 PRINT "*****3497A PERFORMANC
    E TEST*****"
160 PRINT
170 PRINT
180 PRINT "Date:      ",A$
190 PRINT "Serial No:",B$
200 BEEP
210 DISP "Each Performance Test
    has a      corresponding numb
    er   To run"
220 DISP "a test or all the test
    s,  enter the appropriate te
    st number "
230 DISP "The tests and numbers
    are as     follows:"
240 DISP
250 DISP " (Press CONTINUE on th
    e 85A):"
260 PAUSE
270 CLEAR
280 DISP "  TESTS                N
    UMBER"
290 DISP
300 DISP "  All
     1"
310 DISP "  Self-Test
     2"
320 DISP "  Batt & Po-On SRQ
     3"
330 DISP "  SRQ
     4"
340 DISP "  Timer
     5"
350 DISP
360 DISP "What test is to be per
    formed";
370 INPUT I
380 IF I=1 THEN GOTO 490
390 IF I=2 THEN GOSUB 560
400 IF I=3 THEN GOSUB 980
410 IF I=4 THEN GOSUB 1440
420 IF I=5 THEN GOSUB 2020
430 CLEAR 709
440 PRINT
450 PRINT
460 DISP "END OF PERFORMANCE TES
    T"
470 PRINT "****END OF PERFORMANC
    E TEST*****"
480 END
490 GOSUB 560
500 GOSUB 980
510 GOSUB 1440
520 GOSUB 2020
530 GOTO 430
540 !
550 !
560 ! "SELF-TEST AND FRONT PANEL
     TEST ROUTINE"
570 PRINT
580 PRINT
590 PRINT "--------3497A SELF-TE
    ST---------"
600 CLEAR
610 PRINT
620 CLEAR 709 ! RESET 3497A TO I
    TS TURN-ON STATE
630 WAIT 1000
640 OUTPUT 709 ;"ST1" ! ENABLE 3
    497A SELF-TEST
650 WAIT 1000
660 ENTER 709 ; A
670 IF A#800000000 THEN GOTO 870
     ! IF TEST FAILS, GOTO SUBRO
    UTINE TO DETERMINE FAILURE
680 PRINT "Self-Test
       *PASSED*"
690 PRINT
700 BEEP
710 DISP "Is the STANDARD FRONT
    PANEL"
720 DISP "installed (Enter YES o
    r NO)";
730 INPUT A$
740 IF A$="NO" OR A$="no" THEN G
    OTO 830
750 BEEP
760 CLEAR
770 DISP "Are all display indica
    tors ON"
780 DISP "(Enter YES or NO)";
790 INPUT A$
800 IF A$="YES" OR A$="yes" THEN
     PRINT "Front Panel Test
       *PASSED*"
810 IF A$="NO" OR A$="no" THEN P
    RINT "Front Panel Test
      *FAILED*"
820 PRINT
830 CLEAR
840 OUTPUT 709 ;"ST0"
850 PRINT "--------END OF SELF-T
    EST---------"
860 RETURN
870 PRINT "Self-Test
       *FAILED*" ! SELF-TEST FAI
    LURE ROUTINE
880 BEEP
890 PRINT
900 IF A=10 THEN PRINT "Crossboa
    rd Failure"
910 IF A=200 THEN PRINT "Voltmet
    er Failure"
920 IF A=3000 THEN PRINT "Timer
    Failure"
930 PRINT
940 PRINT "Repair 3497A before c
    ontinuing  with the Performa
    nce Test"
950 GOTO 430 ! END PERFORMANCE T
    EST
960 !
970 !
980 ! "BATT  BACKUP & PO-ON SRQ"
990 CLEAR
1000 BEEP
1010 DISP "Before doing the foll
     owing       tests, make sure
      the Continuous"
1020 DISP "Clock Select Jumper a
     nd Power-OnSRQ switch are i
     n the ON"
1030 DISP "position "
1040 DISP
1050 PRINT
1060 DISP "Then Press CONTINUE o
     n the 85A"
1070 PAUSE
1080 CLEAR
1090 PRINT
1100 PRINT "------BATTERY BACKUP
      TEST-------"
1110 PRINT
1120 CLEAR 709 ! RESET 3497A TO
     ITS TURN-ON STATE
1130 WAIT 1000
1140 OUTPUT 709 ;"SI","TD0000230
     000" ! INITIALIZE 3497A AND
      SET TO 23:00 HOURS
1150 BEEP
1160 DISP "Turn 3497A OFF and th
     en ON;"
1170 DISP "then Press CONTINUE o
     n the 85A"
1180 PAUSE
1190 CLEAR
1200 WAIT 2000
1210 OUTPUT 709 ;"TD" ! READ 349
     7A CLOCK
1220 ENTER 709 ; A$
1230 A=VAL(A$[7])
1240 IF A>0 THEN GOTO 1270 ! DET
     ERMINE IF CLOCK RESET TO ZE
     RO OR NOT
1250 PRINT "Battery Backup Test
       *FAILED*"
1260 GOTO 1280
1270 PRINT "Battery Backup Test
       *PASSED*"
1280 PRINT
1290 PRINT "---END OF BATTERY BA
     CKUP TEST---"
1300 ! POWER-ON SRQ TEST
1310 PRINT
1320 PRINT
1330 PRINT "-------POWER-ON SRQ
     TEST---------"
1340 PRINT
1350 P=SPOLL(709) ! READ 3497A S
     TATUS REGISTER
1360 IF BIT(P,5) THEN PRINT "Pow
     er-On SRQ Test        *PASSE
     D*" @ GOTO 1380
1370 PRINT "Power-On SRQ Test
       *FAILED*"
1380 PRINT
1390 CLEAR
1400 PRINT "----END OF POWER-ON
     SRQ TEST----"
1410 RETURN
1420 !
1430 !
1440 ! "SRQ TESTS SUBROUTINES"
1450 B,L,N,Z=0
1460 CLEAR
1470 PRINT
1480 PRINT
1490 PRINT "-----------SRQ TESTS
     ------------"
1500 PRINT
1510 CLEAR 709 ! RESET 3497A TO
     ITS TURN-ON STATE
1520 WAIT 1000
1530 ON INTR 7 GOSUB 1830 ! WHEN
      INTERRUPTED GO TO SRQ SUBP
     OUTINE
1540 ENABLE INTR 7;8
1550 ! MESSAGE NOT EXECUTED SRQ
1560 OUTPUT 709 ;"SE020" ! SET 3
     497A SRQ MASK TO 20
1570 OUTPUT 709 ;"WRONG SYNTAX"
     ! OUTPUT INCORRECT PROGRAM
     CODES TO 3497A
1580 WAIT 1000
1590 IF L=1 THEN GOTO 1610
1600 IF L=0 THEN PRINT "Message
     Not Executed     *FAILED*"
1610 ! TIME ALARM AND TIME INTER
     VAL SRQ TESTS
1620 PRINT
1630 L=0
1640 OUTPUT 709 ;"SE014" ! SET S
     RQ MASK TO 14
1650 OUTPUT 709 ;"TD000000000TA
     000010TI000015" ! SET 3497A
      CLOCK,ALARM,INTERVAL
1660 N=0 ! TIME GENERATION LOOP
1670 N=N+1
1680 WAIT 1000
1690 CLEAR
1700 DISP "PROGRAM OPERATING"
1710 IF N#15 THEN GOTO 1670
1720 IF Z=1 THEN GOTO 1760
1730 IF L=1 THEN GOTO 1780
1740 IF L=0 THEN PRINT "Time Ala
     rm SRQ           *FAILED*"
1750 PRINT
1760 IF B=1 THEN GOTO 1780
1770 IF B=0 THEN PRINT "Time Int
     erval SRQ        *FAILED*"
1780 CLEAR
1790 PRINT
1800 PRINT "--------END OF SRQ T
     ESTS---------"
1810 RETURN
1820 !
1830 P=SPOLL(709) ! ROUTINE TO D
     ETERMINE SRQ BIT
1840 IF BIT(P,4) THEN GOTO 1880
     ! DETERMINE IF THE MESSAGE
     NOT EXECUTED BIT IS TRUE
1850 IF BIT(P,2) THEN GOTO 1910
     ! DETERMINE IF THE TIME ALA
     RM BIT IS TRUE
1860 IF BIT(P,3) THEN GOTO 1950
     ! DETERMINE IF THE TIME INT
     ERVAL BIT IS TRUE
1870 GOTO 1970
1880 PRINT "Message Not Executed
       *PASSED*"
1890 L=1
1900 GOTO 1970
1910 PRINT "Time Alarm SRQ
       *PASSED*"
1920 L,Z=1
1930 PRINT
1940 GOTO 1970
1950 PRINT "Time Interval SRQ
       *PASSED*"
1960 B=1
1970 STATUS 7,1 ; C
1980 ENABLE INTR 7;8
1990 RETURN
```

Figure 4-2. Mainframe (HP-IB) Test Program

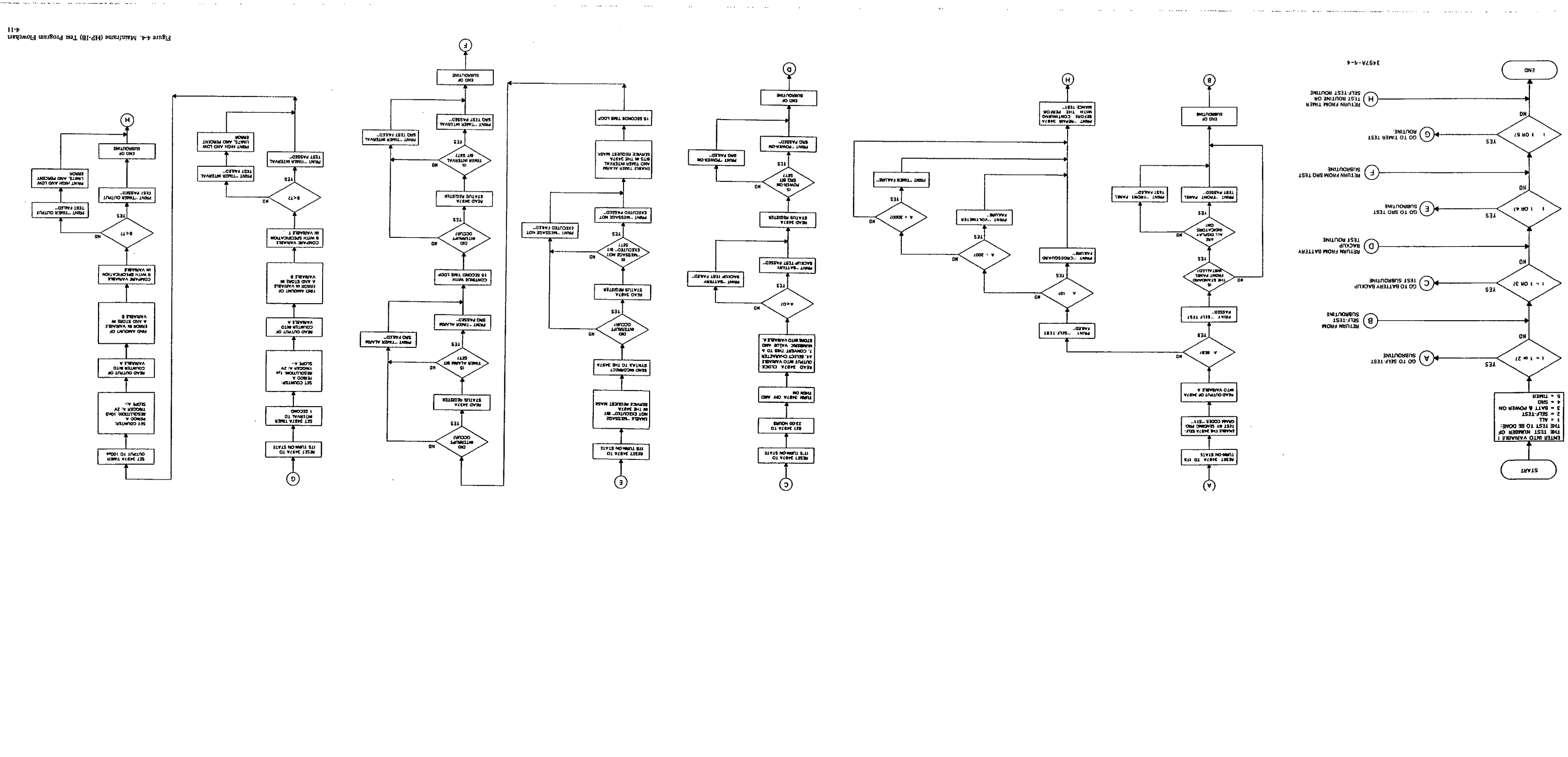


Figure 4-4. Mainframe (HP-IB) Test Program Flowchart

```
2000 !
2010 !
2020 ! "TIMER TEST ROUTINES"
2030 CLEAR
2040 CLEAR 709 ! SET 3497A TO IT
     S TURN-ON STATE
2050 PRINT
2060 PRINT
2070 T=.10005
2080 V=.0002
2090 IMAGE "Max",21X,D.DDDDD
2100 IMAGE "Error",19X,D.DDDDD
2110 IMAGE "Min",21X,D.DDDDD
2120 ! TIMER INTERVAL TEST
2130 PRINT "------TIMER INTERVAL
     TEST-------"
2140 PRINT
2150 CLEAR 710 ! SET 5328A TO IT
     S TURN-ON STATE
2160 REMOTE 710 ! PLACE THE 5328
     A INTO REMOTE
2170 OUTPUT 709 ;"TI1" ! SET 349
     7A TIMER TO 1 SECOND INTERV
     AL
2180 WAIT 1000
2190 OUTPUT 710 ;"PF6G2A3A4A9A+2
     00*"
2200 WAIT 2000
2210 TRIGGER 710
2220 WAIT 2000
2230 ENTER 710 ; A
2240 B=ABS(A-1)
2250 IF B<T THEN GOTO 2330
2260 PRINT "Timer Interval Test
        *FAILED*"
2270 PRINT
2280 PRINT USING 2090 ; T+1
2290 PRINT USING 2100 ; A
2300 PRINT USING 2110 ; 1-T
2310 PRINT
2320 GOTO 2350
2330 PRINT "Timer Interval Test
        *PASSED*"
2340 PRINT
2350 PRINT "---END OF TIMER INTE
     RVAL TEST---"
2360 ! TIMER OUTPUT TEST
2370 PRINT
2380 PRINT
2390 PRINT "-------TIMER OUTPUT
     TEST--------"
2400 PRINT
2410 OUTPUT 709 ;"TO1" ! SET 349
     7A TIMER OUTPUT TO .1 mS
2420 WAIT 1000
2430 OUTPUT 710 ;"PF7G1A37+50*"
2440 TRIGGER 710
2450 ENTER 710 ; A
2460 A=A*10000
2470 B=ABS(A-1)
2480 IF B<V THEN GOTO 2540
2490 PRINT "Timer Output Test
        *FAILED*"
2500 PRINT
2510 PRINT USING 2090 ; V+1
2520 PRINT USING 2100 ; A
2530 PRINT USING 2110 ; 1-V
2540 PRINT "Timer Output Test
        *PASSED*"
2550 PRINT
2560 PRINT "----END OF TIMER OUT
     PUT TEST----"
2570 RETURN
```

Figure 4-2. Mainframe (HP-IB) Test Program (Cont'd)

4-56. Power-On SRQ. This test checks to see if a Power-On SRQ was generated when the power was turned off and on (see the previous test). To do this, the 3497A status register is read to see if the Power-on SRQ bit is set true. If the bit is true, the test passes and if not true, the test fails. It is therefore important to do the Battery Backup Test first and make sure that power is cycled on the 3497A.

NOTE

Make sure the Continuous Clock jumper and Power-On SRQ Switch are in the ON position, when doing the Battery Backup and Power-On SRQ tests. The 3497A is shipped from the factory with both jumper and switch in the OFF position (see Section II of this manual).

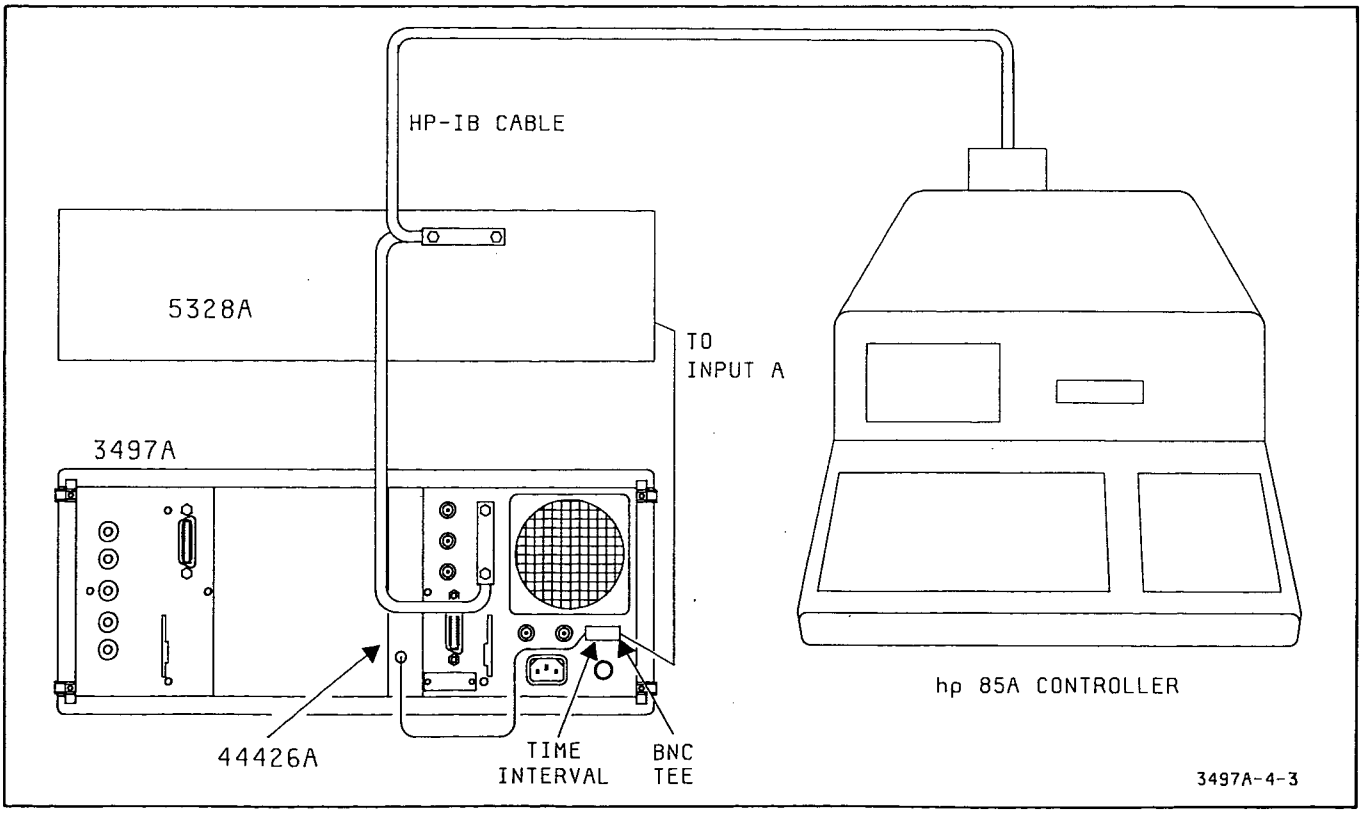


Figure 4-3. Mainframe (HP-IB) Test Connection

4-57. Message Not Executed SRQ. This checks to make sure the 3497A sends an interrupt when it receives an invalid syntax statement (i.e., an incorrect program code or a message that the 3497A cannot execute). The test starts by setting the Message Not Executed bit in the Interrupt Mask true. Next, "WRONG SYNTAX" is sent to the 3497A. The instrument should beep, set the appropriate SRQ bit, and interrupt the computer. The computer then goes to a subroutine to determine if the correct bit is true. If the bit is true, the test passes and if the bit is not true or the computer is not interrupted, the test fails.

4-58. Time Interrupt Test. This test makes sure that an interrupt occurs after a certain time interval. The program starts by setting the Time Interrupt bit in the Interrupt Mask true. Next, a time interval of 2 seconds is specified and the program is halted for 4 seconds. As soon as 2 seconds are completed, the 3497A interrupts the computer. The computer then goes to a subroutine to determine if the correct SRQ bit is set true. If it is true, the test passes and if not true, the test fails. The test also fails if the computer does not get interrupted. After the test, the time interrupt function is disabled.

4-59. Equipment. The required equipment for the performance verification checks is as follows:

Desktop Computer (-hp- Model 85A)
Serial I/O Interface Card (-hp- 82939A)
I/O ROM (-hp- Part No. 00085-15003)

4-60. Test Procedure. The mainframe is tested automatically using the program in Figure 4-5. It is required to leave the Serial Interface Settings and the 3497A in their factory preset positions. If a different computer is to be used, refer to the test block diagram description in Figure 4-6 to write your own program.

a. Make sure that all test equipment and the 3497A are turned off.

b. With the Desktop Computer turned off, install the I/O ROM and Serial I/O Interface Card into the computer.

c. Connect the 3497A to the computer.

d. Turn all the equipment on and make sure the equipment has been operating long enough to meet specifications. The 3497A requires at least a one hour warm-up time.

e. Press RUN on the computer and the test will start.

4-61. PERFORMANCE TEST

4-62. General

4-63. The performance test checks the performance of the voltmeter option. The option requires two separate tests, one is for the dc voltmeter and the other is for the dc current source.

4-64. Because of the accuracy requirements of the voltmeter option (see paragraph 4-34), manual performance tests are performed. This includes configuring the option to the appropriate function and range (e.g., select the 10V Range) using the standard front panel. In addition, the front panel is also used to display the readings taken by the option. If the optional front panel is installed, a computer (like the Model HP-85A) has to be used to configure and read the voltmeter option. Information on how to remotely configure the 3497A is in paragraph 4-73. The performance tests are as follows:

DC Voltmeter Test - paragraph 4-65
DC Current Source Test - paragraph 4-69
Remote Set-up of Voltmeter Option - paragraph 4-73

4-65. DC Voltmeter Test

4-66. The DC Voltmeter Test checks the specified accuracy of the DC Voltmeter (which is part of the voltmeter option, Option 001). This includes the accuracy of all ranges (.1V through 100V). The test limits are printed in Table 4-3 and also on the DC Voltmeter Test Card. Each step on the test card also corresponds to a certain step in the procedure. The corresponding step in the procedure is shown in parenthesis. All test signals are applied to the HI COM and LO COM Input terminals on the Inguard Rear Panel, as shown in Figure 4-7.

4-67. Equipment Required. The following is the required test equipment for the test procedure.

Reference Divider (Fluke Model 750A)
DC Transfer Standard (Fluke Model 731B)
DC Standard (Systron Donner Model M107)
DC Null Voltmeter (Keithley Model 155)

4-68. Test Procedure. Do the following:

a. (Step #1). Reset the 3497A to its turn-on state by pressing the RESET button on the front panel (or, if in remote, clear the instrument by sending CLEAR 709). This sets the 3497A to 5½ Digit Display, Autozero On, and Autorange On.

b. (Step #2). Short the rear HI COM and LO COM Input Terminals. The voltmeter should now be in the .1V Range.

c. Record the reading on the test card and make sure it is within the specified limits shown on the test card and in Table 4-3.

d. (Step #3, 4, and 5). Set the voltmeter to the 1V, 10V, and 100V Ranges (program codes VR2, VR3, and VR4 for the 1V, 10V, and 100V Ranges, respectively). Check and record the readings.

```
 10 ! 3497A PERFORMANCE TEST
 20 ! SERIAL I/O
 30 RESET 10
 40 IMAGE K
 50 DIM A$[15]
 60 CLEAR
 70 PRINT "*****3497A PERFORMANC
    E TEST*****"
 80 PRINT
 90 PRINT
100 PRINT "--------3497A SELF-TE
    ST---------"
110 PRINT
120 OUTPUT 10 USING 40 ; "ST1"
130 WAIT 1000
140 ENTER 10 USING "#,K" ; G
150 IF G=800000000 THEN PRINT "S
    elf-Test                *PASS
    ED*" @ GOTO 220
160 IF G=10 THEN PRINT "Crossgua
    rd Error"
170 IF G=200 THEN PRINT "Voltmet
    er Failure"
180 IF G=3000 THEN PRINT "Timer
    Failure"
190 PRINT
200 PRINT "Repair 3497A before c
    ontinuing  with the Performa
    nce Test"
210 GOTO 1410
220 PRINT
230 BEEP
240 DISP "Is the STANDARD FRONT
    PANEL"
250 DISP "installed (Enter YES o
    r NO)";
260 INPUT A$
270 IF A$="NO" OR A$="no" THEN G
    OTO 370
280 BEEP
290 CLEAR
300 DISP "Are all display indica
    ors ON"
310 DISP "(Enter YES or NO)";
320 INPUT A$
330 IF A$="YES" OR A$="yes" THEN
     PRINT "Front Panel Test
        *PASSED*"
340 IF A$="NO" OR A$="no" THEN P
    RINT "Front Panel Test
      *FAILED*"
350 CLEAR
360 OUTPUT 10 USING 40 ; "ST0"
370 PRINT
380 PRINT "--------END OF SELF-T
    EST---------"
390 PRINT
400 PRINT
410 !
420 !
430 !
440 PRINT "------BATTERY BACKUP
    TEST-------"
450 PRINT
460 OUTPUT 10 USING 40 ; "TD0000
    230000"
470 DISP "Turn the 3497A Power S
    witch OFF and back ON. Then
    press the      HP-85 CONT key
     "
480 DISP
490 DISP "              *NOTE*"
500 DISP
510 DISP "The Power-On SRQ Test
    will FAIL unless this step i
    s performed."
520 BEEP
530 PAUSE
540 CLEAR
550 WAIT 2000
560 OUTPUT 10 USING 40 ; "TD"
570 ENTER 10 USING "#,K" ; A$
580 A=VAL(A$[7])
590 IF A>0 THEN PRINT "Battery T
    est                *PASSED*" @ G
    OTO 650
600 PRINT "Battery Test
      *FAILED*"
610 PRINT
620 PRINT "Make sure the Continu
    ous Clock  Select Jumper is
    in the ON      position."
630 PRINT
640 PRINT "The instrument is shi
    pped with  this jumper in th
    e off position."
650 PRINT
660 PRINT "---END OF BATTERY BAC
    KUP TEST---"
670 PRINT
680 PRINT
690 !
700 !
710 !
720 PRINT "-------POWER-ON SRQ T
    EST---------"
730 PRINT
740 B=0
750 OUTPUT 10 USING 40 ; "SR"
760 ENTER 10 USING "#,K" ; B
770 IF B<>140 THEN PRINT "Power-
    On SRQ              *FAILED*"
    @ GOTO 790
780 PRINT "Power-On SRQ
      *PASSED*"
790 PRINT
800 PRINT "----END OF POWER-ON S
    RQ TEST----"
810 PRINT
820 PRINT
830 !
840 !
850 !
860 PRINT "-MESSAGE NOT EXECUTED
     SRQ TEST--"
870 PRINT
880 RESET 10
890 L=0
900 CONTROL 10,1 ; 128
910 ON INTR 10 GOSUB 1020
920 OUTPUT 10 USING 40 ; "SE120"
930 OUTPUT 10 USING 40 ; "WRONG
    SYNTAX" ! SEND INCORRECT PRO
    GRAM CODES
940 WAIT 1000
950 IF L=0 THEN PRINT "Message N
    ot Executed    *FAILED*"
960 PRINT
970 PRINT "------END OF MESSAGE
    TEST-------"
980 OUTPUT 10 ;"SE0"
990 PRINT
1000 PRINT
1010 GOTO 1140
1020 ! INTERRUPT SERVICE ROUTINE
1030 WAIT 2000
1040 OUTPUT 10 USING 40 ; "SR"
1050 ENTER 10 USING "#,K" ; C
1060 IF C<>120 THEN PRINT "Messa
     ge Not Executed    *FAILED*
     " @ GOTO 1080
1070 PRINT "Message Not Executed
       *PASSED*"
1080 L=1
1090 RETURN
1100 !
1110 !
1120 !
1130 !
1140 PRINT "------TIME INTERRUPT
      TEST-------"
1150 PRINT
1160 RESET 10
1170 L=0
1180 CONTROL 10,1 ; 128
1190 ON INTR 10 GOSUB 1300
1200 OUTPUT 10 USING 40 ; "SE110
     "
1210 OUTPUT 10 USING 40 ; "TI2"
1220 WAIT 4000
1230 IF L=0 THEN PRINT "Time Int
     errupt          *FAILED*"
1240 PRINT
1250 PRINT "---END OF TIME INTER
     RUPT TEST---"
1260 PRINT
1270 PRINT
1280 OUTPUT 10 USING 40 ; "TI0"
1290 GOTO 1410
1300 ! INTERRUPT SERVICE ROUTINE
1310 OUTPUT 10 USING 40 ; "SRSC"
1320 ENTER 10 USING "#,K" ; D
1330 IF D<>110 THEN PRINT "Time
     Interrupt          *FAILED*
     " @ GOTO 1350
1340 PRINT "Time Interrupt
       *PASSED*"
1350 L=1
1360 RETURN
1370 !
1380 !
1390 !
1400 !
1410 PRINT
1420 PRINT "***END OF PERFORMAN
     CE TEST*****"
1430 PRINT
1440 PRINT "  REFER TO ABOVE PRI
     NTOUT FOR      RESULTS"
1450 PRINT
1460 PRINT
1470 PRINT
1480 PRINT
1490 END
```

Figure 4-5. Mainframe (Serial I/O) Test Program

e. (Step #6). Remove the short from the Input Terminals and set the option to the 10V Range. Connect the DC Transfer Standard's "+" terminal to the 3497A's HI COM terminal and "-" terminal to the LO COM terminal.

f. Set the DC Transfer Standard to the 10V Range. Check the reading on the 3497A and record it on the test card.

g. (Step #7). Set the voltmeter option to the 4½ Digit Display mode (program code VD4). Check and record the reading.

h. (Step #8). Set the option to the 3½ Digit Display mode (program code VD3). Check and record the reading.

i. (Step #9). Return the option to the 5½ Digit Display mode and then turn Autozero off (program codes VD5 and VA0). Check and record the reading.

j. (Step #10). Turn Autozero on and set the option to Autorange (program codes VA1 and VR5). Then set the DC Transfer Standard to the 1V Range. Check and record the 3497A's 1V reading.

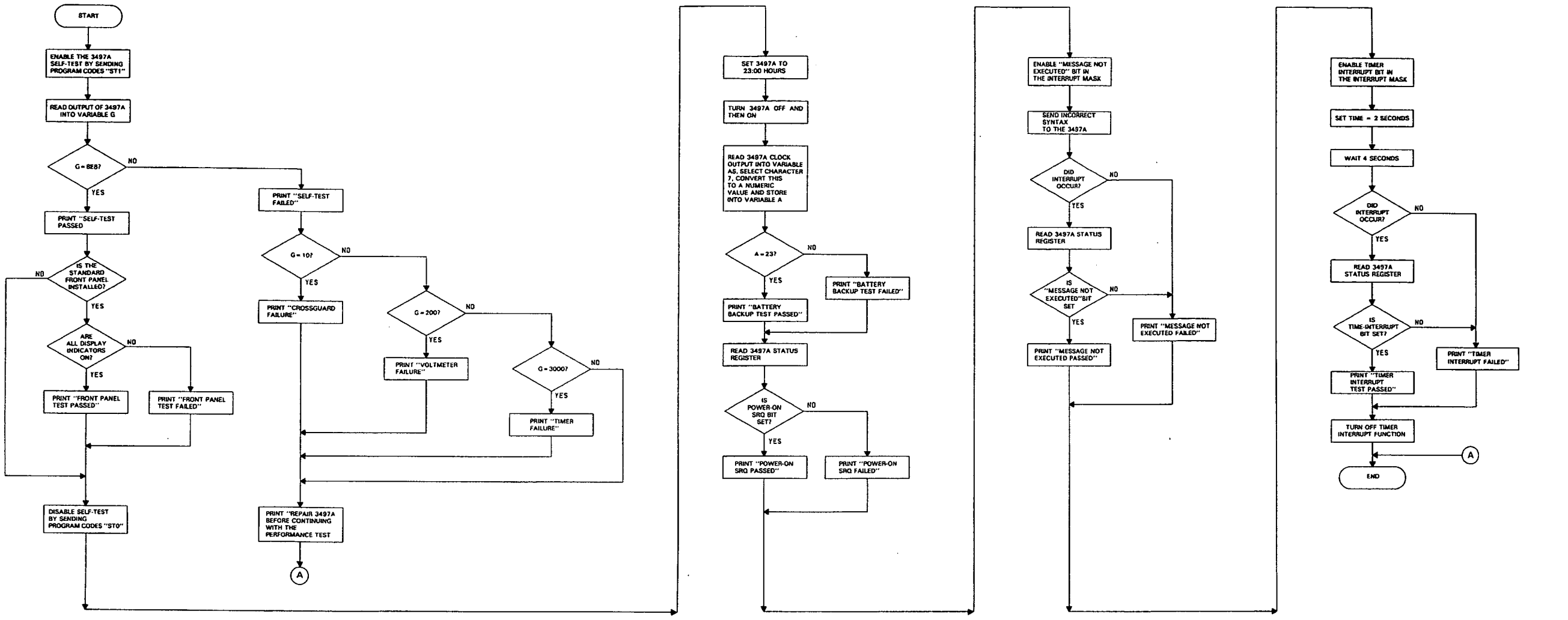


Figure 4-6. Mainframe (Serial I/O) Test Program Flowchart

Table 4-3. DC Voltmeter Test Limits

Step#	Input	Range	Set-Up/ Configuration	24 Hour Limits high	24 Hour Limits low	90 Day Limits high	90 Day Limits low	1 Year Limits high	1 Year Limits low
1	Open	-	Press RESET						
2	Short	Auto	AZ On	+.000003V	-.000003V	+.000003V	-.000003V	+.000003V	-.000003V
3	Short	1V	AZ On	+0.00001V	-0.00001V	+0.00001V	-0.00001V	+0.00001V	-0.00001V
4	Short	10V	AZ On	+00.0001V	-00.0001V	+00.0001V	-00.0001V	+00.0001V	-00.0001V
5	Short	100V	AZ On	+000.001V	-000.001V	+000.001V	-000.001V	+000.001V	-000.001V
6	+10V	10V	AZ On	+10.0003V	+09.9997V	+10.0007V	+09.9993V	+10.0016V	+09.9984V
7	+10V	10V	4 Dig.	+10.002V	+09.998V	+10.002V	+09.998V	+10.003V	+09.997V
8	+10V	10V	3 Dig.	+10.02V	+09.98V	+10.02V	+09.98V	+10.02V	+09.98V
9	+10V	10V	5 Dig. AZ Off	+10.0004V	+09.9996V	+10.0008V	+09.9992V	+10.0017V	+09.9983V
10	+1V	1V	AZ On	+1.00003V	+0.99997V	+1.00007V	+0.99993V	+1.00016V	+0.99984V
11	+.1V	.1V	AZ On	+.100006V	+.099994V	+.100010V	+.099990V	+.100018V	+.099982V
12	+100V	100V	AZ On	+100.003V	+099.997V	+100.007V	+099.993V	+100.016V	+099.984V
13	+1V	10V	AZ On	+01.0001V	+00.9999V	+01.0002V	+00.9998V	+01.0003V	+00.9997V
14	-1V	10V	AZ On	-01.0001V	-00.9999V	-01.0002V	-00.9998V	-01.0003V	-00.9997V
15	-5V	10V	AZ On	-05.0002V	-04.9998V	-05.0004V	-04.9996V	-05.0009V	-04.9991V
16	-10V	10V	AZ On	-10.0003V	-09.9997V	-10.0007V	-09.9993V	-10.0016V	-09.9984V

k. Disconnect the DC Transfer Standard from the instrument.

l. (Step #11). Refer to Figure 4-7. Using short pieces of 20 AWG insulated solid copper wire, connect the DC Transfer Standard and Null Voltmeter to the Reference Divider, as shown in the figure. Turn the output of the DC Volts Standard off. Using 24 inch or shorter shielded cables, connect the DC Standard and 3497A to the Reference Divider, as shown in the figure.

m. Set the Standard Cell Voltage control on the Reference Divider to correspond with the output voltage setting of the DC Transfer Standard. Normally, the Transfer Standard's output should be set to the voltage value of the standard cell used to calibrate the Transfer Standard.

n. Zero the DC Null Voltmeter on the 3 microvolt range and set it to the 300 microvolt range.

o. Set the Reference Divider's Input Voltage Switch to 10V and center its Coarse and Fine adjust controls.

p. Set the Reference Divider's Output Voltage Switch to .1V.

q. Set the DC Standard for an output of +10V and then turn its output on.

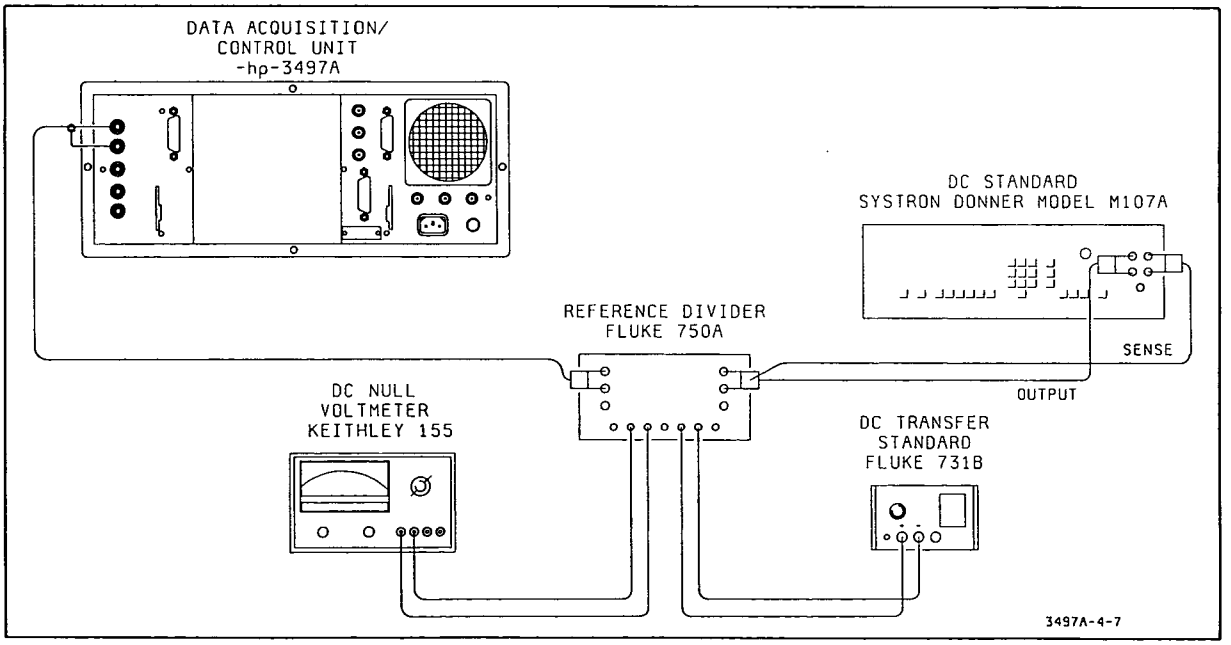


Figure 4-7. DC Voltmeter Test Connection

r. Set the Reference Divider's Standard Cell Switch to the LOCKED position. Adjust the DC Standard's output for a zero reading on the DC Null Voltmeter.

s. Downrange the DC Null Voltmeter and adjust the Reference Divider's Coarse and Fine adjust controls for a zero reading on the Null Voltmeter's 3 microvolt range.

t. Set the Reference Divider's Standard Cell Switch to OPEN. Then set the switch to MOMENTARY and, if necessary, readjust the Fine control for a zero reading on the Null Voltmeter.

u. Check and record the the 3497A's +.1V reading.

NOTE

The Reference Divider's Fine control may have to be readjusted, when the output switch is set to another position.

v. (Step #12). Uprange the Reference Divider's Input Voltage Switch to 100V and then uprange the DC Standard's output to +100V.

CAUTION

Always uprange the Reference Divider Input Voltage Switch before upranging the DC Standard and downrange the DC Standard before downranging the Reference Divider.

w. Uprange the Reference Divider's Output Voltage Switch to 100V. The 3497A DC Voltmeter should uprange to the 100V Range. Check and record the 3497A's +100V reading.

x. (Step #13). Downrange the DC Standard's output to +10V and then downrange the Reference Divider's Input Voltage Switch to 10V.

y. Set the voltmeter option to the 10V Range (program code VR3). Downrange the Reference Divider's Output Switch to 1V. Check and record the 3497A's +1V reading (on the 10V Range).

z. (Step #14). Reverse the input leads going to the 3497A. Check and record the 3497A's -1V reading.

aa. (Step #15). With the 3497A connected as in step z, uprange the Reference Divider's Output Voltage Switch to 5V. Check and record the 3497A's -5V reading.

bb. (Step #16). With the 3497A connected as in step z, uprange the Reference Divider's Output Voltage Switch to 10V. Check and record the 3497A's -10V reading. Turn the DC Standard's output off. Then disconnect the DC Standard, DC Transfer Standard, DC Null Voltmeter, and 3497A from the Reference Divider. This completes the DC Voltmeter Test.

4-69. DC Current Source Test

4-70. This test checks the specified accuracy of the Constant Current Source (part of the voltmeter option). Since the 3497A's DC Voltmeter is used to do the DC Current Test, make sure the voltmeter function is operating correctly before doing the test. The test limits are printed in Table 4-4 and also on the Voltmeter Option Test Card. Each step on the test card also corresponds to a certain step in the procedure. The corresponding step in the procedure is shown in parenthesis.

4-71. Equipment Required. The following is the required test equipment for the test.

Standard Resistors:

10K ohm ±.001% (Guildline Model 9330/10K or 9330A/10k)

100K ohm ±.001% (Guildline Model 9330/100K or 9330A/100K)

4-72. Test Procedure. Do the following:

a. (Step #1). Reset the 3497A by pressing the RESET button on the front panel.

b. (Step #2). Connect the 10K ohm Standard Resistor to the Current Source Output, as shown in Figure 4-8. Also, connect the output to the DC Voltmeter, as shown in the figure.

c. Set the current source for a 1mA output (program code VC3).

d. Check and make sure the reading on the 3497A is within the specified limits shown on the test card and in Table 4-4. Then record the reading on the test card.

e. (Step #3). Change the output current to 100μA (program code VC2). Check and record the reading.

Table 4-4. Current Source Test Limits

Step#	Input	Range	Set-Up/ Configuration	24 Hour Limits high	24 Hour Limits low	90 Day Limits high	90 Day Limits low	1 Year Limits high	1 Year Limits low
1	Open	-	Press RESET						
2	10K ohm	1mA	VM Autorange	+10.0013V	+09.9987V	+10.0025V	+09.9975V	+10.0032V	+09.9968V
3	10K ohm	100μA	VM Autorange	+1.00013V	+0.99987V	+1.00025V	+0.99975V	+1.00032V	+0.99968V
4	100K ohm	10μA	VM Autorange	+1.00013V	+0.99987V	+1.00025V	+0.99975V	+1.00032V	+0.99968V

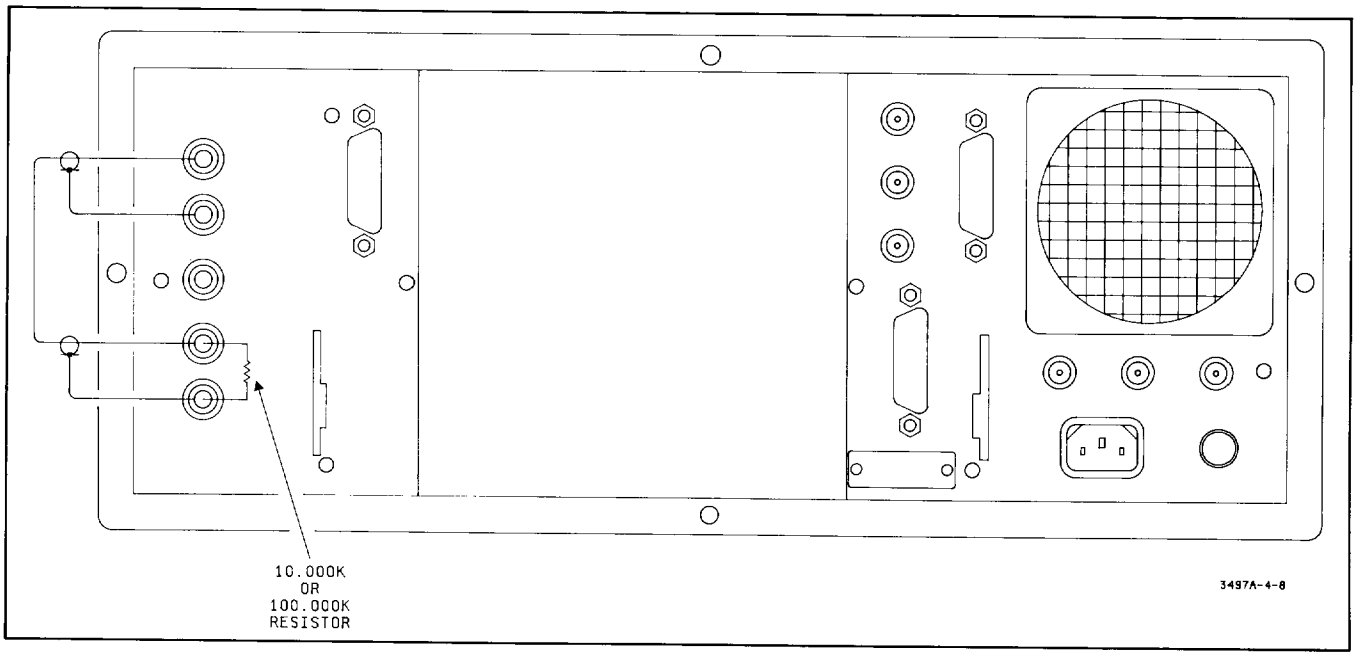


Figure 4-8. DC Current Source Test Connection

f. (Step #4). Replace the 10K ohm resistor with a 100K ohm Standard resistor.

g. Change the output current to 10μA. Check and record the reading.

h. Disconnect the Standard Resistor and DC Voltmeter from the Current Source. This completes the DC Current Test.

4-73. Remote Set-Up of Voltmeter Option

4-74. If the optional front panel (Option 260) is installed, the voltmeter option has to be setup and read remotely. This is done using a Model HP-85A Desktop Computer. Make sure the I/O ROM and I/O card are installed in the computer (see paragraph 4-14 or 4-16). Then connect the computer to the 3497A, as shown in Figure 4-3 (for the standard HP-IB mainframe). An example showing how to send program codes to the 3497A in order to setup the voltmeter option, and how to read the option, follows this paragraph. In the example, the DC Voltmeter is set to the 10V Range (by sending program code VR10) and a reading is then taken.

a. To send program code VR10 to the 3497A, do this:

HP-IB Format - OUTPUT 709 ;"VR10"

Serial I/O - OUTPUT 10 USING "K" ;"VR10"

b. To display the reading of the voltmeter, do this:

HP-IB Format - ENTER 709 ;A

PRINT A

Serial I/O - ENTER 10 USING "#,K" ; A

PRINT A

4-75. VOLTMETER OPTION ADJUSTMENT PROCEDURES

4-76. General

4-77. The following adjustment procedures for the 3497A are used to calibrate the voltmeter option to the listed specifications. When the voltmeter option is adjusted, it should meet its 24 hour specifications. Since, after adjustment of the option, a performance test is required, the adjustment procedures are combined with the corresponding performance tests. The procedures are set up in such a way that the performance tests can be ignored, if so desired.

4-78. Other adjustments of the mainframe and voltmeter options are normally performed after repair or service of the instrument. These include battery charger adjustment for the mainframe, and various offset and reference adjustment for the voltmeter option. These adjustment procedures are in paragraph 4-92 (Miscellaneous Adjustments).

4-79. The following are the voltmeter option adjustment procedures for the 3497A.

DC Voltmeter Adjustment and Performance Test - paragraph 4-80

DC Current Adjustment - paragraph 4-86

4-80. DC Voltmeter Adjustments and Performance Test

4-81. General. The following procedure is used to calibrate the DC Voltmeter to meet its 24 hour accuracy limits. It is recommended that this procedure be performed at 90 day intervals.

4-82. Refer to Table 4-5 for the adjustment and test limits. Each calibration and performance step in the table is also shown in parenthesis in the procedure. Make sure the 3497A has been warmed up for at least one hour before doing any adjusting and testing.

4-83. Adjustment Location. All adjustments are located behind the front panel. To open the front panel, unscrew the captive fastener counter-clockwise until it is free. Then swing the front panel out until it is perpendicular with the frame. The adjustments are at the right side of the instrument (see Figure 4-9).

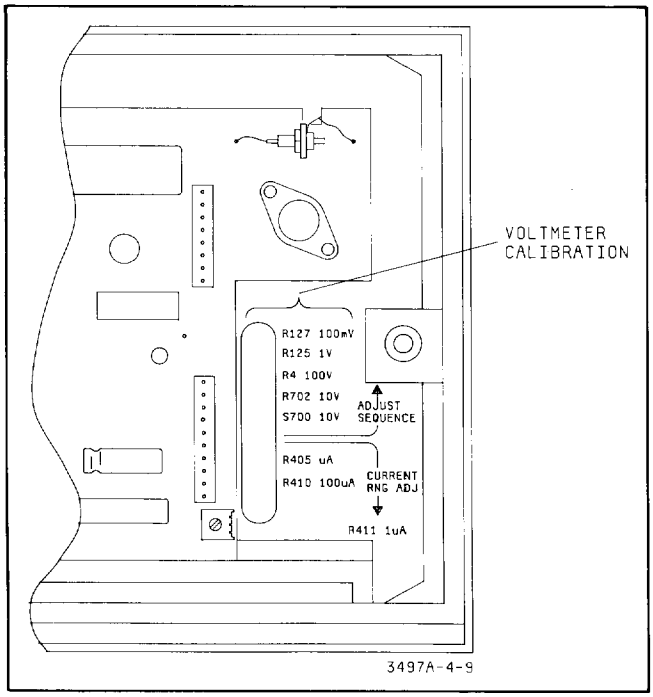


Figure 4-9. Voltmeter Option Adjustment Location

4-84. Equipment Required. The following is the required equipment for the DC Voltmeter adjustment and test procedure.

Reference Divider (Fluke Model 750A)
DC Transfer Standard (Fluke Model 731B)
DC Standard (Systron Donner Model M107)
DC Null Voltmeter (Keithley Model 155)

4-85. Adjustment and Test Procedure. The following tests and adjustments are performed using the standard front panel. If the optional front panel is installed, use a computer (like the Model HP-85A) to setup and read data from the option (see paragraph 4-73). Do the following:

a. (Step #1). Reset the 3497A to its turn-on state by pressing the RESET button on the front panel (or, if in remote, clear the instrument by sending CLEAR 709). This sets the voltmeter to 5½ Digit Display, Autozero On, and Autorange On.

b. If no performance checks are to be made, continue with step c. If the checks are to be performed, do the following:

1. (Step #2). Short the HI COM and LO COM Input Terminals on the rear panel of the 3497A.

2. Make sure the 3497A reading is within the specified limits in Table 4-5.

3. (Step #3, 4 and 5). Set the voltmeter option to the 1V, 10V, and 100V Ranges (program codes VR2, VR3, and VR4, respectively). Check the readings. Then remove the short from the Input Terminals.

c. (Step #6). Set the voltmeter option to the 10V Range (program code VR3). Connect the DC Transfer Standard's "+" terminal to the 3497A's HI COM terminal and the "-" terminal to the LO COM terminal.

d. Set the DC Transfer Standard to the 10V Range. Adjust pot R702 (behind the front panel) for a +10.0000V ±1 count reading on the 3497A display. If able to adjust to the required reading, continue with step e. If unable to adjust, do the following:

1. Turn pot R702 completely counter-clockwise.

2. Turn switch S700 until the 3497A reading is as close to +10V as possible. If the reading is higher than +10.0000V, turn the switch one position for a lees than +10.0000V reading.

3. Adjust pot R702 for a +10.0000V ±1 count reading.

e. If no performance checks are to be made, continue with step f. If the checks are to be performed, do the following:

1. (Step #7). Set the 3497A to the 4 Digit Display mode (program code VD4). Check the reading.

2. (Step #8). Set the 3497A to the 3 Digit Display mode (program code VD3). Check the reading.

3. (Step #9). Return the instrument to the 5 Digit Display mode (program code VD5).

4. Turn Autozero off (program code VA0) and check the reading. Then turn Autozero back on again (program code VA1).

Table 4-5. DC Voltmeter Calibration and Test Limits

Step#	Input	Range	Set-Up/ Configuration	Test Limits high	Test Limits low	Adjust
1	Open	-	Press RESET			
2	Short	Auto	AZ On	+.000003V	-.000003V	
3	Short	1V	AZ On	+0.00001V	-0.00001V	
4	Short	10V	AZ On	+00.0001V	-00.0001V	
5	Short	100V	AZ On	+000.001V	-000.001V	
6	+10V	10V	AZ On	Cal.	Cal.	S700/R702
7	+10V	10V	4 Dig.	+10.002V	+09.998V	
8	+10V	10V	3 Dig.	+10.02V	+09.98V	
9	+10V	10V	5 Dig. AZ Off	+10.0004V	+09.9996V	
10	+1V	1V	AZ On	Cal.	Cal.	R125
11	+.1V	.1V	AZ On	Cal.	Cal.	R127
12	+100V	100V	AZ On	Cal.	Cal.	R4
13	+1V	10V	AZ On	+01.0001V	+00.9999V	
14	-1V	10V	AZ On	-01.0001V	-00.9999V	
15	-5V	10V	AZ On	-05.0002V	-04.9998V	
16	-10V	10V	AZ On	-10.0003V	-09.9997V	

f. (Step #10). Set the DC Voltmeter to Autorange (program code VR5). Set the DC Transfer Standard for +1V output. Adjust pot R125 for a +1.00000V ±1 count reading.

g. Disconnect the DC Transfer Standard from the 3497A.

h. (Step #11). Refer to Figure 4-7. Using short pieces of 20 AWG insulated solid copper wire, connect the DC Transfer Standard and Null Voltmeter to the Reference Divider, as shown in Figure 4-7. Turn the output of the DC Standard off. Using 24 inch or shorter shielded cables, connect the DC Standard to the Reference Divider, as shown in the figure.

i. Set the Standard Cell Voltage control on the Reference Divider to correspond with the output voltage setting of the DC Transfer Standard. Normally the Transfer Standard's output should be set to the voltage value of the standard cell used to calibrate the Transfer Standard.

j. Zero the Null Voltmeter on the 3 microvolt range and then set it to the 300 microvolt range.

k. Set the Reference Divider's Input Voltage Switch to 10V and center its Coarse and Fine adjust controls.

l. Set the Reference Divider's Output Voltage Switch to .1V.

m. Set the DC Standard for an output of +10V and then turn its output on.

n. Set the Reference Divider's Standard Cell Switch to the LOCKED position. Adjust the DC Standard's output for a zero reading on the DC Null Voltmeter.

o. Downrange the Null Voltmeter and adjust the Reference Divider's Coarse and Fine adjust controls for a zero reading on the Null Voltmeter's 3 microvolt range.

p. Set the Reference Divider's Standard Cell Switch to OPEN. Then set the switch to MOMENTARY and, if necessary, readjust the Fine control for a zero reading on the Null Voltmeter.

q. Adjust R127 for a .100000V ±1 count reading on the 3497A display.

NOTE

The Reference Divider's Fine control may have to be readjusted, when the output switch is set to another position.

r. (Step #12). Uprange the Reference Divider's Input Voltage Switch to 100V and then uprange the DC Standard's output to +100V.

CAUTION

Always uprange the Reference Divider Input Voltage Switch before upranging the DC Standard and downrange the DC Standard before downranging the Reference Divider.

s. Uprange the Reference Divider's Output Voltage Switch to 100V. Adjust pot R4 for a +100V ±1 count reading on the display.

t. Downrange the DC Standard's output to +10V and then downrange the Reference Divider's Input Voltage Switch to 10V. If no performance checks are to be made, continue with step u. If the checks are to be performed, do the following:

1. (Step #13). Set the voltmeter option to the 10V Range program code VR3). Downrange the Reference Divider's Output Voltage Switch to 1V.

Check the reading on the 3497A display (+1V on the 10V Range).

2. (Step #14). Reverse the input leads going to the 3497A. Check the -1V reading.

3. (Step #15). Uprange the Reference Divider's Output Voltage Switch to 5V. Check the reading.

4. (Step #16). Uprange the Reference Divider's Output Voltage Switch to 10V. Check the -10V reading.

u. Turn the DC Standard's output off. Then disconnect the DC Standard, DC Transfer Standard, DC Null Voltmeter, and 3497A from the Reference Divider. This completes the DC Voltmeter Adjustment and Performance Test.

4-86. DC Current Adjustment

4-87. General. Since all ranges of the Constant Current Source are calibrated, no performance test is required. Also, since the 3497A's DC Voltmeter is used to calibrate the current source, make sure it is accurate and operating correctly. Perform the DC Voltmeter Performance Test and/or Adjustment procedures before calibrating the current source.

4-88. The calibration set-up information is in Table 4-6. Each calibration step in the table is also shown in parenthesis in the adjustment procedure. Make sure the 3497A has been warmed up for at least one hour, before doing the calibration.

4-89. Adjustment Location. All adjustment locations are behind the front panel. To open the front panel, unscrew the captive fastener counter-clockwise until it is free. Then swing the front panel out until it is perpendicular with the frame. The adjustments are at the right side of the instrument (see Figure 4-9).

Table 4-6. DC Current Calibration

Step#	Input	Range	Set-Up/ Configuration	Adjust
1	Open	-	Press RESET	
2	10K ohm	1mA	VM Autorange	R411
3	10K ohm	100μA	VM Autorange	R410
4	100K ohm	10μA	VM Autorange	R409

4-90. Equipment Required. The following is the required test equipment for the DC Current Adjustment and Test.

Standard Resistors:

10K ohm ±.001% (Guildline Model 9330/10K or 9330A/10K)

100K ohm ±.001% (Guildline Model 9330/100K or 9330A/100K)

4-91. Adjustment Procedure. Do the following:

a. (Step #1). Reset the 3497A by pressing the RESET button on the front panel.

b. (Step #2). Connect the 10K ohm Standard Resistor to the Current Source Output, as shown in Figure 4-8. Also, connect the output to the DC Voltmeter, as shown in the figure.

c. Set the current source for a 1mA output (program code VC3).

d. Adjust R411 for +10.0000V ±1 count reading on the 3497A display. If unable to adjust to the specified limits, the coarse adjustment procedure for the current source should be performed. This procedure is in paragraph 4-92 (Miscellaneous Adjustments). If unable to do a coarse adjustment, go to Service Group C for troubleshooting.

e. (Step #3). Change the output current to 100μA (program code VC2). Adjust R410 for a +1.00000 ±1 count reading on the 3497A display.

f. (Step #4). Replace the 10K ohm resistor with a 100K ohm Standard Resistor.

g. Change the output current to 10μA (program code VC1). Adjust R409 for a +1.00000V ±1 count reading on the 3497A display.

h. Disconnect the Standard Resistor and DC Voltmeter from the current source. This completes the DC Current Adjustments.

4-92. MISCELLANEOUS ADJUSTMENTS

4-93. The following adjustment procedures are for the 3497A mainframes (HP-IB and Serial I/O) and the voltmeter option. The procedures are normally performed after servicing the instrument or, in the case of the voltmeter option, if unable to calibrate the voltmeter to specifications. Under normal conditions, these adjustments are not necessary. The following are the miscellaneous adjustment procedures for the 3497A.

Battery Charger Adjustment - paragraph 4-97
Thermocouple Reference Adjustment - paragraph 4-101
Procedure to Gain Access to the Voltmeter Option - paragraph 4-105

-12V Reference Coarse Adjust - paragraph 4-107
DC Voltmeter Offset Adjustment - paragraph 4-111
Switch Feedthrough and Pre-Charge Adjustment - paragraph 4-114

Input Amplifier Offset Adjustment - paragraph 4-118
Current Source Coarse Adjustment - paragraph 4-122

4-94. Adjustment Locations

4-95. The Battery Charger Adjustments and Thermocouple Adjustments are mainframe adjustments and are performed on the mainframe power supply board. Information on how to get to those adjustments is located in the adjustment procedures themselves.

4-96. The voltmeter adjustments are located on the voltmeter option board. To get to those adjustments, the board needs to be removed from the instrument. A separate removal procedure is in paragraph 4-105. Do the removal procedure first before doing any of the voltmeter option adjustments.

4-97. Battery Charger Adjustment

4-98. The battery charger adjustment sets the correct voltage used to charge the battery. This should be performed after repairing the battery charger circuitry. Also, if it is suspected that the battery is being overcharged, perform the adjustment. A battery that is overcharged has a shorter than normal life expectancy.

4-99. Equipment Required. The required equipment is a High Impedance Digital Voltmeter (like the -hp- Model 3456A) with appropriate test leads. If the voltmeter is not available, others, like the -hp- Models 3468A or 3478A Digital Multimeters (or equivalent), may also be used. Other equipment required is a 0-15V power supply. The recommended model is the -hp- Model 6215A.

4-100. Adjustment Procedure. Do the following:

a. Disconnect all external connector cards and signal lines from the rear of the 3497A. The ac power line cord may remain connected.

WARNING

Components on portions of the power supply board are at guard potential and not at ground potential; they may represent a serious shock hazard.

b. Turn the 3497A off.

c. Open the front panel by unscrewing the captive fastener counter-clockwise until it is free. Then swing the front panel out until it is perpendicular with the frame.

d. Behind the front panel in front of the mainframe boards is the power supply board (A16 Assembly). At this time, the board is covered with a metal shield. Remove the two screws that hold the shield in place and then remove the shield.

e. Refer to Figure 4-10 and locate diode A16CR2. Using a clip lead, connect the anode (TP2) of the diode to chassis ground (TP1), as shown in Figure 4-10.

f. Set the external power supply to a little less than 5V. Then connect the positive output of the power supply to the cathode (TP3) of A16CR2, as shown in Figure 4-10. Connect the negative output of the power supply to chassis ground.

g. Turn the 3497A on. Note that the "CHARGE" LED on the power supply board is on.

h. Increase the voltage on the external power supply until the "CHARGE" LED goes out. Measure the voltage using the test Digital Voltmeter and make sure it is between 7.95V and 8.05V.

i. If the voltage is correct, no adjustment is necessary. If the voltage is incorrect, the battery charger circuitry is out of adjustment. To readjust the circuitry, do the following:

1. Leave the clip lead and external power supply connected (see steps e and f).

2. Adjust the external power supply for exactly 8V (use the test Digital Voltmeter).

3. Locate potentiometer A16R10 and turn it fully clockwise. The "CHARGE" LED should be on.

4. Turn A16R10 slowly counter-clockwise until the "CHARGE" LED barely turns off.

5. Check for the proper setting of A16R10 by reducing the external power supply voltage to less than 5V and repeat step h. If the LED still does not turn off at 8V, readjust A16R10 until it does.

j. If no more adjustments to the mainframe are to be performed (see next paragraph), turn the 3497A off, and remove the external power supply, the short from diode A16CR2, and the test Digital Voltmeter. Replace the power supply shield, and close and fasten the front panel.

4-101. Thermocouple Reference Adjustment

4-102. This adjustment need only be performed if a Relay Multiplexer Assembly with Thermocouple Compensation (Option 020) is installed in the 3497A. A reference voltage is adjusted to improve the thermocouple reference output accuracy.

4-103. Equipment Required. The required equipment is a High Impedance Digital Voltmeter (like the -hp- Model 3456A) with appropriate test leads. If the voltmeter is not available, others, like the -hp- Models 3468A or 3478A Digital Multimeters (or equivalent), may also be used.

4-104. Adjustment Procedure. The adjustment procedure requires that one or more jumpers, located on the 3497A's

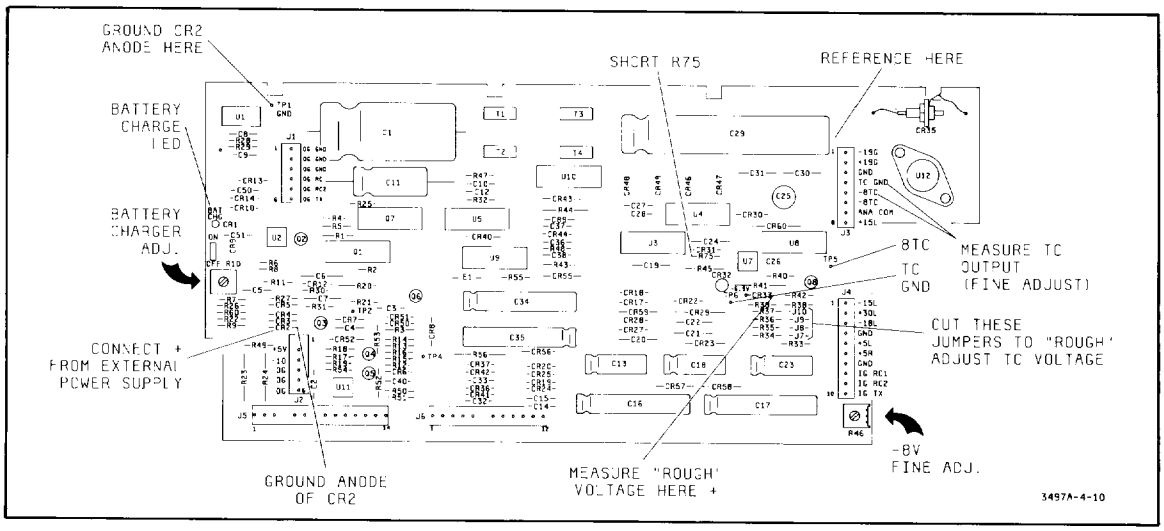


Figure 4-10. Mainframe Adjustment Locations

mainframe power supply board, may have to be changed. Do the following:

a. Disconnect all external connector cards and signal lines from the rear of the 3497A. The ac power line cord may remain connected.

WARNING

Components on portions of the power supply board are at guard potential and not at ground potential; they may represent a serious shock hazard.

b. Make sure the 3497A is turned off.

c. Open the front panel by unscrewing the captive fastener counter-clockwise until it is free. Then swing the front panel out until it is perpendicular with the frame.

d. Behind the front panel in front of the mainframe boards is the power supply board. At this time, the board is covered with a metal shield. Remove the two screws that hold the shield in place and then remove the shield.

e. Turn the 3497A on.

f. Connect the test voltmeter to the fourth (TC GND) and fifth (-8TC) pins of A16J3 or connect to TP5 (-8TC) and TP6 (TC GND), as shown in Figure 4-10.

g. Adjust A16R46 for a reading of -8.000V on the test voltmeter.

h. If the -8V can be adjusted using A16R46, continue with step i. If the -8V cannot be adjusted using A16R46, perform the following coarse adjustment of the thermocouple reference voltage.

1. Turn the 3497A off. Refer to Figure 4-11 and install any missing jumpers (A16J7 through J10).

2. Refer to Figure 4-10 and locate resistor A16R75 on the power supply board. Short across the resistor.

3. Next, locate A16C29 and connect the negative lead of the test Digital Voltmeter to the negative lead of the capacitor, as shown in Figure 4-10. Then locate diode CR33 and connect the positive lead of the voltmeter to the cathode of the diode, as shown in the figure.

4. Turn the 3497A on.

5. Note the voltage reading on the test voltmeter.

6. Refer to Table 4-7 and select the appropriate jumpers that corresponds to the voltage noted in the previous step.

7. Once the correct jumpers are selected, remove the short from A16R75.

8. Repeat steps f and g to do the -8V fine adjustment.

i. Turn the 3497A off and disconnect the test voltmeter from the power supply board. Then replace the power supply shield, and close and fasten the front panel. This completes the Thermocouple Reference Adjustment.

4-105. Procedure to Gain Access to the Voltmeter Option

4-106. The following procedure is used to gain access to the voltmeter option to adjust the option. Since the voltmeter board is mounted on the inguard controller board, the Inguard Controller board has to be removed before access to the voltmeter board is possible. Do the following:

VOLTMETER OPTION PERFORMANCE TEST CARD

1 YEAR LIMITS

Hewlett-Packard Model 3497A
Data Acquisition/Control Unit

Serial Number_____ Test Performed By_____
Date_____

DC Volts Test

Step#	Input to Option	Set-Up and Configuration	High Limit	Reading	Low Limit	Test Pass	Test Fail
1	Open	Press RESET					
2	Short	.1V Range	+.000003V	_____	−.000003V	___	___
3	Short	1V Range	+0.00001V	_____	−0.00001V	___	___
4	Short	10V Range	+00.0001V	_____	−00.0001V	___	___
5	Short	100V Range	+000.001V	_____	−000.001V	___	___
6	+10V	10V Range	+10.0016V	_____	+09.9984V	___	___
7	+10V	4 Digit	+10.003V	_____	+09.997V	___	___
8	+10V	3 Digit	+10.02V	_____	+09.98V	___	___
9	+10V	5 Digit					
		AZ off	+10.0017V	_____	+09.9983V	___	___
10	+1V	1V Range					
		AZ on	+1.00016V	_____	+0.99984V	___	___
11	+.1V	.1V Range	+.100018V	_____	+.099982V	___	___
12	+100V	100V Range	+100.016V	_____	+099.984V	___	___
13	+1V	10V Range	+01.0003V	_____	+00.9997V	___	___
14	−1V	10V Range	−01.0003V	_____	−00.9997V	___	___
15	−5V	10V Range	−05.0009V	_____	−04.9991V	___	___
16	−10V	10V Range	−10.0016V	_____	−09.9984V	___	___

DC Current Test

Step#	Input to Option	Set-Up and Configuration	High Limit	Reading	Low Limit	Test Pass	Test Fail
1	Open	Press RESET					
2	10K ohm	1mA Range	+10.0032V	_____	+09.9968V	___	___
3	10K ohm	100μA Range	+1.00032V	_____	+0.99968V	___	___
4	100K ohm	10μA Range	+1.00032V	_____	+0.99968V	___	___

a. Turn the 3497A off and remove the power line cable from the instrument.

b. If the rear panel safety cover is in place, remove the cover by removing the two screws that hold it in place. Then remove the rear cover bracket by removing the screws that hold the bracket in place.

c. Refer to Figure 4-11. Note that the Inguard Controller board is held in place by two mounting screws. Loosen the screws, but do not remove them. They are held in place by a rubber grommet.

d. Locate the built-in finger ring, shown in Figure 4-11, and pull on the ring to remove the board from the 3497A chassis.

e. On the inguard assembly, locate the voltmeter board. Then locate the metal shield on the board, as shown in Figure 4-12. Remove the four machine bolts located near the corners of the shield and then remove the shield, as shown in the figure.

Table 4-7. Thermocouple Voltage Jumper Selection

Voltage at Cathode CR33		Jumpers			
Min	Max	J7	J8	J9	J10
6.62	6.6859	X	X	X	X
6.6860	6.7424		X	X	X
6.7425	6.7945	X		X	X
6.7946	6.8324			X	X
6.8325	6.8866	X	X		X
6.8867	6.9276		X		X
6.9277	6.9657	X			X
6.9658	7.0012				X
7.0013	7.0343	X	X	X	
7.0344	7.0653		X	X	
7.0654	7.0943	X		X	
7.0944	7.1216			X	
7.1217	7.1474	X	X		
7.1475	7.1716		X		
7.1717	7.1946	X			
7.1947	7.2180				

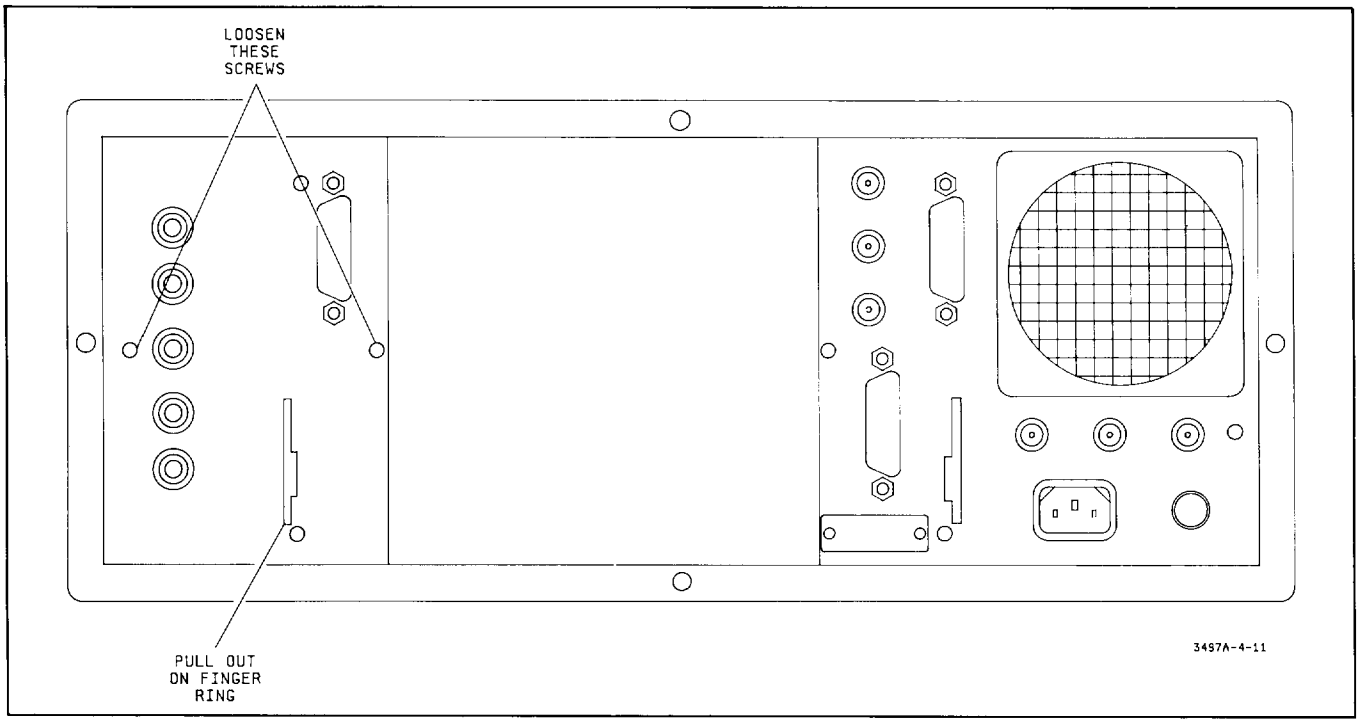


Figure 4-11. Inguard Board Mounting Screws and Finger Ring

f. When the shield is removed, the Inguard Controller can then be reconnected to the 3497A using a Board Extender (-hp- Part No. 03497-67913). The voltmeter board can then be adjusted. Acquire a Board Extender and do the following:

1. Locate the slot in the 3497A mainframe marked "INGUARD CONTROLLER" and align the Board Extender with that slot. Then push the extender into the slot until it seats firmly in the motherboard socket.

2. Plug the cable from the Board Extender onto the Inguard Controller board.

g. Replace the power cable on the 3497A and turn the instrument on. Let it warm up to operating temperature. The voltmeter option board is ready for adjustments.

h. After adjustment of the voltmeter option, replace the board back in the instrument. Do the following:

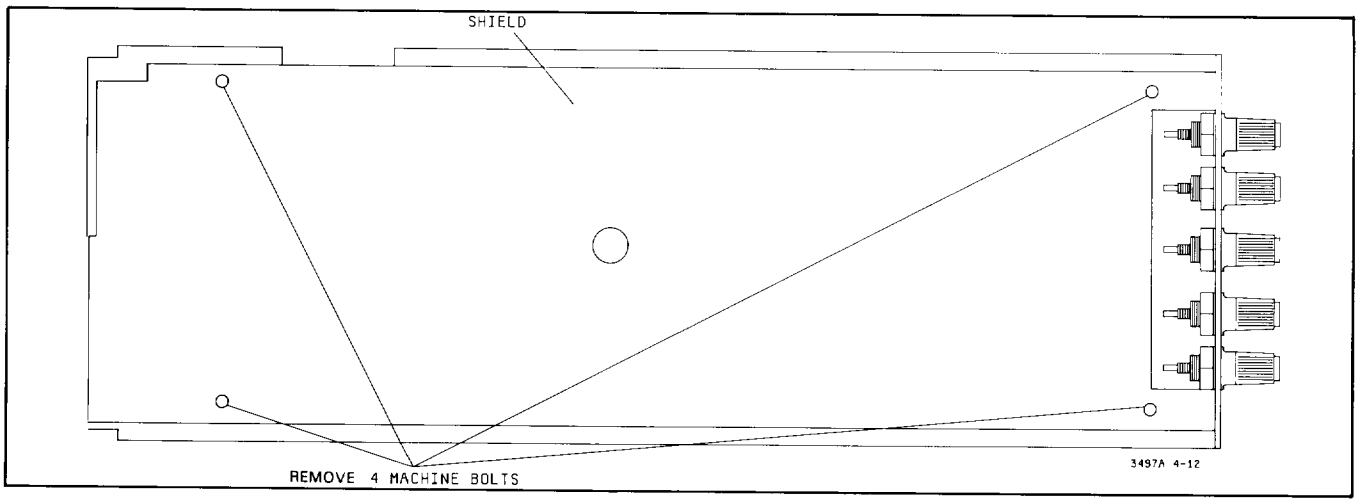


Figure 4-12. Removing Voltmeter Shield

1. Turn the 3497A off and remove the power line cable from the instrument.

2. Remove the Inguard Controller board from the Board Extender and then remove the Board Extender from the instrument.

3. Replace the shield over the voltmeter board. Then replace and tighten the four mounting bolts.

4. Locate the slot in the 3497A mainframe marked "INGUARD CONTROLLER" and align the Inguard Controller board with that slot. Then push the board into the slot until it seats firmly in the motherboard socket.

5. Locate the mounting screws, shown in Figure 4-11, and tighten the screws. Reinstall the rear cover bracket.

4-107. -12V Reference Coarse Adjust

4-108. This adjustment is performed if unable to calibrate the DC Voltmeter to the specified limits or after servicing the voltmeter. Make sure the voltmeter board is accessible by performing the procedure in paragraph 4-105.

4-109. Equipment Required. The required equipment is a DC Transfer Standard (Fluke Model 731B).

4-110. Adjustment Procedure. Do the following:

a. Locate the -12V Reference Jumpers (J700 to J707; see Figure 4-14). Place all jumpers to the left, as shown in Figure 4-13. Set switch S700 to position "6" and adjust pot R702 to its counter-clockwise position. (Refer to Figure 4-14 to determine the location of S700 and R702 on the voltmeter option board.)

b. Using the front panel, set the DC Voltmeter to the 10V Range (or send program code VR3, if in remote).

c. Set the DC Transfer Standard to the 10V Range. Connect the standard's "+" output to the 3497A's HI COM terminal and its "-" output to the LO COM terminal.

d. Starting with jumper J700 (bottom jumper) and working up to J707, move one jumper at a time to the right position. If the reading on the display goes above +10V, return the jumper which was moved last back to the left position. Otherwise leave the jumper in the right position.

e. When all jumpers have been placed in the appropriate position, adjust S700 clockwise until the display shows close to but not above +10V.

f. This completes the -12V Reference Coarse Adjustment. Perform the adjustment procedure in paragraph 4-80 in this section of the manual.

4-111. DC Voltmeter Offset Adjustment

4-112. Perform this adjustment only after servicing the input switching circuitry of the DC Voltmeter. It consists of selecting padding resistors to enable the DC Voltmeter to read zero volts at the lowest range. Make sure the voltmeter board is accessible by performing the procedure in paragraph 4-105.

4-113. Adjustment Procedure. Do the following:

a. Refer to Figure 4-14 and locate R36. If there is no R36 mounted on the voltmeter board, continue with the next step. If R36 is mounted on the board, remove it. If a soldering iron was used to remove R36, give enough time for the circuitry to stabilize. Then continue with the next step.

b. Using the front panel, set the DC Voltmeter to the .1V Range (or send program code VR1, if in remote) and short the HI COM and LOW COM Input terminals.

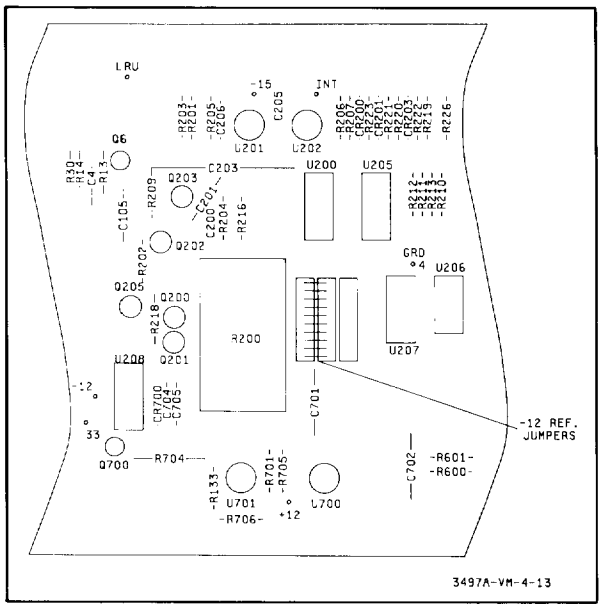


Figure 4-13. Reference Jumpers

c. Note the reading of the DC Voltmeter.

d. If the reading is zero volts, no padding is required.

e. If the reading is more than 2 counts (i.e., 2 microvolts), padding will not bring the reading to zero volts. The voltmeter needs service (go to Service Group C).

f. If the reading is not zero volts but is smaller than ±2 counts (±2 microvolts), padding is required. This is done by selecting a padding resistor (R36) to bring the reading to zero. Use a 6.8M ohm or 8.2M ohm (-hp- Part No. 0698-6592 and 0699-0741, respectively) resistor if the reading is between 1 to 2 counts (microvolts) and use a 12M ohm resistor (-hp- Part No. 0699-0740) if below 1 count (microvolt). Select the appropriate placement of the resistor by doing the following:

1. If the offset is negative, connect resistor R36 to the −12V position, as shown in Figure 4-14.

2. If the offset is positive, connect resistor R36 to the +12V position, as shown in Figure 4-14.

4-114. Switch Feedthrough and Pre-Charge Adjustment

4-115. Perform this adjustment only after servicing the input switching circuitry of the DC Voltmeter. Make sure the voltmeter board is accessible by performing the procedure in paragraph 4-105.

4-116. Equipment Required. The required equipment is a DC Transfer Standard (Fluke Model 731B).

4-117. Adjustment Procedure. Do the following:

a. Refer to Figure 4-14 and adjust R28 (Pre-charge adjust) to the center of its rotation.

b. Using the front panel, set the dc voltmeter to the 1V Range (or send program code VR2, if in remote).

c. Attach a 1M ohm resistor across the HI COM and LO COM Input terminals.

d. Refer to Figure 4-14 and adjust R8 until the voltmeter reading is 0.00000V. If any noise is noted, adjust R8 until the noise is centered around the zero volts reading.

e. Remove the 1M ohm resistor from the input terminals and connect a .15 microfarad capacitor in its place. Temporarily short across the capacitor to remove any charge on the capacitor. Wait about five seconds and note the voltmeter reading.

f. If the reading is within ±2 microvolts (±2 counts) and stable, no further adjustments are necessary. Remove the capacitor and the adjustment is completed.

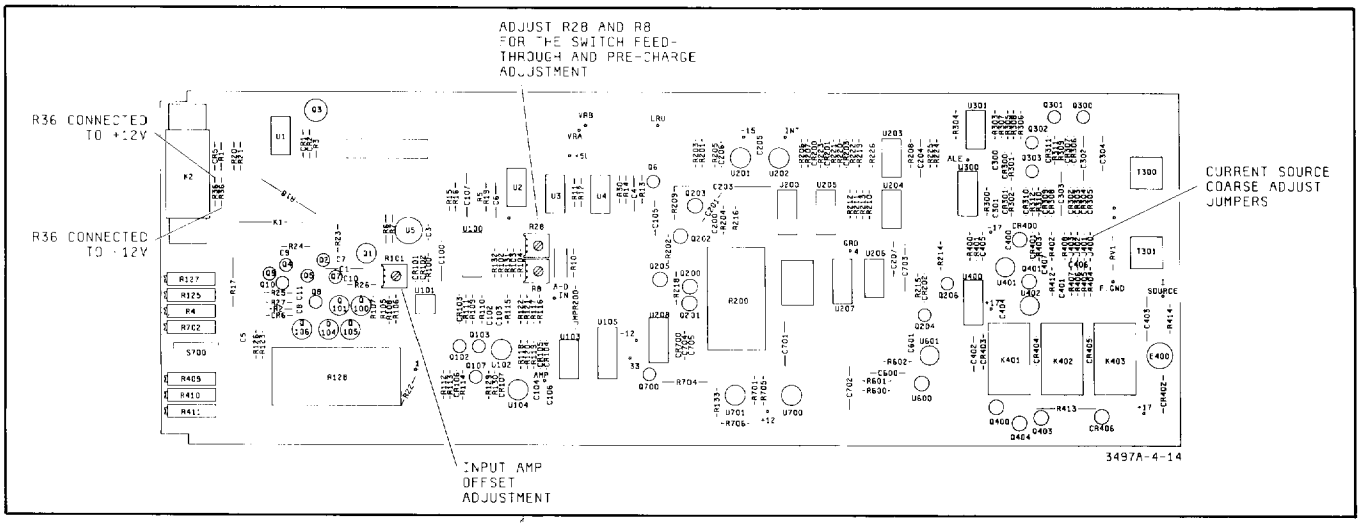


Figure 4-14. Miscellaneous Voltmeter Option Adjustment Locations

g. If the reading is greater than ±2 microvolts (±2 counts), slightly readjust R28 until the reading is zero volts. Then remove the capacitor and go back to step c.

4-118. Input Amplifier Offset Adjustment

4-119. Perform this adjustment only after servicing the input amplifier circuitry of the DC Voltmeter. Make sure the voltmeter board is accessible by performing the procedure in paragraph 4-105.

4-120. Equipment Required. The required equipment is a High Impedance Digital Voltmeter (like the -hp- Model 3456A) with appropriate test leads. If the voltmeter is not available, others, like the -hp- Models 3468A or 3478A Digital Multimeters (or equivalent), may also be used.

4-121. Adjustment Procedure. Do the following:

a. Using the front panel, set the DC Voltmeter to the 10V Range (or send program code VR3, if in remote) and short the HI COM and LOW COM Input terminals.

b. Connect the test Digital Voltmeter between TP A-D IN (see Figure 4-14) and the LO COM terminal.

c. Refer to Figure 4-14 and adjust R101 for a 0V ±5 microvolt reading on the test voltmeter.

d. Remove the test voltmeter. This completes the adjustment.

4-122. Current Source Coarse Adjustment

4-123. Do this adjustment only if unable to calibrate the current source or after repairing the current source. Make sure the voltmeter board is accessible by performing the procedure in paragraph 4-105.

4-124. Adjustment Procedure. Do the following:

a. Refer to Figure 4-14 and locate the four current source jumpers on the voltmeter board. Replace any jumpers that are missing.

b. Connect a 10K ohm resistor across the current source output terminals (located at the inguard rear panel). Then connect the HI COM and LO COM Input terminals to the current source terminals. This is done because the 3497A voltmeter is used to measure the voltage across the 10K ohm resistor.

c. Set the current source to the 1mA Range (send program code VC3, if in remote).

d. Using the DC Voltmeter of the 3497A, measure the voltage across the 10K ohm resistor. Note the voltage value.

e. Refer to Table 4-8 and, dependent on the voltage value noted in the previous step, cut the appropriate jumper(s) as shown in the table. This completes the current source coarse adjustment. Go to paragraph 4-86 to calibrate the current source.

Table 4-8. Current Source Jumpers

Voltmeter Reading	Cut Jumper
9.900	Cut none
9.8295	J403
9.7590	J402
9.6885	J403 & J402
9.6180	J401
9.5475	J401 & J403
9.4770	J401 & J402
9.4065	J401, J402 & J403
9.3360	J400
9.2655	J400 & J403
9.1951	J400 & J402
9.1246	J400, J402 & J403
9.0541	J400 & J401
8.9836	J400, J401 & J403
8.9131	J400, J401 & J402
8.8426	Cut all jumpers

VOLTMETER OPTION PERFORMANCE TEST CARD

24 HOUR LIMITS

Hewlett-Packard Model 3497A
Data Acquisition/Control Unit

Serial Number_____ Test Performed By_____
Date_____

DC Voltmeter Test

Step#	Input to Option	Set-Up and Configuration	High Limit	Reading	Low Limit	Test Pass	Test Fail
1	Open	Press RESET				____	____
2	Short	.1V Range	+.000003V	_____	−.000003V	____	____
3	Short	1V Range	+0.00001V	_____	−0.00001V	____	____
4	Short	10V Range	+00.0001V	_____	−00.0001V	____	____
5	Short	100V Range	+000.001V	_____	−000.001V	____	____
6	+10V	10V Range	+10.0003V	_____	+09.9997V	____	____
7	+10V	4 Digit	+10.002V	_____	+09.998V	____	____
8	+10V	3 Digit	+10.02V	_____	+09.98V	____	____
9	+10V	5 Digit					
		AZ off	+10.0004V	_____	+09.9996V	____	____
10	+1V	1V Range					
		AZ on	+1.00003V	_____	+0.99997V	____	____
11	+.1V	.1V Range	+.100006V	_____	+.099994V	____	____
12	+100V	100V Range	+100.003V	_____	+099.997V	____	____
13	+1V	10 V Range	+01.0001V	_____	+00.9999V	____	____
14	−1V	10V Range	−01.0001V	_____	−00.9999V	____	____
15	−5V	10V Range	−05.0002V	_____	−04.9998V	____	____
16	−10V	10V Range	−10.0003V	_____	−09.9997V	____	____

DC Current Test

Step#	Input to Option	Set-Up and Configuration	High Limit	Reading	Low Limit	Test Pass	Test Fail
1	Open	Press RESET					
2	10K ohm	1mA Range	+10.0013V	_____	+09.9987V	____	____
3	10K ohm	100μA Range	+1.00013V	_____	+0.99987V	____	____
4	100K ohm	10μA Range	+1.00013V	_____	+0.99987V	____	____

VOLTMETER OPTION PERFORMANCE TEST CARD

90 DAY LIMITS

Hewlett-Packard Model 3497A
Data Acquisition/Control Unit

Serial Number_____ Test Performed By_____
Date_____

DC Voltmeter Test

Step#	Input to Option	Set-Up and Configuration	High Limit	Reading	Low Limit	Test Pass	Test Fail
1	Open	Press RESET				____	____
2	Short	.1V Range	+.000003V	_____	-.000003V	____	____
3	Short	1V Range	+0.00001V	_____	-0.00001V	____	____
4	Short	10V Range	+00.0001V	_____	-00.0001V	____	____
5	Short	100V Range	+000.001V	_____	-000.001V	____	____
6	+10V	10V Range	+10.0007V	_____	+09.9993V	____	____
7	+10V	4 Digit	+10.002V	_____	+09.998V	____	____
8	+10V	3 Digit	+10.02V	_____	+09.98V	____	____
9	+10V	5 Digit					
		AZ off	+10.0008V	_____	+09.9992V	____	____
10	+1V	1V Range					
		AZ on	+1.00007V	_____	+0.99993V	____	____
11	+.1V	.1V Range	+.100010V	_____	+.099990V	____	____
12	+100V	100V Range	+100.007V	_____	+099.993V	____	____
13	+1V	10V Range	+01.0002V	_____	+00.9998V	____	____
14	-1V	10V Range	-01.0002V	_____	-00.9998V	____	____
15	-5V	10V Range	-05.0004V	_____	-04.9996V	____	____
16	-10V	10V Range	-10.0007V	_____	-09.9993V	____	____

DC Current Test

Step#	Input to Option	Set-Up and Configuration	High Limit	Reading	Low Limit	Test Pass	Test Fail
1	Open	Press RESET					
2	10K ohm	1mA Range	+10.0025V	_____	+09.9975V	____	____
3	10K ohm	100μA Range	+1.00025V	_____	+0.99975V	____	____
4	100K ohm	10μA Range	+1.00025V	_____	+0.99975V	____	____

VOLTMETER OPTION PERFORMANCE TEST CARD

1 YEAR LIMITS

Hewlett-Packard Model 3497A
Data Acquisition/Control Unit

Serial Number_____ Test Performed By_____
Date_____

DC Volts Test

Step#	Input to Option	Set-Up and Configuration	High Limit	Reading	Low Limit	Test Pass	Test Fail
1	Open	Press RESET					
2	Short	.1V Range	+.000003V	_____	−.000003V	___	___
3	Short	1V Range	+0.00001V	_____	−0.00001V	___	___
4	Short	10V Range	+00.0001V	_____	−00.0001V	___	___
5	Short	100V Range	+000.001V	_____	−000.001V	___	___
6	+10V	10V Range	+10.0016V	_____	+09.9984V	___	___
7	+10V	4 Digit	+10.003V	_____	+09.997V	___	___
8	+10V	3 Digit	+10.02V	_____	+09.98V	___	___
9	+10V	5 Digit AZ off	+10.0017V	_____	+09.9983V	___	___
10	+1V	1V Range AZ on	+1.00016V	_____	+0.99984V	___	___
11	+.1V	.1V Range	+.100018V	_____	+.099982V	___	___
12	+100V	100V Range	+100.016V	_____	+099.984V	___	___
13	+1V	10V Range	+01.0003V	_____	+00.9997V	___	___
14	−1V	10V Range	−01.0003V	_____	−00.9997V	___	___
15	−5V	10V Range	−05.0009V	_____	−04.9991V	___	___
16	−10V	10V Range	−10.0016V	_____	−09.9984V	___	___

DC Current Test

Step#	Input to Option	Set-Up and Configuration	High Limit	Reading	Low Limit	Test Pass	Test Fail
1	Open	Press RESET					
2	10K ohm	1mA Range	+10.0032V	_____	+09.9968V	___	___
3	10K ohm	100μA Range	+1.00032V	_____	+0.99968V	___	___
4	100K ohm	10μA Range	+1.00032V	_____	+0.99968V	___	___

SECTION V
REPLACEABLE PARTS

5-1. INTRODUCTION

5-2. This section contains information concerning replaceable parts. Table 5-1 lists abbreviations used in the parts list and throughout the manual. Table 5-2 lists names and addresses that correspond to the manufacturer's five digit code numbers. Table 5-3 lists all replaceable parts in order of their reference designators and indicates the description and Hewlett-Packard part number of each part.

5-3. EXCHANGE ASSEMBLIES

5-4. Many assemblies listed in Table 5-3 are a part of Hewlett-Packard's Blue Stripe Exchange program. New assemblies required for spare parts stock must be ordered by the new assembly part number listed in Table 5-3. Factory repaired and tested assemblies are available on a trade in basis only.

5-5. REPLACEABLE PARTS

5-6. Table 5-3 is the list of replaceable parts and is organized in alphanumerical order by reference designator. The information for each part consist of the following:

a. Reference Designator.

b. Hewlett-Packard part number and the check digit.

c. The total quantity (Qty) used on the assembly. It is given only at the first appearance of the part on the list.

d. The description of the part.

e. A five digit code that indicates the manufacturer of the part.

f. The manufacturer's part number.

5-7. ORDERING INFORMATION

5-8. To obtain replacement parts, address order or inquiry to your nearest Hewlett-Packard Sales and Service Office listed at the end of this manual. Identify the part by its Hewlett-Packard part number and include the instrument model and serial numbers.

5-9. NON-LISTED PARTS

5-10. To obtain a part that is not listed, include the following:

a. Instrument model number.
b. Instrument serial number.
c. Description of part.
d. Function and location of the part.

Table 5-1. List of Abbreviations

ABBREVIATIONS

Ag . . . silver	Hz . . . hertz (cycle(s) per second)	NPO . . . negative positive zero (zero temperature coefficient)	sl . . . slide
Al . . . aluminum			SPDT . . . single-pole double-throw
A . . . ampere(s)	ID . . . inside diameter	ns . . . nanosecond(s) = 10^{-9} seconds	SPST . . . single-pole single-throw
Au . . . gold	impg . . . impregnated	nsr . . . not separately replaceable	
	incd . . . incandescent		Ta . . . tantalum
C . . . capacitor	ins . . . insulation(ed)	Ω . . . ohm(s)	TC . . . temperature coefficient
cer . . . ceramic		obd . . . order by description	TiO_2 . . . titanium dioxide
coef . . . coefficient	kΩ . . . kilohm(s) = 10^{+3} ohms	OD . . . outside diameter	tog . . . toggle
com . . . common	kHz . . . kilohertz = 10^{+3} hertz		tol . . . tolerance
comp . . . composition		p . . . peak	trim . . . trimmer
conn . . . connection	L . . . inductor	pA . . . picoampere(s)	TSTR . . . transistor
	lin . . . linear taper	pc . . . printed circuit	
dep . . . deposited	log . . . logarithmic taper	pF . . . picofarad(s) 10^{-12} farads	V . . . volt(s)
DPDT . . . double-pole double-throw		piv . . . peak inverse voltage	vacw . . . alternating current working voltage
DPST . . . double-pole single-throw	mA . . . milliampere(s) = 10^{-3} amperes	p/o . . . part of	var . . . variable
	MHZ . . . megahertz = 10^{+6} hertz	pos . . . position(s)	vdcw . . . direct current working voltage
elect . . . electrolytic	MΩ . . . megohm(s) = 10^{+6} ohms	poly . . . polystyrene	
encap . . . encapsulated	met film . . . metal film	pot . . . potentiometer	W . . . watt(s)
	mfr . . . manufacturer	p-p . . . peak-to-peak	w/ . . . with
F . . . farad(s)	ms . . . millisecond	ppm . . . parts per million	wiv . . . working inverse voltage
FET . . . field effect transistor	mtg . . . mounting	prec . . . precision (temperature coefficient, long term stability and/or tolerance)	w/o . . . without
fxd . . . fixed	mV . . . millivolt(s) = 10^{-3} volts		ww . . . wirewound
	μF . . . microfarad(s)		
GaAs . . . gallium arsenide	μs . . . microsecond(s)	R . . . resistor	
GHz . . . gigahertz = 10^{+9} hertz	μV . . . microvolt(s) = 10^{-6} volts	Rh . . . rhodium	
gd . . . guard(ed)	my . . . Mylar ®	rms . . . root-mean-square	* . . . optimum value selected at factory, average value shown (part may be omitted)
Ge . . . germanium		rot . . . rotary	** . . . no standard type number assigned selected or special type
gnd . . . ground(ed)	nA . . . nanoampere(s) = 10^{-9} amperes		
	NC . . . normally closed	Se . . . selenium	® Dupont de Nemours
H . . . henry(ies)	Ne . . . neon	sect . . . section(s)	
Hg . . . mercury	NO . . . normally open	Si . . . silicon	

DESIGNATORS

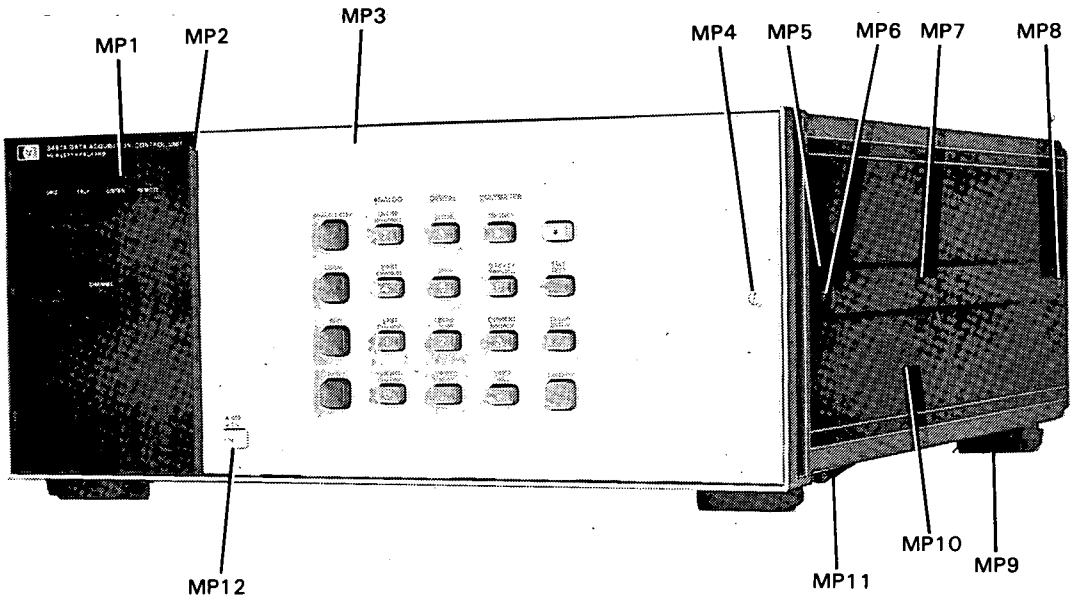
A . . . assembly	FL . . . filter	Q . . . transistor	TS . . . terminal strip
B . . . motor	HR . . . heater	QCR . . . transistor-diode	U . . . microcircuit
BT . . . battery	IC . . . integrated circuit	R(p) . . . resistor(pack)	V . . . vacuum tube, neon bulb, photocell, etc.
C . . . capacitor	J . . . jack	RT . . . thermistor	W . . . cable
CR . . . diode or thyristor	K . . . relay	S . . . switch	X . . . socket
DL . . . delay line	L . . . inductor	T . . . transformer	XDS . . . lampholder
DS . . . lamp	M . . . meter	TB . . . terminal board	XF . . . fuseholder
E . . . misc electronic part	MP . . . mechanical part	TC . . . thermocouple	Y . . . crystal
F . . . fuse	P . . . plug	TP . . . test point	Z . . . network

Table 5-2. Code List of Manufacturers

Mfr.	Manufacturer Name	Address
00000	Any satisfactory supplier	
00494	Addressograph Multigraph Corp	Cleveland OH 44117
01121	Allen-Bradley Co	Milwaukee WI 53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas TX 75222
02111	Spectrol Electronics Corp	City of Ind CA 91745
03508	GE Co Semiconductor Prod Dept	Auburn NY 13201
03888	KDI Pyrofilm Corp	Whippany NJ 07981
04713	Motorola Semiconductor Products	Phoenix AZ 85008
07263	Fairchild Semiconductor Div	Mountain View CA 94042
17856	Siliconix Inc	Santa Clara CA 95054
19701	Mepco/Electra Corp	Mineral Wells TX 76067
20932	Emcon Div ITW	San Diego CA 92129
24546	Corning Glass Works (Bradford)	Bradford PA 16701
27014	National Semiconductor Corp	Santa Clara CA 95051
27167	Corning Glass Works (Wilmington)	Wilmington NC 28401
28480	Hewlett-Packard Co Corporate Hq	Palo Alto CA 94304
3L585	RCA Corp Solid State Div	Somerville NJ
32293	Intersil Inc	Cupertino CA 95014
34335	Advanced Micro Devices Inc	Sunnyvale CA 94086
34649	Intel Corp	Mountain View CA 95051
50088	Mostek Corp	Carrollton TX 75006
50522	General Instr Corp Opto Div	Palo Alto CA 94304
52763	Stettner Electronics Inc	Chattanooga TN 13035
56289	Sprague Electric Co	North Adams MA 01247
72136	Electro Motive Corp	Florence SC 06226
75042	TRW Inc Philadelphia Div	Philadelphia PA 19108

NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.



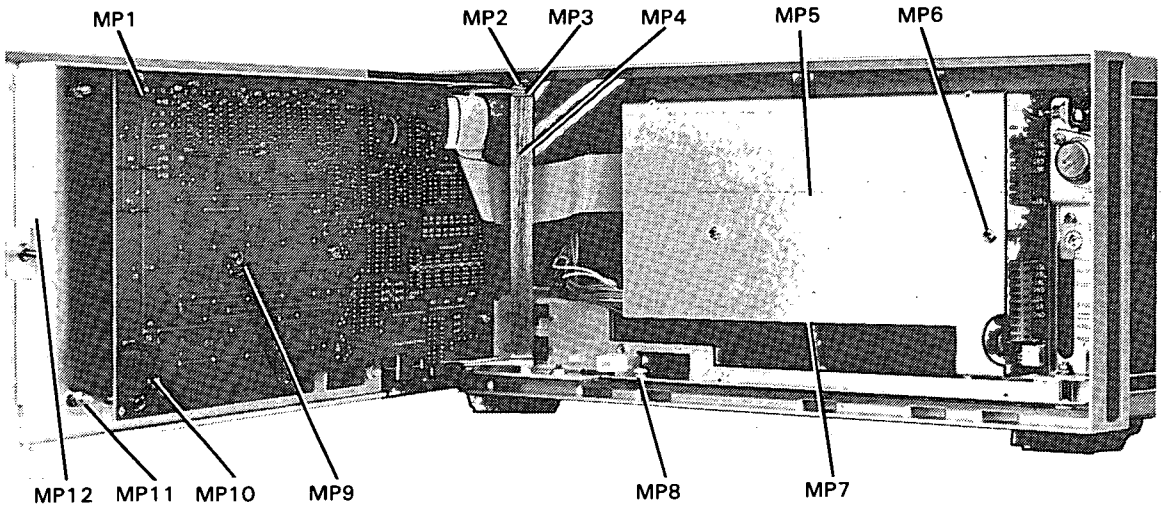
Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	03497-69301	9	1	Window Assembly	ALL
MP2	4040-1644	0	1	Divider Strip	ALL
MP3	03497-60201	0	1	Panel-Dress-Finish	ALL
MP4	1390-0505	8	1	Screw-Captive:M3.5-40	ALL
MP5	5040-7219	8	1	Strap Handle, Cap-Front	ALL
MP6	2680-0172	1	2	Screw-Mach: 10-32x.375	ALL
MP7	5060-9804	3	1	Strap Handle 18 in	ALL
MP8	5040-7220	1	1	Strap Handle, Cap-Rear	ALL
MP9	5040-7201	8	4	Foot	ALL
MP10	5060-9884	9	1	Side Cover, w/Handle Recess	ALL
MP11	1460-1345	5	2	Tilt Stand	ALL
MP12	5041-1907	1	1	Key Cap-Line*	2011A&BELOW
MP12	5041-1682	9	1	Key Cap-Line*	2222A&ABOVE

*See Front Panel Parts for other key cap part numbers.

Figure 5-1. Front and Right Side View of 3497A.

NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.

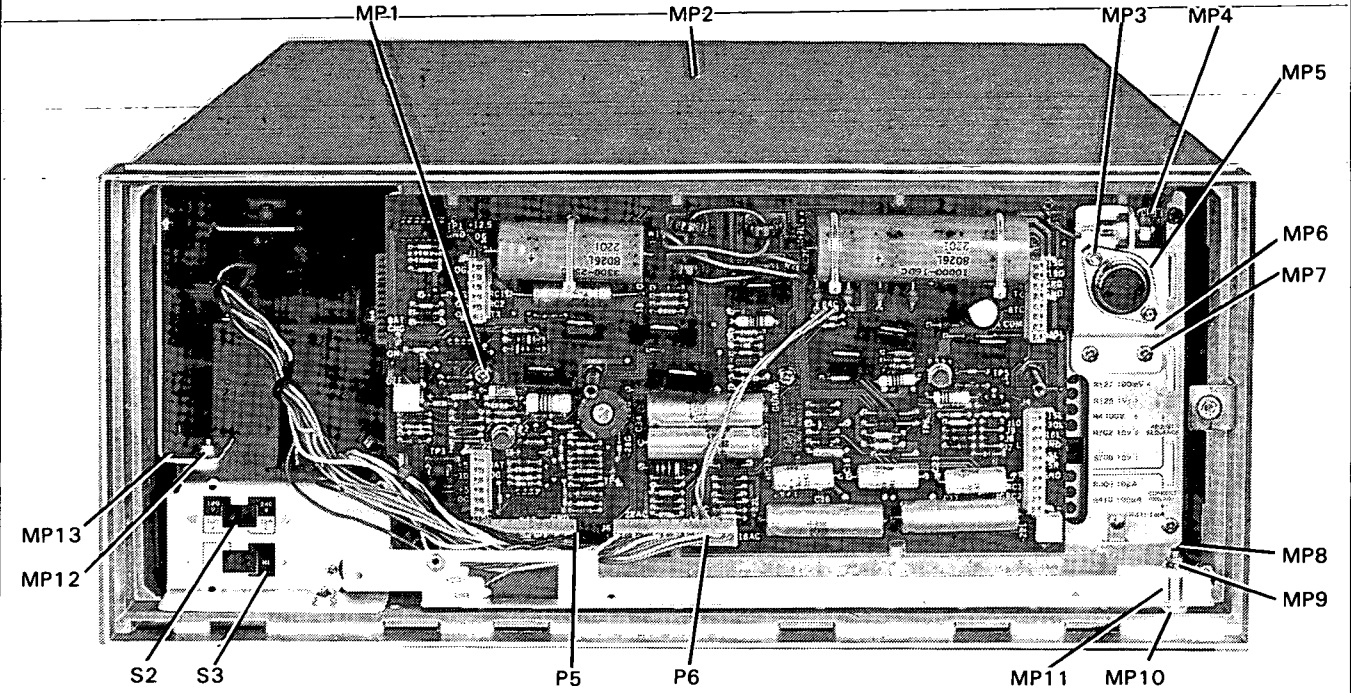


Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	03497-66503	7	1	Front Panel Board	ALL
MP1	7204-0351	5	1	LED Support	ALL
MP2	0380-1259	9	2	Standoff,Hinge	ALL
MP3	3050-1000	2	2	Washer-Teflon	ALL
MP4	1600-0966	2	1	Hinge	ALL
MP5	03497-00604	1	1	Front Shield	2011A&BELOW
MP5	03497-00613	2	1	Front Shield	2222A&ABOVE
MP6	0515-0225	4	2	Screw-Mach:M3.5x0.60x10	ALL
MP7	0460-0203	1	1	Tape-Elec .75ft	ALL
MP8	2360-0286	0	1	Screw-Plastic-Mach:6-32	2011A&BELOW
MP9	0515-0225	4	4	Screw-Mach:M3.5x0.60x10	ALL
MP10	0960-0561	4	1	Audio Transducer	ALL
MP11	0535-0006	1	4	Nut M4x.7	ALL
MP11	2190-0017	4	4	Split Lockwasher	ALL
MP11	3050-0001	1	4	Flat Washer	ALL
MP12	0403-0381	6	1	Bumper,Plastic	ALL

Figure 5-2. Front View with Front Panel Open.

NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.

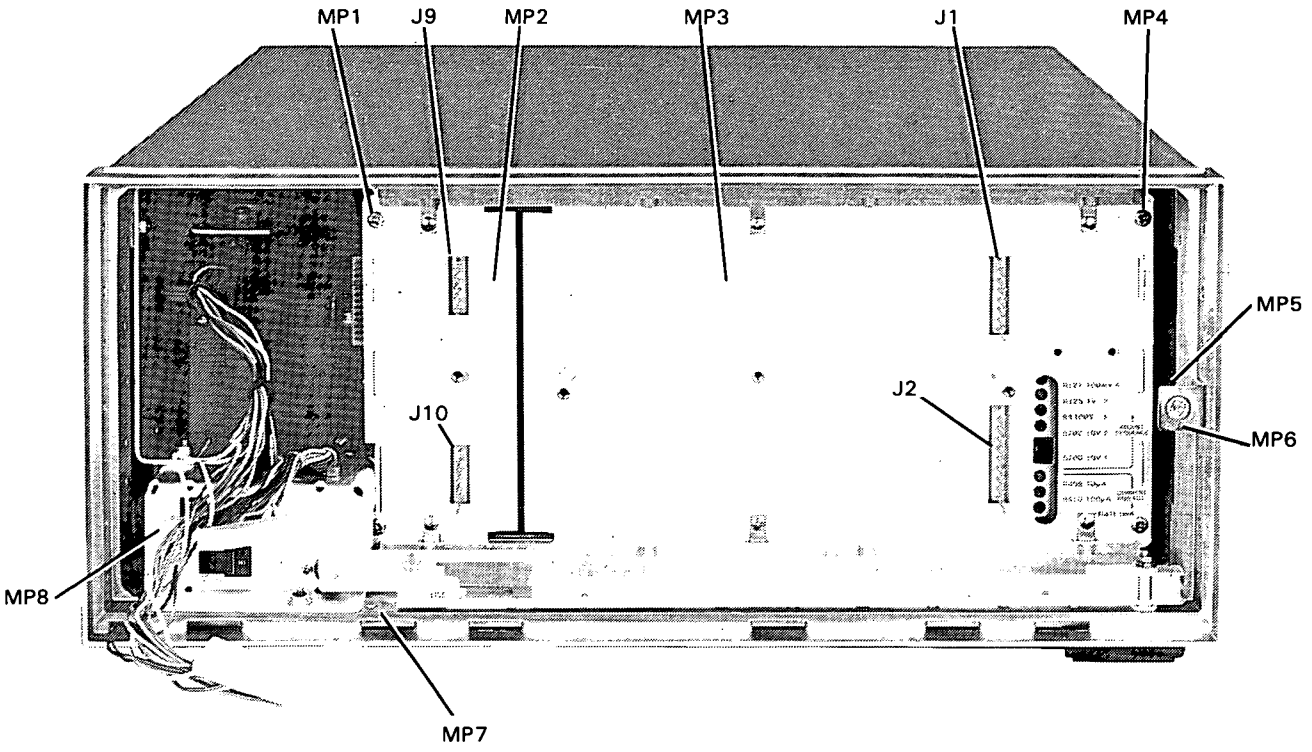


Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	0515-0212	9	2	Screw-Mach:M3.5x0.60x6	ALL
MP2	5060-9835	0	1	Top Cover	ALL
MP3	0535-0004	9	2	Nut Hex:M3.5x.5	ALL
MP3	0515-0054	7	2	Screw-Mach:M3.0x.5	ALL
MP4	2740-0002	4	1	Nut	ALL
MP5	1200-0043	8	1	Insulator-Xstr Thrm-Cndct	ALL
MP6	03497-01101	5	1	Heat Sink	ALL
MP7	0515-0212	9	2	Screw-Mach:M3.5x0.60x6	ALL
MP8	2510-0127	7	1	Screw-Mach:8-32	2011A&BELOW
MP9	2580-0015	9	1	Nut-Hex-Dbl Cham	2011A&BELOW
MP9	2190-0073	2	1	Lockwasher	2011A&BELOW
MP9	0350-0001	7	2	Washer-Flat	2011A&BELOW
MP10	3050-0180	7	2	Washer-Teflon	2011A&BELOW
MP11	0380-0010	8	1	Spacer-Round	2011A&BELOW
MP12	0515-0210	7	3	Screw-Mach:M4x0.70x8	2011A&BELOW
MP13	03497-04102	2	1	Side Plate	2011A&BELOW
MP13	03497-04103	3	2	Side Plate	2222A&ABOVE
P5	1251-5154	9	1	Conn 14P F Pst	ALL
P6	1251-3279	5	1	Conn 12P F Pst	ALL
	1251-3073	7	12	Contact-Conn F	ALL
S2/S3	3101-2298	1	2	Slide Switch-Voltage Select	2011A&BELOW
S2/S3	3101-2298	1	2	Slide Switch-Voltage Select	2222A&ABOVE

Figure 5-3. Front View with Front Panel and Front Shield Removed.

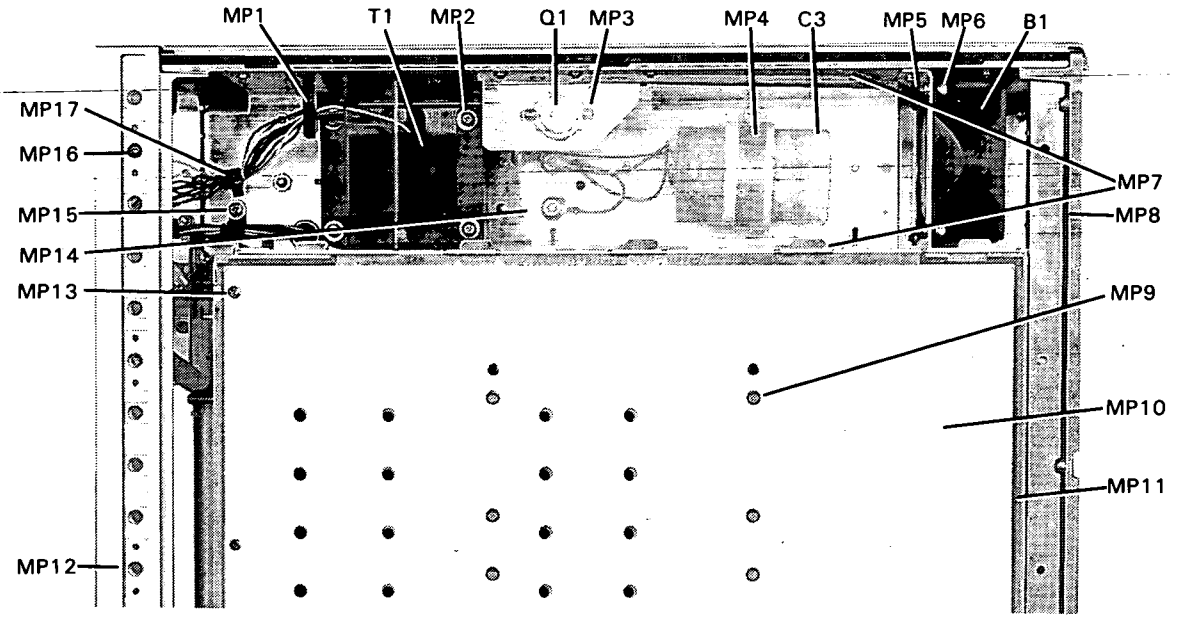
NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.



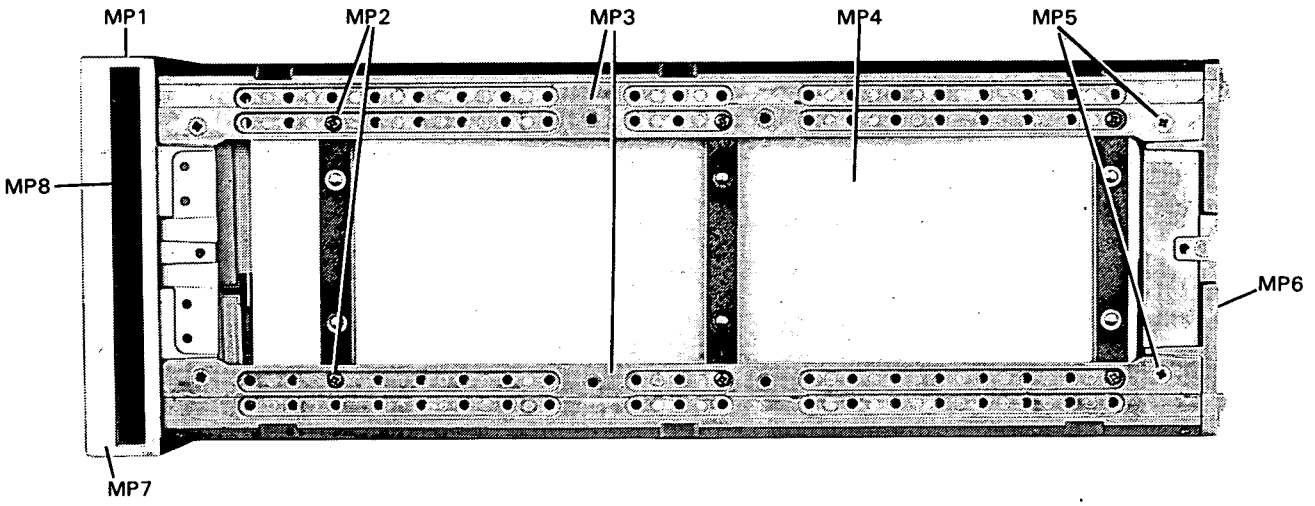
Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	0515-0212	9	2	Screw:Mach:M3.5x0.60x6	ALL
MP2	03497-00101	3	1	Left Deck	ALL
MP3	03497-00102	4	1	Right Deck	ALL
MP4	0515-0212	9	2	Screw-Mach:M3.5x0.60x6	ALL
MP5	0515-0222	1	1	Screw-Mach:M3.5x10Fh,Lk	ALL
MP6	03497-01207	2	1	Panel Latch Bracket	ALL
MP7	03497-01209	4	1	Actuator Bracket: On/Off Sw	2011A&BELOW
MP7	03497-01212	9	1	Pushrod Bracket	2222A&ABOVE
MP7	5041-3180	6	1	Pushrod	2222A&ABOVE
MP7	0515-0218	5	2	Screw-Mach:M3.5x6 LK	2222A&ABOVE
MP8	03497-00103	5	1	Main Deck	2011A&BELOW
MP8	03497-00105	7	1	Main Deck	2222A&ABOVE
J1	1251-6184	7	1	Connector 8-pin M Post Type	ALL
J2	1251-6194	9	1	Connector 10-Pin M Post Type	ALL
J9	1251-6583	0	1	Connector 6-Pin M Post Type	ALL
J10	1251-6583	0	1	Connector 6-Pin M Post Type	ALL

Figure 5-4. Front View of Chassis Showing Left and Right Decks.



Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	1400-1037	6	1	Stand-Off,Short	ALL
MP2	0515-0156	0	4	Screw-Mach:M4.0x55,Pan	ALL
MP2	0390-0006	3	4	Nylon Spacer	ALL
MP2	3050-0071	5	4	Flat Washer	ALL
MP2	2190-0073	2	4	Split Washer	ALL
MP3	0624-0034	4	2	Screw-Tapping:6-20x.625	ALL
MP3	2190-0007	2	2	Internal Washer	ALL
MP3	1200-0043	8	1	Insulator-Xstr Thrm-Cndct	ALL
MP4	1400-0423	2	1	Pipe Clamp	ALL
MP4	0460-0332	7	1	Foam Tape	ALL
MP5	03497-01201	6	1	Fan Bracket	ALL
MP6	0515-0138	8	4	Screw-Mach:M4.0x10 Hex	ALL
MP6	2190-0073	2	4	Split Lock-Washer	ALL
MP7	0403-0302	1	2	Nylon Guide	ALL
MP8	5020-8806	9	1	Rear Frame	ALL
MP9	0515-0224	3	6	Screw-Mach:M3.5x12	ALL
MP10	03497-00606	3	1	Top Shield	ALL
MP11	4040-1685	9	1	Card Cage	ALL
MP12	5020-8805	8	1	Front Frame	ALL
MP13	0515-0260	7	1	Screw	ALL
MP13	2190-0918	4	1	Flat Washer	ALL
MP13	3050-0066	8	1	Flat Washer	ALL
MP13	3050-1027	3	1	Insulator	ALL
MP14	03497-04108	8	1	Air Deflector (Clear Plastic)	ALL
MP15	0515-0053	6	1	Screw-Mach:M4.0x10	ALL
MP16	0515-0222	1	1	Screw-Mach:M3.5x10	ALL
MP17	1400-1036	5	1	Stand-Off,Long	ALL
B1	03497-68501	9	1	Fan	ALL
C3	0180-3026	8	1	Capacitor Fixed 29000μF 20VDC	ALL
Q1	1854-0439	1	1	Transistor-NPN	ALL
T1	9100-4270	7	1	Power Transformer	ALL

Figure 5-5. Top View of Chassis.

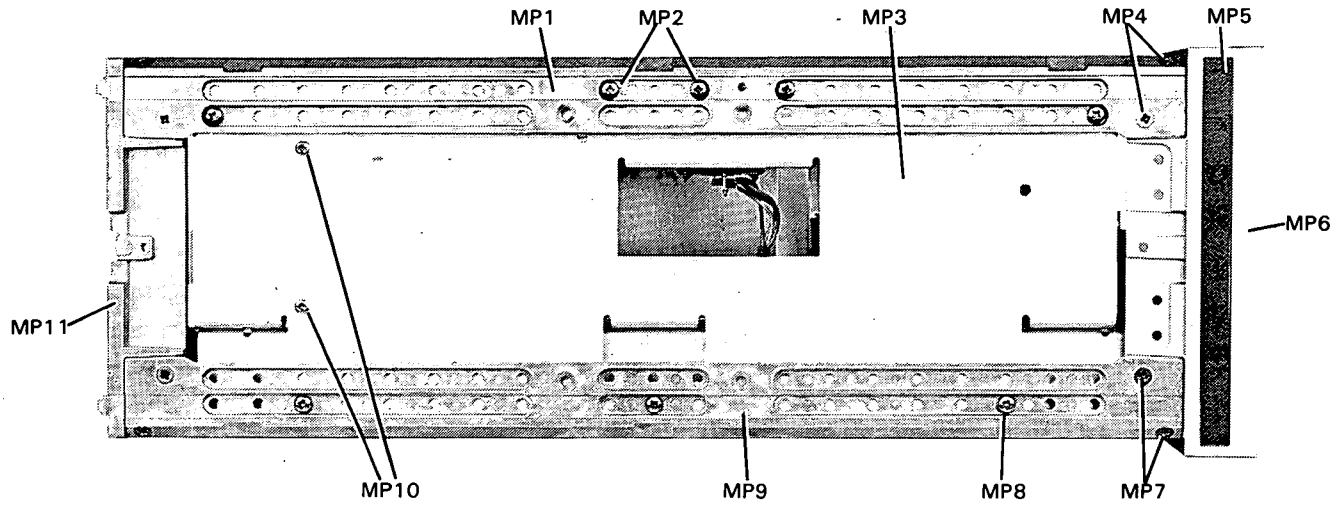


Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	5040-7202	9	1	Top Trim,Front Frame	ALL
MP2	0515-0225	4	6	Screw-Mach:M3.5x 0.60x10	ALL
MP3	5020-8837	6	2	Corner Strut	ALL
MP4	03497-04702	8	1	Right Support	ALL
MP5	2510-0192	6	8	Screw-Mach:8-32x.25	ALL
MP6	5020-8806	9	1	Rear Frame	ALL
MP7	5020-8805	8	1	Front Frame	ALL
MP8	5001-0440	1	1	Trim,Side	ALL

Figure 5-6. Right Side View of Chassis with Side Cover Removed.

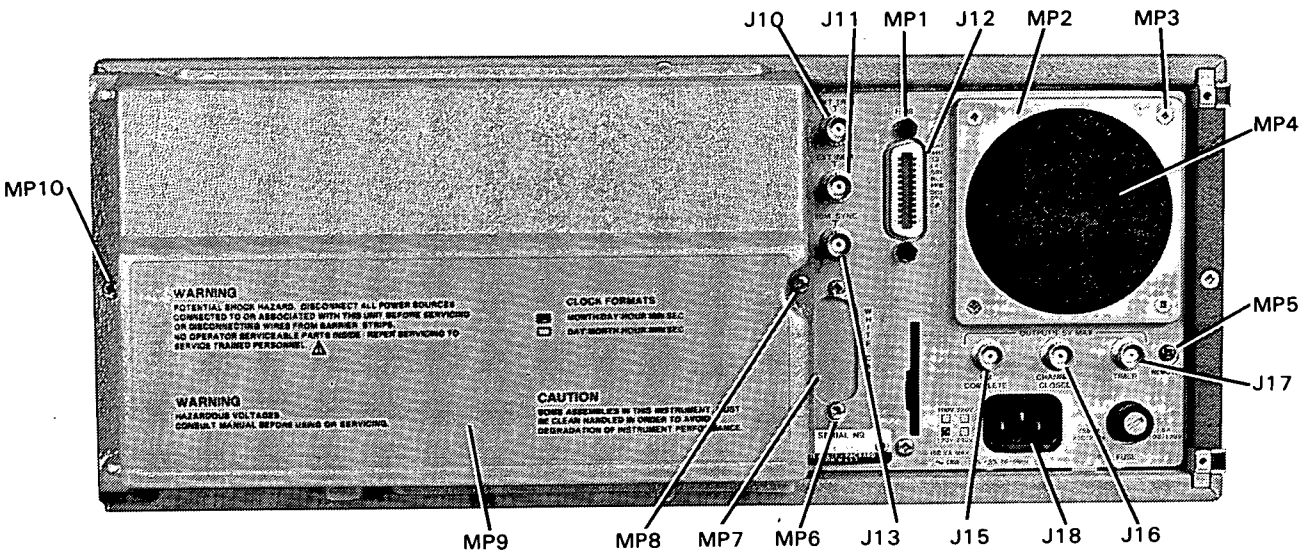
NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.



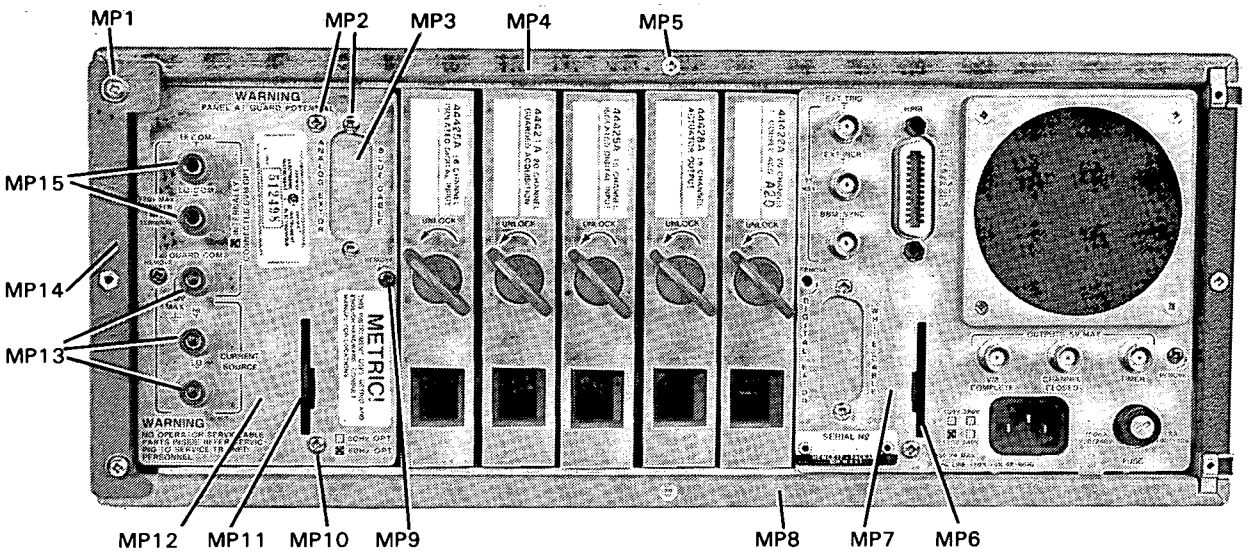
Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	03497-26601	2	1	Corner Strut Modified	ALL
MP2	0515-0210	7	5	Screw-Mach:M4x0.70x8	ALL
MP3	03497-04102	2	1	Side Plate	2011A&BELOW
MP3	03497-04103	3	1	Side Plate	2222A&ABOVE
MP4	2510-0192	6	4	Screw-Mach:8-32x.25	ALL
MP5	5001-0440	1	1	Side Trim	ALL
MP6	5020-8805	8	1	Front Frame	ALL
MP7	2510-0192	6	4	Screw-Mach:8-32x.25	ALL
MP8	0515-0210	9	3	Screw-Mach:M4x0.70x8	ALL
MP9	5020-8837	6	1	Corner Strut	ALL
MP10	0515-0212	9	2	Screw-Mach:m3.5x0.60x6	ALL
MP11	5020-8806	9	1	Rear Frame	ALL

Figure 5-7. Left Side View of Chassis with Side Cover Removed.



Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	0380-1289	5	2	Standoff-Hx M3.5x5	ALL
MP2	5041-2385	1	1	Housing, Fan,Filter	ALL
MP3	0515-0211	8	4	Screw-Mach:M3x0.50x6	ALL
MP4	3150-0233	3	1	FM-Polyu .25T	ALL
MP4	3150-0232	2	1	Filter-Air,SS	ALL
MP5	0515-0224	3	1	Screw-Mach:M3.5x12	ALL
MP5	0900-0010	2	1	O Ring Retainer .101 ID	ALL
MP6	0515-0212	9	2	Screw-Mach:M3.5x0.60x6	ALL
MP7	03497-04107	7	1	Plate-Butch	ALL
MP8	0515-0260	7	1	Screw-Mach:M3.5x0.60x16	ALL
MP8	0900-0010	2	1	O Ring Retainer .101 ID	ALL
MP9	4040-1859	9	1	Rear Cover	ALL
MP10	0515-0212	9	1	Screw-Mach:M3.5x0.60x6	ALL
MP10	0900-0010	2	1	O Ring Retainer .101 ID	ALL
J10,11 13,15 16,17	1250-0083	1	6	Connector-RF BNC F	ALL
J12	8120-3280	8	1	Cable Assy-HP-IB	ALL
J12	8120-3399	0	1	Cable Assy-RS23/423	ALL
J18	9100-3121	5	1	Line Filter	ALL

Figure 5-8. Rear View with Rear Cover Installed.

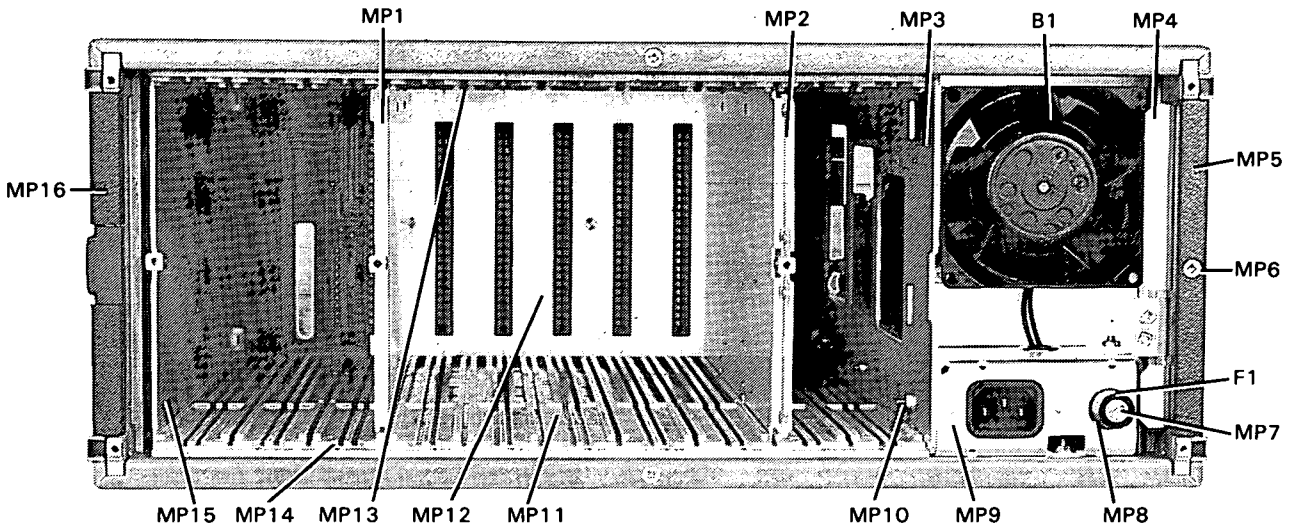


Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	2360-0195	0	2	Screw-Mach:6-32	ALL
MP1	2190-0198	2	2	Split Lock-Washer	ALL
MP1	3050-0066	8	2	Flat Washer	ALL
MP2	0515-0212	9	3	Screw-Mach:M3.5x0.60x6	ALL
MP3	03497-04107	7	1	Plate-Butch	ALL
MP4	5060-9835	0	1	Top Cover	ALL
MP5	0570-1171	7	1	Screw-Cover Mtg	ALL
MP5	0510-0043	4	1	Ring-Ret .141 Dia	ALL
MP6	5040-6843	2	1	PC Board Extractor	ALL
MP7	03497-01204	9	1	Control Bracket	ALL
MP8	5060-9847	4	1	Bottom Cover	ALL
MP9	0515-0224	3	3	Screw-Mach:M3.5x12	ALL
MP9	0900-0010	2	2	O Ring Retainer .101 ID	ALL
MP10	0515-0212	9	1	Screw-Mach:M3.5x0.60x6	ALL
MP11	5040-6843	2	1	PC Board Extractor	ALL
MP12	03497-00204	7	1	Rear Panel A/D	ALL
MP13	1510-0091	3	3	Bndg Post Assy	ALL
MP14	03498-01204	0	1	Bracket-Rear Cover	ALL
MP15	1510-0111	8	2	Bndg Post Assy	ALL

Figure 5-9. Rear View with Rear Cover Removed.

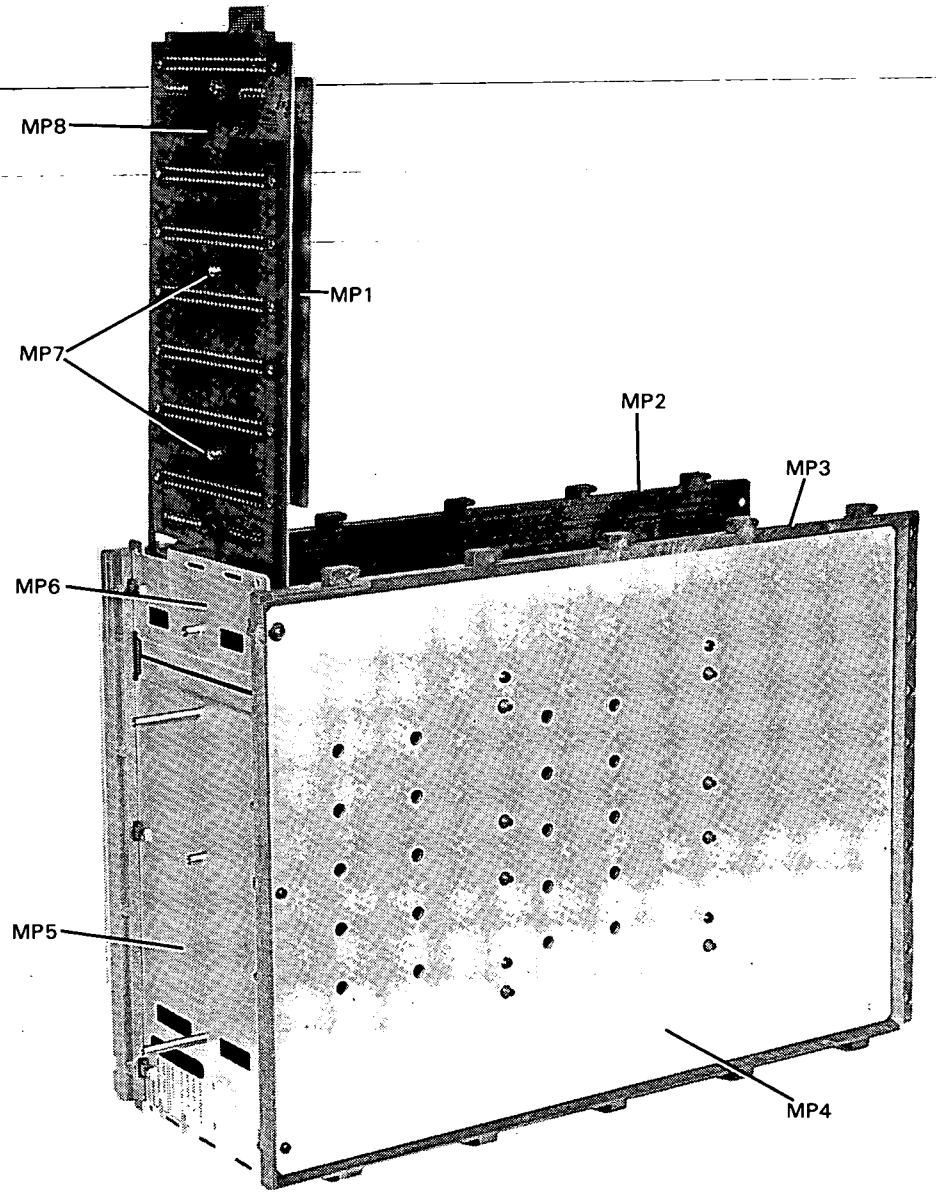
NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.



Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	03497-00603	0	1	Right Shield	ALL
MP2	03497-00602	9	1	Left Shield	ALL
MP3	03497-04701	7	1	Left Support	ALL
MP4	03497-01206	1	1	Rear Bracket	2011A&BELOW
MP4	03497-01211	8	1	Rear Bracket	2222A&ABOVE
MP4	2510-0286	9	2	Screw-Mach:8x.188 LK	ALL
MP5	5060-9862	3	1	Side Cover-Standard	ALL
MP6	0570-1171	7	1	Screw-Cover Mtg	ALL
MP6	0510-0043	4	1	Ring-Ret .141 Dia	ALL
MP7	2110-0565	9	1	Fuseholder Cap	ALL
MP8	2110-0564	8	1	Fuseholder Body	ALL
MP8	2110-0569	3	1	Fuseholder Nut	ALL
MP8	1400-0900	9	1	Rubber Washer	ALL
MP9	03497-00103	5	1	Main Deck	2011A&BELOW
MP9	03497-00105	7	1	Main Deck	2222A&ABOVE
MP10	0515-0210	7	3	Screw-Mach:M4x0.70x8	ALL
MP11	4040-1685	9	1	Half Card Cage (Bottom)	ALL
MP12	03497-00605	2	1	Connector Shield	ALL
MP13	4040-1685	9	1	Half Card Cage (Top)	ALL
MP14	7120-0373	3	1	Label	ALL
MP15	03497-04702	8	1	Right Support	ALL
MP16	5060-9884	9	1	Side Cover,w/Handle Recess	ALL
B10	3497-68501	9	1	Fan	ALL
F1	2100-0043	8	1	Fuse 1.5A 250V (120V option)	ALL
F1	2100-0063	2	1	Fuse .75A 250V (220V option)	ALL

Figure 5-10. Rear View of Chassis.

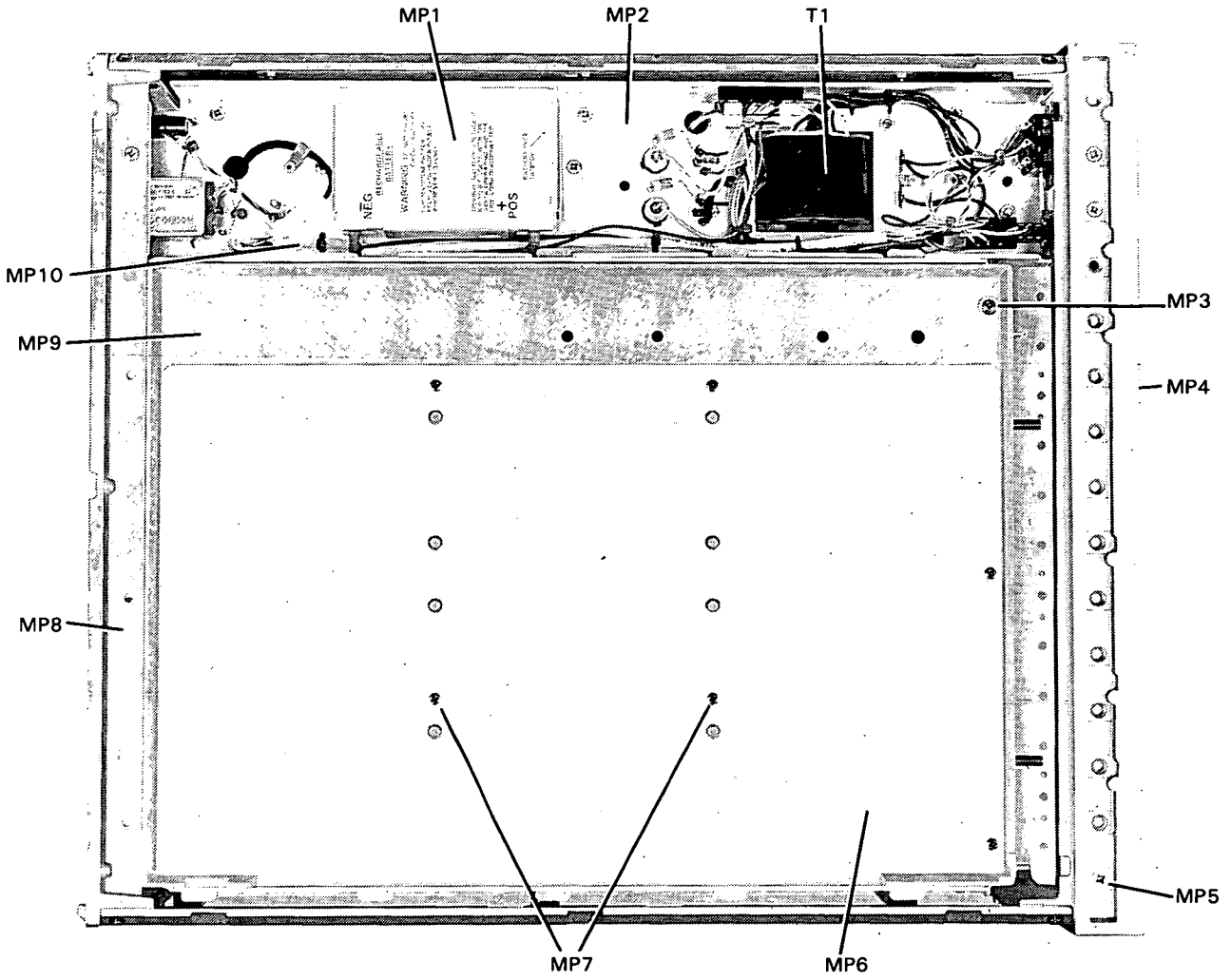


Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	03497-00605	2	1	Connector Shield	ALL
MP2	4040-1685	9	1	Bottom Card Cage	ALL
MP3	4040-1685	9	1	Top Card Cage	ALL
MP4	03497-00606	3	1	Top Shield	ALL
MP5	03497-00102	4	1	Right Deck	ALL
MP6	03497-00101	3	1	Left Deck	ALL
MP7	0515-0212	9	3	Screw-Mach:M3.5x0.60x6	ALL
MP8	03497-66504	8	1	Mother Board	ALL

Figure 5-11. View of Mother Board Assembly Positioned for Insertion into Card Cage.

NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.

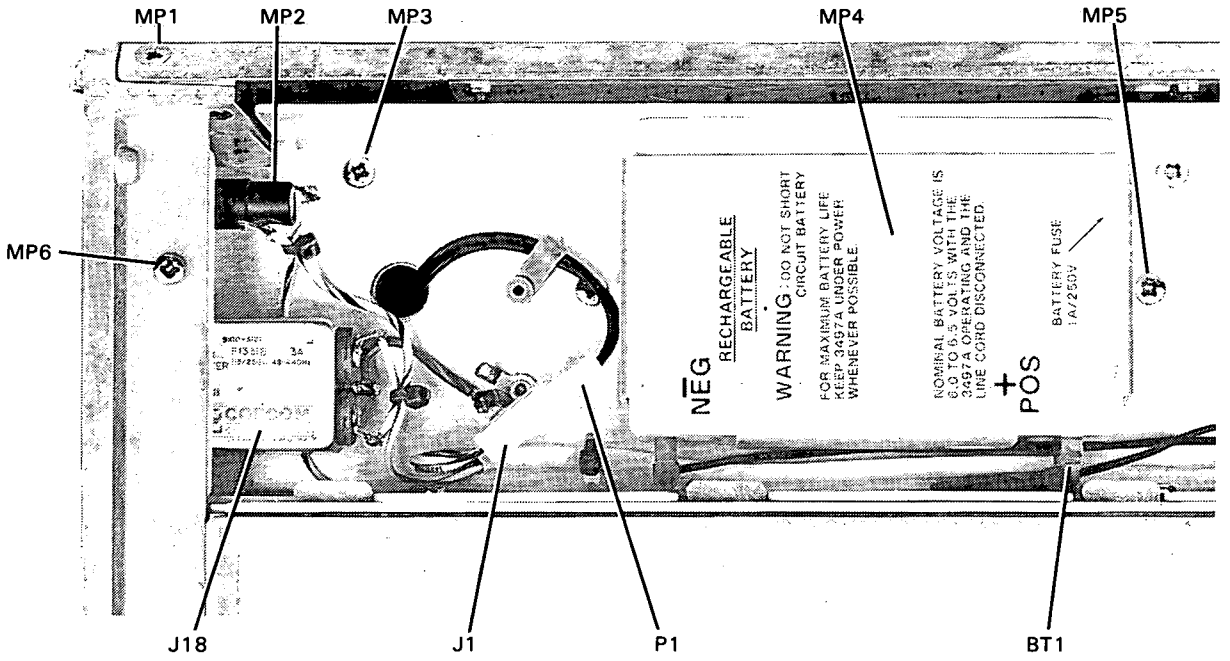


Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	03497-01205	0	1	Battery Bracket	2011A&BELOW
MP1	03497-01210	7	1	Battery Bracket	2222A&ABOVE
MP2	03497-00103	5	1	Main Deck	2011A&BELOW
MP2	03497-00105	7	1	Main Deck	2222A&ABOVE
MP3	0515-0224	3	1	Screw-Mach:M3.5x12	ALL
MP3	2190-0918	4	1	Split Lockwasher	ALL
MP3	3050-0066	8	1	Flat Washer	ALL
MP4	5020-8805	8	1	Front Frame	ALL
MP5	2510-0127	7	1	Screw-Mach:8-32 FH	ALL
MP6	03497-00601	8	1	Bottom Shield	ALL
MP7	0515-0224	3	6	Screw-Mach:M3.5x0.60x12	ALL
MP8	5020-8806	9	1	Rear Frame	ALL
MP9	4020-1685	9	1	Card Cage	ALL
MP10	03497-61603	8	1	Battery Cable	2011A&BELOW
MP10	03497-61612	9	1	Battery Cable	2222A&ABOVE
T1	9100-4270	7	1	Power Transformer	ALL

Figure 5-12. Bottom View of Chassis.

NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.

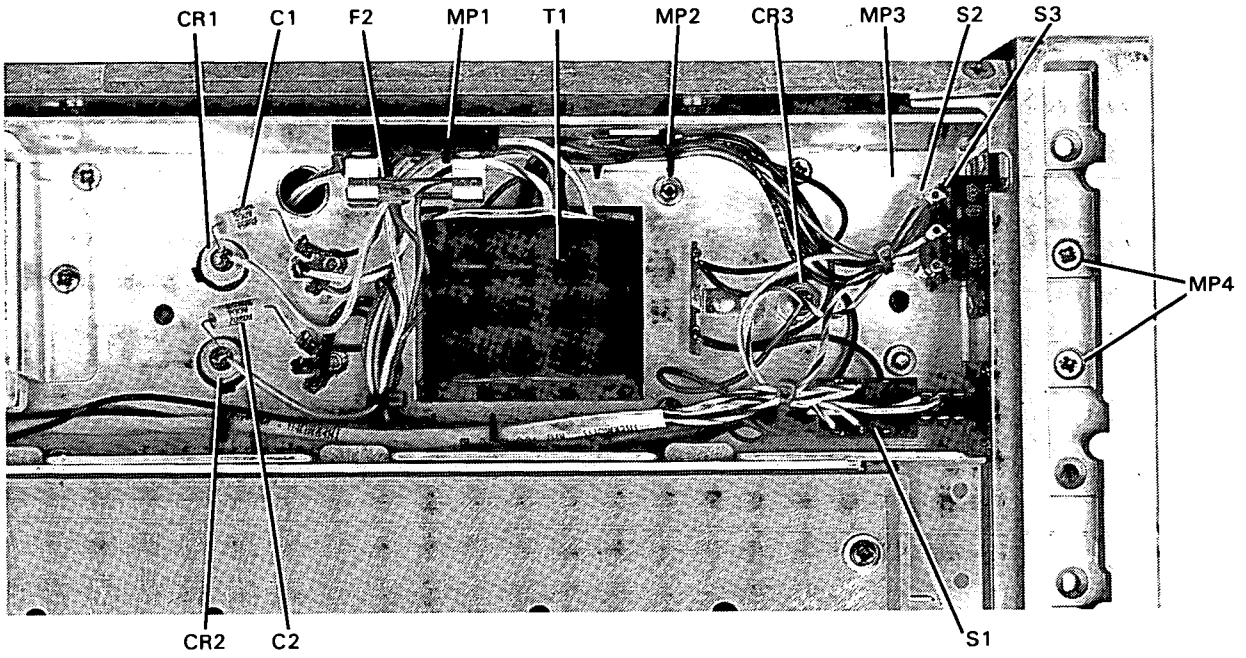


Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	2510-0192	6	4	Screw-Mach:8-32x.250	ALL
MP2	2110-0564	8	1	Fuseholder Body	ALL
MP3	0515-0210	7	3	Screw-Mach:M4x0.70x8	ALL
MP4	03497-01205	0	1	Battery Bracket	2011A&BELOW
MP4	03497-01210	7	1	Battery Bracket	2222A&ABOVE
MP5	0515-0210	7	2	Screw-Mach:M4x0.70x8	ALL
MP6	0515-0225	4	1	Screw-Mach:M3.5x0.60x10	ALL
MP6	0535-0007	2	1	Nut Hx M3.5x0.6	ALL
BT1	1420-0233	4	1	Battery-6V Rechargeable	ALL
J1	1251-3977	0	1	Conn 2 Pin UT	ALL
J18	9100-3121	5	1	Line Filter-22 TML	ALL
P1	1251-3982	7	1	Conn 2 Pin F UT	ALL

Figure 5-13. Bottom View of Rear Portion of Main Deck.

NOTE

The picture in this figure applies to 3497A's with Serial Prefixes 2011A and below. For other prefixes, refer to the Prefix column in the table (located in this figure) to determine the correct part numbers for the other prefixes.



Reference Designator	-hp- Part Number	C D	Qty	Description	Prefix
MP1	1400-0008	9	1	Fuseholder Block	ALL
MP2	1400-0783	7	2	Cable Clamp .25x.483	ALL
MP3	03497-00103	5	1	Main Deck	2011A&BELOW
MP3	03497-00105	7	1	Main Deck	2222A&ABOVE
MP4	0515-0222	1	2	Screw-Mach:M3.5x10	ALL
C1/C2	0160-0162	5	2	Capacitor-Fxd .022UF ± 10%	ALL
CR1/CR2	1901-0496	1	1	Diode-Pwr Rect 100V 12A	ALL
	2740-0003	5	2	Nut-Diode	ALL
CR3	9102-1232	7	1	Diode-Znr 5.6V	ALL
F2	2110-0001	8	1	Fuse 1A 250V	ALL
S1	3100-0481	8	1	Switch-Pushbutton	ALL
	0515-0226	5	2	Screw-Mach:M2.5x6	ALL
S2/S3	3101-2298	1	1	Switch-Slide	ALL
T1	9100-4270	7	1	Power Transformer	ALL

Figure 5-14. Bottom View of Front Portion of Main Deck.

Table 5-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	03497-66533	3	1	SERIAL I/O & OUTGUARD CONTROLLER ASSY	28480	03497-66533
	03497-80232	9		A1 & A17 PC ASSY W/BACK PANEL	28480	03497-80232
A1C1	0180-0309	4	19	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C2	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C3	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C4	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C5	0160-4814	2	1	CAPACITOR-FXD 150PF +-5% 100VDC CER	28480	0160-4814
A1C6	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C7	0160-3847	9	3	CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
A1C8	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C9	0160-4810	8	2	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A1C10	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C11	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A1C12	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C13	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C14	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C15	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C16	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C18	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C19	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C20	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C21	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C22	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C23	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C24	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A1C26	0160-0571	0	5	CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A1C27	0160-0570	9	1	CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A1C28	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
A1C29	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
A1C30	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A1C31	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A1C32	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A1C33	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A1CR1	1901-0040	1	12	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR6	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR8	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR9	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR10	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR11	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR12	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR13	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR14	1902-0052	7	1	DIODE-ZNR 6.81V 2% DO-35 PD=.4W	28480	1902-0052
A1CR15	1902-0631	8	2	DIODE-ZNR 1N5351B 14V 5% PD=5W TC=+75%	04713	1N5351B
A1CR16	1902-0631	8		DIODE-ZNR 1N5351B 14V 5% PD=5W TC=+75%	04713	1N5351B
A1J1	1251-7447	7	1	CONNECTOR-34 PIN, MALE	28480	1251-7447
A1J3	1251-6263	3	2	CONNECTOR-14 PIN, FEMALE POST	28480	1251-6263
A1J4	1251-6263	3		CONNECTOR-14 PIN, FEMALE POST	28480	1251-6263
A1J10	1250-0083	1	6	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A1J11	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A1J13	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A1J15	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A1J16	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A1J17	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A1JM1	8159-0005	0	5	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A1JM4	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A1JM6	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A1JM9	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A1JM10	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
A1L1	9100-3547	9	1	INDUCTOR RF-CH-MLD 4.3UH 5% .166DX.385LG	28480	9100-3547
A1L2	9100-3551	5	1	INDUCTOR RF-CH-MLD 1UH 5% .166DX.385LG	28480	9100-3551
A1MP2	0515-0165	1	2	SCREW-MACH M3.5 X 0.6 12MM-LG PAN-HD	28480	0515-0165
A1MP3	5041-2385	1	1	HOUSING FAN-FILTER	28480	5041-2385
A1MP4	0515-0219	6	4	SCREW-MACH M3 X 0.5 6MM-LG 90-DEG-FLH-HD	00000	ORDER BY DESCRIPTION
A1MP5	3150-0233	3	1	FOAM-POLYU .25T	28480	3150-0233
	3150-0232	2	1	FILTER-AIR 3.25 DIA	28480	3150-0232
A1MP6	0515-0224	3	1	SCREW-MACH M3.5 X 0.6 12MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1MP7	0515-0210	7	2	SCREW-MACH M4 X 0.7 8MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1MP8	03497-04107	7	1	BUTCH PLATE	28480	03497-04107
A1MP9	0515-0212	9	4	SCREW-MACH M3.5 X 0.6 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1MP10	5040-6843	2	1	EXTRACTOR-PC BOARD	28480	5040-6843

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R1	0683-2225	3	4	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R2	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R3	0683-1015	7	7	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R4	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R5	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R6	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R7	0683-3325	6	3	RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A1R9	0683-1035	1	5	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R10	0683-1025	9	10	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R11	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R12	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R14	0683-4725	2	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A1R15	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R16	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R17	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R18	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A1R19	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R20	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R21	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R22	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R23	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A1R24	0683-1055	5	1	RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
A1R25	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R26	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R28	0683-3025	3	1	RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A1R29	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R30	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R31	0698-4485	2	3	RESISTOR 23.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2322-F
A1R32	0698-4485	2		RESISTOR 23.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2322-F
A1R33	0683-8235	7	1	RESISTOR 82K 5% .25W FC TC=-400/+800	01121	CB8235
A1R34	0698-4485	2		RESISTOR 23.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2322-F
A1R35	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R36	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R37	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R38	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A1R39	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A1R40	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R41	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R42	0683-6225	1	1	RESISTOR 6.2K 5% .25W FC TC=-400/+700	01121	CB6225
A1R43	0698-3132	4	1	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A1R44	0683-4735	4	2	RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
A1R45	0683-4735	4		RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
A1R46	0683-2025	1	1	RESISTOR 2K 5% .25W FC TC=-400/+700	01121	CB2025
A1R47	0687-1501	4	2	RESISTOR 15 10% .5W CC TC=0+412	01121	EB1501
A1R48	0687-1501	4		RESISTOR 15 10% .5W CC TC=0+412	01121	EB1501
A1R49	0683-5615	1	1	RESISTOR 560 5% .25W FC TC=-400/+600	01121	CB5615
A1RP1	1810-0269	3	2	NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A1RP2	1810-0136	3	1	NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0136
A1RP3	1810-0307	0	1	NETWORK-CNDCT MODULE DIP; 16 PINS; 0.100	28480	1810-0307
A1RP4	1810-0281	9	1	NETWORK-RES 10-SIP100.0K OHM X 9	01121	210A104
A1RP5	1810-0269	3		NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A1RP6	1810-0368	3	1	NETWORK-RES 6-SIP10.0K OHM X 5	01121	206A103
A1RP7	1810-0566	3	1	RESISTOR SIP 15K OHM	28480	1810-0566
A1RP8	1810-0552	7	1	RESISTIVE NETWORK-SIP 6.0K OHM	28480	1810-0552
A1S1	3101-1973	7		WITCH-SLIDE 7-14A 50V	28480	3101-1973
A1S2	3101-1860	1		WITCH-D.I.P.	28480	3101-1860
A1TP1-A1TP29	1251-0600	0	29	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A1U1	1820-2594	2	1	IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
A1U2	1820-1759	9	3	IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A1U3	1820-1491	6	2	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A1U4	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
A1U5	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U6	1820-2117	5	2	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
A1U7	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
A1U8	1820-2443	0	1	IC UART	28480	1820-2443
A1U10	1820-2036	7	1	IC DRVR NMOS CLOCK DRVR	04713	MC6875L
A1U11	1820-2137	9	1	IC MICPROC NMOS 8-BIT	04713	MC68A00P
A1U13	1820-1199	1	3	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U14	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U15	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A1U16	1820-1826	1	1	IC-MASKED ROM	01295	SN75112N
A1U18	1820-1209	4	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N

See introduction to this section for ordering information
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Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U19	1820-1112	8	6	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A1U20	1818-1825	5	1	IC-MASKED ROM	50088	MK36000N-5 MASKED
A1U21	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A1U22	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U23	1820-1205	0	1	IC GATE TTL LS AND DUAL 4-INP	01295	SN74LS21N
A1U24	1818-1827	7	1	IC-MASKED ROM	50088	MK36000N-5 MASKED
A1U25	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A1U26	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U28	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U29	1820-1491	6		IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A1U30	1818-1213	5	1	IC-MK4118P-4 8K	50088	MK4118AP-4
A1U31	1820-1216	3	4	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U32	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U33	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U34	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
A1U35	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U36	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U37	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A1U39	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U40	1820-1975	1	1	IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN	01295	SN74LS165N
A1U41	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A1U42	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A1U43	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A1U44	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A1U45	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U46	1820-0514	2	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7426N
A1U49	1821-0001	4	1	TRANSISTOR ARRAY 14-PIN PLSTC DIP	3L585	CA3046
A1U50	1820-1433	6	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A1U51	1858-0054	4	1	TRANSISTOR ARRAY 16-PIN PLSTC DIP	28480	1858-0054
A1U61	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U62	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U63	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A1W1	8120-3399	0	1	CABLE-RS232/423	28480	8120-3399
	13222-60001	8	1	US MODEM CABLE ASSEMBLY	28480	13222-60001
A1Y1	0410-1382	4	1	CRYSTAL	28480	0410-1382
				A1 ASSY MISC. PARTS		
	0515-0211	8	2	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
	0590-1025	2	2	THREADED INSERT	00000	ORDER BY DESCRIPTION
	1200-0473	8	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0473
	8150-4074	3	1	WIRE-STRANDED (GRN)	28480	8150-4074
	8150-4073	2	1	WIRE-STRANDED (RED)	28480	8150-4073
	03497-00208	1	40	1PANEL CONTROL	28480	03497-00208
	03497-01208	3	50	1BRACKET CONTROL	28480	03497-01208
	0380-1055	3	10	4SPACER,SNAP-IN .5 LG.	00000	ORDER BY DESCRIPTION
	5000-9043	6	20	1EXTRACTOR-PIN	28480	5000-9043
	7122-0058	5	30	1PLATE-SERIAL HP (USA)	28480	7122-0058

See introduction to this section for ordering information
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Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	03497-66502	6	1	INGUARD CONTROL ASSEMBLY	28480	03497-66502
A2C1	0180-0309	4	5	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A2C2	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A2C3	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A2C4	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A2C5	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A2C100	0180-0291	3	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A2C201	0160-2257	3	1	CAPACITOR-FXD 10PF +-5% 500VDC CER 0+-60	28480	0160-2257
A2C202	0121-0046	2	1	CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A2C203	0160-4807	3	1	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
A2CR1	1901-0040	1	3	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR6	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2E1	1970-0084	8	1	TUBE-ELECTRON SURGE V PTCTR	28480	1970-0084
A2J1	1251-4813	5	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-4813
A2J2	1251-4047	7	3	CONNECTOR 3-PIN M POST TYPE	28480	1251-4047
A2J3	1251-4047	7		CONNECTOR 3-PIN M POST TYPE	28480	1251-4047
A2J4	1251-4484	6	1	CONNECTOR 4-PIN M POST TYPE	28480	1251-4484
A2J5	1251-4047	7		CONNECTOR 3-PIN M POST TYPE	28480	1251-4047
A2J7	1200-0583	1	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0583
A2P1	1258-0141	8	5	JUMPER-REM	28480	1258-0141
A2P2	1258-0141	8		JUMPER-REM	28480	1258-0141
A2P3	1258-0141	8		JUMPER-REM	28480	1258-0141
A2P4	1258-0141	8		JUMPER-REM	28480	1258-0141
A2P5	1258-0141	8		JUMPER-REM	28480	1258-0141
A2R100	0683-5125	8	2	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A2R101	0683-1025	9	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A2R102	0683-1035	1	1	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R103	0683-3325	6	9	RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R104	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R105	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A2R106	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R107	0683-5125	8		RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A2R108	0698-8776	2	1	RESISTOR 10 5% .25W CC TC=-400/+500	28480	0698-8776
A2R201	1810-0279	5	2	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
A2R202	0757-0437	2	2	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A2R203	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
A2R204	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A2R206	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R207	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R208	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R209	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R210	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R211	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R212	0757-0410	1	2	RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R213	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A2R214	0698-4443	2	1	RESISTOR 4.53K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4531-F
A2R215	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R216	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2U1	1820-1432	5	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
A2U2	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A2U3	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A2U4	1820-1202	7	2	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A2U5	1820-1445	0	1	IC LCH TTL LS 4-BIT	01295	SN74LS375N
A2U6	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A2U7	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A2U8	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U110	1820-1272	1	1	IC BFR TTL LS NOR QUAD 2-INP	01295	SN74LS33N
A2U111	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A2U112	1820-1759	9	2	IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A2U113	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U114	1820-1433	6	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A2U115	1820-1975	1	1	IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN	01295	SN74LS165N
A2U116	1821-0001	4	1	TRANSISTOR ARRAY 14-PIN PLSTC DIP	3L585	CA3046
A2U117	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A2U118	1820-0583	5	1	IC GATE TTL L NAND QUAD 2-INP	01295	SN74L00N
A2U119	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U120	1820-0514	2	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7426N
A2U201	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N

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Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2U202	1820-1491	6	1	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A2U203	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A2U204	1820-2532	8	1	IC-MICROPROCESSOR NMOS 8-BIT	28480	1820-2532
A2U205	1820-2177	7	1	IC MICPROC-ACCESS NMOS 4-BIT	34649	P8243
A2U206	1820-1426	7	2	IC DCDR TTL LS BCD-TO-DEC 4-TO-10-LINE	01295	SN74LS145N
A2U207	1820-1483	6	3	IC GATE CMOS OR QUAD 2-INP	3L585	CD4071BE
A2U208	1820-1426	7		IC DCDR TTL LS BCD-TO-DEC 4-TO-10-LINE	01295	SN74LS145N
A2U209	1820-1483	6		IC GATE CMOS OR QUAD 2-INP	3L585	CD4071BE
A2U210	1820-1483	6		IC GATE CMOS OR QUAD 2-INP	3L585	CD4071BE
A2U211	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U212	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A2U213	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U214	1826-0412	1	1	IC COMPARATOR PRCN DUAL 8-DIP-P PKG	27014	LM393N
A2Y1	0410-1226	5	1	CRYSTAL-QUARTZ 5.85 MHZ HC-25/U-HLDR	28480	0410-1226
A2Y1	0410-1225	4	1	CRYSTAL-QUARTZ 4.875 MHZ HC-25/U-HLDR	28480	0410-1225
				A2 ASSY MISC. PARTS		
	7175-0057	5	22	WIRE JUMPER (J10-J31)	28480	7175-0057
	1200-0546	6	1	SOCKET-XTAL 2-CONT HC-25/U DIP-SLDR	28480	1200-0546
	1200-0659	2	1	SOCKET-IC 40-CONT DIP-SLDR	28480	1200-0659

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	03497-66503	7	1	FRONT PANEL ASSEMBLY	28480	03497-66503
A3C1	0180-0309	4	13	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C2	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C3	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C4	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C5	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C6	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C7	0180-1743	2	1	CAPACITOR-FXD .1UF+-10% 35VDC TA	56289	150D104X9035A2
A3C8	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A3C10	0180-0291	3	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A3C11	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C12	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C13	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C14	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C15	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C16	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C17	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3CR1	1990-0757	4	20	LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR2	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR3	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR4	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR5	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR6	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR7	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR8	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR9	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR10	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR11	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR12	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR13	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR14	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR15	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR16	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR17	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR18	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR19	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR20	1990-0757	4		LED-LAMP LUM-INT=1MCD IF=35MA-MAX BVR=5V	50522	MV57124
A3CR21	1990-0547	0	1	LED-LAMP LUM-INT=2MCD IF=20MA-MAX BVR=5V	28480	5082-4684,SEL IV
A3CR22	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR23	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3DS1	1990-0699	3	3	LED-LIGHT BAR MODULE LUM-INT=7MCD	28480	1LM1-2350
A3DS2	1990-0619	7	3	DISPLAY-NUM-SEG 1-CHAR .3-H	28480	5082-7613
A3DS3	1990-0619	7		DISPLAY-NUM-SEG 1-CHAR .3-H	28480	5082-7613
A3DS4	1990-0619	7		DISPLAY-NUM-SEG 1-CHAR .3-H	28480	5082-7613
A3DS5	1990-0699	3		LED-LIGHT BAR MODULE LUM-INT=7MCD	28480	1LM1-2350
A3DS6	1990-0649	3	1	DISPLAY-NUM-SEG	28480	5082-7616
A3DS7	1990-0631	3	6	LED-LAMP LUM-INT=1MCD IF=30MA-MAX BVR=5V	28480	HLMP-0501
A3DS8	1990-0631	3		LED-LAMP LUM-INT=1MCD IF=30MA-MAX BVR=5V	28480	HLMP-0501
A3DS9	1990-0631	3		LED-LAMP LUM-INT=1MCD IF=30MA-MAX BVR=5V	28480	HLMP-0501
A3DS10	1990-0631	3		LED-LAMP LUM-INT=1MCD IF=30MA-MAX BVR=5V	28480	HLMP-0501
A3DS11	1990-0631	3		LED-LAMP LUM-INT=1MCD IF=30MA-MAX BVR=5V	28480	HLMP-0501
A3DS12	1990-0631	3		LED-LAMP LUM-INT=1MCD IF=30MA-MAX BVR=5V	28480	HLMP-0501
A3DS13	1990-0759	6	1	LED-LIGHT BAR MODULE LUM-INT=3MCD	28480	HLMP-2620
A3DS14	1990-0696	0	3	LED-LIGHT BAR MODULE LUM-INT=3MCD	28480	1LM1-2300
A3DS15	1990-0696	0		LED-LIGHT BAR MODULE LUM-INT=3MCD	28480	1LM1-2300
A3DS16	1990-0699	3		LED-LIGHT BAR MODULE LUM-INT=7MCD	28480	1LM1-2350
A3DS17	1990-0696	0		LED-LIGHT BAR MODULE LUM-INT=3MCD	28480	1LM1-2300
A3R1	0683-3015	1	6	RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A3R2	0683-3015	1		RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A3R3	0683-7505	2	3	RESISTOR 75 5% .25W FC TC=-400/+500	01121	CB7505
A3R4	0683-3015	1		RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A3R5	0683-1515	2	7	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A3R6	0683-7505	2		RESISTOR 75 5% .25W FC TC=-400/+500	01121	CB7505
A3R7	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A3R9	0683-3015	1		RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A3R10	0683-3015	1		RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A3R11	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A3R12	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A3R13	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A3R14	0683-7505	2		RESISTOR 75 5% .25W FC TC=-400/+500	01121	CB7505
A3R15	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A3R16	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R17	0683-1025	9	4	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A3R19	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A3R20	0683-3315	4	1	RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
A3R21	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A3R22	0683-1035	1	5	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3R23	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3R24	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3R25	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3R26	0683-4735	4	2	RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
A3R27	0683-3035	5	1	RESISTOR 30K 5% .25W FC TC=-400/+800	01121	CB3035
A3R28	0683-4735	4		RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
A3R29	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A3R30	0683-3015	1		RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A3R31	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3R32	0683-4725	2	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A3R33	0683-7535	8	1	RESISTOR 75K 5% .25W FC TC=-400/+800	01121	CB7535
A3R34	0683-6215	9	1	RESISTOR 620 5% .25W FC TC=-400/+600	01121	CB6215
A3RP1	1810-0272	8	2	NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A3RP2	1810-0317	2	3	NETWORK-RES 14-DIP510.0 OHM X 7	01121	314B511
A3RP3	1810-0317	2		NETWORK-RES 14-DIP510.0 OHM X 7	01121	314B511
A3RP4	1810-0317	2		NETWORK-RES 14-DIP510.0 OHM X 7	01121	314B511
A3RP5	1810-0269	3	1	NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A3RP6	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A3S1	5060-9436	7	20	PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S2	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S3	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S4	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S5	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S6	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S7	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S8	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S9	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S10	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S11	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S12	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S13	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S14	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S15	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S16	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S17	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S18	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S19	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3S20	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A3U1	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A3U2	1820-2462	3	3	IC DRVR CMOS DSPL DRVR BCD-TO-7-SEG	04713	MC14513BCP
A3U3	1820-1730	6	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U4	1820-2132	4	1	IC DRVR CMOS LED DRVR	32293	ICM7218A
A3U5	1820-2462	3		IC DRVR CMOS DSPL DRVR BCD-TO-7-SEG	04713	MC14513BCP
A3U6	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U7	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U8	1820-2462	3		IC DRVR CMOS DSPL DRVR BCD-TO-7-SEG	04713	MC14513BCP
A3U9	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U11	1820-1740	8	1	IC DRVR TTL DSPL DRVR	27014	DS8863N
A3U12	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U13	1820-1759	9	1	IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A3U14	1820-2309	7	1	IC ENCDR CMOS	27014	MM74C923N
A3U15	1820-1976	2	1	IC BFR CMOS NON-INV HEX	34585	CD4050BE
A3U16	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A3U17	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U18	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U20	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U21	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U22	1820-1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U23	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3W1	03497-61606	1	1	CABLE ASSEMBLY	28480	03497-61606
				A3 ASSY MISC. PARTS		
	1450-0595	4	1	STANDOFF LED POLYPHENYL SULFIDE; 60 MM	28480	1450-0595

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	03497-66504	8	1	MOTHER BOARD	28480	03497-66504
A4J1	1251-3962	3	1	CONNECTOR 8-PIN F POST TYPE	28480	1251-3962
A4J2	1251-6062	0	1	CONNECTOR 10-PIN F POST TYPE	28480	1251-6062
A4J3	1251-6542	1	7	CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480	1251-6542
A4J4	1251-6542	1		CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480	1251-6542
A4J5	1251-6542	1		CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480	1251-6542
A4J6	1251-6542	1		CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480	1251-6542
A4J7	1251-6542	1		CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480	1251-6542
A4J8	1251-6542	1		CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480	1251-6542
A4J9	1251-3961	2	2	CONNECTOR 6-PIN F POST TYPE	28480	1251-3961
A4J10	1251-3961	2		CONNECTOR 6-PIN F POST TYPE	28480	1251-3961
A4J11	1251-6542	1		CONNECTOR-PC EDGE 25-CONT/ROW 2-ROWS	28480	1251-6542

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	03497-66505	9	1	VOLTMETER ASSEMBLY	28480	03497-66505
A5C1	0160-4438	6	1	CAPACITOR-FXD 470PF +-2.5%_160VDC_POLYP	28480	0160-4438
A5C3	0160-2199	2	2	CAPACITOR-FXD 30PF +-5% 300VDC MICA	28480	0160-2199
A5C4	0180-0195	6	1	CAPACITOR-FXD .33UF+-20% 35VDC TA	56289	150D334X0035A2
A5C5	0160-4682	2	1	CAPACITOR-FXD 1000PF +-2.5% 160VDC POLYP	28480	0160-4682
A5C6	0180-0309	4	3	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A5C7	0160-3876	4	5	CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A5C8	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A5C9	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A5C10	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A5C11	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A5C100	0160-0158	9	1	CAPACITOR-FXD 5600PF +-10% 200VDC POLYE	28480	0160-0158
A5C102	0140-0196	3	1	CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300WV1CR
A5C103	0160-0362	7	1	CAPACITOR-FXD 510PF +-5% 300VDC MICA	28480	0160-0362
A5C104	0160-2199	2		CAPACITOR-FXD 30PF +-5% 300VDC MICA	28480	0160-2199
A5C105	0180-0291	3	2	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A5C106	0160-0574	3	1	CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-0574
A5C107	0180-0116	1	7	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C200	0140-0149	6	1	CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
A5C201	0160-5104	5	1	CAPACITOR-FXD .0039UF .05% POLYP	28480	0160-5104
A5C203	0160-4603	7	1	CAPACITOR-FXD 1UF +-20% 200VDC MET-POLYP	28480	0160-4603
A5C204	0160-0161	4	1	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A5C205	0160-0576	5	1	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A5C206	0160-0127	2	1	CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
A5C207	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A5C300	0160-2208	4	2	CAPACITOR-FXD 330PF +-5% 300VDC MICA	28480	0160-2208
A5C301	0160-2208	4		CAPACITOR-FXD 330PF +-5% 300VDC MICA	28480	0160-2208
A5C302	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C303	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C304	0180-0229	7	1	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A5C400	0160-2204	0	2	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A5C401	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A5C402	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A5C403	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C404	0140-0205	5	1	CAPACITOR-FXD 62PF +-5% 300VDC MICA	72136	DM15E620J0300WV1CR
A5C405	0160-4571	8	3	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A5C406	0160-4810	8	1	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A5C600	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A5C601	0140-0190	7	1	CAPACITOR-FXD 39PF +-5% 300VDC MICA	72136	DM15E390J0300WV1CR
A5C701	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C702	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C407	0160-4810	8	1	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A5C703	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A5C704	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A5C705	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A5C706	0180-0210	6	1	CAPACITOR-FXD 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A5CR1	1901-0050	3	12	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR5	1902-3190	0	2	DIODE-ZNR 13V 5% DO-35 PD=.4W TC=+.06%	28480	1902-3190
A5CR6	1902-3190	0		DIODE-ZNR 13V 5% DO-35 PD=.4W TC=+.06%	28480	1902-3190
A5CR101	1901-0518	8	3	DIODE-SM SIG SCHOTTKY	28480	1901-0518
A5CR102	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
A5CR103	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR104	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR105	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR106	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR107	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR200	1901-0376	6	2	DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A5CR201	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A5CR202	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR300	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR301	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR302	1901-0025	2	8	DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5CR303	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5CR203	1901-0518			DIODE-SM SIG SCHOTTKY	28480	1901-0518
A5CR304	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5CR305	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5CR306	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5CR307	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5CR308	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5CR309	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
A5CR310	1902-3222	9	2	DIODE-ZNR 17.4V 5% DO-35 PD=.4W	28480	1902-3222
A5CR311	1902-3222	9		DIODE-ZNR 17.4V 5% DO-35 PD=.4W	28480	1902-3222
A5CR400	1902-1331	7	1	DIODE-ZNR 6.9V 4% TO-92 TC=+.0015%	28480	1902-1331
A5CR401	1902-0962	8	1	DIODE-ZNR 15V 5% DO-35 PD=.4W TC=+.087%	28480	1902-0962
A5CR402	1901-0029	6	1	DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A5CR403	1901-0040	1	3	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A5CR404	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A5CR405	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A5CR406	1901-0586	0	1	DIODE-GEN PRP 30V 25MA TO-72	28480	1901-0586
A5CR700	1902-3149	9	1	DIODE-ZNR 9.09V 5% DO-35 PD=.4W	28480	1902-3149
A5E400	1970-0084	8		TUBE-ELECTRON SURGE V PTCTR	28480	1970-0084
A5E400	1970-0084	8	2	TUBE-ELECTRON SURGE V PTCTR	28480	1970-0084
A5K1	0490-0663	0	1	RELAY-REED 1A 500MA 1000VDC 5VDC-COIL	28480	0490-0663
A5K2	0490-1238	7	1	RELAY-REED 2A 1200VDC 15VDC-COIL 15VA	28480	0490-1238
A5K401	0490-1260	5	3	SWITCH-REED 3A DRY 1A 250V 3.6-AT	28480	0490-1260
A5K402	0490-1260	5		SWITCH-REED 3A DRY 1A 250V 3.6-AT	28480	0490-1260
A5K403	0490-1260	5		SWITCH-REED 3A DRY 1A 250V 3.6-AT	28480	0490-1260
A5P700	1200-0867	4	3	SOCKET-STRP 8-CONT SIP DIP-SLDR	28480	1200-0867
A5P701	1200-0867	4		SOCKET-STRP 8-CONT SIP DIP-SLDR	28480	1200-0867
A5P702	1200-0867	4		SOCKET-STRP 8-CONT SIP DIP-SLDR	28480	1200-0867
A5Q1	1855-0243	7	1	TRANSISTOR-JFET DUAL N-CHAN TO-71 SI	28480	1855-0243
A5Q2	1855-0298	2	8	TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0298
A5Q3	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A5Q4	1855-0298	2		TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0298
A5Q5	1855-0298	2		TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0298
A5Q6	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A5Q7	1855-0298	2		TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0298
A5Q8	1855-0298	2		TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0298
A5Q9	1855-0298	2		TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0298
A5Q10	1855-0298	2		TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0298
A5Q100	1855-0247	1	1	TRANSISTOR-JFET DUAL N-CHAN D-MODE TO-71	28480	1855-0247
A5Q101	1855-0246	0	1	TRANSISTOR-JFET DUAL N-CHAN D-MODE TO-71	28480	1855-0246
A5Q102	1855-0386	9	2	TRANSISTOR J-FET 2N4392 N-CHAN D-MODE	04713	2N4392
A5Q103	1855-0386	9		TRANSISTOR J-FET 2N4392 N-CHAN D-MODE	04713	2N4392
A5Q104	1855-0341	6	1	TRANSISTOR J-FET 2N4338 N-CHAN D-MODE	17856	2N4338
A5Q105	1855-0270	0	3	TRANSISTOR J-FET N-CHAN D-MODE TO-92 SI	28480	1855-0270
A5Q106	1855-0270	0		TRANSISTOR J-FET N-CHAN D-MODE TO-92 SI	28480	1855-0270
A5Q107	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A5Q200	1855-0414	4	1	TRANSISTOR J-FET 2N4393 N-CHAN D-MODE	04713	2N4393
A5Q201	1855-0420	2	1	TRANSISTOR J-FET 2N4391 N-CHAN D-MODE	01295	2N4391
A5Q202	1855-0460	0	1	TRANSISTOR J-FET N-CHAN	28480	1855-0460
A5Q203	1855-0429	1	2	TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0429
A5Q204	1853-0066	8	1	TRANSISTOR PNP SI TO-92 PD=625MW	28480	1853-0066
A5Q205	1855-0270	0		TRANSISTOR J-FET N-CHAN D-MODE TO-92 SI	28480	1855-0270
A5Q206	1854-0296	8	1	TRANSISTOR NPN SI TO-92 PD=310MW	28480	1854-0296
A5Q300	1853-0320	7	2	TRANSISTOR PNP 2N4032 SI TO-5 PD=800MW	07263	2N4032
A5Q301	1853-0320	7		TRANSISTOR PNP 2N4032 SI TO-5 PD=800MW	07263	2N4032
A5Q302	1853-0086	2	1	TRANSISTOR PNP SI PD=310MW FT=40MHZ	27014	2N5087
A5Q303	1854-0087	5	1	TRANSISTOR NPN SI PD=360MW FT=75MHZ	28480	1854-0087
A5Q400	1855-0429	1		TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0429
A5Q401	1855-0298	2		TRANSISTOR J-FET N-CHAN D-MODE TO-92	28480	1855-0298
A5Q403	1854-0079	5	2	TRANSISTOR NPN 2N3439 SI TO-5 PD=1W	3L585	2N3439
A5Q404	1854-0079	5		TRANSISTOR NPN 2N3439 SI TO-5 PD=1W	3L585	2N3439
A5Q700	1853-0089	5	1	TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A5R1	0698-3158	4	2	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A5R2	0698-3158	4		RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A5R3	0683-1535	6	1	RESISTOR 15K 5% .25W FC TC=-400/+800	01121	CB1535
A5R4	2100-3052	4	1	RESISTOR-TRMR 50 10% C SIDE-ADJ 17-TRN	02111	43P500
A5R5	0683-1045	3	6	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R6	0757-0442	9	11	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R7	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R8	2100-3253	7	2	RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	28480	2100-3253
A5R10	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R11	0683-3025	3	2	RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A5R12	0683-2025	1	2	RESISTOR 2K 5% .25W FC TC=-400/+700	01121	CB2025
A5R13	0757-0161	9	2	RESISTOR 604 1% .125W F TC=0+-100	24546	C4-1/8-T0-604R-F
A5R14	0757-0422	5	1	RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A5R15	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R16	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R17	0692-4735	3	2	RESISTOR 47K 5% 2W CC TC=0+765	01121	HB4735
A5R18	0692-4735	3		RESISTOR 47K 5% 2W CC TC=0+765	01121	HB4735
A5R19	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R20	0683-3025	3		RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A5R21	0683-2025	1		RESISTOR 2K 5% .25W FC TC=-400/+700	01121	CB2025

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R22	0698-3179	9	2	RESISTOR 2.55K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2551
A5R23	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R25	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R26	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R27	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R28	2100-3253	7		RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	28480	2100-3253
A5R30	0698-3152	8	1	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A5R35	0698-6254	7	1	RESISTOR 1.8 5% .5W CC TC=0+412	01121	EB18G5
A5R36*	0686-2265	7	1	RESISTOR 22M 5% .5W CC TC=0+1059	01121	EB2265
A5R100	0698-3151	7	1	RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A5R101	2100-0568	1	1	RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A5R102	0698-4500	2	2	RESISTOR 57.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5762-F
A5R103	0757-0446	3	6	RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A5R104	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A5R105	0757-0449	6	6	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A5R106	0757-0483	8	2	RESISTOR 562K 1% .125W F TC=0+-100	28480	0757-0483
A5R107	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A5R108	0757-0483	8		RESISTOR 562K 1% .125W F TC=0+-100	28480	0757-0483
A5R109	0698-3156	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A5R110	0698-3451	0	1	RESISTOR 133K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1333-F
A5R111	0757-0317	7	1	RESISTOR 1.33K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1331-F
A5R112	0698-4516	0	1	RESISTOR 113K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1133-F
A5R113	0698-4495	4	2	RESISTOR 37.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3742-F
A5R114	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
A5R115	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A5R116	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R117	0698-4507	9	1	RESISTOR 76.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7682-F
A5R118	0698-4513	7	1	RESISTOR 97.6K 1% .125W F TC=0+-100	03888	PME55-1/8-T0-9762-F
A5R119	0698-4529	5	2	RESISTOR 226K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2263-F
A5R120	0698-4529	5		RESISTOR 226K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2263-F
A5R121	0698-4487	4	2	RESISTOR 25.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2552-F
A5R122	0698-3179	9		RESISTOR 2.55K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2551
A5R123	0698-4539	7	1	RESISTOR 402K 1% .125W F TC=0+-100	28480	0698-4539
A5R125	2100-3095	5	2	RESISTOR-TRMR 200 10% C SIDE-ADJ 17-TRN	02111	43P201
A5R126	0698-4531	9	1	RESISTOR 267K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2673-F
A5R127	2100-3095	5		RESISTOR-TRMR 200 10% C SIDE-ADJ 17-TRN	02111	43P201
A5R128	1QD4-0044	1	1	SIGNAL-CONDITIONING FINELINE	28480	1QD4-0044
A5R129	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A5R130	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R131	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A5R132	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A5R133	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R200	1QE7-0057	3	1	A-D FINELINE	28480	1QE7-0057
A5R201	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A5R202	0698-4495	4		RESISTOR 37.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3742-F
A5R203	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A5R204	0757-0161	9		RESISTOR 604 1% .125W F TC=0+-100	24546	C4-1/8-T0-604R-F
A5R205	0757-0410	1	2	RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A5R206	0757-0453	2	1	RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
A5R207	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R208	0698-3279	0	2	RESISTOR 4.99K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4991-F
A5R209	0757-0410	1		RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A5R210	0683-1035	1	4	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A5R211	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A5R212	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A5R213	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A5R214	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A5R215	0698-4471	6	1	RESISTOR 7.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7151-F
A5R216	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R218	0698-4515	9	1	RESISTOR 107K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1073-F
A5R219	0757-0272	3	2	RESISTOR 52.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5232-F
A5R220	0757-0457	6	2	RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A5R221	0757-0457	6		RESISTOR 47.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4752-F
A5R222	0757-0272	3		RESISTOR 52.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5232-F
A5R223	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A5R224	0757-0273	4	3	RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A5R225	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A5R226	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R300	0698-3279	0		RESISTOR 4.99K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4991-F
A5R301	0698-4537	5	2	RESISTOR 357K 1% .125W F TC=0+-100	28480	0698-4537
A5R302	0698-4537	5		RESISTOR 357K 1% .125W F TC=0+-100	28480	0698-4537
A5R303	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A5R304	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A5R305	0757-0426	9	2	RESISTOR 1.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1301-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R306	0698-4470	5	2	RESISTOR 6.98K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6981-F
A5R307	0757-0426	9		RESISTOR 1.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1301-F
A5R308	0698-4470	5		RESISTOR 6.98K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6981-F
A5R309	0698-4483	0	2	RESISTOR 18.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1872-F
A5R310	0698-4483	0		RESISTOR 18.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1872-F
A5R311	0698-4480	7	2	RESISTOR 15.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1582-F
A5R312	0698-4480	7		RESISTOR 15.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1582-F
A5R400	0757-0440	7	1	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A5R401	0757-0436	1	1	RESISTOR 4.32K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4321-F
A5R402	0699-0489	0	1	RESISTOR 16.15K .1% .1W F TC=0+-5	28480	0699-0489
A5R403	0698-7848	7	1	RESISTOR 1.25K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1251-B
A5R404	0698-7668	9	1	RESISTOR 39.91K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-39911-B
A5R405	0698-7678	1	1	RESISTOR 79.81K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-79811-B
A5R406	0698-4211	2	1	RESISTOR 158K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1583-F
A5R407	0698-3457	6	1	RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A5R408	0698-4500	2		RESISTOR 57.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5762-F
A5R409	2100-3054	6	3	RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	02111	43P503
A5R410	2100-3054	6		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	02111	43P503
A5R411	2100-3054	6		RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN	02111	43P503
A5R412	0757-0486	1	1	RESISTOR 750K 1% .125W F TC=0+-100	28480	0757-0486
A5R413	0764-0028	2	1	RESISTOR 100K 5% 2W MO TC=0+-200	28480	0764-0028
A5R414	0698-8776	2	1	RESISTOR 10 5% .25W CC TC=-400/+500	28480	0698-8776
A5R600	0698-4202	1	1	RESISTOR 8.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8871-F
A5R601	0757-0434	9	1	RESISTOR 3.65K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3651-F
A5R602	0698-4487	4		RESISTOR 25.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2552-F
A5R701	0698-3228	9	1	RESISTOR 49.9K 1% .125W F TC=0+-100	28480	0698-3228
A5R702	2100-3094	4	1	RESISTOR-TRMR 100K 10% C SIDE-ADJ 17-TRN	02111	43P104
A5R704	0690-3911	1	1	RESISTOR 390 10% 1W CC TC=0+529	01121	GB3911
A5R705	0698-3511	3	1	RESISTOR 665 1% .125W F TC=0+-100	24546	C4-1/8-T0-665R-F
A5R706	0698-3271	2	1	RESISTOR 115K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1153-F
A5RT1	0837-0196	0	1	SUPPR-V 430V	28480	0837-0196
A5S700	3100-3364	2	1	SWITCH-ROTARY 16 PIN DIP 4PDT	28480	3100-3364
A5T300	9100-2623	0	2	TRANSFORMER-PULSE 200 TURN; CENTER TAP	28480	9100-2623
A5T301	9100-2623	0		TRANSFORMER-PULSE 200 TURN; CENTER TAP	28480	9100-2623
A5U1	1826-0138	8	7	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A5U2	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A5U3	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A5U4	1820-1273	2	1	IC BFR TTL LS NOR QUAD 2-INP	01295	SN74LS28N
A5U5	1826-0059	2	3	IC OP AMP GP TO-99 PKG	01295	LM201AL
A5U100	1858-0054	4	1	TRANSISTOR ARRAY 16-PIN PLSTC DIP	28480	1858-0054
A5U101	1826-0371	1	1	IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	27014	LF256H
A5U102	1826-0059	2		IC OP AMP GP TO-99 PKG	01295	LM201AL
A5U103	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A5U104	1826-0059	2		IC OP AMP GP TO-99 PKG	01295	LM201AL
A5U105	1820-1962	6	1	IC DCDR CMOS BCD-TO-DEC	3L585	CD4028BE
A5U200	1820-1746	4	2	IC BFR CMOS INV HEX	04713	MC14049UBCP
A5U201	1826-0340	4	1	IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	28480	1826-0340
A5U202	1826-0685	0	1	IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	27014	LF351H
A5U203	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A5U204	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A5U205	1820-1556	4	1	IC DCDR CMOS BIN 2-TO-4-LINE DUAL 2-INP	3L585	CD4555BF
A5U206	1820-1601	0	1	IC GATE CMOS EXCL-OR QUAD 2-INP	3L585	CD4070BE
A5U207	1820-2258	5	1	IC FF CMOS D-TYPE POS-EDGE-TRIG COM	04713	MC14174BCP
A5U208	1820-1746	4		IC BFR CMOS INV HEX	04713	MC14049UBCP
A5U300	1820-1991	1	1	IC CNTR TTL LS DECD DUAL 4-BIT	01295	SN74LS390N
A5U301	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A5U400	1820-1426	7	1	IC DCDR TTL LS BCD-TO-DEC 4-TO-10-LINE	01295	SN74LS145N
A5U401	1820-0478	7	2	IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	27014	LM308H
A5U402	1820-0478	7		IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	27014	LM308H
A5U600	1826-0330	2	1	V REF PRCN TO-46	27014	LM299H
A5U601	1826-0471	2	1	IC OP AMP LOW-DRIFT TO-99 PKG	28480	1826-0471
A5U700	1826-0043	4	2	IC OP AMP GP TO-99 PKG	3L585	CA307T
A5U701	1826-0043	4		IC OP AMP GP TO-99 PKG	3L585	CA307T
A5W1	03497-61604	9	1	CABLE ASSEMBLY-CONTROL	28480	03497-61604
				A5 ASSEMBLY MECHANICAL PARTS		
	03497-00607	4	1	A/D COVER	28480	03497-00607
	0515-0064	9	4	SCREW-MACH:M3.0X16(A/D COVER SCREWS)	28480	0515-0064

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A16	03497-66516	2	1	POWER SUPPLY ASSEMBLY	28480	03497-66516
A16C1	0180-3028	0	1	CAPACITOR-FXD 3300UF+75-10% 25VDC AL	28480	0180-3028
A16C2	0160-3847	9	1	CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
A16C3	0180-0197	8	2	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A16C4	0180-0309	4	4	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A16C5	0160-4571	8	13	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C6	0160-0159	0	1	CAPACITOR-FXD 6800PF +-10% 200VDC POLYE	28480	0160-0159
A16C7	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A16C8	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C9	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C10	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A16C11	0180-2506	7	1	CAPACITOR-FXD 470UF+50-10% 25VDC AL	28480	0180-2506
A16C13	0180-0141	2	3	CAPACITOR-FXD 50UF+75-10% 50VDC AL	56289	30D506G050DD2
A16C14	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C15	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C16	0180-2779	6	4	CAPACITOR-FXD 470UF+75-10% 50VDC AL	56289	30D477G050FK2
A16C17	0180-2779	6		CAPACITOR-FXD 470UF+75-10% 50VDC AL	56289	30D477G050FK2
A16C18	0180-0141	2		CAPACITOR-FXD 50UF+75-10% 50VDC AL	56289	30D506G050DD2
A16C19	0180-0195	6	1	CAPACITOR-FXD .33UF+-20% 35VDC TA	56289	150D334X0035A2
A16C20	0180-1846	6	1	CAPACITOR-FXD 2.2UF+-10% 35VDC TA	56289	150D225X9035B2
A16C21	0180-0291	3	6	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A16C22	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A16C23	0180-0141	2		CAPACITOR-FXD 50UF+75-10% 50VDC AL	56289	30D506G050DD2
A16C24	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A16C25	0180-0692	8	1	CAPACITOR-FXD 220UF+50-10% 35VDC AL	00494	35VBSL220
A16C26	0160-4807	3	1	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
A16C27	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C28	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C29	0180-3027	9	1	CAPACITOR-FXD .01F+75-10% 16VDC AL	28480	0180-3027
A16C30	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A16C31	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A16C32	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C33	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C34	0180-2779	6		CAPACITOR-FXD 470UF+75-10% 50VDC AL	56289	30D477G050FK2
A16C35	0180-2779	6		CAPACITOR-FXD 470UF+75-10% 50VDC AL	56289	30D477G050FK2
A16C36	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C37	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C38	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A16C39	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A16C40	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A16C50	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16C51	0160-4571	8		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A16CR1	1990-0453	7	1	LED-LAMP LUM-INT=800UCD IF=50MA-MAX	28480	5082-4487
A16CR2	1901-0044	5	5	DIODE-SWITCHING 50V 50MA 6NS	28480	1901-0044
A16CR3	1901-0044	5		DIODE-SWITCHING 50V 50MA 6NS	28480	1901-0044
A16CR4	1901-0044	5		DIODE-SWITCHING 50V 50MA 6NS	28480	1901-0044
A16CR5	1901-0044	5		DIODE-SWITCHING 50V 50MA 6NS	28480	1901-0044
A16CR6	1902-1344	2	1	DIODE-ZNR 4.3V 2% DO-35 PD=.25W	28480	1902-1344
A16CR7	1901-0704	4	11	DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR8	1902-3125	1	1	DIODE-ZNR 6.98V 2% DO-35 PD=.4W	28480	1902-3125
A16CR9	1901-0026	3	4	DIODE-PWR RECT 200V 750MA DO-29	28480	1901-0026
A16CR10	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901-0026
A16CR12	1901-0044	5		DIODE-SWITCHING 50V 50MA 6NS	28480	1901-0044
A16CR13	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901-0026
A16CR14	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901-0026
A16CR17	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR18	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR19	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR20	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR22	1902-0632	9	2	DIODE-ZNR 1N5354B 17V 5% PD=5W TC=+75%	04713	1N5354B
A16CR23	1902-0657	8	1	DIODE-ZNR 43.2V 5% DO-15 PD=1W TC=+.08%	28480	1902-0657
A16CR24	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR25	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR27	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR28	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR29	1902-0632	9		DIODE-ZNR 1N5354B 17V 5% PD=5W TC=+75%	04713	1N5354B
A16CR30	1902-0244	9	1	DIODE-ZNR 30V 5% PD=1W IR=5UA	28480	1902-0244
A16CR31	1902-3030	7	1	DIODE-ZNR 3.01V 5% DO-7 PD=.4W TC=-.067%	28480	1902-3030
A16CR32	1902-1331	7	1	DIODE-ZNR 6.9V 4% TO-92 TC=+.0015%	28480	1902-1331
A16CR33	1902-3190	0	1	DIODE-ZNR 13V 5% DO-35 PD=.4W TC=+.06%	28480	1902-3190
A16CR35	1902-1232	7	1	DIODE-ZNR 1N3997RA 5.6V 5% DO-4 PD=10W	04713	1N3997RA
A16CR36	1901-0743	1	4	DIODE-PWR	28480	1901-0743

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A16CR37	1901-0743	1	4	DIODE-PWR RECT	28480	1901-0743
A16CR41	1901-0743	1	4	DIODE-PWR RECT	28480	1901-0743
A16CR42	1901-0743	1	4	DIODE-PWR RECT	28480	1901-0743
A16CR44	1902-3062	5	1	DIODE-ZNR 3.92V 5% DO-35 PD=.4W	28480	1902-3062
A16CR45	1902-1288	3	2	DIODE-ZNR 1N5358B 22V 5% PD=5W TC=+75%	04713	1N5358B
A16CR46	1901-0673	6	4	DIODE-PWR RECT 100V 5A SUS	03508	A15A
A16CR47	1901-0673	6		DIODE-PWR RECT 100V 5A SUS	03508	A15A
A16CR48	1901-0673	6		DIODE-PWR RECT 100V 5A SUS	03508	A15A
A16CR49	1901-0673	6		DIODE-PWR RECT 100V 5A SUS	03508	A15A
A16CR50	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR51	1901-0704	4		DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A16CR52	1902-0522	6	1	DIODE-ZNR 1N5340B 6V 5% PD=5W IR=1UA	04713	1N5340B
A16CR55	1902-1288	3		DIODE-ZNR 1N5358B 22V 5% PD=5W TC=+75%	04713	1N5358B
A16CR56	1902-1345	3	1	DIODE-ZNR 1N5365B 36V 5% PD=5W IR=500NA	04713	1N5365B
A16CR59	1902-1291	8	1	DIODE-ZNR 1N5338B 5.1V 5% PD=5W IR=1UA	04713	1N5338B
A16CR60	1902-0556	6	1	DIODE-ZNR 20V 5% PD=1W IR=5UA	28480	1902-0556
A16J5	1251-4659	7	1	CONNECTOR 14-PIN M POST TYPE	28480	1251-4659
A16J6	1251-3197	6	1	CONNECTOR 12-PIN M POST TYPE	28480	1251-3197
A16J7	1251-4822	6	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-4822
A16P1	1251-5894	4	2	CONNECTOR 6-PIN F POST TYPE	28480	1251-5894
A16P2	1251-5894	4		CONNECTOR 6-PIN F POST TYPE	28480	1251-5894
A16P3	1251-6062	0	1	CONNECTOR 10-PIN F POST TYPE	28480	1251-6062
A16P4	1251-3962	3	1	CONNECTOR 8-PIN F POST TYPE	28480	1251-3962
	1258-0141	8	1	JUMPER-REM	28480	1258-0141
A16Q1	1853-0394	5	2	TRANSISTOR PNP SI TO-220AB PD=40W	04713	MJE 2370
	1205-0318	0	7	HEAT SINK SGL TO-220-CS	28480	1205-0318
A16Q2	1854-0215	1	2	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A16Q3	1853-0320	7	1	TRANSISTOR PNP 2N4032 SI TO-5 PD=800MW	07263	2N4032
A16Q4	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A16Q5	1854-0087	5	1	TRANSISTOR NPN SI PD=360MW FT=75MHZ	28480	1854-0087
A16Q6	1854-0039	7	1	TRANSISTOR NPN 2N3053S SI TO-39 PD=1W	3L585	2N3053S
A16Q7	1853-0394	5		TRANSISTOR PNP SI TO-220AB PD=40W	04713	MJE 2370
	1205-0318	0		HEAT SINK SGL TO-220-CS	28480	1205-0318
A16Q8	1853-0016	8	1	TRANSISTOR PNP SI TO-92 PD=300MW	28480	1853-0016
A16R1	0698-5139	5	1	RESISTOR 3.9 5% .5W CC TC=0+412	01121	EB39G5
A16R2	0683-1625	5	1	RESISTOR 1.6K 5% .25W FC TC=-400/+700	01121	CB1625
A16R3	0683-2035	3	2	RESISTOR 20K 5% .25W FC TC=-400/+800	01121	CB2035
A16R4	0683-2035	3		RESISTOR 20K 5% .25W FC TC=-400/+800	01121	CB2035
A16R5	0686-3915	6	1	RESISTOR 390 5% .5W CC TC=0+529	01121	EB3915
A16R6	0683-5125	8	2	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A16R7	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A16R8	0698-3266	5	1	RESISTOR 237K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2373-F
A16R9	0757-0442	9	5	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A16R10	2100-0567	0	1	RESISTOR-TRMR 2K 10% C TOP-ADJ 1-TRN	28480	2100-0567
A16R11	0698-3264	3	1	RESISTOR 11.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1182-F
A16R12	0698-3225	6	1	RESISTOR 1.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1431-F
A16R13	0683-1025	9	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A16R14	0683-4725	2	4	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A16R15	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A16R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A16R17	0698-4483	0	1	RESISTOR 18.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1872-F
A16R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A16R19	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A16R20	0698-3611	4	1	RESISTOR 27 5% 2W MO TC=0+-200	27167	FP42-2-T00-27R0-J
A16R21	0683-3915	0	1	RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A16R22	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A16R23	0811-3290	7	2	RESISTOR .1 5% 2W PW TC=0+-800	28480	0811-3290
A16R24	0811-3290	7		RESISTOR .1 5% 2W PW TC=0+-800	28480	0811-3290
A16R25	0683-3005	9	1	RESISTOR 30 5% .25W FC TC=-400/+500	01121	CB3005
A16R26	0698-3152	8	1	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A16R27	0698-3495	2	1	RESISTOR 866 1% .125W F TC=0+-100	24546	C4-1/8-T0-866R-F
A16R28	0698-3223	4	1	RESISTOR 1.24K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1241-F
A16R29	0698-3151	7	1	RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A16R30	0757-0460	1	1	RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A16R31	0683-4715	0	1	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A16R33	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A16R34	0698-4308	8	1	RESISTOR 16.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1692-F
A16R35	0698-8060	7	1	RESISTOR 8.64K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-8641-B
A16R36	0698-6842	9	1	RESISTOR 4.32K .5% .125W F TC=0+-50	24546	NC55-1/8-T2-4321-D
A16R37	0698-6446	9	1	RESISTOR 2.162K .1% .125W F TC=0+-25	28480	0698-6446
A16R38	0698-6362	8	1	RESISTOR 1K .1% .125W F TC=0+-25	28480	0698-6362
A16R39	0698-3155	1	1	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A16R40	0683-5125	8		RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A16R41	0760-0024	0	1	RESISTOR 100 5% 1W MO TC=0+-200	28480	0760-0024

See introduction to this section for ordering information
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Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A16R42	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A16R43	0698-4406	7	1	RESISTOR 115 1% .125W F TC=0+-100	24546	C4-1/8-T0-115R-F
A16R44	0757-0817	2	2	RESISTOR 750 1% .5W F TC=0+-100	28480	0757-0817
A16R45	0757-0817	2		RESISTOR 750 1% .5W F TC=0+-100	28480	0757-0817
A16R46	2100-0558	9	1	RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	28480	2100-0558
A16R48	0757-0737	5	1	RESISTOR 1.62K 1% .25W F TC=0+-100	24546	C5-1/4-T0-1621-F
A16R50	0698-3268	7	1	RESISTOR 11.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1152-F
A16R51	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A16R52	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A16R53	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A16R54	0683-1035	1	1	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A16R55	0683-1005	5	2	RESISTOR 10 5% .25W FC TC=-400/+500	01121	CB1005
A16R56	0811-1674	7	1	RESISTOR 4.7 5% 2W PW TC=0+-400	75042	BWH2-4R7-J
A16R60	0683-3315	4	1	RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
A16R75	0683-1005	5		RESISTOR 10 5% .25W FC TC=-400/+500	01121	CB1005
A16RT49	0837-0225	6	2	THERMISTOR DISC 2.5-OHM	28480	0837-0225
A16RT80	0837-0225	6		THERMISTOR DISC 2.5-OHM	28480	0837-0225
A16RV1	0837-0196	0	1	SUPPR-V 430V	28480	0837-0196
A16T1	9100-2616	1	4	TRANSFORMER-PULSE BIFILAR WOUND; 18.0 MM	28480	9100-2616
A16T2	9100-2616	1		TRANSFORMER-PULSE BIFILAR WOUND; 18.0 MM	28480	9100-2616
A16T3	9100-2616	1		TRANSFORMER-PULSE BIFILAR WOUND; 18.0 MM	28480	9100-2616
A16T4	9100-2616	1		TRANSFORMER-PULSE BIFILAR WOUND; 18.0 MM	28480	9100-2616
A16U1	1826-0409	6	1	IC 723 V RGLTR 14-DIP-C	04713	MC1723L
A16U2	1826-0346	0	2	IC OP AMP GP DUAL 8-DIP-P PKG	27014	LM358N
A16U3	1826-0277	6	1	IC V RGLTR TO-220	27014	LM320T-15
	1205-0318	0		HEAT SINK SGL TO-220-CS	28480	1205-0318
A16U4	1826-0617	8	1	IC-VOLTAGE REGULATOR TO-220	28480	1826-0617
	1205-0318	0		HEAT SINK SGL TO-220-CS	28480	1205-0318
A16U7	1820-0223	0	1	IC OP AMP GP TO-99 PKG	3L585	CA301AT
A16U8	1826-0214	1	2	IC V RGLTR TO-220	04713	MC7915CT
	1205-0318	0		HEAT SINK SGL TO-220-CS	28480	1205-0318
A16U9	1826-0393	7	1	IC V RGLTR TO-220	27014	LM317T
	1205-0318	0		HEAT SINK SGL TO-220-CS	28480	1205-0318
A16U10	1826-0214	1		IC V RGLTR TO-220	04713	MC7915CT
	1205-0318	0		HEAT SINK SGL TO-220-CS	28480	1205-0318
A16U11	1826-0346	0		IC OP AMP GP DUAL 8-DIP-P PKG	27014	LM358N
A16U12	1826-0181	1	1	IC V RGLTR TO-3	27014	LM323K
				A16 ASSY MISC. PARTS		
	03497-01101	5	1	HEAT SINK	28480	03497-01101
	1200-0080	3	1	INSULATOR-DIO ALUMINUM HD-ANDZ	28480	1200-0080
	1205-0011	0	1	HEAT SINK TO-5/TO-39-CS	28480	1205-0011
	1200-0043	8	1	INSULATOR-XSTR ALUMINUM	28480	1200-0043
	0515-0054	7	1	SCREW-MACH M3 X 0.5 10MM-LG PAN-HD	28480	0515-0054
	0535-0004	9	1	NUT-HEX DBL-CHAM M3 X 0.5 2.4MM-THK	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A17	03497-66517	3	1	TIMER/PACER ASSEMBLY	28480	03497-66517
A17C1	0180-0309	4	5	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A17C2	0160-4791	4	2	CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30	28480	0160-4791
A17C3	0160-4791	4		CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30	28480	0160-4791
A17C4	0180-0291	3	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A17C6	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A17C7	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A17C8	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A17C9	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A17C10	0160-3873	1	1	CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A17J1	1251-6584	1	2	CONNECTOR-14 PIN MALE POST	28480	1251-6584
A17J2	1251-6584	1		CONNECTOR-14 PIN MALE POST	28480	1251-6584
A17Q1	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A17R1	0683-4725	2	2	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A17R2	0683-1035	1	8	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A17R3	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A17R4	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A17R5	0683-1025	9	3	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A17R6	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A17R7	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A17R8	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A17R9	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A17R10	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A17R11	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A17R12	0683-1045	3	1	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A17R14	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A17R15	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A17R16	0683-4335	0	1	RESISTOR 43K 5% .25W FC TC=-400/+800	01121	CB4335
A17RP1	1810-0269	3	3	NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A17RP2	1810-0269	3		NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A17RP3	1810-0269	3		NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A17RP4	1810-0307	0	1	NETWORK-CNDCT MODULE DIP; 16 PINS; 0.100	28480	1810-0307
A17TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17TP7	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17TP8	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17TP9	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A17U1	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A17U2	1820-2383	7	1	IC CNTR CMOS DIV-X-N DUAL 4-INP	04713	MC14569BCP
A17U3	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A17U4	1820-2533	9	1		28480	1820-2533
A17U6	1820-1175	3	4	IC CNTR CMOS BCD POS-EDGE-TRIG 4-BIT	04713	MC14522BCP
A17U7	1820-1175	3		IC CNTR CMOS BCD POS-EDGE-TRIG 4-BIT	04713	MC14522BCP
A17U8	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A17U9	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A17U10	1820-1175	3		IC CNTR CMOS BCD POS-EDGE-TRIG 4-BIT	04713	MC14522BCP
A17U11	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A17U12	1820-1759	9	1	IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A17U13	1820-1175	3		IC CNTR CMOS BCD POS-EDGE-TRIG 4-BIT	04713	MC14522BCP
A17Y1	0410-1285	6	1	CRYSTAL-2.4576 MHZ	28480	0410-1285
				A17 ASSY MISC. PARTS		
	0380-1263	5	1	STANDOFF	28480	0380-1263
	1200-0473	8	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0473
	1251-0600	0	10	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A21	03497-66521	9	1	OUTGUARD & HP-IB CONTROLLER ASSY	28480	03497-66521
A21C1	0180-0309	4	19	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C2	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C3	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C4	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C5	0160-4814	2	1	CAPACITOR-FXD 150PF +-5% 100VDC CER	28480	0160-4814
A21C6	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C7	0160-4571	8	1	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-4571
A21C8	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C9	0160-4810	8	2	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A21C10	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C11	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A21C12	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C13	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C14	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C15	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C16	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C18	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C19	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C20	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C21	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C22	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C23	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C24	0180-0309	4		CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A21C25	0160-4532	1	1	CAPACITOR-FXD 1000PF +-20% 50VDC CER	28480	0160-4532
A21C26	0160-0571	0	1	CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A21C27	0160-0570	9	1	CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A21C30	0160-4808			CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
A21CR1	1901-0040	1	12	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR6	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR8	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR9	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR10	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR11	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR12	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21CR13	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A21J1	1200-0583	1	2	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0583
A21J2	1200-0583	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0583
A21J3	1251-6263	3	2	CONNECTOR 14-PIN F POST TYPE	28480	1251-6263
A21J4	1251-6263	3		CONNECTOR 14-PIN F POST TYPE	28480	1251-6263
A21L1	9100-3547	9	1	INDUCTOR RF-CH-MLD 4.3UH 5% .166DX.385LG	28480	9100-3547
A21L2	9100-3551	5	1	INDUCTOR RF-CH-MLD 1UH 5% .166DX.385LG	28480	9100-3551
A21R1	0683-2225	3	4	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A21R2	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A21R3	0683-1015	7	7	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A21R4	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A21R5	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A21R6	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A21R7	0687-3325	4	1	RESISTOR 3.3K OHM 5% .25W FC TC=400/+600	28480	0687-3325
A21R9	0683-1035	1	6	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A21R10	0683-1025	9	8	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A21R11	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A21R12	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A21R14	0683-4725	2	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A21R15	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A21R16	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A21R17	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A21R18	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A21R19	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A21R20	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A21R21	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A21R22	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A21R24	0683-1055	5	1	RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
A21R25	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A21R26	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A21R28	0683-3025	3	1	RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A21R29	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A21R30	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A21R31	0698-4485	2	3	RESISTOR 23.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2322-F
A21R32	0698-4485	2		RESISTOR 23.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2322-F
A21R33	0683-8235	7	1	RESISTOR 82K 5% .25W FC TC=-400/+800	01121	CB8235
A21R34	0698-4485	2		RESISTOR 23.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2322-F
A21R35	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A21R36	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A21R37	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A21R38	0683-3325	6	2	RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A21R39	0683-3325	6		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A21R40	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A21R41	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A21R42	0683-6225	1	1	RESISTOR 6.2K 5% .25W FC TC=-400/+700	01121	CB6225
A21R43	0698-3132	4	1	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A21RP1	1810-0269	3	2	NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A21RP2	1810-0136	3	1	NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0136
A21RP3	1810-0307	0	1	NETWORK-CNDCT MODULE DIP; 16 PINS; 0.100	28480	1810-0307
A21RP4	1810-0281	9	1	NETWORK-RES 10-SIP100.0K OHM X 9	01121	210A104
A21RP5	1810-0269	3		NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A21S1	3101-1973	7	1	SWITCH-SL 7-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-1973
A21U1	1820-2485	0	1	IC RCVR TTL LS BUS OCTL	01295	SN75160N
A21U2	1820-1759	9	3	IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A21U3	1820-1491	6	2	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A21U4	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
A21U5	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A21U7	1820-2483	8	1	IC RCVR TTL LS BUS OCTL	01295	SN75161N
A21U8	1820-2428	1	1		28480	1820-2428
A21U10	1820-2036	7	1	IC DRVR NMOS CLOCK DRVR	04713	MC6875L
A21U11	1820-2137	9	1	IC MICPROC NMOS 8-BIT	04713	MC68A00P
A21U13	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A21U14	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A21U15	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A21U16	1818-1353	4	1	IC NMOS 65536 (64K) ROM 300-NS 3-S	50088	MK36000N-5 MASKED
A21U18	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A21U19	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A21U20	1818-1352	3	1	IC NMOS 32768 (32K) ROM 450-NS 3-S	34335	AM9232BPC MASKED
A21U21	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A21U22	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A21U23	1820-1205	0	1	IC GATE TTL LS AND DUAL 4-INP	01295	SN74LS21N
A21U24	1818-1354	5	1	IC NMOS 65536 (64K) ROM 300-NS 3-S	50088	MK36000N-5 MASKED
A21U25	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A21U26	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A21U28	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A21U29	1820-1491	6		IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A21U30	1818-1960	9	1	IC-1K X 8-BIT RAM	28480	1818-1960
A21U31	1820-1216	3	4	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A21U32	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A21U33	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A21U34	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
A21U35	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A21U36	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A21U37	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A21U39	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A21U40	1820-1975	1	1	IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN	01295	SN74LS165N
A21U41	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A21U42	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A21U43	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A21U44	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A21U45	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A21U46	1820-0514	2	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7426N
A21U49	1821-0001	4	1	TRANSISTOR ARRAY 14-PIN PLSTC DIP	3L585	CA3046
A21U50	1820-1433	6	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A21U51	1858-0054	4	1	TRANSISTOR ARRAY 16-PIN PLSTC DIP	28480	1858-0054
A21Y1	0410-1218	5	1	CRYSTAL-6.0 MHZ	28480	0410-1218
				A21 ASSY MISC. PARTS		
	1200-0473	8	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0473
	1200-0634	3	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0634
	1251-0600	0	1	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number	
				CHASSIS COMPONENTS (MECHANICAL)			
	5020-8805	8	1	FRONT FRAME	28480	5020-8805	
	5020-8806	9	1	REAR FRAME	28480	5020-8806	
	5020-8837	6	3	CORNER STRUT	28480	5020-8837	
	03497-26601	2	1	CORNER STRUT MODIFIED	28480	03497-26601	
	5001-0440	1	2	TRIM, SIDE	28480	5001-0440	
	5040-7202	9	1	TRIM, TOP	28480	5040-7202	USE ENGLISH
	5060-9804	3	1	STRAP HANDLE 18 IN.	28480	5060-9804	FASTENERS
	5040-7219	8	1	STRAP HANDLE, CAP-FRONT	28480	5040-7219	
	5040-7220	1	1	STRAP HANDLE, CAP-REAR	28480	5040-7220	
	5060-9835	0	1	TOP COVER	28480	5060-9835	
	5060-9847	4	1	BOTTOM COVER	28480	5060-9847	
	5060-9862	3	1	SIDE COVER	28480	5060-9862	
	5060-9884	9	1	SIDE COVER STANDARD	28480	5060-9884	
	5040-7201	8	4	FOOT (STANDARD)	28480	5040-7201	
	1460-1345	5	2	TILT STAND	28480	1460-1345	
	4040-1685	9	2	HALF CARD CAGE	28480	4040-1685	
	03497-00101	3	1	LEFT DECK	28480	03497-00101	
	03497-00102	4	1	RIGHT DECK	28480	03497-00102	
	03497-00105	7	1	MAIN DECK	28480	03497-00103	
	03497-00104	6	1	A/D DECK	28480	03497-00104	
	03497-00204	7	1	REAR PANEL A/D	28480	03497-00204	
	03497-00601	8	1	BOTTOM SHIELD	28480	03497-00601	
	03497-00606	3	1	TOP SHIELD	28480	03497-00606	
	03497-00602	9	1	LEFT SHIELD	28480	03497-00602	
	03497-00603	0	1	RIGHT SHIELD	28480	03497-00603	
	03497-00613	2	1	FRONT SHIELD	28480	03497-00604	USE METRIC FASTENERS
	03497-00605	2	1	CONNECTOR SHIELD	28480	03497-00605	
	03497-04701	7	1	LEFT SUPPORT	28480	03497-04701	
	03497-04702	8	1	RIGHT SUPPORT	28480	03497-04702	
	03497-04103	3	1	PLATE SIDE	28480	03497-04102	
	03497-04108	8	1	DEFLECTOR, AIR	28480	03497-04108	
	5041-2385	1	1	HOUSING, FAN FILTER	28480	5041-2385	
	03497-01201	6	1	FAN BRACKET	28480	03497-01201	
	03497-01204	9	1	CONTROL BRACKET	28480	03497-01204	
	03497-01210	7	1	BATTERY BRACKET	28480	03497-01205	
	03497-01211	8	1	REAR BRACKET	28480	03497-01206	
	03497-01207	2	1	PANEL LATCH BRACKET	28480	03497-01207	
	1600-0966	2	1	HINGE	28480	1600-0966	
	4040-1859	9	1	REAR COVER	28480	4040-1859	
	03498-01204	0	1	BRACKET-REAR COVER	28480	03498-01204	
				NOTE MOST OF THE ABOVE CHASSIS COMPONENTS ARE ILLUSTRATED IN FIGURES 6-1 TO 6-14.			

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-3. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				CHASSIS MOUNTED COMPONENTS (ELECTRICAL)		
B1	03497-68501	9	1	FAN-COOLING ASSEMBLY	28480	03497-68501
BT1	1420-0233	4	1	BATTERY-6V RECHARGEABLE	28480	1420-0233
C1	0160-0162	5	2	CAPACITOR-FXD .022UF +-10% 200VDC POLYE	28480	0160-0162
C2	0160-0162	5		CAPACITOR-FXD .022UF +-10% 200VDC POLYE	28480	0160-0162
C3	0180-3026	4	1	CAPACITOR-FXD 29,000 UF 20VDC	56289	36DX293G020BB2A
CR1	1901-0496	1	2	DIODE-PWR RECT 100V 12A DO-4	04713	MR1121
CR2	1901-0496	1		DIODE-PWR RECT 100V 12A DO-4	04713	MR1121
CR3	1902-1232	7	1	DIODE-ZNR 5.6V	28480	1902-1232
F1	2110-0043	8	1	FUSE 1.5 AMP NTD 250V (110/120V OPTIONS)	75915	31201.5
	2110-0063	2	1	FUSE .75 AMP NTD 250V (220/240V OPTIONS)	75915	312.750
	2110-0564	8	1	FUSEHOLDER BODY 12A MAX FOR UL	H9027	031.1657
	2110-0565	9	1	FUSEHOLDER CAP 12A MAX FOR UL	28480	2110-0565
F2	2110-0001	8		FUSE 1A 250V 1.25X .25 UL	75915	312001
	1400-0008	9	1	FUSEHOLDER-BLOCK 15A 250V	28480	1400-0008
J18	9100-3121	5	1	LINE FILTER	28480	9100-3121
Q1	1854-0439	1	1	TRANSISTOR NPN	04713	SJ2922
S1	3101-0481	0	1	SWITCH-PUSHBUTTON	28480	3100-0481
S2	3101-2298	1	2	SWITCH-SLIDE	28480	3101-2298
S3	3101-2298	1		SWITCH-SLIDE	28480	3101-2298
T1	9100-4270	7	1	TRANSFORMER-POWER	28480	9100-2629
				MISCELLANEOUS COMPONENTS		
	03497-04107	7	1	PLATE-BUTCH	28480	03497-04107
	7120-8607	2	1	LABEL-METRIC	28480	7120-8607
	7122-0058	5	1	PLATE-SERIAL	28480	7122-0058
	5040-6843	2	1	EXTRACTOR-PC BOARD	28480	5040-6843
	5000-9043	6	1	PIN-EXTRACTOR	28480	5000-9043
	3150-0232	2	1	FILTER-AIR	28480	3150-0232
	7121-1139	3	1	LABEL-3497A COMMANDS	28480	7121-1139
				CONNECTORS		
J1	1251-3977	0	1	CONNECTOR 2 PIN M UTILITY	27264	03-06-2023
P1	1251-3982	7	1	CONNECTOR 2 PIN F UTILITY	27264	03-06-1023
	1250-0083	1	6	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	1510-0091	3	3	BINDING POST SGL SGL-TUR JGK RED (GUARD & CURRENT SOURCE)	28480	1510-0091
	1510-0111	8	2	BINDING POST SGL SGL-TUR JGK RED (VM INPUT)	28480	1510-0111
	8120-3057	7	1		28480	8120-3057
				CABLES		
J12	8120-3280	8	1	CABLE ASSY-HPIB	28480	8120-3280
W1	03497-61602	7	1	CABLE (VM INPUT)	28480	03497-61602
	8120-3995	2	1	CABLE, BATTERY	28480	8120-3995
				NOTE		
				MOST OF THE ABOVE COMPONENTS ARE ILLUSTRATED IN FIGURES 6-1 TO 6-14.		

See introduction to this section for ordering information
*Indicates factory selected value

SECTION VI
BACKDATING

Not applicable.

SECTION VII
THEORY OF OPERATION

7-1. INTRODUCTION

7-2. This section of the manual has the theory of operation for the 3497A mainframes (both HP-IB and Serial I/O), front panel, and voltmeter option. If the standard front panel or voltmeter option are deleted, ignore the explanation for that circuitry. The theory of operation is separated as follows:

3497A Description - paragraph 7-3
Mainframe Block Diagram Theory of Operation - paragraph 7-6
Outguard Controller Circuitry Description - paragraph 7-11
HP-IB Circuitry Description - paragraph 7-53
Serial I/O Circuitry Description - paragraph 7-55
Timer/Pacer Circuitry Description - paragraph 7-57
Front Panel Circuitry Description - paragraph 7-82
Crossguard Logic Circuitry Description - paragraph 7-99
Inguard Logic Circuitry Description - paragraph 7-110
Voltmeter Block Diagram Theory of Operation - paragraph 7-126
DC Voltmeter Circuitry Description - paragraph 7-135
DC Current Source Circuitry Description - paragraph 7-209
Power Supplies - paragraph 7-221

7-3. 3497A DESCRIPTION

7-4. The 3497A consists of a mainframe and a variety of plug-in options. The mainframe is used to control instrument operation, including the plug-in options. The front panel is part of the mainframe, but the plug-in options are not. The plug-in options do, however, need the mainframe to operate.

7-5. Two different types of mainframes are available for the 3497A. One mainframe (the standard mainframe) may be remotely programmed and controlled by an HP-IB compatible computer or controller. The other mainframe may be remotely programmed and controlled over the Serial I/O Bus (RS-232C or RS-449/423). Remote control is the only difference between the two mainframes; other circuitry in the mainframes is the same (e.g., Inguard Logic Circuitry, etc.). Both mainframes can be locally programmed using the standard front panel. Local programming is not available, if the standard front panel is deleted (Option 260).

7-6. MAINFRAME BLOCK DIAGRAM THEORY OF OPERATION

7-7. Refer to Figure 7-1 for the following explanation of the mainframe block diagram theory of operation (both Serial I/O and HP-IB mainframes).

7-8. The mainframe consists of two major sections, Outguard and Inguard. The Outguard Section controls the operation of the instrument and the digital plug-in options. It also has the circuitry to interface with the HP-IB or Serial I/O, and the front panel. Since the Outguard Section controls the whole instrument, it also controls the Inguard Section. Communication between the inguard and outguard sections is over the Crossguard Logic Circuitry. The Inguard Section controls the operation of the analog plug-in options and the voltmeter option.

7-9. The Outguard Section consists of an outguard controller, timer/pacer circuitry, front panel, HP-IB or Serial I/O circuitry, and other associated circuitry. The outguard controller board has the main circuitry which controls the operation of the instrument. The front panel is used to display readings and to transfer information from the keyboard circuitry to the outguard controller. The HP-IB or Serial I/O circuitry transfers information between the outguard controller and the HP-IB or Serial I/O, respectively. The timer/pacer circuitry is used to run the instrument's real time clock and output Timer Output and Timer Interval pulses (at the rear panel TIMER output port).

7-10. The Inguard Section consists of an inguard controller, A/D logic, and (if Option 001 is installed) the voltmeter circuitry. The inguard controller is the main circuitry in the inguard section and it controls the operation of the inguard circuitry, including the voltmeter option and the analog plug-in options. The A/D logic is used to control the A/D (analog-to-digital) operation of the voltmeter option and is only used if the option is installed. It is, however, part of the inguard circuitry whether the voltmeter option is installed or not.

7-11. OUTGUARD CONTROLLER CIRCUITRY DESCRIPTION

7-12. For the following explanation of the standard (HP-IB) mainframe, refer to Figure 8-E-3 (Outguard and HP-IB Controller Block Diagram) and Schematic A1 (Outguard Controller and HP-IB Controller). For the explanation on the Serial I/O mainframe, refer to Figure 8-E-5 (Outguard and Serial I/O Controller Block Diagram) and Schematic A2 (Outguard and Serial I/O Controller). All figures and schematics are located in Service Group E.

7-13. The main part of the outguard section, the outguard controller, consists mostly of the outguard processor (U11), a RAM , and various ROMs. The outguard processor in conjunction with the ROMs and the RAM control the digital communication between the front panel

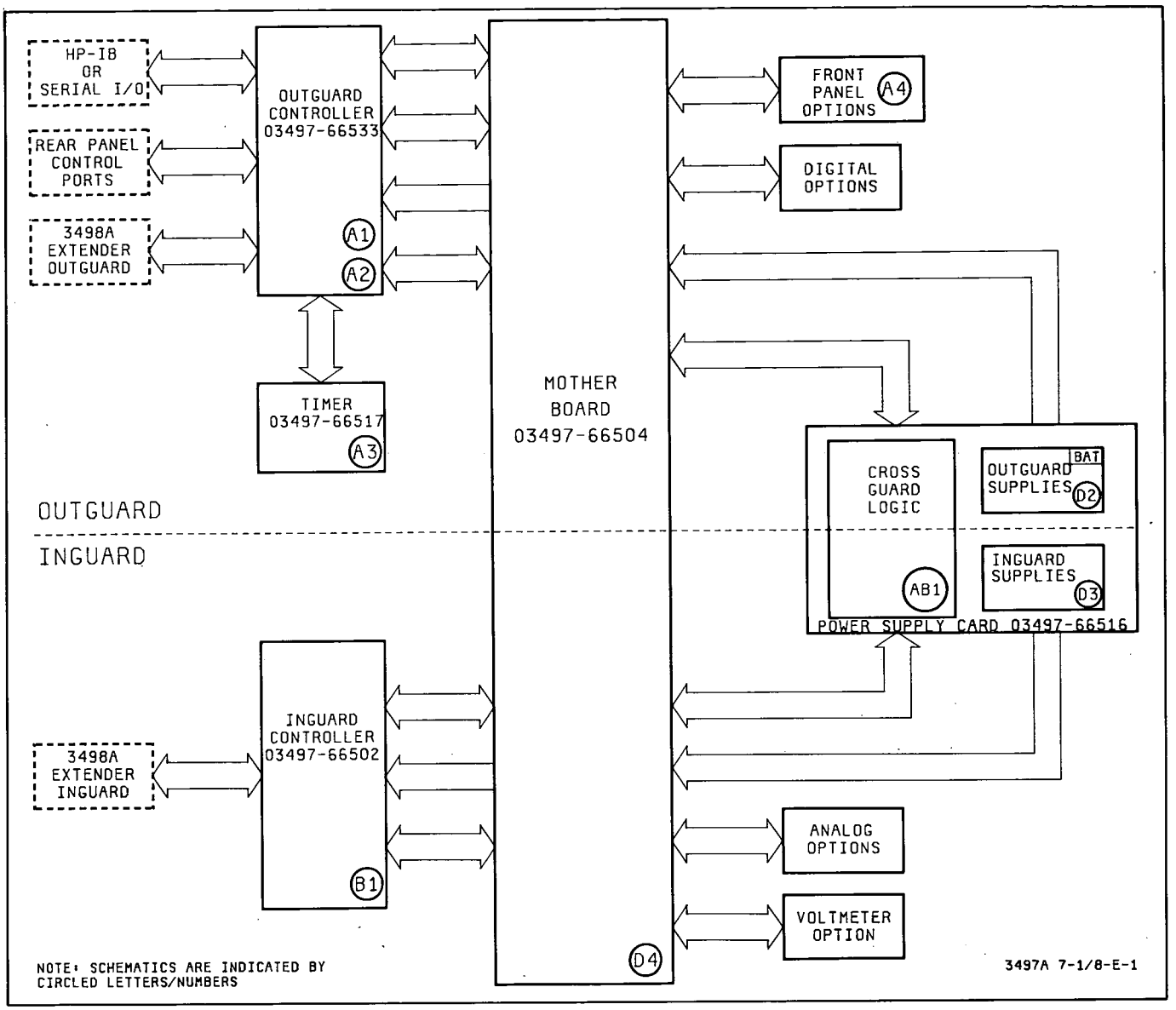


Figure 7-1. Block Diagram of the 3497A Mainframe

(both keyboard and display), HP-IB or Serial I/O circuitry, and Inguard Section. In addition, the processor also controls the timer/pacer circuitry, 3498A Extender (digital functions only), rear panel ports, and digital plug-in options.

7-14. Outguard Processor

7-15. The outguard processor (U11) communicates with the ROMs (U12, U16, U20, and U24) and the RAM (U30) using a 16 bit address bus (A0 through A15) and an 8 bit data bus (D0 through D7). Communications with the other circuits (e.g., front panel, HP-IB, etc.) is over part of the address bus and all of the data bus. Communication using the data bus is through a bi-directional buffer (U34). The data lines become the buffered data lines (BD0 through BD7) after going through the buffer. The direction of the buffer is controlled by address line A15 and R/W latch U19A. The necessary clock and reset signals for the processor are generated by U10 (see paragraph 7-19 through 7-26). The processor pin assignments and corresponding functions are given in Table 7-1.

7-16. ROMs (U12, 16, 20, and 24) and RAM (U30)

7-17. ROM U12 is an optional 32K ROM and is only installed if the counter option (Option 060) is installed in the instrument. If the counter option is not installed, U12 is an empty socket. ROMs U16 and U24 are both 64K ROMs and ROM U20 is a 132K ROM and all ROMs contain the system firmware, including the signature analysis (SA) routines. A ROM is selected by ROM select decoder U15A in conjunction with U22B. The decoder is enabled when address line A15 is high. A particular ROM is selected by address lines A13 and A14. These address lines are also used to select peripheral decoders U31 through U33, when address line A15 is low. In addition to ROMs U16, U20, and U24, there is an additional space for

Table 7-1. Microprocessor Pin Assignments

Signal Designation	Pin Number	Type	Function	Signal Designation	Pin Number	Type	Function
VSS	1	Input	Circuit GND.	A0-A15	9-20 22-25	Output	Address Bus.
HALT	2	Input	This line is tied to + 5V through a 10k Ω pull up resistor. This high state causes the uP to fetch and execute instructions without ever entering a wait (or halt) state. If this line was allowed to go low, the uP would enter a wait state after executing the instruction being currently processed.	VSS	21	Input	Circuit GND.
				D0-D7	26-33	Input/ Output	Data Bus.
				R/W	34	Output	Read/Write Line. When high, the uP will input data (read); when low, the uP will output data (write).
01	3	Input	Phase 1 clock from the U10 clock generator.	STANDBY	35	Input	Not used.
IRQ	4	Input	Interrupt Request. When this line goes low, the uP will complete the instruction it is executing and begin an interrupt sequence (assuming it's interrupt mask bit is not set in its condition code register).	DBE	36	Input	Data Bus Enable. When high, this will enable the data bus output drivers. The data bus output drivers are disabled internally when the uP goes to the read state.
				02	37	Input	Phase 2 clock from U10 clock generator.
VMA	5	Output	Valid Memory Address. The uP drives this line high to indicate that a valid address is present on the address bus.	XTAL	38	Input	Crystal Input. Not used.
				TSC	39	Input	Three State Control. When high, the uP tri-states the address and data buses. This releases the buses to be used by other devices. However, TSC must not be held high longer than 4.5 uS or the uP will clear its internal memory.
NMI	6	Input	Non-Maskable Interrupt. This line is tied to + 5V through a 10k Ω pull up resistor. If this line was permitted to go low, which it isn't, it would cause a non-maskable interrupt sequence to be generated.	RESET	40	Input	This line resets the uP. The U10 clock generator activates this line in conjunction with 01 and 02 to properly initialize the uP.
BA	7	Output	Bus Available. Not used.				
VCC	8	Input	+ 5V.				

another ROM (U9). This space is for possible future applications.

7-18. RAM U30 is a 1Kx8 RAM that is enabled when pin 15 of decoder U31 goes low. When enabled, the RAM can be written to when pin 8 of U18 is low and can be read from when this pin is high. The jumper wire used to tie the most significant bit of the RAM address high is there for future expansion to a 2Kx8 RAM.

7-19. Power-On and Low Power Reset

7-20. The processor needs to be reset to a defined state after power-on occurs. The reset occurs when its RST line (reset at U11 pin 40) changes from a low to a high state. This is developed by the clock generator, U10, when its pin 12 input (RESET) changes from low to high. The low to high input at pin 12 of U10 is developed by U51.

7-21. After the 3497A is turned on, it takes a little time for the instrument's power supplies to come up to the correct values. During this time, the RESET input at pin 12 of U10 (i.e., output at U51 pin 9) is low. This makes the output at pin 14 of U10 also low and prevents the processor from turning on. When the power supplies come up to the correct value, the clock signals for the processor (at pins 1 and 2 of U10) are then generated and output by U10. At the time when the power supplies are up, pin 9 of U51 (RESET input at pin 12 of U10) also goes high. This in turn sets the output at pin 14 of U10 high after at least eight clock cycles have been generated by U10. This is determined by U10. When pin 14 of U10 goes high, the processor's RST line goes high and the processor is set to its turn-on state.

7-22. During a low power or brown out condition, C24 discharges through U51. After it has discharged sufficiently, the reset signal to the processor is activated. This keeps the processor in a known state and prevents it from performing illegal operations or entering into illegal states.

7-23. Clock Circuitry

7-24. The outguard processor requires two clock signals which are generated by clock generator U10. The signals, called $\phi 1$ and $\phi 2$, are 180 degrees out of phase and are at a frequency of 1.5MHz.

7-25. A 3MHz signal, output at pin 5 of U10, is also developed by the clock generator U10 and crystal Y1. This clocks the clock stretcher U14. The D input at pin 2 of U14 is 1.5MHz and comes from the B$\phi 2$ output of U10. The B$\phi 2$ output makes the duty time of the Q output of

U14 greater than the D input. The output is then routed to the DBE input of the processor to enable the data bus drivers (see DBE explanation in Table 7-1). The clock stretcher waveforms are shown in Figure 7-2.

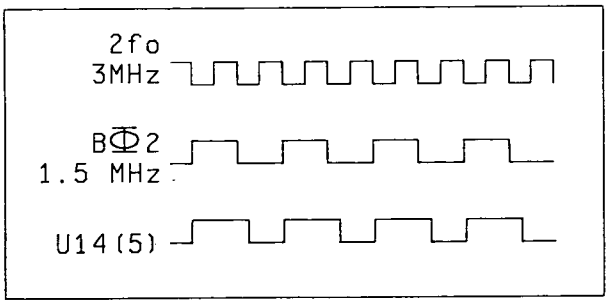


Figure 7-2. Clock Stretcher Waveforms

7-26. The output at pin 6 of U14 is delayed by U13C and U13D for approximately 20nS. This output is then used to clock the R/W latch (U19A) and Extender Buffer Enable flip-flop (U19B). The signal is also ANDed with VMA from the processor to clear the Valid Memory Address latch (U14). The 20nS delay gives the data inputs to U19A and U19B time to settle before U19 is clocked.

7-27. Status Read Circuitry

7-28. The Status Read buffer is U41. It is used to buffer the various status signals to be read by the microprocessor. The buffer, when enabled by peripheral decoder U33 (pin 14 of U33), is read by the processor via bi-directional buffer U34.

7-29. Different circuitry, like the timer circuitry and digital plug-in options, can interrupt the processor. The interrupts are generated via AND gate U23A. If any input to U23A is low, the gate generates an interrupt. When the processor detects an interrupt, it reads the Status Read buffer to determine what is interrupting and responds accordingly.

7-30. Latches U25A and U25B are for external increment and external voltmeter trigger input pulses, respectively. These latches, when set, notify the processor of their respective functions when a status read is performed on buffer U41. The processor clears these latches with signals generated by peripheral decoders U31 and U32. Refer to paragraph 7-51 and 7-48 for more information on the external increment and external voltmeter trigger operations, respectively.

7-31. Interfacing to the 3498A Extender

7-32. The 3498A Extender is interfaced to the outguard controller over tri-state bus transceiver U4. The transceiver is enabled when the U19B Extender Buffer Enable flip-flop is cleared. The flip-flop is cleared by the Extender Read/Write signals that are generated by peripheral decoder U31. The direction of U4 is determined by the R/W latch U19A. When U19A is cleared, data is output to the 3498A and when U19A is set, data is input from the 3498A to the outguard processor. The data lines going to the 3498A, after going through the bus transceiver U4, are called ED0 through ED7 instead of D0 through D7.

7-33. Resistor pack RP2, consisting of pull-up and pull-down resistors, permits the Extender Data Bus to float to about 3.4V, regardless of the number of Digital Extenders connected. This reduces crosstalk between commonly bused instruments and creates a better bus transmission environment.

7-34. The address bus to the 3498A Extender is transferred through buffers U3A, U3B, and U5. The address lines going to the Extender, after going through buffer U3 and U5, then change from A0 through A7 to EA0 through EA7. The different address bits of the bus are defined as follows:

a. Bits EA0, EA1, and EA2 are used for register select on the digital plug-in options (refer to the option manual for a detailed description).

b. Bits EA3, EA4, EA5, and EA6 are used to decode one of the ten selectable slots of the 3498A Extender card cage.

c. Bits EA7, EA8, and EA9 determine the 3498A Extender box address. Note that Address 0 cannot be used for an extender because it is always reserved for the 3497A.

7-35. The digital extender interrupt signal is not generated by the 3498A Extender but by the digital plug-in option in the extender. The extender is only used to transfer the interrupt signal from the plug-in to the outguard controller. Refer to the plug-in option's service manual for more information on the interrupt operation.

7-36. The digital extender reset signal is asserted with a mainframe reset. This reset will open all 16 channel actuator relays, initialize all digital option handshake lines, and disable the interrupt capability on 16 channel digital input cards.

7-37. A digital extender plug-in option is enabled by peripheral decoder U31 and permits the 3498A Extender to send information to the 3497A outguard circuitry.

7-38. A digital extender write is also enabled by a peripheral control signal from U31 and enables the 3498A Extender to receive information from the 3497A.

7-39. Address Bus Peripheral Control

7-40. The address bus, bits A0 through A15, is used to control the peripheral decoders (see next paragraph), digital plug-in options, and the 3498A Extender. The significance of the address bits are as follows:

a. A0, A1, and A2 select the digital plug-in options.

b. A3, A4, and A5 are decoded by U45 to determine the slot select enable for the 3497A card cage. This enable allows the plug-in option within the addressed slot to begin operating. The only valid slots for the 3497A are from 0 to 4.

c. A6, A7, A8, and A9 are not coded for use by the mainframe outguard control. However, in the 3498A Extender, A6 is used for an additional bit to decode slot select. A7, A8, and A9 are used for the 3498A Extender box address. The 3497A has an address of 0.

d. A10, A11, and A12 are coded for peripheral select (see next paragraph).

e. A13 and A14 are ROM select signals when A15 is high and peripheral address signals when A15 is low. The ROM select decoder (U15A) is enabled when A15 is high and the peripheral address decoder (U15B) is selected when A15 is low.

7-41. Peripheral Decoding

7-42. The peripheral decoders are used to control the 3497A's front panel, timer/pacer, rear panel BNC ports, digital plug-in options, etc. The decoders consist of U31, U32, and U33. When address decoder U15B is enabled (address line A15 is low), U15B decodes address A13 and A14 to select one of the peripheral decoders. In addition, the Valid Memory Address latch output (U14 pin 9) is also used in selecting one of the peripheral decoders. Once a decoder is selected, buffered address lines BA10, BA11, and BA12 (see next paragraph) are decoded by the decoders to generate the necessary output pulses (500nS wide) to control the 3497A's peripheral circuitry (front panel, timer/pacer, etc.).

7-43. Address lines A0 through A2 and A10 through A12, before going to the peripheral decoders and other parts of the 3497A, go through buffer U29. These lines then become buffered address lines BA0 through BA2 and BA10 through BA12.

7-44. Break Before Make (BBM) Sync Output Signal

7-45. The Break Before Make Sync Signal, output at the 3497A's rear panel "BBM SYNC" connector, shows that a channel closure has occurred within the 3497A/3498A system. Typically, BBM is used for HP-IB applications where multiple 3497As are used in a system. When used in this fashion, all the BBM outputs of the 3497A's in the system are wired ANDed. If any one BBM signal goes low, it will be noted by the other 3497As that a channel closure has occurred. Further channel closure will not be allowed until BBM goes high again.

7-46. The BBM signal is sent out by U21 and U18A. While a channel is opening, the inguard controller sends a message to the outguard processor over the data bus with D7 on the bus set to 0. The outguard processor responds immediately by generating a peripheral BBM clock pulse (U32 pin 15). This latches a low into U21 and prohibits other channels from closing. Then, when that channel opens, the inguard controller sends another message to the outguard processor but, at this time, with D7 set to 1. The outguard processor then generates another BBM clock pulse via U32 pin 15 causing a 1 to be latched by U21. This enables the next channel to be closed.

7-47. Input and Output Ports

7-48. External Trigger. This port is an input port and is only operational if the voltmeter option (Option 001) is installed in the 3497A. The voltmeter option has to be set to the External Trigger mode to externally trigger it.

7-49. When a negative going trigger pulse is applied to the EXT TRIG input port, it gets inverted by U13A. The output of U13A then clocks flip-flop U25B which makes its Q output go high. This high is fed to the Read Status Buffer (U41 pin 16) and when the buffer is enabled, the outguard processor reads the buffer and determines that a trigger was initiated. The processor then takes the appropriate action. After this action is taken, flip-flop U25B is cleared by the processor using peripheral decoder U31 (pin 7).

7-50. Only negative pulses applied to the input port will cause a trigger since the port is tied to +5V through R2. Resistor R17, and diodes CR11 and CR13 are used for input protection.

7-51. External Increment. This input port is used to increment the 20 Channel Relay Board (Option 010 and/or Option 020) to the next channel. The operation is similar to the external trigger operation (see paragraph 7-48 and 7-49) in that a negative pulse is applied to the EXT INCR port, then inverted by U13B which clocks U25A. The Q output of U25A is applied to pin 18 of U41 which transfers the information to the processor upon being read. Flip-flop U25A is cleared by the processor using decoder U32 (pin 11).

7-52. Channel Closed and Voltmeter Complete. These are output ports and output a pulse at the CHANNEL CLOSED and the VM COMPLETE ports after a channel is closed on the Channel Relay Board or the voltmeter option has completed a measurement cycle, respectively. The output pulses (positive pulses) are generated by peripheral decoder U32. Diodes CR3 through CR6 are protection diodes to protect U32 in case a voltage or signal is inadvertently applied to the output ports.

7-53. HP-IB CIRCUITRY DESCRIPTION

7-54. All interfacing between the outguard processor and the HP-IB (Hewlett-Packard Interface Bus) is accomplished by the HP-IB controller (U8) and two bidirectional bus drivers (U1 and U7). The HP-IB controller changes the data sent and received by the outguard controller to the necessary HP-IB information (e.g., Listen,

Talk, etc.). The bus drivers transfer the information between the HP-IB and the HP-IB controller. Other HP-IB circuitry includes the Address Switch and a buffer, which are used to set the 3497A's HP-IB address. In addition, the circuitry includes a flip-flop that is used only for the Talk-Only mode. The HP-IB circuitry operation is as follows (refer to Figure 8-E-3 and Schematic A1, in Service Group E, for the explanation):

a. The HP-IB controller (U8) is continuously clocked by the Bϕ signal at pin 7 of U10. This clock is necessary for the controller to operate.

b. The HP-IB controller is also reset at power-on. This is done by the same line that resets the outguard controller at power-on.

c. For the HP-IB controller to send or receive data, its CS line (Chip Select at pin 3 of U8) has to be low. This low is generated by the outguard controller using peripheral decoder U31 (pin 14).

d. When the HP-IB controller is addressed by the outguard controller and the R/W (Read/Write) line of U8 is low, data is then transferred to the HP-IB controller by the outguard controller. Depending on the address selected, U8 interprets the data as commands (ATN, SRQ, etc.) or data (DI01 or DI07). The data is transferred over the outguard controller's data lines (D0 through D7) and addressing is done over the A0 through A2 address lines, which are the R0 through R2 lines of U8. The R/$\overline{W}$ line of U8 gets its low from the R/W line of the outguard processor.

e. The HP-IB controller develops an interrupt when it needs to send data to the outguard controller. The interrupt occurs when the INT line of U8 (pin 40) goes low. Since the line connects to AND gate U23A (pin 5), U23A interrupts the outguard processor.

f. When U8 is addressed by the outguard controller and the R/W line is high, data is transferred to the outguard controller from the HP-IB controller. This data is also sent over the data lines (D0 through D7) and may be remote data from the Bus (Remote, Local, etc.).

g. The address switch setting is determined by the outguard controller using the HP-IB controller and buffer U2. When U8 is addressed (and depending on the address) the $\overline{ASE}$ line of U8 (pin 4) is set low. This enables buffer U2. The output of the buffer is then read by the main controller over the data lines. The address switch setting can then be determined since the switch is connected to the input of the buffer. The only part of the switch not directly connected to the buffer is the Talk-Only switch. It goes through flip-flop U21B. This is to make sure that the Talk-Only mode cannot be selected while the instrument is on. To select the mode, turn the instrument off. Then set the address switch to the correct setting. After turning the 3497A on, the instrument is then set to the Talk-Only mode.

h. The bi-directional bus drivers transfer data to or from the HP-IB depending on the position of the Talker/Listener outputs of the HP-IB controller (T/R1 and T/R2 at U8 pins 27 and 28, respectively). When the lines are high, data is transferred from the HP-IB controller to the HP-IB. When the lines are low, data is transferred from the Bus to the HP-IB controller.

7-55. SERIAL I/O CIRCUITRY DESCRIPTION

7-56. Interfacing between the outguard controller and the Serial I/O is accomplished using the Universal Asynchronous Receiver Transmitter U8 (UART). The transmitter is controlled by the outguard controller and is used to convert the incoming serial data stream into parallel data. It also converts parallel data from the outguard processor to serial data for transmission. The UART also has handshake lines which are used when the 3497A is configured for modem operation. Additional circuitry includes a buffer and configuration switch S1 (which is used to configure the 3497A to different speed of operation, word length/parity, etc.). Another circuit is switch S2. It is used to select the instrument for either the RS-232C interface or the RS-449/423 interface. The Serial I/O circuitry operation is as follows (refer to Figure 8-E-5 and Schematic A2, in Service Group E, for the explanation):

a. The UART (U8) is, as is the outguard processor, reset at power-on. This is done by NOR gate U62D which receives its input from the same line that resets the outguard controller at power-on.

b. For the UART to send or receive data, its $\overline{CS2}$ (Chip Select 2 at pin 3 of U8) has to be low. This low is generated by the outguard controller using peripheral decoder U31 (pin 14).

c. When the UART is addressed by the outguard controller and its $\overline{DISTR}$ line is low, data is then transferred to the UART by the outguard controller. The data is transferred over the outguard controller's data lines (D0 through D7) and addressing is done over the A0 through A2 address lines. The $\overline{DISTR}$ line gets its low from the R/$\overline{W}$ line of the outguard processor.

d. The UART generates an interrupt when it needs to send data to the outguard controller. The interrupt occurs when the $\overline{INT}$ line of U8 (pin 30) goes low. Since the line connects to AND gate U23A (pin 5) through NOR gate U62D, U23A interrupts the outguard processor.

e. When U8 is addressed by the outguard controller and the $\overline{DISTR}$ line is high, data is transferred to the outguard controller from the UART. This data is also sent over the data lines (D0 through D7).

f. The UART operates at TTL levels and the Serial I/O operates at positive and negative voltage levels (RS-232C voltage levels). Because of this, the voltage levels are shifted to TTL levels by U1A through U1D as is the data sent to the UART. Likewise, U6 and U7 change the TTL levels from the UART to the RS-232C voltage levels for transmission over the serial bus. The data is sent to the bus using line SDA and received from the bus using line RDB.

g. The configuration switch setting is determined by the outguard controller using buffer U2. When the buffer is enabled by the outguard processor, using decoder U31 (pin 10), the output of the buffer is then read by the main controller over the data lines. The switch setting can then be determined since the switch is connected to the input of the buffer.

7-57. TIMER/PACER CIRCUITRY DESCRIPTION

7-58. The Timer/Pacer Circuitry is on a small board that plugs into the Outguard Controller Board. The circuitry has two timing related circuits, a timer and a pacer, in addition to a real time clock. Unless otherwise noted, refer to Figure 8-E-7 (Timer/Pacer Block Diagram) and Schematic A3 for the following explanation on the timer and the pacer circuitry. Both Figure 8-E-7 and Schematic A3 are in Service Group E.

7-59. Timer Circuitry Operation

7-60. The main part of the circuitry is U4, a microcomputer (μC), which is configured as a non-volatile real-time clock. In addition, the μC also has a programmable alarm function, programmable timer interval outputs, and control circuitry for the gating logic. The alarm can be set at any time in the 24 hour clock. The timer interval outputs can be set from 1 second to 11 days. The gating logic is used to select the timer or pacer operations.

7-61. Microcomputer (U4). The microcomputer (μC) is controlled by the outguard controller. This is accomplished using the buffered data bus (BD0 through BD7). The pin assignments of U4 and corresponding functions are located in Table 7-2.

7-62. The commands from the outguard controller (sent over data bus BD0 through BD7) consists of input or output set-up information for U4. When U4 has assumed the proper state, the data bus is then used to transfer data. As an example, suppose that the real time clock is to be set. First, the outguard controller flags U4 that it wants to talk. The μC then reads the data bus which contains a command that the clock is being set and that the next byte of data will be the time. A similar sequence occurs when the alarm function and timer interval are set, or when the time of day or elapsed time is read.

7-63. The μC needs to be initialized (i.e., reset) after power-on occurs. This is done by the RESET line which is also used to reset the outguard processor (U11 on Schematic A1 or A2). A high on the line shows that the Outguard Section of the 3497A has power. The reset signal is connected to the base of Q1 where it is inverted and then connected to the P22 (pin 23) port of U4. Refer to Table 7-2 for more information on port P22.

7-64. Buffer U12 is used to output data from the μC to the outguard controller. The buffer is a tri-state device enabled by the outguard controller (READ TIME from U35 pin 9 on Schematic A1 or A2). Refer to paragraph 7-66 for more information on data transfer.

7-65. All power supplies for U4 are from the line marked "BATTERY" on the schematic. This supply provides power from the 3497A's ac power source, except when power fails. If a power failure occurs, battery power is switched in immediately and the Time of Day (TD) and Elapsed Time (TE) functions are backed up. These are the only functions that are backed up, all other functions (pacer, etc.) have to be selected again.

7-66. Data Transfer to Timer. Data from the buffered data bus is latched to U4 using octal D type latch U9. When the output enable line of U9 (pin 1) is high, its output is placed in a high impedance state. No data is being transferred to the μC. When the output enable line is low, the D inputs of U9 are transferred to the Q outputs with the rising edge of the TIMCTL clock at pin 11 of U9. The TIMCTL clock is generated by the outguard controller (from U33 pin 12 on Schematic A1 or A2). The outputs are enabled by the μC and the outguard controller provides the clock to latch the data.

7-67. Sending data to the timer circuitry is explained as follows:

a. To send data to the timer, line SR/$\overline{W}$ (from U19A pin 6 on Schematic A1 or A2) is set high. This line is also the D input to flip-flop U3A.

b. When U9 pin 11 (the TIMCTL line) is pulsed, data over D0 through D7 is transferred into latch U9.

c. Since the TIMCTL line also clocks U3A, the flip-flop sets the P23 line of U4 low. The low on line P23 is read by the microcomputer which then enables the output of U9. The data in U9 is then latched into the microcomputer. The microcomputer then interprets the data and takes the appropriate action. The data may include the commands to send data back to the outguard processor. If this is the case, the μC will then be enabled to send data (see paragraph 7-66).

d. After the data has been transferred, the P03 line of U4 goes low and then high again. This clocks flip-flop U3B into a set state and in turn causes the TIMER PCTL line to go low.

e. A low on the TIMER PCTL line is sensed by the outguard controller and it knows that data transfer is complete.

Table 7-2. Microcomputer (U4) Pin Assignments

Signal Designation	Pin Number	Type	Function
----	1	----	Not used
XTAL2	2	Input	Crystal input for the internal oscillator.
XTAL2	3	Input	Crystal input for the internal oscillator.
RESET	4	Input	When low, this will initialize the uC.
SS	5		Single Step. Not used. This line is made inactive by being tied to +5V through a 1k Ohm pullup resistor.
INT	6		Interrupt. Not used. This line is made inactive by being tied to +5V through a 1k Ω pullup resistor.
EA	7		External Access. Not used. Tied to ground.
RD	8		Read Strobe. Not used.
PSEN	9		Not used.
WR	10		Write Strobe. Not used
ALE	11	Output	Address Latch Enable. This signal, although not used by external circuitry, is activated with each cycle. This makes it useful to check the internal clock of the uC.
P00-P07	12-19	Input/ Output	Bi-directional Data Bus. Only pins 12 thru 16 are connected. Pins 17, 18 and 19 are not used. These lines are used as output control lines as follows: pin 12 - used to enable U9 when the Outguard uP notifies it has data to send; pin 13 - used in conjunction with pin 14 to specify whether the pacer or the uC will be outputting the timer interval signal; pin 14 - the pacer can only generate a timer interval from 100 uS to approximately 1 S (in 100 uS steps). The uC can generate a timer interval from 1 S to 11 days (in 1 S steps). By using pins 13 and 14, the uC can control whether the uC or the pacer outputs the timer interval signal. If pin 13 is low, the interval signal is output by the pacer; if pin 13 is high, the uC outputs the interval signal on pin 14;
			pin 15 - this line is used by the uC to clock U3B; pin 16 - this line is the Timer Interrupt Output Signal. It is active whenever a time match is made from a Timer Alarm Function, or a Timer Interval signal from a "TI" command occurs. It is used to generate an interrupt to the Outguard uP when the mask is properly set.
GND	20	Input	Circuit GND.
P20	21	Input	A jumper wire ties this line to ground and formats the date as dd:mm:yy. If the jumper is removed, the date format will be mm:dd:yy.
P21	22		Not used.
P22	23	Input	The timer uC is battery powered. This line monitors the power of the Outguard uP and, if it is lost, it permits the timer uC to go into a mode which conserves battery power.
P23	24	Input	This is a read/write line from the Outguard uP. When low, the timer uC is being directed to send data via the U9 buffer; when high the timer uC is being directed to receive data.
PROG		25	Not used.
VDD	26	Input	+5V.
P10-P17	27-34	Input/ Output	Bi-directional Port which connects to the data bus that goes to the Outguard uP.
P24-P27		35-38	Not used.
T1	39	Input	This input is monitored to sense a change in the Q output of U3B. This change will occur only when the Outguard uP wants a data exchange and issues a TIMCTL signal. When this signal is detected, the R/W line (pin 24) is sampled to see if the operation will be a read or a write.
VCC	40	Input	+5V.

7-68. Data sent from the timer occurs as follows:

a. Buffer U12 is enabled by the outguard controller by setting the READ TIME line low.

b. Since U4 previously received the commands to transfer data to the outguard controller (see previous paragraph), the microcomputer sets its P00 line high to disable U9. Data is then transferred to the data bus using buffer U12.

c. At the same time, line P03 is pulsed and sets flip-flop U3B. This in turn sets the TIMER PCTL line low.

d. A low on the TIMER PCTL line is sensed by the outguard controller and it knows that data is ready.

7-69. Timer Alarm. The timer alarm enable information and set-up information going to U4 comes from the outguard controller over the data lines (see paragraph 7-66). Once U4 is set up and the selected alarm time is reached, the TIMER INTERRUPT line (U4 pin 16) goes low. This line will then interrupt the outguard processor (using AND gate U23A; see Schematics A1 or A2). The outguard processor will then take the appropriate action. The timer alarm is only enabled if the timer alarm bit in the Service Request Mask (SRQ) is set.

7-70. Timer Interval. The timer interval pulses are generated by U4 and output at its P02 line (pin 14). The information for the time period of the pulses and if the pulses are to be output, comes from the outguard controller using the data bus. When this information is received, the P01 (U4 pin 13) line of the μC goes high. This high sets-up the gating logic in such a way (see paragraph 7-80), that the timer interval pulses will be output over the TIMER line, instead of the timer output pulses.

7-71. Pacer Circuitry Operation

7-72. The pacer circuitry is used to generate the timer output pulses, which have a time range from 100μS to 999mS. The pacer circuitry consists of four BCD counters (U6, U7, U10, and U13) and two data latches (U8 and U11). The circuitry receives its program information from the outguard controller.

7-73. Data latches U8 and U11 are type D latches and transfer BCD data from the outguard controller to the counters. This data is then used to program the counters. Latch U11 and U8 transfer data when they are clocked by the LO PACER INT and HI PACER INT lines. The signal on these lines is also generated by the outguard controller using peripheral decoder U32 (see Schematics A1 or A2). The operation of the counters is explained in the following paragraphs.

7-74. The counters are programmable divide-by-N counters. Each counter has internal circuitry that divides the input clock frequency (CLK inputs at pin 6) by 10 and then outputs the new frequency (Q4 outputs at pin 1). The first counter (U10) input is at 10KHz which gets divided down to 1KHz. Since the counters are configured for a ripple count, the Q4 outputs of U13 and U7 are 100Hz and 10Hz, respectively. The output of U6 is not connected.

7-75. The 10KHz clock input to the first counter (U10) is generated by BCD counter U2. The input to U2 is at 1.5MHz (the BBϕ2 clock from U13F; see Schematics A1 or A2) and, since U2 is configured to divide by 150, the output frequency is divided down to 10KHz.

7-76. The CF (cascade feedback) input of each programmable counter will, if held low, disable the counter 0 output. When CF is high, the 0 output will be at a frequency which is equal to the input clock divided by the decimal equivalent of the BCD input. The PE (preset enable) line, when pulsed, loads the BCD inputs, which determines what the 0 output frequency will be.

7-77. An example on how the pacer circuitry operates follows this paragraph. In the example, each counter is loaded in with a BCD number of 0101 (decimal 5). As you go through the example, keep in mind that the Q4 and 0 outputs of the counters are independent from each other. The Q4 outputs are at a frequency 1/10 of the input clock and that the 0 outputs are the decimal equivalent of the loaded in BCD number. Also, the 0 output is enabled when CF input to the counter is high and disabled when low. The example is as follows:

a. A BCD number of 0101 (decimal 5) is loaded into each counter by latches U8 and U11.

b. Counter U6 is being clocked at 10Hz by U7 and its CF line is held high. This enables its 0 output continuously. However, until U6 reaches a terminal count, its 0 output will be low. Since the 0 output of U6 is connected to the CF input of U7, a low causes the 0 output of U7 to be disabled.

c. When U6 starts to count, its 0 output pulses high after .5 seconds. This is because U6 is clocked at 10Hz and the BCD number loaded in is 0101 or 5 (10Hz divided by 5 = 2 or .5 seconds).

d. When the 0 output of U6 goes high, counter U7 is enabled and starts counting via its CF input. The 0 output of U7 goes high after .05 seconds (100Hz divided by 5 = 20Hz or .05 seconds).

e. When the 0 output of U7 goes high, counter U13 is enabled and starts counting via its CF input. The 0 output of U13 goes high after .005 seconds (1KHz divided by 5 = 200Hz or .005 seconds).

f. Counter U10 finally starts counting and reaches its terminal count of .0005 seconds (10KHz divided by 5 = 2KHz or .0005 seconds).

g. When U10 reaches its terminal state, its 0 output line sets the gating logic (U1A and U1B) to output the timer output pulse. In this example, the cumulative time of all counters to reach their terminal counts are .5555 seconds (.5 + .05 + .005 + .0005 seconds). This makes the output pulse time .5555 seconds.

h. At this time, when the 0 output of U10 goes high, the PE line of all counters go high. This is because the output of U10 is connected to all the PE lines of the counter.

i. The next BCD numbers are then loaded into the counters and the cycle repeats.

7-78. In the previous example, a time of .5555 seconds was used. If the time is to be increased, then the BCD numbers loaded into the counters must be larger. If the time is to be decreased, the numbers need to be smaller. The larger the BCD number, the longer it will take to reach the terminal count. The same number does not have to be sent to each counter.

7-79. When a code pattern is sent to U6 that has its C and D lines (pins 2 and 14) high, the output of U1D goes low and resets the μC (U4). The code to reset the μC will not occur unless U4 is to be reset. The code will not affect the U6 counter, since U4 will keep the pacer output disabled using the gating logic (see next paragraph).

7-80. Gating Logic

7-81. The gating logic, consisting of U1A, U1B, U1C, and U1D, is used to select either the time interval or timer output pulses. (The pulses are generated by the timer and pacer circuitry, respectively.) If the pacer pulses are to be output, U4 will set its P01 line low and its P02 line high. This allows the 0 output of U10 to be gated through U1A. If the timer pulses are to be output, U4 will hold its P01 line high. Gate U1A will then be disabled causing its output (pin 3) to go high. This in turn permits P02 to be gated through U1B.

7-82. FRONT PANEL CIRCUITRY DESCRIPTION

7-83. The 3497A can be obtained with two different types of front panels: the standard or the optional (Option 260) front panel. The standard front panel includes the keyboard circuitry, two display circuits, various annunciators, and a beeper circuit. The optional front panel has no internal circuitry (i.e., no keyboard, display, and beeper), except for an on/off switch and a power indicator.

7-84. The front panel circuitry is explained in the following paragraphs. Since the optional front panel has very little circuitry, no explanation is given for that panel. Unless otherwise noted, refer to Schematic A4 (in Service Group E) for the explanation on the standard front panel.

7-85. Display and Annunciator Circuitry

7-86. The display and annunciator circuitry can be separated into the following: main display circuitry, channel display circuitry, and annunciator circuitry. All of the display and annunciator circuitry is controlled by the outguard controller using the buffered data bus (BD0 through BD7) and three buffered address lines (BA0 through BA3). (The address and data lines are also used by the keyboard circuitry, see paragraph 7-95.) The display and annunciator circuitry is continuously scanned and updated by the outguard controller.

7-87. Data Transfer and Display Circuitry Selection. The address bits, BA0 through BA3, enable and select the various display and annunciator circuitry. The data bits (BD0 through BD7) send display data to the circuitry to update the displays and annunciators. The operation is as follows:

a. The buffered address bits, BA0 through BA3, are applied to decoders U20 and U21.

b. When the decoders are enabled, the buffered address bits are decoded and the resultant Y0 to Y6 decoder outputs then enable the various display and/or annunciator circuitry. The decoders are enabled when the DISP STRB I and DISP STRB II lines go from high to low. These lines come from the outguard controller through peripheral decoder U32 and U33, respectively (see Schematics A1 or A2).

c. Since one output of U20 (pin 13) is connected to the enable line of octal flip-flop U7 (which is used as a latch), the address bits enable U7 to transfer data on the buffered data lines to the display and annunciator circuitry. This data (which is DB0 through DB7 after going through U7) is used to turn on a particular annunciator or a particular segment on a display LED.

7-88. Main Display Circuitry. The main display circuitry consists of a Display Driver/Multiplexer (U4) and LED displays (DS6 through DS12). All of the displays, except the sample light (i.e., the D.P. LED) of DS6 (see next paragraph), are continuously scanned and updated by U4. U4 is able to do this since all of the required circuitry to turn on, scan, and drive the displays is internal to U4. The Display Driver/Multiplexer reads the data bus (DB0 through DB7), when enabled, and drives the displays directly. The displays are sequentially turned on by the B0 through B6 outputs of U4 with the appropriate segments selected by the "a" through "g" and D.P. outputs of U4. Since the displays are configured as common anode displays, the B0 through B6 outputs of U4 are high, and the "a" through "g" and D.P. outputs are low to turn on the display segments and decimal points. The Display Driver/Multiplexer is enabled by D flip-flop U17B which in turn is clocked and cleared by U21.

7-89. Dependent on the instrument function selected, the sample light of DS6 can be either off or on, or toggling at a specified rate. This is controlled by the outguard controller using decoder U21 and monostable multivibrator U22A. The operation is as follows:

a. If the light is to toggle (i.e., turn off and on), U22A is clocked by decoder U21. The $\overline{1Q}$ output of U22A then goes low for about 100mS and turns the sample light on for that amount of time. A low level is used since the cathode of the sample light LED is connected to +5V through R4. The time of the low level is determined by R26 and C13.

b. If the light is to be turned on and remain on, U22A is again clocked by decoder U21. The only difference is that the multivibrator will be clocked again before U22A changes state (i.e., before the 100mS are up). This action continues as long as the light is to remain on.

c. If the light is to remain off, U22A is not clocked at all. Its $\overline{1Q}$ output remains high and keeps the LED off.

7-90. Channel Display Circuitry. The channel display circuitry consist of three LED displays (DS2 through DS4) and three BCD to 7 segment decoder/drivers (U2, U5, and U8). The circuitry operation is as follows:

a. Each LED display is scanned and turned on by its own decoder/driver. The decoder/driver for display DS2, DS3, and DS4 are U8, U5, and U2, respectively.

b. The decoder/drivers U2 and U5 are enabled by flip-flop U18A and decoder/driver U8 is enabled by U18B.

c. When a decoder/driver is enabled, data from the data bus (DB0 through DB7) is then latched into the decoder/driver. The data is then decoded by the decoder/driver itself and is then used to turn on the appropriate segment of the display. Since the cathodes of the displays, pins 2 and 9 on the display socket, are connected to ground, a high level (+5V) from the outputs of the decoder/driver turns the display segments on. Decoder/drivers U2 and U8 receive display data from data bits DB0 through DB3 and U5 receives the data from bits DB4 through DB7.

d. The U18A and B flip-flops, when clocked by decoder U20, generate the decoder/driver enable pulses. The flip-flops are then cleared by U20.

e. The pulses from U20 (to clock U18A and B) go through pulse stretcher circuitry U15A through U15D, before going to the flip-flop. The pulse stretcher circuitry delays the clock pulse to make sure the decoder/drivers have enough time to update and strobe the displays.

7-91. The decimal point of DS4 is turned on by monostable multivibrator U22B, instead of decoder/driver U2. The multivibrator is clocked by decoder U20 and a positive 160mS wide pulse is then generated at U22B's 2Q output. As long as the pulse is positive, diode CR23 does not conduct and the cathode of the decimal point LED is high. This turns the LED on. The pulse length is determined by the time constants of C17 and R33. When the multivibrator's 2Q output goes low, diode CR23 conducts and brings pin 10 of DS4 low. This turns the decimal point off.

7-92. Annunciator Circuitry. The annunciator circuitry consists of a four section D flip-flop U1, four octal flip-flops U3, U6, U9, and U12, a driver U11, and various LED annunciators. Each annunciator, except the function annunciators (DCV, SEC, etc.), is turned on or off and is driven by a corresponding flip-flop. The flip-flops are clocked by decoder U21 (which receives its information from the BA0 through BA2 address lines). When a flip-flop is clocked its Q outputs go high or low, dependent on the state of the D inputs of the flip-flop. A low output turns the LED on and a high output turns the LED off. The state of the D inputs depends on the state of the DB0 through DB7 data bits.

7-93. A single output of a flip-flop can sink enough current to turn on one annunciator LED. If more than one LED is used by an annunciator (e.g., the 1mA annunciator, DS17, uses two LEDs), each additional LED needs an additional output of the flip-flop. The required data to turn on the additional LEDs comes from the outguard controller. The only exception to this are the LEDs controlled by flip-flop U12. Since only one line is used to turn on two or more LEDs, driver U11 is used to sink the necessary current to turn the LEDs on.

7-94. Display Ready Circuitry. The display and annunciator circuitry, after it has received display data from the outguard controller, remains on a certain time before it is updated again. The Display Data Ready circuitry makes sure that the circuitry has enough time. The operation is as follows:

a. After data is sent to the display circuitry, the outguard controller sends a clock pulse (using decoder U20) to monostable multivibrator U23A.

b. A positive 100mS wide pulse is then generated by U23A and is applied to the A7 input of octal buffer U13. The pulse width is determined by the time constants of C14 and R27.

c. Since buffer U13 is continuously enabled by the outguard controller, it will read U13 and determine if the A7 input is high or low. The buffer is enabled by the outguard controller using decoder U20, and Schmitt Triggers U16B and C. (Buffer U13 is also used for the keyboard circuitry; see paragraph 7-95).

d. When the pulse at the A7 input of U13 goes low, the outguard controller reads this and knows that the display is ready to be updated. The 100mS wide pulse makes sure the display will not be updated until the pulse goes low.

7-95. Keyboard Circuitry

7-96. The keyboard circuitry consist of octal buffer U13, key encoder U14, and a keyboard (i.e., the front panel switches). The front panel switches are connected in a 4x5 matrix which is capable of decoding a total of 20 switches. The keyboard operation is as follows:

a. One side of the keyboard matrix is connected to the X1 through X4 lines of the encoder (U14) and the other side of the matrix is connected to the Y1 through Y5 lines of the encoder. Capacitors C7 and C8 are there to prevent keybounce.

b. When a front panel key is pressed, the encoder (U14) determines the key by checking the state of its Y1 through Y5 and X1 through X4 lines. For example, if the S0 switch is shorted (i.e., Analog Step Key pressed), lines X1 and Y1 are shorted to each other.

c. This is detected by U14 and the encoder then clocks flip-flop U17A. The clock signal is output at pin 13 of U14 and, after it is delayed by buffer U15E, it is applied to the flip-flop.

d. The flip-flop then sets its $\overline{Q}$ line low which interrupts the outguard processor (see Schematics A1 or A2). The $\overline{Q}$ output is the keyboard interrupt line $\overline{KBD}$ INT.

e. The outguard controller then enables buffer U13 and reads its output using the buffered data lines (BD0 through BD7). Since the output of the key encoder is connected to the input of U13, the outguard controller can then determine which key is pressed, by reading the output data of U13. Each pressed key develops certain highs and lows on the output of U13. These highs and lows are then used by the outguard controller to determine which key is pressed. Although buffer U13 is normally enabled to update the display (see paragraph 7-94), it may not be enabled at the time a key is pressed. In this case, the interrupt on the outguard processor will cause the processor to enable the buffer.

f. Once the outguard controller determines which key is pressed, it takes the appropriate action (changes functions, triggers, etc.). At this time, flip-flop U17A is cleared by the controller using decoder U20 and the flip-flop is ready for another interrupt.

7-97. Beeper Circuitry

7-98. The beeper is the small speaker connected to transistor Q1. When the beeper is to be turned on, monostable multivibrator U23A is clocked by the outguard controller using decoder U20. The multivibrator then generates a positive going 63mS pulse at its $\overline{Q1}$ output (pin 13). The pulse width (i.e., 63mS) is determined by C14 and R27. Since the output of U23A is connected to one input (pin 1) gate U16A and the other input (pin 2) is high, the output of U16A (pin 3) goes low. This turns on $\overline{Q1}$ which turns the beeper on. The high at pin 2 of U16A is developed by the +5V power supply using capacitor C10, and resistors R31 and R32. With pin 3 of U16A low, capacitor C10 is discharged and, after C10 is discharged to a TTL low level, sets pin 2 of U16A low which sets pin 3 of U16A high. This turns the beeper off. Normally the 63mS pulse will also go low during this time. With a high at pin 3, capacitor C10 is charged again. If another high (i.e., 63mS pulse) is applied to pint 1 of U16A, pin 3 of U16A will not change state until C10 is charged up. Capacitor C10 makes sure that the beeper will turn off, even if the applied pulse remains high.

7-99. CROSSGUARD LOGIC CIRCUITRY DESCRIPTION

7-100. Communications between the 3497A's Outguard Circuitry (i.e., the outguard controller) and the Inguard Circuitry (i.e., the inguard controller) is accomplished using the crossguard logic circuitry. The circuitry has two major parts to it: one part sends data from the outguard to the inguard and the other sends data from the inguard to the outguard. The circuitry is described in the following paragraphs. Refer to Schematic AB1 for the explanation.

7-101. Sending Data from Outguard to Inguard

7-102. The circuitry that transfers data from the outguard to the inguard has a transmitter, which sends the data, and a receiver, which receives the data. The transmitter changes parallel data to a serial data stream and then sends the data stream to the receiver, using isolation transformers. The receiver reads the data from the transformers, changes it back to parallel data, and then transfers it to the inguard controller. The transmitter and receiver are transformer coupled to allow the inguard and outguard circuitry to float from each other. This is because the outguard circuitry is referenced to the instrument's chassis and the inguard circuitry is floating. The transformers are located on the power supply board (A16 Assembly).

7-103. Transmitter Circuitry. The transmitter circuitry is part of the outguard and consists mostly of shift register U40, counter U35, drivers U46A through U46D, and associated circuitry. Data to be sent to the inguard comes from the outguard as parallel data which is changed to a serial data stream by the transmitter circuitry. The serial data stream is comprised of nine bits. The first bit, called the start bit, is always high. It tells the inguard processor (when it receives the data) that a data byte is available from the outguard controller. The other eight bits in the data byte are the data bits and can be high or low. An example of the data byte is in Figure 7-3. The

transmitter operation is as follows:

a. The data bits are received, over the buffered data bus (BD0 through BD7,) by the crossguard circuitry. This data is applied to shift register U40 which then changes the data from parallel to serial data.

b. The serial data bits are then clocked through flip-flop U42A to the U46 drivers. The drivers are used to drive isolation transformers T1/T3. The clock signal comes from Bϕ2, after going through flip-flops U43A and U37A. The flip-flops are used to slow the transfer speed by dividing the Bϕ clock down by 2 (750KHz).

c. The data transfer is started when the SR/$\overline{W}$ line and the IG XFR line (from the outguard controller) goes high. This enables U40 and U46 (after going through flip-flop U37A and NOR gate U36A).

d. During time when data is transferred, counter U35 is clocked each time a bit is transferred from the drivers to the transformers. The counter increments by one until it reaches nine (eight data bits plus the start bit). It then resets the transmitter circuitry (i.e., U40, U42A, U42B, and U37A), using gates U26C, U26D, and U36B. The circuitry is now ready for more data.

7-104. Receiver. The receiver is part of the inguard and consists primarily of transistor array U116, shift register U114, and associated circuitry. The receiver receives serial data from the isolation transformers and changes it back to parallel data. This data is then transferred to the inguard controller. The inguard controller takes the data and sends it back to the outguard controller over the crossguard logic. This lets the outguard controller know that the correct data was received by the inguard controller (i.e., inguard processor). The inguard controller then takes the appropriate action (dependent on the data received). The operation is as follows:

a. The nine data bits are applied to transistor array U116 from isolation transformers T1/T3. The array serves two functions, it develops a clock signal using the data bits and also sends the data bits to shift register U114. The clock signal is used to clock the shift register.

b. Each time the shift register is clocked, a bit is shifted into U114. When the 7th bit is shifted in, the QG output of U114 (pin 12) will go high. This is because the 7th bit shifted in at this time is the start bit, which is always high. When flip-flop U113A is clocked (by the clock signal generated by U116), its $\overline{Q}$ line goes low. This low interrupts the inguard processor.

c. During the time when the processor interrupt is generated, the last bits (8th and 9th bits) are shifted

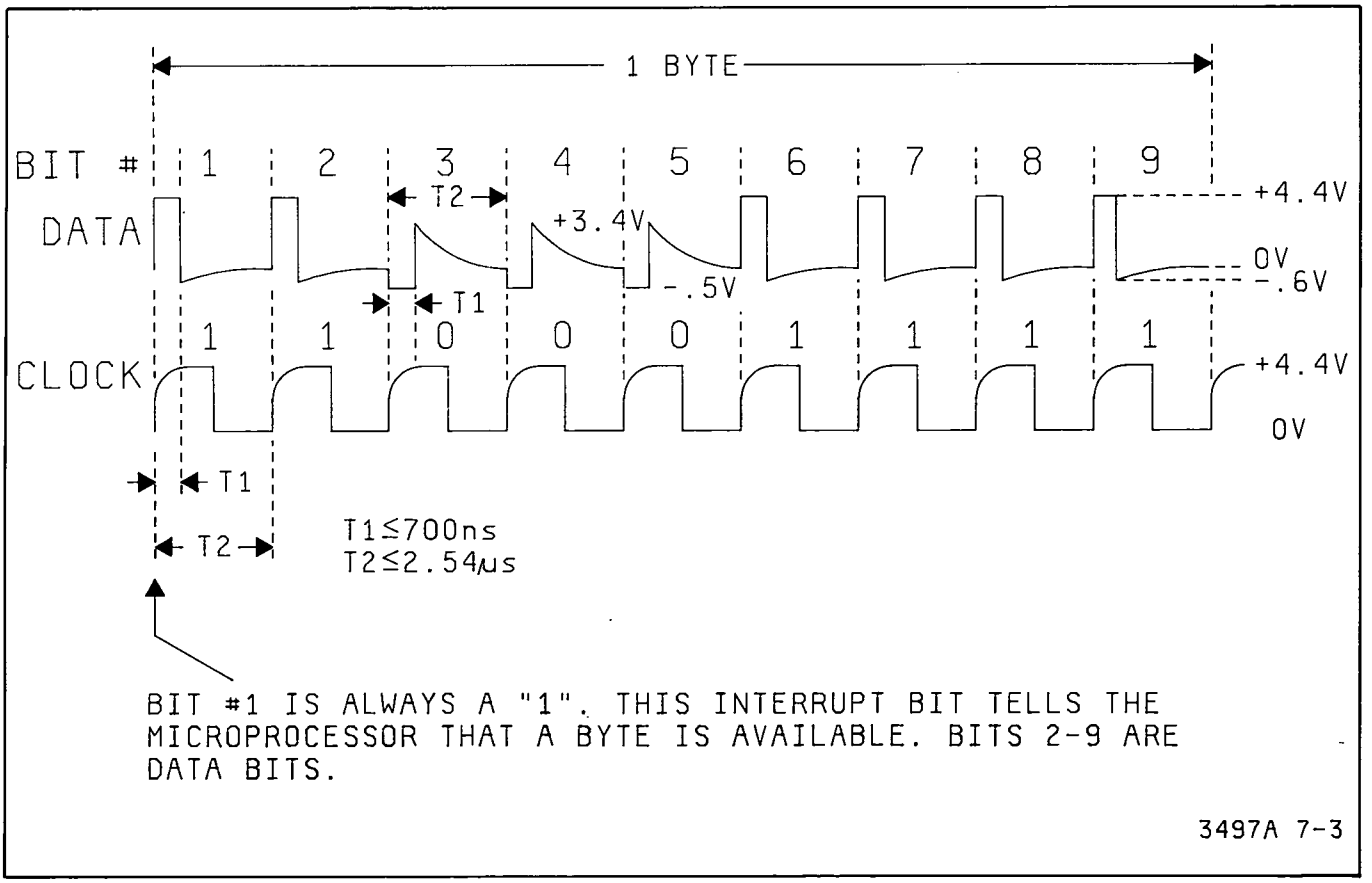


Figure 7-3. Data Byte Sent Over the Crossguard (from outguard to inguard)

in. When the 9th bit is shifted in, the first bit (start bit) is shifted out. This leaves the eight bits following the first bit in the register. These bits are the data bits and are applied to buffer U112.

d. When the inguard processor is interrupted, it knows that data is ready to be read. The processor then sets its $\overline{\text{READ}}$ line low which enables buffer U112. The buffer then outputs the data from the shift register to the processor, using the inguard data bus (DB0 through DB7). A low $\overline{\text{READ}}$ line also clears flip-flop U113A and buffer U112. The line is also used to clock flip-flop U113B which then clears U114. Flip-flop U113B is then cleared by the inguard's ALE clock (Address Latch Enable from inguard processor) using NOR gat U110B.

e. When the data is received by the inguard processor, the processor then sends the same data back to the outguard controller. This lets the outguard controller know that the correct data was received. The data is also sent using a transmitter and receiver (see paragraph 7-106).

7-105. Another circuit, NOR Gates U110A and U110C, is used to reset the inguard processor after power-on occurs. After power-on occurs, the outguard processor is set to its turn-on state. The processor then sets all bits on the serial stream, sent to the inguard processor, high. After all the eight data bits are shifted into U114, all of its QA through QH outputs are then high. This makes the output of NAND gate U111 go low. A low then sets the output of U110A high which sets the output of U110C low. Since the output of U110C is the inguard processor's reset line, the processor is then reset to its turn-on state.

7-106. Sending Data from Inguard to Outguard

7-107. The circuitry and operation is similar to the circuitry and operation used to send data from the outguard to the inguard. The data sent is also comprised of nine bits with the first bit, which is also called the start bit, always high (see Figure 7-3). The circuitry also has a transmitter and receiver with the transmitter part of the inguard and the receiver part of the outguard. The transmitter consists of shift register U115, flip-flop U119, counter U117, and associated circuitry. The receiver is part of the outguard and consists of transistor array U49, shift register U50, buffer U44, flip-flops U37B and U43A, and associated circuitry. The operation is explained in the following paragraphs.

7-108. Transmitter. Parallel data is sent over the inguard data lines to shift register U115. When U115 is enabled by a low on the $\overline{\text{WRT}}$ line (from the inguard processor) and clocked by the ALE clock, the data bits are shifted in and converted to a serial bit stream by U115. This is output to drivers U120A through U120D using flip-flop U119A. The data is then output to isolation transformers T4/T2, when the drivers are enabled by NAND gates U119C and U118D. While data is shifted into U115, counter U117 increments at each ALD count. After nine bits are shifted into U115, counter U117 QA and AD outputs go low. This brings the output of NOR gate high which clears flip-flop U119B. The flip-flop in turn disables drivers U120A through U120D using gates U118C and U118B. No more data is output until the inguard processor is ready to send new data (i.e., set the $\overline{\text{WRT}}$ line low).

7-109. Receiver. The serial stream is applied from T4/T2 to transistor array U49 and shift register U50. A clock signal is then generated from the data stream by U49. This clock signal is used to clock U50 and flip-flop U37A. When U50 is clocked, the data bits are shifted into the shift register. When the 8th bit is shifted in, the QH output of U50 goes high. This is since at this time, the first data bit (i.e., the start bit) shifted in is always high. Flip-flop U37B changes state and its Q output goes high. This is the BYTE AVAILABLE line to the outguard controller which lets the controller know that data is ready. The controller then sets the SR/$\overline{\text{W}}$ line low and the IG XFR high line. This in turn enables buffer U44 and parallel data is sent to the controller using the buffered data lines. Then, U50 is cleared by the DBE (Data Bus Enable) line using gate U36D and flip-flop U43A.

7-110. INGUARD LOGIC CIRCUITRY DESCRIPTION

7-111. The inguard logic circuitry consists of two major sections: the inguard controller and the A/D logic. The inguard controller is used to control the operation of the inguard circuitry, which includes the analog plug-in options and the A/D logic. The A/D logic, in conjunction with the inguard controller, controls the operation of the voltmeter option (if the option is installed). Since the A/D logic is only used by the voltmeter option, the circuitry explanation is included with the voltmeter option explanation (see paragraph 7-186). Unless otherwise noted, refer to Figure 8-E-11 (Inguard Controller Block Diagram) and Schematic B1 for the explanation on the inguard controller circuitry. Both the figure and the schematic are in Service Group E.

7-112. The main part of the inguard controller circuitry and the inguard logic is the inguard microprocessor U204. Other inguard logic circuitry is used to select the different channels (i.e., relays) on the analog plug-in options. This circuitry is controlled by the processor. The inguard controller (or processor) circuitry is explained in the following paragraphs.

7-113. Inguard Processor

7-114. The following explains the inguard processor circuitry.

a. The inguard processor (U204) has internal to it, in addition to the processor circuitry itself, a 1Kx8 ROM and a 64x8 RAM. The ROM, in conjunction with the internal processor circuitry, controls the inguard circuitry operation. The RAM is used to store data re-

ceived from the outguard and also readings taken by the voltmeter option.

b. In addition to the ROM and RAM, the processor also has an onboard oscillator and clock, and an 8-bit timer/counter. The frequency and stability of the clock is determined by crystal Y1. The oscillator and clock output, called ALE (Address Latch Enable), is used as the main inguard circuitry clock. The counter in conjunction with the ALE clock is used with the voltmeter option's A/D (Analog to Digital) operation. The time period of the ALE clock is 2.564μS if the 5.85MHz crystal (Y1) is installed (for 60Hz operation) and 3.077μS if the 4.875MHz crystal is installed (for 50Hz operation).

c. Other parts of U204 are the ports (P10 through P17 and P20 through P27), lines T0 and T1, and the PROG line. The ports and lines are used to control the inguard circuitry (e.g., port extender U205 and the A/D logic). Ports P17, P20 through P26, and the PROG line are used by the port extender to select the channels in the analog plug-in options. Ports P10 through P16, P24 and P25, and lines T0 and T1 are used by the A/D logic to control the voltmeter option's A/D operation.

d. The inguard processor uses data lines (DB0 through DB7) to send data to the outguard controller and also to receive data from the outguard controller. The data is sent over the crossguard circuitry (see paragraph 7-89). This includes set-up information to the inguard and measurement data to the outguard.

e. Other outputs from U204 are the $\overline{\text{READ}}$ and $\overline{\text{WRT}}$ lines which are used to read or write to the crossguard logic circuitry located in the inguard (see paragraph 7-99 for the operation).

f. The processor can also be interrupted in order to read the data bus. This is done using the $\overline{\text{INT}}$ line to the processor. A low on the line interrupts the processor which then goes to a pre-defined state.

7-115. After instrument power-on occurs, to prevent the processor from performing an incorrect action (like closing relays, etc), it is placed into its reset state. It will remain in that state until the +5V power supply is above approximately +3.3V. This is accomplished by keeping the processor's $\overline{\text{RESET}}$ line low, until the power supply is above +3.3V. The operation is as follows:

a. When the 3497A is turned on, the +5V power supply starts to come up. At a certain point, +.6V is then developed across CR1 and applied to pin 2 of comparator U214.

b. As long as the +5V power supply is below approximately +3.3V, the voltage at pin 3 of U214 is below +.6V (the voltage is developed by divider R214 and R215). This sets the output of U214 low.

c. When the +5V power supply goes above +3.3V, the voltage at pin 3 of U214 goes above +.6V. The output of the comparator then changes state and charges up the capacitor connected to the comparator's high output. When the capacitor is charged, the RESET line goes high and the processor is enabled.

7-116. Analog Plug-In Option Control

7-117. The analog plug-in options receive channel closure data from the inguard controller. The data is modified and transferred to the options using a port extender, decoders, buffers, drivers, and associated circuitry. The resultant data is then decoded by the plug-in options to close the appropriate channel (i.e., relay). The same circuitry is also used to transfer data from the inguard controller to the 3498A Extender (if the extender is connected to the 3497A). The 3498A does some more decoding of the data before the resultant data is transferred to the plug-in options that are installed in the 3498A. The 3497A Analog Plug-in Control circuitry and operation is explained in the following paragraphs.

7-118. Port Extender. Port extender U205 extends the output ports of the inguard processor. The port extender, a CMOS device, is the main integrated circuit used by the inguard processor to develop the data that is used by the analog plug-in options to close the selected channels (of the options). The operation is as follows:

a. When the PROG line of the inguard processor goes from high to low, the port extender selects one or more of the extender's output ports (ports 4 through 7 of U205). This depends on the state of the P20 to P23 inputs to the extender. For example, certain highs and lows on the P20 to P23 inputs select certain output ports.

b. When the PROG line goes from low to high, the state of the selected output ports of the extender is then selected. For example, certain highs and lows on the P20 to P23 inputs set the output lines of the selected output ports of U205 to a certain state.

7-119. Century and Decade Address Circuitry. The 3497A can have a maximum of five analog plug-in options with each option having two decades of ten channels each. The first ten channels are in decade A and the second ten channels are in decade B. This makes a total of 100 channels for all possible analog plug-in options in the 3497A mainframe. The channels are selected by the $\overline{\text{DECA0}}$, $\overline{\text{DECB0}}$, $\overline{\text{DECA1}}$, $\overline{\text{DECB1}}$, etc., lines and the UN0 through UN3 lines. The $\overline{\text{DECA0}}$, $\overline{\text{DECB0}}$, etc., lines select the A and B decades of a plug-in option in a particular slot. For example, line $\overline{\text{DECA0}}$ selects decade A on the option located in slot 0 (the first slot) and line $\overline{\text{DECB0}}$ selects the other decade (i.e., decade B) on the same option. The $\overline{\text{DECA1}}$ and $\overline{\text{DECB1}}$ lines select the channels on the option in slot 1 (the second slot), and so on. The UN0 through UN3 lines select a particular channel in the selected decade. Once the correct lines are

enabled, the LATCH line (from U205 pin 15) goes low and the plug-in option then enables the correct channels.

7-120. Since a total number of 100 channels can be selected, the address of the channels is normally from "0 to 99". Address "0" is the first channel (channel 0) and address "99" the 100th channel (channel 99), and so on. The channel addresses can, however, be changed from "0 to 99" to "100 to 199", "200 to 299", all the way up to "900 to 999". The 3497A leaves the factory with an address range of "0 to 99". The address range is selected by the Century Address jumpers. To change the addresses to "300 to 399", for example, remove the jumper connected from 0 output (U206 pin 1) to A0, A1, etc. Then, while leaving A0, A1, B0, B1, etc., connected to each other, install a jumper from the 3 output (pin 4) of U206 to A0, A1, B0, B1, etc. For more information on how to configure the 3497A to different century addresses, refer to the 3497A Operating, Programming, and Configuration Manual.

7-121. In addition to the Century Address jumpers, there are also the Decade Address jumpers. These jumpers can be selected to close a channel on more than one decade by using an address for closing only one channel. For example, if channel 1 (the second channel in decade A) is to be closed, the address for that channel is sent. Since this channel is on decade A, the decade is selected by setting line $\overline{\text{DECA0}}$ true. The channel is then closed when the appropriate UN0 through UN3 lines are selected. If, besides channel 1, the corresponding channel in decade B (the second channel in the decade, which is channel 11) also needs to be closed by the same address, the Decade Address jumpers have to be changed. This is accomplished by removing the jumper between B0 and the 1 output (pin 2) of U208 and installing it between B0 and 0 output (pin 1) of U208. When an address to close channel 1 on decade A is now sent, channel (i.e., Channel 11) on decade B also closes.

7-122. The data to select decades A and B and the individual channels on the analog plug-in options, comes from port extender U205. The following explains the operation of the option control circuitry. It is assumed, in the explanation, that a channel in decade A of the plug-in option located in the first slot of the mainframe is to be selected.

a. The CE0 through CE3 lines are for the century address, the DC0 through DC3 lines are for the decade address, and the UN0 through UN3 lines select the individual channels. All of these data lines come from U205. The CE and DC data lines are applied to BCD-to-decimal decoders U206 and U208, respectively. The UN0 to UN3 lines are applied to the plug-in option directly.

b. The decoders decode the CE and DC data and the appropriate outputs of the decoder are set low (true) or high (not true). If, for example, a channel on decade A of the option in slot 0 is to be selected, the 0 outputs of both U206 and U208 will be low. The rest will be high.

c. The low outputs are applied through the Century and Decade Address jumpers to exclusive OR gate U207A. (It is assumed that the jumpers are in the factory selected setting.)

d. The output of U207A goes low and the $\overline{\text{DECA0}}$ line goes true. This selects the A decade of the plug-in option located in slot 1, when the LATCH line (at U205 pin 15) is low. At this time, the port extender also sets the UN0 through UN3 lines to a certain state which are then used to select the appropriate channel.

7-123. Analog Extender Control. Similar to selecting channels on the analog plug-in options in the 3497A, the CE0 through CE3 and DC0 through DC3 lines select the various A and B decades of the options in the 3498A Extender. In addition, the UN0 through UN3 lines also select the channels in the selected A and B decades of the options. The CE0 through CE3 and DC0 through DC3 lines are transferred over buffer U203 to the 3498A. The UN0 through UN3 and the LATCH lines are transferred to the 3498A by bus driver U203.

7-124. Break/Make Operation and Circuitry. Before the inguard controller attempts to close a new channel on an analog plug-in option, it makes sure that the present channel "breaks" (opens) before the new channel "makes" (closes). The controller does this by monitoring the $\overline{\text{BREAK}}$ and $\overline{\text{MAKE}}$ lines from the plug-in option (and/or digital extender). The operation is as follows:

a. When no channel closure data to the plug-in options is sent, the $\overline{\text{MAKE}}$ and $\overline{\text{BREAK}}$ lines are normally high. This is set by the options themselves.

b. A high on the lines makes the output of NAND gate U212A low. This is because all inputs to the gate are high, including the output of D flip-flop U213B.

c. When the inguard controller is ready to send a channel closure command, it sets all the UN0 through UN3 lines and decade address lines high. The controller then sets the (L) LATCH line low to transfer the state of the UN0 through UN3 and decade address lines to the option. The option itself will then generate a low on the $\overline{\text{BREAK}}$ line for approximately 540μS. This low is applied to gate U212A and flip-flops U213. The flip-flops are used to prevent possible racing conditions. A low on gate U212A makes its output go high. Because the inguard processor's P17 port is connected to the output of U212A, the port is also high and the processor knows that no further commands should be sent to the option until port P17 goes low.

d. When the 540μS are up, the $\overline{\text{BREAK}}$ line goes high. The processor's P17 port changes state and the processor then commands the option, using the decade and UN0 through UN3 lines, to close the selected channel.

e. When the $\overline{\text{BREAK}}$ line is high, the inguard processor then, dependent on which decade (A or B) is to be enabled, sets the appropriate decade address line low. The option then sets the $\overline{\text{MAKE}}$ line low, for about 1.1mS, and closes the selected channel. The output of U212A (i.e., input to port P17) goes low again and the processor then knows that the channel is being closed and no new data is to be sent.

f. When the $\overline{\text{MAKE}}$ line finally goes high and the output of U213B and the $\overline{\text{BREAK}}$ line are both high, the output of U212A goes low. The processor then knows that the option is ready for new data.

7-125. Option Sense Circuitry. When channel closure data is sent to a plug-in option, the inguard controller then determines (senses) if the option has received the data and if the option is in the appropriate slot. The circuitry that determines this includes U211, U212B, and U201A. Once this is determined, the information is passed on to the outguard controller. The outguard controller then toggles (i.e., turn on and off) the LED near the channel display LEDs at the front panel. The option sense circuitry operation is as follows:

a. After the plug-in option receives the channel closure data and then closes the selected channel, it sets the $\overline{\text{MAKE}}$ line low (see paragraph 7-124).

b. When the $\overline{\text{MAKE}}$ line is low, a high output at NAND gate U201A is developed. This high clocks flip-flop U211 which then sets its $\overline{\text{Q}}$ output low.

c. A low at $\overline{\text{Q}}$ sets the output of U201D high and lets the controller know that the option has received the data. It then passes the information on to the main controller.

d. After the inguard controller receives the data from U211, it sets all of the UN0 through UN3 lines high. Since lines UN2 and UN3 are connected to U212B, the output of U212B goes low and clears flip-flop U211. The $\overline{\text{Q}}$ output of U211 then goes high.

7-126. VOLTMETER BLOCK DIAGRAM THEORY OF OPERATION

7-127. General

7-128. The following paragraphs have the block diagram theory of operation of the 3497A's voltmeter option (Option 001). Refer to the simplified block diagram in Figure 7-4 for the explanation.

7-129. The voltmeter circuitry can be separated into two major sections: DC Voltmeter and DC Current Source. The voltmeter circuitry can measure dc voltages from 0V to $\pm$120V using four ranges: .1V, 1V, 10V, and 100V. The current source can output a current of either 10μA, 100μA, or 1mA. The ranges for both the dc voltmeter and current source are selected by the inguard controller, which in turn receives its instructions from the outguard controller. The A/D (analog-to-digital) operation is also controlled by the inguard controller using the A/D logic.

7-130. DC Voltmeter

7-131. The dc voltmeter circuitry consists of the following:

Input Switching
Input Amplifier
A/D Converter
A/D Logic
Reference Supplies

7-132. To help understand the operation of the dc voltmeter circuitry, a typical measurement sequence is explained as follows:

a. The outguard controller receives the set-up (range, autorange, etc.) information locally from the front panel, or remotely over the HP-IB or Serial I/O bus. This information is then transferred to the inguard controller. The inguard controller configures the voltmeter option's input switching and input amplifier circuit to the selected range.

b. Once the circuitry is configured, the input voltage to be measured is then applied to the input switching circuitry. The input voltage is applied to the rear panel HI COM and LO COM Input terminals. The purpose of the input switching circuitry is to do the following:

1. Connects the voltmeter's input voltage to the input amplifier. It also attenuates the input voltage by "100", if on the 100V range, before applying the voltage to the input amplifier.

2. Connects the input of the input amplifier to ground (LO COM terminal) for a zero measurement (see step e).

3. Generates the gate bias voltage for the FET switches located in the input switching circuitry.

c. After going through the input switching circuitry, the output of the circuitry is then applied to the input amplifier. The amplifier does the following:

1. The amplifier is used as a buffer between the input terminals and the A/D converter.

2. The amplifier amplifies the input voltage to provide a ± 10V output (i.e., A/D converter input) for all full scale inputs on any range. For example, if the .1V Range is selected and + .1V is applied to the voltmeter, the output of the amplifier is + 10V. No amplification is performed on the 10V Range. However, the amplifier is still used as a buffer.

d. The output of the input amplifier is applied to the A/D converter. The converter then changes the voltage to digital information which is then transferred to the inguard controller by the A/D logic. The digital information is the actual measurement of the voltage applied to the input terminals. If the Autozero function is selected (see step e), a zero reading is subtracted from the input reading by the inguard processor. The result is transferred to the outguard controller. The outguard controller then outputs the reading to the front panel and/or over the HP-IB, or stores it in memory (if Reading Storage is enabled).

e. In addition to the measurement sequence in steps a to d, the voltmeter circuitry makes another measurement called a zero measurement. The measurement is made by connecting the input of the input amplifier to ground (i.e., to the LO COM input terminal). The offset of the input amplifier and any offsets developed in the input switching circuitry is then measured. This measurement is the zero measurement. After the zero measurement is made, the input amplifier is disconnected from ground and a regular input measurement is then made. After the input measurement, the zero measurement is then subtracted from the input measurement. The result will be the displayed reading. The zero measurement is only performed if the Autozero function is enabled. When the function is disabled, one zero measurement is made which is subtracted from the input measurements that follow. A zero measurement is also made when ranges are changed. No other zero measurements are made until the Autozero function is re-enabled.

7-133. DC Current Source

7-134. The dc current source consists of the following:

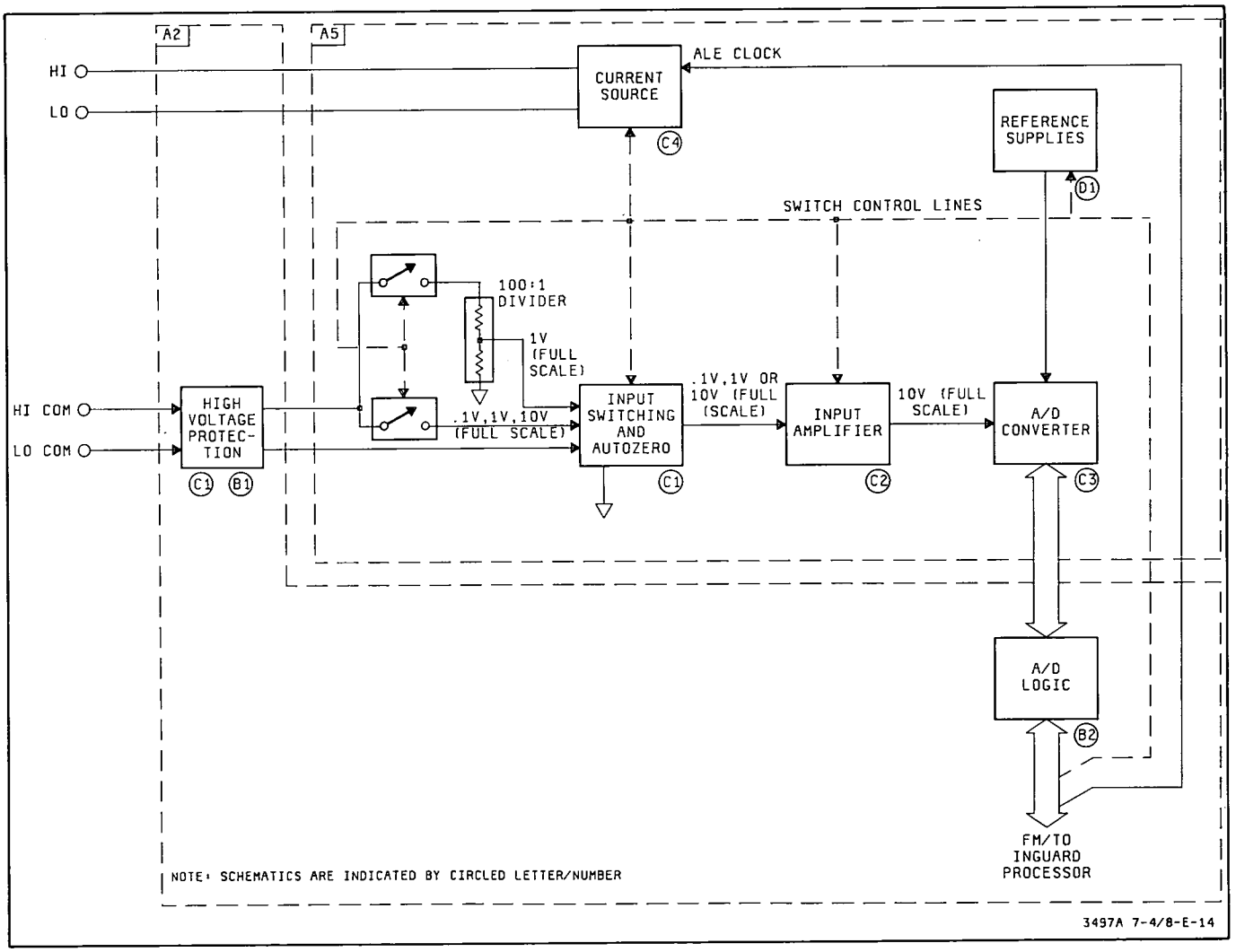


Figure 7-4. Voltmeter Option Simplified Block Diagram

Floating Power Supply
Reference Supply
Gate Bias Amplifier
High Voltage Protection

The operation is as follows:

a. The floating power supply develops the necessary voltages for the current-generating circuitry of the current source (i.e., Reference Supply, Gate Bias Amplifier). The supply consists of two floating supplies which in effect isolate the current source from the rest of the 3497A circuitry.

b. The reference supply makes sure that the output currents are stable.

c. The gate bias amplifier is used to bias the output FET which regulates the current flow.

d. The high voltage protection circuit is used to protect the current source from excessive voltages that may be accidently applied to the current source output terminals.

7-135. DC VOLTMETER CIRCUITRY DESCRIPTION

7-136. General

7-137. The following paragraphs describes the dc voltmeter circuitry. The explanation is separated as follows:

Input Switching Circuitry- paragraph 7-139
Input Amplifier Circuitry - paragraph 7-150
A/D Conversion - paragraph 7-158
A/D Logic -paragraph 7-186
Reference Supplies - paragraph 7-204

Except for the A/D logic, all circuitry is on the voltmeter option printed circuit board. Since the A/D logic is part of the inguard controller circuitry, the circuitry is on the inguard controller board. The circuitry is, however, only used by the voltmeter option and is therefore included in the following explanations.

7-138. The components (i.e., transistors, resistors, etc.) in the different voltmeter circuits have their own numbering structure. For example, all components used by the input amplifier are numbered in the "100" series (e.g., R101, C102, etc.). The circuitry and corresponding numbering structure is as follows:

Component Numbering	Voltmeter Circuitry
Units and 10 series	Input Switching
100 series	Input Amplifier
200 series	A/D Converter
600 700 series	Reference Supplies

7-139. Input Switching

7-140. Refer to Schematic C1 for the following discussion on the input switching circuitry. The circuitry consists of the following:

Overvoltage Protection
Input Switching Paths
Autozero Switching
Gate Bias Amplifier
Charge Conditioning
Switch Control

7-141. Overvoltage Protection. The protection circuitry has two parts to it, high voltage protection and low voltage protection. The circuitry operation is as follows:

a. High Voltage Protection. This circuit protects the voltmeter option's input circuitry from voltages above 400V. The circuit is located on the inguard controller board and consists of a 400V surge voltage protector (E1 on the A2 assembly) in series with a 10 ohm resistor. The circuitry is connected between the HI COM and LO COM Input terminals and conducts with a peak voltage level of 400V (±20%). When E1 conducts, a low impedance path across the input terminals is provided. The 10 ohm resistor, R108, limits the current going through E1.

b. Low Voltage Protection. This circuit protects the input circuitry from voltages between 120V and 400V. Voltage protection is provided by FETs Q9 and Q10 in conjunction with resistor R17, and by the 100:1 resistor divider on R128. The FETs are part of the input path which is selected on the .1V, 1V, and 10V ranges (low voltage range input path, see paragraph 7-142a). The resistor divider is part of the input path selected on the 100V range (the high voltage range input path, see paragraph 7-142b). The operation is as follows:

1. Refer to Figure 7-5A (Simplified Input Switching Circuitry). FETs Q9 and Q10 are connected as diodes with Q9 connected to +12.6V and Q10 connected to -12.6V. If the voltage on the input path exeeds +12.6V, Q9 conducts keeping the path at a +12.6V level. The FET conducts since its source and drain is at +12.6V. If the voltage on the path exceeds -12.6V, Q10 conducts keeping the path at a -12.6V level. The FET conducts since its gate is at -12.6V. With either Q9 or Q10 conducting, the difference between the input voltage and the ±12.6V will be across R17 thereby keeping the voltage on the input path at ≤ ±12.6V.

2. If an overload voltage is applied to the high voltage range input path, the voltage will be divided down by the resistor divider on R128 to a safe value.

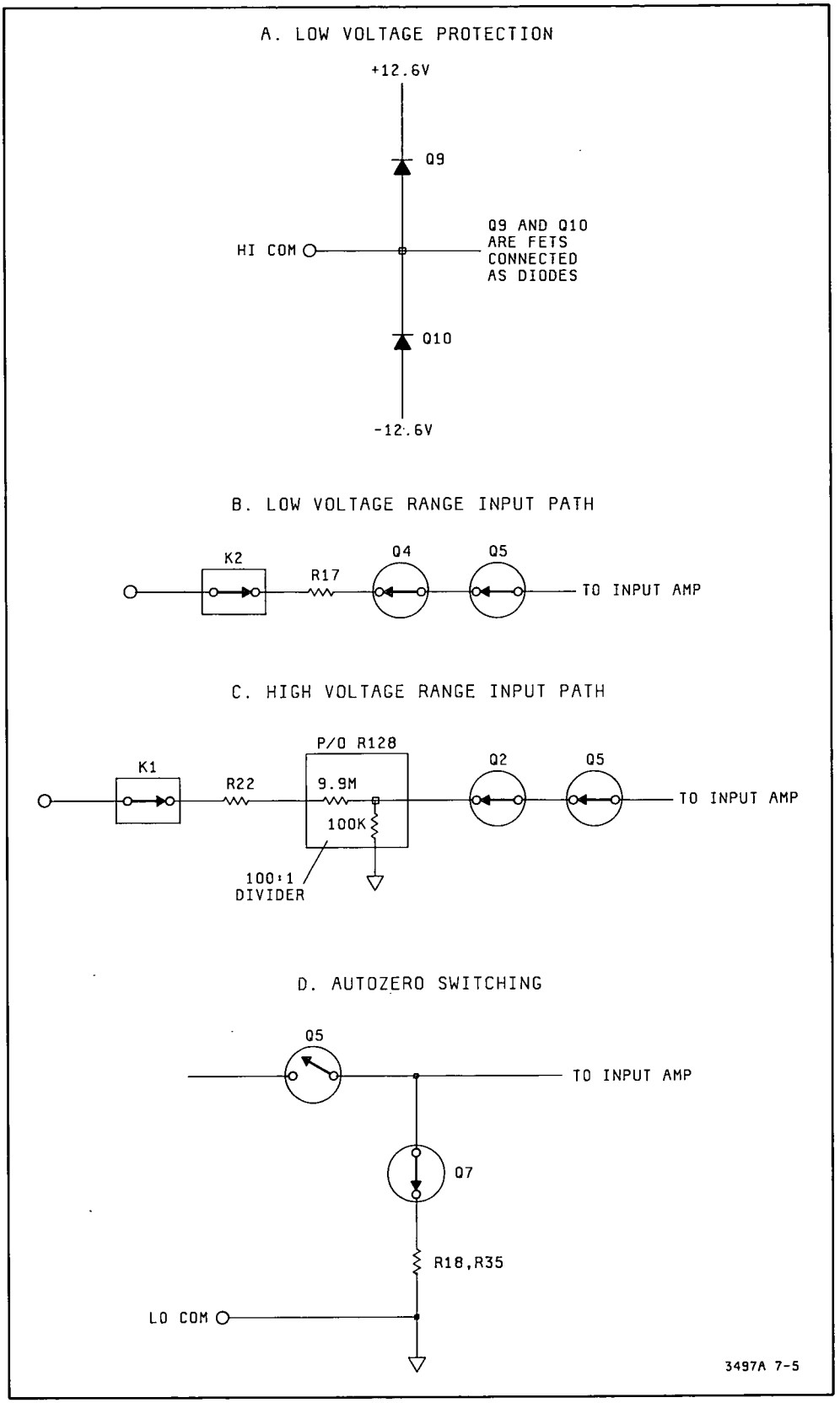


Figure 7-5. Simplified Input Switching Circuitry

7-142. Input Switching Paths. This circuitry consists mostly of FETs and relay switches. The purpose of the switches is to provide two input paths, low voltage range and high voltage range, to the input amplifier. The following explains the two input paths.

a. Low Voltage Range Input Path (Figure 7-5B). The path consists of relay K2, resistor R17, and FETs Q4 and Q5. This path is used only on the 1V through 10V ranges and its purpose is to connect the voltage at the HI COM input terminal to the input amplifier. Capacitor C5 on the path is used to shunt high frequency ac signals on the input path to ground.

b. High Voltage Range Input Path (Figure 7-5C). The path consists of relay K1, resistor R22, the 100:1 resistor divider in R128, and FETs Q2 and Q5. The purpose of the path is to attenuate input voltages (at the HI COM terminal) by a factor of "100" and then connect the resultant voltage to the input amplifier. This path is used only on the 100V range. Capacitor C1 is used to shunt high frequency ac signals on the input path to ground.

7-143. Autozero Switching (Figure 7-5D). When the Autozero function is enabled, the input of the input amplifier is connected to ground (using the autozero switching circuitry). This is accomplished by turning FET switch Q7 on and turning FET Q5 off. At this time, the input at the HI COM terminal is removed from the input amplifier and the amplifier is instead connected through Q7, R35, and R18 to ground. When the amplifier is connected to ground, a zero measurement (i.e., offset measurement) is then made and the resultant reading is stored into the inguard processor's memory. After this, Q7 is turned off and Q5 is turned on and the input at the input terminal is connected to the input amplifier. A regular input measurement is then made. The Autozero cycle continues as long as the function is enabled.

7-144. Another circuit, which is part of the zero measurement circuitry, is resistors R35 and R36. The resistors are used to cancel out any small voltages generated by the printed circuit board ground traces. Resistor R36 applies a small voltage to the ground trace which then cancels out the voltage on the trace. The power supply to which R36 is connected (+12.6V or -12.6V) and also the value of R36 depends on the value and polarity of the voltage generated by the traces.

7-145. Charge Conditioning. When the Autozero function is enabled, FETs Q5 and Q7 are continually turned on and off. This action can generate noise spikes on the input paths between the HI COM terminal and Q5. If any voltage source applied to the input terminals has a high output impedance, the noise spikes can cause erroneous readings. The Switch Feedthrough Adjust and Pre-Charge Adjust circuitry is used to cancel out the noise spikes.

7-146. A stray capacitance can exist between the input path going to the input amplifier and ground. If the Autozero function is enabled and a zero measurement is made, the input to the input amplifier will be at approximately zero volts. After the zero measurement is completed, the input voltage at the HI COM terminal is applied to the input amplifier and charges the stray capacitance. If the input voltage comes from a source with a high output impedance, charging the capacitor can temporarily load down the source. The pre-charge stage prevents this from happening. The operation is as follows:

a. After the zero measurement is made, FET switch Q7 turns off and Q5 remains off.

b. Switch Q8 then turns on and the output of the gate bias amplifier is applied to the input of the input amplifier. Since the gate bias amplifier output has the same amplitude and polarity as the input voltage, the stray capacitance is charged up to that voltage.

c. Switch Q8 is then turned off and Q5 is turned on. The input voltage is then applied to the input amplifier and a regular input measurement is made.

d. This sequence occurs after each zero measurement.

7-147. Switch Control. There are two types of switches used in the input switching circuitry: FETs and relays. During a measurement cycle (i.e., zero measurement and input measurement), all of the relays and some of the FET switches are in a static state, and other FET switches are in a dynamic state. A static state is when a switch is set on or off and remains in that state throughout the entire measurement cycle. A dynamic state is when the switch turns on to off, or vice versa, during a measurement cycle. The switches which are used to select the high and low voltage range paths are normally in a static state, and the switches used in the Autozero function are usually in a dynamic state.

7-148. The FET switches are turned on and off using comparators, which have open collector transistor outputs. The outputs of the comparators are connected to the gates of the FETs and, through pull-up resistors, to the output of the gate bias amplifier. When the output of a comparator goes high, it will be at the gate bias voltage, and when the output goes low, it will be at -18V (i.e., the -18V power supply). A typical comparator/FET switch is shown in Figure 7-6. The following explains the switch control circuitry operation.

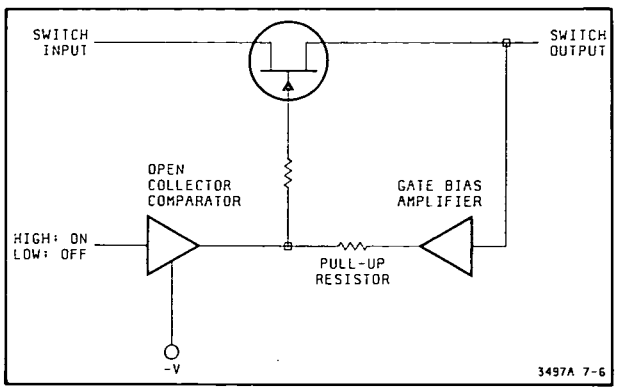


Figure 7-6. Typical Comparator/FET Switch Circuit

a. Static Switches. These switches are relays K1 and K2, and FETs Q2 and Q4. The switches are set, using the LDCL line, to the appropriate state using comparators. With LDCL line a TTL low, the low voltage range input path is selected (i.e, K2 and Q4 on) and with LDCL high, the high voltage range input path is selected (i.e., K1 and Q2 on). The LDCL line is set by the inguard controller. The operation of the static switches is as follows:

1. When the LDCL line is low, the outputs of comparators U1A and U1B, and U2A float to the +5V and +15V power supplies, respectively. This is because the comparators have open collector outputs and their positive inputs are at +2V. The +2V for U2 comes from dividers R11 and R12, and the +2V for U1 comes from R20 and R21.

2. With LDCL low, the output of comparator U1B tries to go to +5V through R3. This turns transistor Q3 on. The collector of Q3 goes low and, since the collector is connected to one side of the relay coil of K2 and the other side of the coil is at +15V, the relay turns on. With LDCL low, the output of comparator U1A also goes to +5V, and turns K1 off. Also, the output of comparator U2A goes to the gate bias voltage and turns Q4 on.

3. When the LDCL line is high, the output of comparator U2D goes to the gate bias voltage and turns Q2 on. This is because the negative input of U2D is at +2V and the comparator also has an open collector output. With LDCL high, the outputs of U1A and U1B float to ground and the output of U2A floats to -18V. The zero output (i.e., ground) of U1A turns K1 on and the -18V output of U2A turns Q4 off. The zero output of U1B turns Q3 off and makes the collector of Q3 go high. This turns K2 off.

b. Dynamic Switches. The dynamic switches consist of Q5, Q7, and Q8 and are turned on and off using the HDZ line. This state of the line is also controlled by the inguard controller. The switch operation is as follows:

1. When the input measurement is made, line HDZ is a TTL low. This low makes pin 1 and pin 10 of U4A high and pin 13 low. With the flip-flop (consisting of U4C and U4D) in this condition, the output of comparator U2B (pin 1) is at the gate bias voltage, and the outputs of comparators U2C (pin 14) and U3B (pin 1) are at -18V. This is since the comparators have open collector outputs and their positive inputs are at +2V. The +2V comes from divider R11 and R12. With the outputs of U2B high, and U2C and U3B low, FET Q5 is on, and FETs Q7 and Q8 are off.

2. After the input measurement is completed and the zero measurement begins, line HDZ goes high. This brings pin 1 of U4 low which turns transistor Q6 on. The collector of Q6 goes high and, since pin 12 of U4D is low, the flip-flop changes state (U4C pin 10 goes low and U4D pin 13 goes high). FET Q5 then turns off and FET Q7 turns on.

3. After the zero measurement is completed, line HDZ goes back to low. This low sets pin 1 of U4A high and turns off Q6. Capacitor C4 is then charged up through R13. This keeps pin 8 of U4C high for a time which depends on the value of C4 and R13.

4. With pin 8 of U4C high and pin 12 of U4D now low, pin 13 of U4D goes low. Since pin 10 of U4C is still low, the output of U4B goes high. This in turn sets the output of comparator U3B to the gate bias voltage and Q8 turns on. FET Q8 remains on until C4 is charged up. Then pin 10 of U4C goes high and Q5 is back on again (see step 1).

7-149. Gate Bias Amplifier. In order for a FET switch to turn on and remain on, the voltage between its source and gate should be at approximately zero volts. This is accomplished by applying a gate bias voltage to the gate which is at the same value and polarity as the voltage at the source. The gate bias amplifier is used to supply the correct gate bias voltage to turn the FETs on. The amplifier is only used for the FETs in the input switching circuitry. The following describes the gate bias amplifier. Refer to Figure 7-6 for the description.

a. The gate bias amplifier is a unity gain non-inverting amplifier consisting of Q1, U5, and associated circuitry. The amplifier output will therefore be approximately the same value and polarity as the input. The input to the amplifier comes from the summing node of Q2, Q4, and Q5.

b. Because of the amplifier's high input impedance, any loading on the Q2, Q4, and Q5 summing node is prevented.

c. Since the output of the amplifier is connected through resistors to the gates of the switching FETs,

the voltage between the gate and source of a FET will be approximately zero volts (when the FET is turned on; see paragraph 7-148a).

7-150. Input Amplifier

7-151. The input amplifier, in conjunction with the input switching circuitry, is used to condition the input signal. This is done in order to apply the same full scale voltage (i.e., 10V dc) to the A/D converter for all full scale inputs to the voltmeter option. The amplifier is non-inverting with selectable gains. Unless otherwise noted, refer to Schematic C2 for the following explanation on the input amplifier.

7-152. The input amplifier consists of a dc amplifier, integrator amplifier, and feedback circuitry. The output of the input switching circuitry is applied to the dc amplifier which is then used to drive the integrator amplifier. The output of the integrator amplifier is the input to the A/D converter. The polarity and amplitude of the voltage applied to the A/D converter depends on the value and polarity of the voltage applied to the input amplifier and the selected gain. A simplified schematic of the input amplifier is in Figure 7-7.

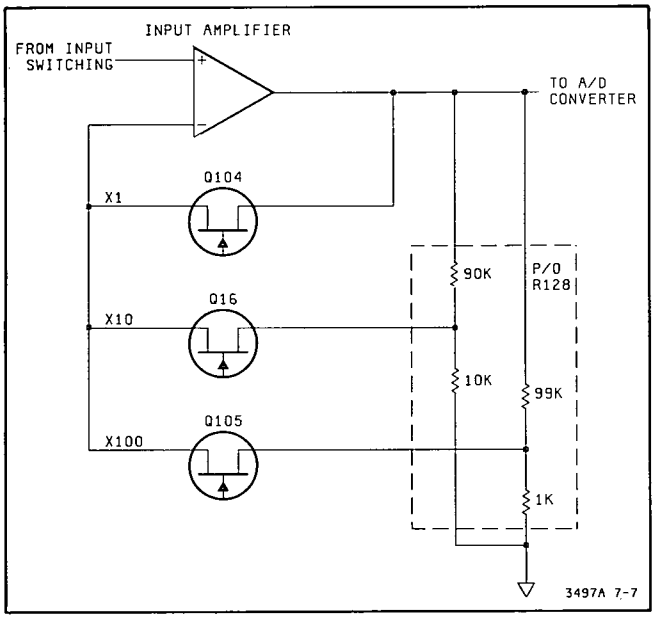


Figure 7-7. Simplified Schematic of the Input Amplifier

7-153. Other circuitry of the input amplifier includes the +18V, +30V, and +2V power supplies, and diodes CR104 and CR105. The power supplies are used by the amplifier and also by the inguard switching circuitry. Diodes CR104 and CR105 are connected to the output of the input amplifier to limit the output voltage. Since CR104 and CR105 are connected to -15V and +15V, respectively, the output of the amplifier is limited to ±15.6V.

7-154. DC Amplifier. The dc amplifier has two parts to it which are explained as follows:

a. One part of the dc amplifier is two dual FETs (Q100 and Q101), connected in cascade, which provide the high input impedance of the amplifier. The impedance is high since the FET bias current is negligible. To improve the stability of the amplifier, a current source, consisting of two pnp and two npn transistors, provides a stable current to the dual FETs. The two npn and two pnp transistors are connected to sense two current mirrors, the 12V A reference and the 18V supply. The stability of the circuit is also improved by having the FET's load resistors in the same package as the main feedback resitors. The good stability of the FETs also improves the stability of the input amplifier itself.

b. The other part of the dc amplifier is U101. The output of U101 is normally at approximately +5V since the "+" and "-" inputs of the amplifier are equal. The output is at +5V since +5V is applied to the "+" terminal through R106 and since R106 has the same value as feedback resistor R108.

7-155. Integrator Amplifier. The integrator amplifier consists mostly of U102 and feedback capacitor C103. The bandwidth of the amplifier depends on the gain selected: X1, X10, or X100. Resistor R110 is used in the X1 gain configuration, resistor R109 in parallel with R110 is in the X10 gain configuration, and R111 in parallel with R110 is in the X100 gain configuration. Resistors R109 and R111 are selected using switching FETs Q102 and Q103, respectively.

7-156. Feedback Circuitry. The feedback circuitry is used to select the different gains of the input amplifier. The selectable gains are X1, X10, and X100 which are determined by the feedback resistors located in resistor network R128. The appropriate resistors are selected by switching FETs Q104, Q106, and Q105 for the X1, X10, and X100 gains, respectively. The FETs are selected by decoder U105 and the decoder receives its information from the inguard controller. A high output from the decoder sets the output of the corresponding comparator (U103) high. This high output then turns the appropriate FET(s) on (see paragraph 7-148 for an explanation on the comparator operation). The decoder logic states, voltmeter ranges, and corresponding gains and FETs are listed in Table 7-3.

7-157. Power Supplies. The following are the power supplies which are part of the input amplifier circuitry.

a. +18V Supply. This supply is the positive power supply for U102 and U5 (see Schematic C1). Its voltage is developed by transistor Q107 and associated circuitry. The +15V supply voltage is also developed by this circuitry.

b. +30V Supply. This supply is only used by the input amplifier and its voltage is developed using op amp U104 and associated circuitry. The voltage level and stability depends on the +12V (applied to the positive input of U104) and feedback resistors R129 and R130.

Table 7-3. Decoder Logic States and Gains Selected

Line VRA	Line VRB	U105 Output pin 1	U105 Output pin 3	U105 Output pin 14	Range	Gain	FETs Enabled
Low	Low	Low	High	Low	.1V	X100 (HA100)	Q103,Q105
Low	High	Low	Low	High	1V,100V*	X10 (HA10)	Q102,Q106
High	Low	High	Low	Low	10V	X1 (HA1)	Q104

*The X10 gain is used with the 100:1 divider on the 100V range

7-158. A/D Conversion

7-159. The voltmeter option's A/D Converter is used to change dc voltages to digital information. The circuitry consists of an A/D input switching circuitry, integrator, slope amp, comparator, A/D Autozero circuitry, and overload detector circuitry. Other circuitry includes the slope control circuit. This circuit generates the necessary signals to control the operation of the A/D converter. The circuitry is controlled by the inguard controller using the A/D logic. Although the A/D logic is used to control the A/D converter circuitry, it is part of the inguard logic. Since its only use is to control the operation of the A/D converter, it is included with the A/D converter explanation. For an explanation on the A/D converter circuitry and the A/D logic, refer to paragraphs 7-177 and 7-186, respectively. The following paragraphs have the voltmeter option's A/D conversion method.

7-160. A/D Conversion Method. The A/D conversion method used by the 3497A voltmeter option is called Multi-Slope II which has two operating states: runup and rundown. The option's most significant digits are developed during runup (see paragraph 7-169) and the least significant digits are developed during rundown. The integration time depends on the selected Number Of Digits Displayed (3½, 4½, or 5½). Since the rundown time is a fixed time for any digit displayed, a change in the runup time changes the total integration time. To help understand Multi-Slope II, first consider the operation of the Dual-Slope Conversion method. This method is explained in the next paragraph.

7-161. Dual-Slope Conversion. In dual-slope conversion, an integrator capacitor charges for a fixed time period (as shown in Figure 7-8), which is done during runup. The charging rate and the resultant amplitude of the charge is proportional to the voltage applied to the integrator. After runup, the integrator capacitor is then discharged at a fixed rate determined by a known reference voltage and is done during rundown. Since the discharge rate is constant, the discharge time is proportional to the amplitude of the charge (input voltage). The amplitude level can then be determined by the discharge time.

7-162. Multi-Slope II Conversion. Multi-Slope II is similar to Dual-Slope in that a capacitor is charged and discharged by the input voltage and by a known reference voltages. The following paragraphs explain the Multi-Slope II operation (runup and rundown). Unless otherwise noted, refer to Schematic C3 for the explanation.

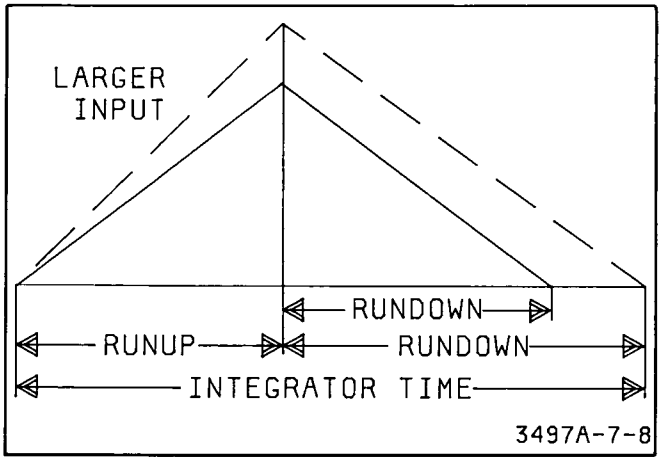


Figure 7-8. Dual Slope Conversion

7-163. Explanation of Runup. The runup operation lasts for a set time period with the amount of time dependent on the Number Of Digits Displayed (see paragraph 7-168). Each time period is divided into a certain number of A/D counts with each count equal to 5 ALE cycles (Address Latch Enable clock from the inguard controller). The A/D counts in the 5½ Digit mode are a total of 1300 counts and the number of counts in the 4¼ Digit mode are 130. Since all the digits in the 3½ Digit mode are developed by the rundown operation, there is very little runup time (13 A/D counts) in that mode. Refer to paragraph 7-168 for more information on the runup time. The following is a simplified explanation of runup. Refer to Figures 7-9 and 7-10 for the explanation.

a. When runup starts, the input voltage (i.e., input amplifier output) is applied to Q202 (part of the integrator) for a set time period (T1). The resultant input current (Iin) then charges integrator capacitor C201 and a certain slope (output of the integrator at TP INT) is then developed. The direction and steepness of the slope depends on the polarity of the input voltage. In the example, a negative input voltage is assumed and, since the integrator inverts the input current, the output slope is positive. (Note: The input voltage is always applied during runup.)

b. After time period T1, the inguard controller determines the direction of the slope. Since the slope is positive (the input current is negative), a positive going current is applied to the integrator for set time period T2. Since this current is larger than the input current and also at opposite polarity, the resultant cur-

rent (applied current minus input current) charges C201 in the opposite direction (i.e., first discharges and then charges C201). This generates a negative going output slope.

c. When time T2 is completed, the inguard controller determines if the output slope has crossed zero. Since zero crossing is detected, a current with the same value as the previously applied current, but at opposite polarity (same polarity as input current), is then applied for time period T3. This current plus the input current then charges C201. Since both currents charge C201, the output slope becomes steeper and, as shown in Figure 7-10, crosses zero.

d. After T3, the inguard controller again checks for zero crossing. Since zero crossing occurred, the current with its polarity opposite to the input current is applied for time period T4. This time period and the periods that follow are the same time as period T3. In the example, zero crossing occurs during T4 (this will vary with different A/D inputs).

e. If, after T4, zero crossing is detected, the current with the same polarity as the input current is reapplied. If, after T4, no zero crossing is detected, the current with the opposite polarity is reapplied. This will be reapplied again, until zero crossing is detected. Since zero crossing is detected in the example, the current with the same polarity as the input current is applied.

f. The operation in step e continues until the runup operation is completed. During the runup operation, a counter in the inguard processor increments during the positive going slope periods and decrements during the negative going slope periods. The counter, in effect, is used to determine the amount of charge added and subtracted from the input voltage. From that information, the most significant digits of the voltmeter's reading is calculated.

7-164. Detailed Explanation of Runup. Figure 7-11 illustrates the runup operation using the 4½ Digit mode (the 5½ Digit mode is similar). Refer to the figure for the explanation in the following steps. The solid lines (in the figure) showing the runup sequence is for a hypothetical input value. The dashed lines are for a larger hypothetical input value.

a. When runup starts, the integrator capacitor (C201) is charged by the input current for time period T1. This current is applied through the 108.33K ohm resistor and input switch Q201 to the integrator (Q202 and U201). Since, in the example, the input current is a negative current, the output slope at TP INT is positive. If the current would have been positive, the output slope would be negative.

b. Time period T1 takes a total of 1.2 A/D counts and, since no current except the input current is applied to the integrator, it is called a no current condition. The resultant output slope is called slope S + 0.

c. After period T1, the inguard processor detects the direction of the current by noting the position of the HCP line (output of comparator U203D). A low on the HCP line shows a positive slope and a high a negative slope. Since, in the example, the slope is positive, HCP will be low.

d. A known current with opposite polarity to the input current is then applied to the integrator for time period T2 (4 A/D counts). This current is called S + 4 and the resultant output slope is called slope S + 4. If the input current would have been positive, the applied current, called S-4, would have been negative. This current has the same value as the S + 4 current, but at opposite polarity. It would have developed a positive going output slope called slope S-4.

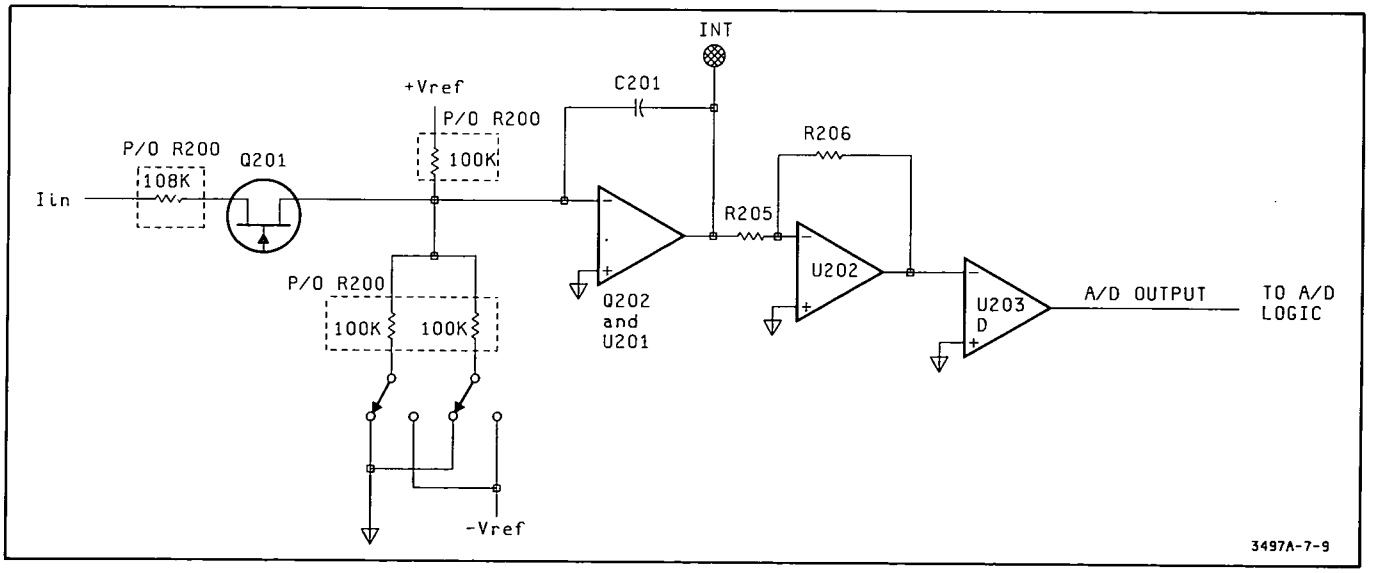


Figure 7-9. Simplified A/D Converter

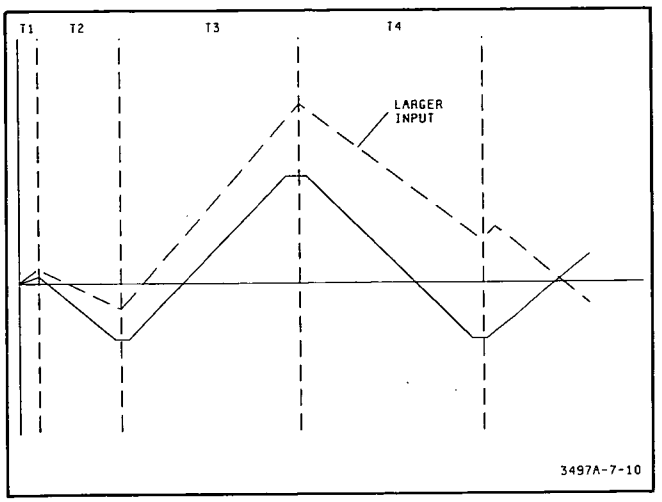


Figure 7-10. Integrator Output Slopes

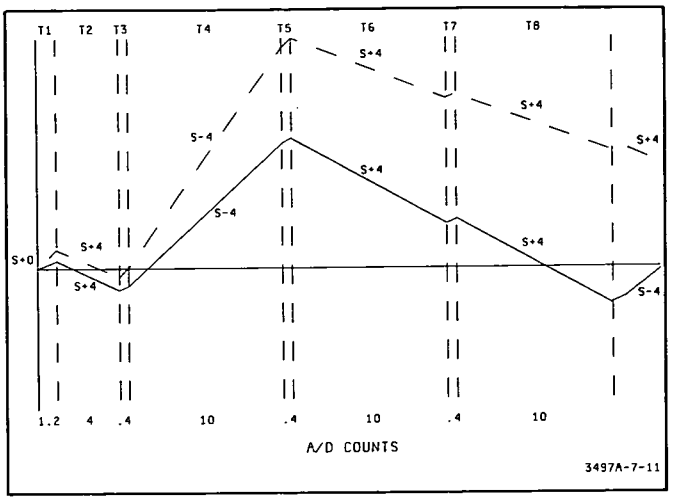


Figure 7-11. Runup Slopes (4½ Digit Mode)

e. After time period T2, current S + 4 is removed. A no current condition (slope S-0) will then exist for .4 A/D counts during time period T3. The charge rate of capacitor C201 is again determined by only the input current. Slope S-0 is also a no current condition, as is slope S + 0. The major difference is that the slopes are generated differently (see paragraph 7-166). Slope S-0 is selected since the previous no current condition was slope S + 0. The slopes alternate with each other (S + 0, S-0, S + 0, etc.) for each no current condition, in runup only.

f. When time T3 is completed, an S-4 current is applied for 10 A/D counts during time period T4. The S-4 current has the same value as S + 4, but at opposite polarity. This charges C201 in the other direction (i.e., the capacitor is discharged and then charged in the other direction).

g. After time T4, the S-4 current is removed and no current (slope S + 0) is applied for time T5. Time T5 is as long as time period T3 (.4 A/D counts). This is also the time period for the S-0 and S + 0 slopes that follow.

h. When T5 is completed, and since zero crossing occurred during time T4, current S + 4 is applied for time T6 (10 A/D counts). Again, after T6, a no current condition (S-0) exists for time T7 (.4 A/D counts).

i. After T7, current S + 4 is applied again since no zero crossing occurred during T6. The S + 4 current is applied during T8. Time T8, and the time periods for slopes S-4 and S + 4 that follow, are also 10 A/D counts.

j. When time T8 is completed, no current (slope S + 0) is applied and then current S-4 is applied (since zero crossing was detected). Then S + 4 is applied (since zero crossing is detected) and so on. This takes place until the runup time is completed. Either current S + 4 or current S-4 is selected, dependent on whether zero crossing occurs, until the runup time is completed.

k. Once the runup operation is completed, the inguard procesor then determines the most significant digit of the reading. The counter in the inguard processor increments for each positive going slope and decrements for each negative going slope. The only exception is the first S-4 or S + 4 slope; it is ignored when doing the calculations. Using the information in the counter, the digits are developed. For other than a zero reading, the number of S + 4 slopes will always be different than the number of S-4 slopes. For a perfect zero reading, the number of S + 4 slopes will be the same as the number of S-4 slopes (with the first S-4 or S + 4 slope ignored). This is represented in Figure 7-12.

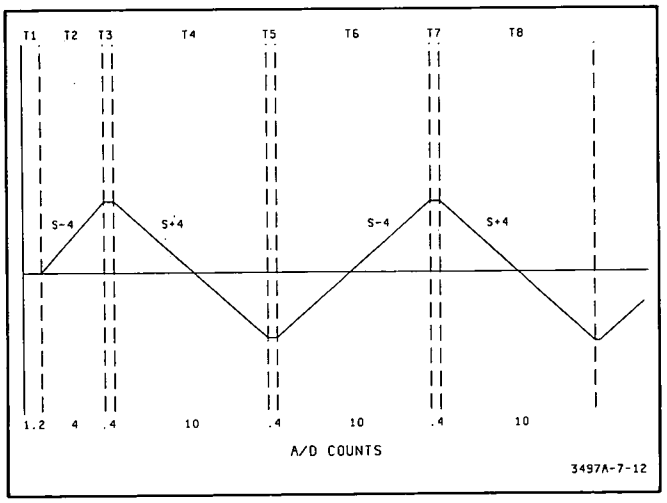


Figure 7-12. Runup Slopes For Zero Inputs (4½ Digit Mode)

7-165. Slope S + 4 and S-4 Generation. The following explains how the currents for slopes S + 4 and S-4 are generated.

a. Slope S+4. Refer to Figure 7-13. Note that both Y1 and Y2 paths are connected to ground. Since the summing node of the paths is a virtual ground and Y1 and Y2 are also connected to ground, no current flows between the paths and the summing node. Current does flow from +Vref (Positive Reference Voltage, +12V) through a 100K ohm resistor into the integrator capacitor (C). This generates a negative going output slope.

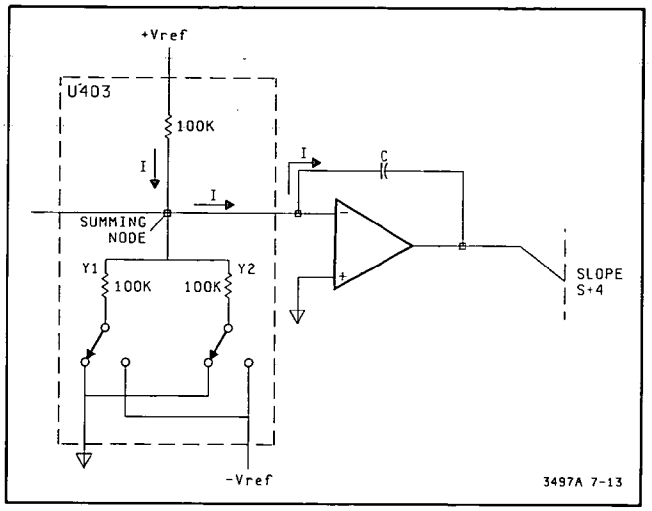


Figure 7-13. Slope S+4 Generation

b. Slope S-4. Refer to Figure 7-14. Note that both Y1 and Y2 paths are connected to −Vref (Negative Reference Voltage, −12VA). Since the summing node is a virtual ground, current flows from +Vref through a 100K ohm resistor and paths Y1 and Y2 to −Vref. Current also flows from the integrator capacitor (C) to −Vref. This current is generated because the total resistance of the Y1 and Y2 paths is smaller than the 100K ohm resistor from +Vref. The current from +Vref plus the current from the capacitor equals the total current through paths Y1 and Y2. Since the total resistance of paths Y1 and Y2 is 50K ohms, the current from +Vref (I1) and the current from the capacitor (I2) is half as large as the total Y1 and Y2 current (I3). The resultant output slope is positive.

7-166. Slope S+0 and S-0 Generation. Refer to Figure 7-15. Note that one side of a 100K ohm resistor (Y1 path) is connected to ground and the other side is connected to the summing node. Since the 100K ohm resistor from +Vref (Y3 path) and the 100K ohm resistor from -Vref (Y2 path) are also connected to the summing node, no current flows from the integrator capacitor (C). This is because the resistance value of path Y2 and Y3 is the same and makes the current value of paths Y2 and Y3 the same (but opposite polarity). This is true for both slopes S+0 and S-0. The only difference is that paths Y1 and Y2 are switched when the slopes are switched (Y1 to ground and Y2 to -Vref, or Y2 to ground and Y1 to -Vref).

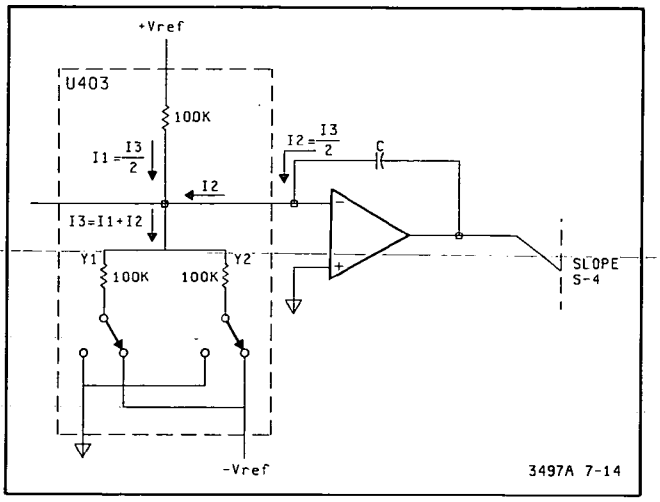


Figure 7-14. Slope S-4 Generation

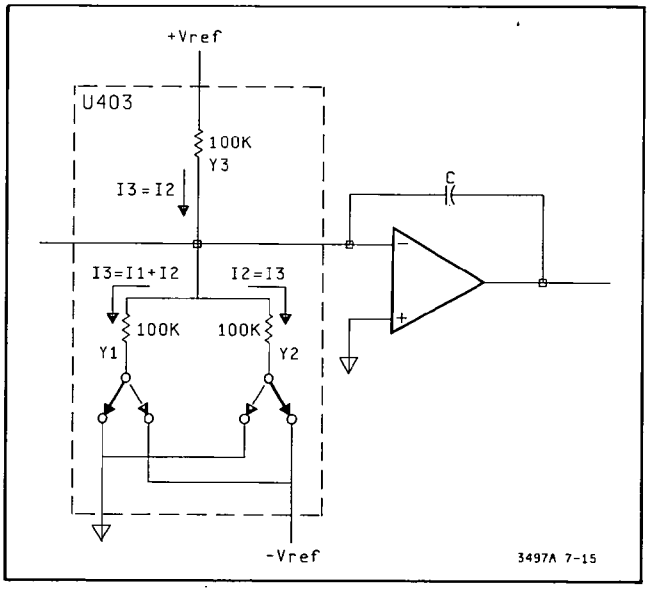


Figure 7-15. Slope S+0 and S-0 Generation

7-167. Runup Times. The A/D converter's runup time, known as Power Line Cycles, depends on the number of digits selected (5½, 4½, or 3½). The different times for both the 50Hz and 60Hz power frequency configurations are listed in Table 7-4.

Table 7-4. Runup Times

Power Line Cycles	Number of Digits Displayed	Runup Time 50Hz	60Hz
1	5½	20mS	16.67mS
.1	4½	2mS	1.67mS
.01	3½	.2mS	.167mS

7-168. Runup Timing. The total runup time takes a certain number of A/D counts with each count equal to 5 ALE cycles (Address Latch Enable clock from the inguard controller). Since the different runup times depend on the number of digits selected, the number of A/D counts will also be different for the diffferent display modes. While looking at Figure 7-16 again, note that the output slopes (i.e., S+4, S-4, etc.) are enabled for certain number of A/D counts (4 counts, 10 counts, etc.). This also changes with the different display modes. This in addition to the total number A/D counts is given in Figures 7-16 and 7-17 for the 5½ and 4½ modes, respectively.

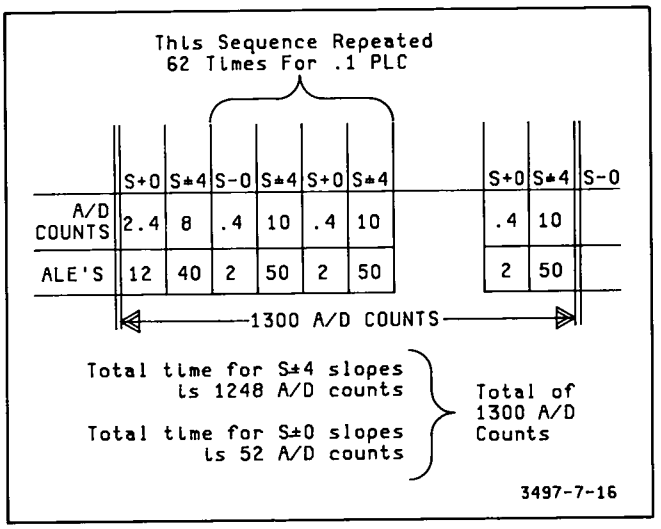


Figure 7-16. Runup Timing for 5½ Digits Displayed (1 PLC)

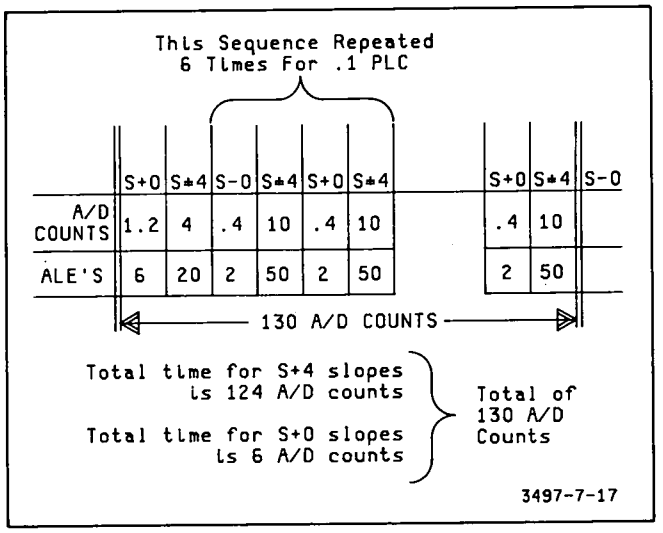


Figure 7-17. Runup Timing for 4½ Digits Displayed (.1 PLC)

7-169. Digit Generation. Runup is used to develop the two most significant digits in the 5½ digit mode and the most significant digit in the 4½ digit mode. The three least significant digits are developed by rundown (see next paragraph). Rundown actually develops four digits with the last digit rounded off to the next higher digit.

7-170. Rundown. When runup is completed, the voltage at the A/D Converter's input is removed and the input is then connected to ground (through Q200 and Q205). The rundown operation then starts. Rundown is used to determine the three least significant digits of the voltmeter option's reading.

7-171. After runup is completed, a voltage (or charge) remains on the integrator with its amplitude and polarity dependent on the last current applied (S+4 or S-4) and the input voltage (applied during runup). By obtaining the value of the remaining voltage, the least significant digits can then be determined. The voltage value is obtained by applying various currents to the integrator and determining how long the currents have to be applied for the resultant output slopes at the integrator to cross zero.

7-172. The currents applied to the integrator are called S-4, S+4, S-3, S+2, and S-1 currents and the resultant output slopes are the S-4, S+4, S-3, S+2, and S-1 slopes. The currents are applied in this order: S-4 or S+4, S-4, S+4, S-3, S+2, and S-1. Each one of the currents are applied (in the given order) to the integrator until the output slopes cross zero. The S-4 and S+4 currents have the same polarity and value as the S-4 and S+4 currents used in the runup operation (see paragraph 165). The other currents are at a different value (see paragraph 7-173). Refer to Figure 7-18 for the following explanation on the rundown operation.

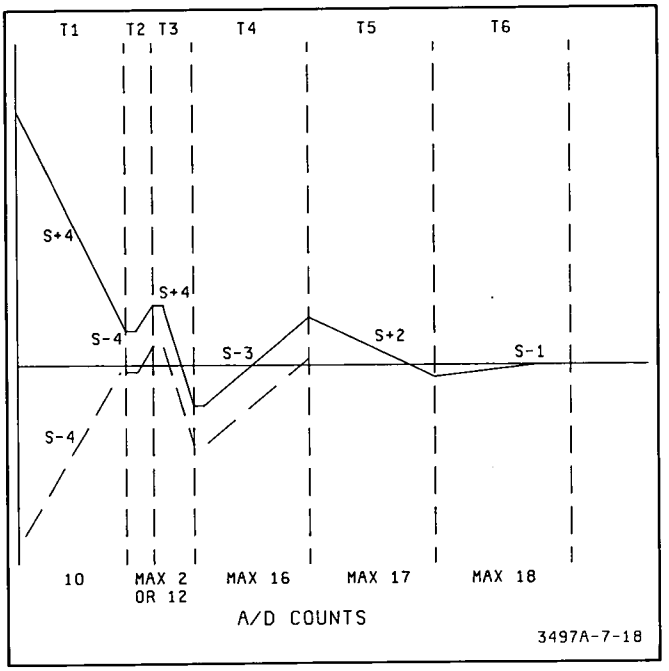


Figure 7-18. Rundown Slopes

a. After runup, the input voltage to the A/D converter is removed and the input of the converter is connected to ground (through Q200 and Q205). The inguard controller then determines the polarity of the remaining voltage on the integrator (C201). Depending on the

polarity, either an S-4 or S + 4 current is applied to the integrator for 10 A/D counts (time T1 in the figure). If the remaining voltage on the integrator is positive, an S + 4 current is applied. If the voltage is negative, an S-4 current is applied (dashed lines in Figure 7-18). The resultant output slopes at TP INT are negative going slope S + 4 or positive going slope S − 4. The currents are applied to make sure the slopes that follow will be able to cross zero.

b. When the S + 4 current or S-4 current is removed, a no current condition (slope S + 0, see paragraph 7-166) will exist for a short period of time. This condition will also exist between the S-4, S + 4, S + 3, etc., currents that follow. Unlike it is in runup, only an S + 0 condition will exist instead of alternating S + 0 and S-0 conditions.

c. The next current, an S-4 current, is applied for 2 A/D counts or a maximum of 12 A/D counts (time period T2). This depends on the polarity of the integrator output, after the previously applied S-4 current or S + 4 current. If the output slope was positive, the S-4 current is applied for 2 A/D counts. If the slope was negative, the S-4 current is applied until the resultant S-4 slope crosses zero (dashed lines in the figure). This time can be a maximum of 12 A/D counts. The S-4 current is removed within 1 A/D count after crossing zero or, if the slope was positive, after 2 A/D counts are completed.

d. After current S-4 is removed, a no current condition (S + 0) will again exist for a short time period. After that, current S + 4 is applied (time T3). Similar to the operation in the previous step, this current is applied either for 2 A/D counts or until the output slope crosses zero. This time can also be a maximum of 12 A/D counts. Here again, this depends on the polarity of the integrator output. Current S + 4 is also removed within 1 A/D count after crossing zero or after the 2 A/D counts are completed.

e. Again a no current condition exists for a short time. Then current S-3 is applied (time T4) until slope S-3 crosses zero. This current is 1/10 the value of the S + 4 current (same polarity as S + 4) and can be applied for a maximum of 16 A/D counts. The current is removed within 1 A/D count after zero crossing occurs. Under normal condition, the resultant S + 3 output slope will always cross zero.

f. When current S-3 is removed, a no current condition will again exist. Then current S + 2 is applied (time T5). This current is 1/100 the value of current S + 4 (1/10 the value of current S-3, but at opposite polarity) and is applied until slope S + 2 crosses zero. This time can be a maximum of 17 A/D counts. Zero crossing should occur during this time and the current is also removed within 1 A/D count after zero crossing occurs.

g. Then, a no current again exists and, after that, current S-1 is applied (time T6). This current is 1/1000 the value of current S-4 (1/10 the value of of S + 2 and 1/100 the value of S-3). The current is applied until slope S-1 crosses zero. This can be a maximum time of 18 A/D counts.

h. After slope S-1 crosses zero, the A/D operation is complete. The inguard controller then uses the time it took for the different slopes (S-4, S + 4, etc.) to cross zero and determine the least significant digits. The 10 A/D counts, when the first S-4 or S + 4 were applied, are also included to determine the digits.

7-173. Rundown Slope Generation. The S-4 and S + 4 slopes are generated the same way it was done for the runup operation (see paragraphs 7-165). The only difference is that they are developed with the input current removed. The S + 0 slope is generated the same way as the S + 0 slope in runup (see paragraph 7-166). The S-3 and S-1 currents use the same circuitry configuration as the S-4 current (see Figure 7-14), but use different resistor values. The resistor values are such that the S-3 current is 1/10 the S-4 current and the S-1 current is 1/1000 the S-4 current. The S + 2 current uses the same circuitry configuration as the S + 4 current (see Figure 7-13). In this case, the resistor values chosen are such that the S + 2 currents is 1/100 the value of S + 4 current.

7-174. Rundown Timing. Each applied current during rundown has a certain time (i.e., A/D counts) in which the corresponding output slopes can cross zero. This is represented in Figure 7-19. The order in which the different currents are applied is also shown in the figure. The total rundown time is a maximum of 1.2mS. In rundown, as in runup, one A/D count also equals 5 ALE clock cycles.

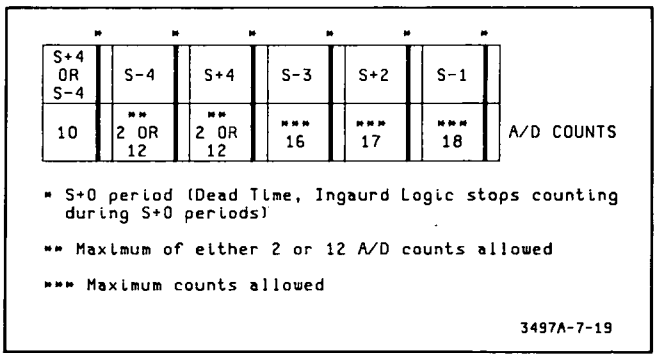


Figure 7-19. Rundown Timing

7-175. A/D Autozero Operation. One other A/D operation is A/D Autozero. This is NOT the same as the voltmeter's Autozero function (input amp connected to ground, see paragraph 7-143), it is only for the A/D converter. The purpose of A/D Autozero is to compensate for any offsets developed by inaccuracies between the positive and negative reference supplies, the resistors

used to develop the S-4, S + 4, etc., currents, and the integrator circuitry. While referring to Figure 7-15, note that + Vref is connected to one side of a 100K ohm resistor and -Vref to one side of another 100K ohm resistor. The other ends of the resistors are connected to each other and also to the integrator. If the absolute values of the + Vref and -Vref voltages are exactly equal and the resistors are also equal, the current going into the integrator is exactly zero. Since the resistors and reference supplies are not exactly equal (they are, however, very stable), a small offset current is generated. This current plus the offset developed by the integrator itself, develops an offset voltage at the output of the integrator. This offset voltage can cause inaccuracies. The A/D Autozero circuitry compensate for that offset voltage.

7-176. The A/D Autozero operation takes place between any measurement cycle (i.e., rundown and runup). During this time, the integrator is configured for a no current condition (S + 0). FET switch Q203 (see Schematic C3) is then turned on and the resultant offset at the integrator output (TP INT) is then stored (through R209) by the Autozero capacitor (C203). When the A/D runup operation starts, Q203 turns off. Since the stored voltage on C203 is connected to the positive input of the integrator (pin 6 of Q202), an offset voltage is generated. This offset is at opposite polarity and has the same amplitude as the offset generated by the references, resistors, and integrator. Both offsets in effect cancel each other out and the integrator output is at zero volts.

7-177. A/D Converter Circuitry

7-178. The A/D Converter Circuitry consists of the following:

A/D Input Switching (Q200, Q201, and Q205)
Integrator (Q202, U201, and C201)
Slope Amp (U202)
Comparator (U203D)
A/D Autozero Circuitry (Q203 and C203)
Overload Detector (U203A to U203C)
Slope Control Circuit (R200, U200, and U205 to U208)

Refer to Schematic C3 for the following explanation on the A/D Converter Circuitry.

7-179. A/D Input Switching. The purpose of this circuit is to do either of two things: connect the input of the A/D converter to the integrator or connect the integrator to ground (LO COM Terminal). The operation is as follows:

a. During runup, when the input of the A/D converter is to be connected to the integrator, FET Q201 is turned on and Q200 and Q205 are off. FET Q201 is turned on by setting its gate to zero volts. This zero volt level comes from the slope control circuit (see paragraph 7-185). Since the gate of Q201 is also connected to inverter U200A, the output of the inverter is -12V which turn FETs Q200 and Q205 off.

b. During rundown, when the integrator input is connected to ground (zero volts input), FETs Q200 and Q205 are on and Q201 is off. FET Q201 is turned off by setting its gate to -12V (from the slope control circuit). This turns FETs Q200 and Q205 on since the -12V is inverted by U200A. The integrator input is then connected through R218 and Q205 to ground. Resistor R218 is used to keep the integrator input impedance the same with Q201 on or off. FET Q200 is used to set the source of Q201 to zero volts which prevents Q201 from being turned on (i.e., forward biased).

7-180. Integrator. The S-4, S + 4, etc., slopes are generated by the integrator using the S-4, S + 4, etc., currents (plus input current, only during runup). The integrator consists of Q202, U201, C201, and associated circuitry. The circuitry is a differential amplifier with capacitance feedback. The slopes are developed by charging and discharging capacitor C201 using the applied S-4, S + 4, etc., currents (plus input current, only during runup).

7-181. Slope Amp. The slope amp is used to amplify the integrator output and connect it to the comparator and A/D Autozero FET. The amplifier makes sure that any low integrator output levels are large enough for the comparator (U203D) to quickly detect zero crossings of the integrator output slopes. The amplifier output is also used to charge the A/D Autozero capacitor (C203). The amplifier is an inverting amplifier with a gain of X100. The gain is determined by feedback resistor R206 and input resistor R205. The output of the amplifier is clamped to ± .6V by CR200 and CR201 to speed up the comparator operation. Diode CR200 also prevents the negative terminal of comparator U203D from going below -.6V. Since the positive terminal of U203D is connected to ground, a large negative voltage on the negative terminal could damage the comparator. Diode CR200 prevents this from happening.

7-182. Comparator. The comparator (U203D) output is used by the inguard controller to determine voltmeter reading. Since the comparator's positive terminal is connected to ground, a voltage on its negative terminal that is above ground (>0V) develops a low output (0V) and a voltage below ground (<0V) develops a high output (+5V).

7-183. A/D Autozero Circuitry. Refer to paragraph 7-174 for the purpose and operation of the A/D Autozero circuitry. The A/D Autozero voltage is developed across C203 when Q203 is turned on. The FET is on when its gate is at zero volts which is developed by latch U207.

7-184. Overload Detector. The overload detector circuitry, consisting of U203A through U203C and associated circuitry, is enabled when the integrator output slope or voltage exceeds ± 12.4V (which is 124% of full scale). When the output is above ± 12.4V, the output of U203C (pin 14) goes low which flags and tells the inguard controller that an overload condition exists. The

A/D operation will then be aborted and a new A/D operation is started. This is repeated until the integrator output is below ± 12.4V. The overload detector operation is as follows:

a. As long as the integrator output is below ± 12.4V, the outputs of U203A and U203 are high. This is because the positive terminal of U203B is above zero volts and the negative terminal of U203A is below zero volts. The terminals are at those levels since R222 is connected to -12V and R219 to + 12V.

b. If the voltage or slope at the integrator output is above + 12.4V, the negative terminal of U203A is above zero and its output goes low. If the integrator voltage is below -12.4V, the positive terminal of U203B is below zero and its output goes low. Since U203A and U203B both have open collector transistor outputs, a low output on either comparator will make the output of the other comparator also low. Diode CR203 makes sure that the negative terminal of U203A does not go below -.6V to prevent U203A from being damaged.

c. A low output from either U203A and U203B will make the positive terminal of U203C low. This makes the output of U203C low, showing an overload condition.

7-185. Slope Control Circuit. The slope control circuit, consisting of R200, U200, and U204 through U208, generate the various S-4, S + 4, S-3, etc., currents. The circuitry receives its information from the A/D logic which receives its information from the inguard controller. Except for U204, the integrated circuits used are all CMOS devices. The following explains the slope control circuit operation.

a. The HSA, HSB, HSC, and LRU inputs to level shifter (i.e., comparator) U204 are used to select the runup and rundown operations, and the different currents (S-4, S + 4, etc.) used in the rundown and runup operations. The inputs to U204 are at TTL logic levels (low = 0V, high = + 5V) and the outputs are shifted to CMOS levels (low = -12V, high = 0V). This is since the CMOS devices in the slope control circuit operate at 0 and -12V levels (because the power supplies for the devices is the -12VA reference supply). Since the HSA, HSB, etc., lines are connected to the negative terminals of U204, a 0 (low) input is shifted to -12V and a + 5V (high) input is shifted to 0.

b. Except for the HRU line, the $\overline{A}$, $\overline{B}$, and $\overline{C}$ lines are decoded by decoder U205 in conjunction with the exclusive OR gates in U206. This decoded information selects the various currents.

c. The decoded information, in addition to the HRU line, is latched to the appropriate devices by U207 during each cycle of the ALE clock. The clock input to U207 is the same as the ALE clock, after the clock level has been shifted from TTL levels to CMOS levels by Q206 and Q204.

d. The output of the latch are the AZ (Autozero), HRU (high runup), and the current select lines. A high HRU line enables Q201 and disables Q200 and Q205 (see paragraph 7-179). A high on the AZ line enables Q203. The other outputs of U207 go to inverter/buffer U208.

e. The S-4, S + 4, etc., currents are generated by inverter/buffer U208 in conjunction with resistor network R200. If an input of a buffer in U208 is at -12V, the corresponding output is 0V which generates a positive current. The polarity of the current depends on the + 12V reference and its value depends on the reference supply and the resistors in R200. If an input of a buffer in U208 is at 0V, the corresponding output is -12V which generates a negative current. The polarity of the current depends on the -12VA reference (connected to U208) and its value depends on the reference supply and the resistors in R200.

7-186. A/D Logic

7-187. To understand the operation of the A/D logic, the voltmeter option's A/D converter operation needs to be known. Read paragraph 7-157 before reading the following explanation. Refer to Figure 7-20 and Schematics B1 and B2 for the following explanation on the A/D logic operation and circuitry.

7-188. A/D Logic Operation. The A/D logic is part of a loop that includes the inguard processor (U204) and comparator U203D in the A/D converter circuitry. This loop is used to control the A/D operation. The A/D logic does the following.

a. Latches and transfers the current select data to the A/D converter during runup and rundown. This data is used to select the different S-4, S + 4, etc., currents.

b. In rundown, the logic and the inguard processor count the amount of time it takes for the different S-4, S + 4, S-3, etc., slopes to cross zero.

c. Disables the A/D operation if the A/D converter is in overload.

7-189. A/D Logic Operation during Runup. During runup, latch U5 is always enabled by the inguard processor and the data to select the appropriate S + 4, S-4, etc., currents is latched to the A/D converter by U5. At this time, line LRU (Low Runup) is set low by the processor which places the A/D converter into the runup mode.

7-190. The current select data comes from the inguard processor over the AVM, BVM, and CVM lines. Lines BVM and CVM are used to select the current value and line AVM selects the polarity of the current. These lines

(after going through latch U5) become the HSA, HSB, and HSC lines, respectively. The correct state of the HSA, HSB, and HSC lines to select the different currents is given in Figure 7-20.

7-191. In order for latch U4 to be enabled, one or more of the HSA, $\overline{\text{HSB}}$, and $\overline{\text{HSC}}$ lines must be low, and the QD output of counter U1 must also be low. A low on at least one of the HSA, $\overline{\text{HSB}}$, and $\overline{\text{HSC}}$ is normally generated when any S-4, S+4, etc., current is selected. The QD output of counter U1 will also be low since the counter is disabled during runup. The counter is disabled when the RESET line from port P31 of the inguard processor is high. A low on any one of the HSA, $\overline{\text{HSB}}$, and $\overline{\text{HSC}}$ lines outputs a high at NAND gate U4A. The high at the output develops a low at the output of NOR gate U3A. Since the QD output of U1 is low, the D output of flip-flop U8 is low which makes the output of NOR gate U3B low. This low is inverted by NAND gate U2A and enables latch U5.

7-192. The runup mode is selected when the HRU line and the LOV (Low Overload) line are both high. At this time, the output of NAND gate U4C is low. Since the output is the LRU line, the runup mode is selected. The HRU line is set high by the inguard controller and the LOV line is high if no overload condition exists in the A/D converter (see paragraph 7-184).

7-193. A/D Logic Operation during Rundown. During rundown, as in runup, the A/D logic in conjunction with the inguard processor selects the different currents. The A/D logic is also used to determine how long the currents are to remain on.

7-194. Refer to Figures 7-18 and 7-20 for the following explanation on the A/D logic operation during rundown.

a. After runup is completed, the input to the A/D converter is removed and the integrator input is then connected to ground. This is accomplished by setting the HRU line from the inguard processor low. Dependent on the polarity of the remaining voltage on the integrator capacitor, either an S-4 or S+4 current is applied for 10 A/D counts. After the 10 A/D counts are completed, a no current condition (S+0) is selected by the processor for a short time.

b. After the S+0 slope, an S-4 current is always selected. At this time, 4-bit counter U1 is enabled by the inguard processor. The counter then starts incrementing during each ALE cycle. When the counter is clocked by the ALE clock five times, it sets its QC output high (see U1 outputs in Figure 7-20). This high strobes the internal counter of the inguard processor and lets the processor know that one A/D count is completed.

c. If after the one A/D count (i.e., five ALE cycles) no zero crossing is detected (HCP line from the A/D converter changes state), the 5 ALE count is again started by counter U1. (In the example of Figure 7-18, no zero crossing is detected.)

d. If zero crossing was detected, the applied current is removed and a no current condition, S+0, is selected for a certain time. At this time, the QD output of counter U1 goes high (see U1 outputs in Figure 7-20) and the counter is placed in a wait state. This state remains until the S+0 period is completed. The same takes place for any S+0 condition in rundown. Zero crossing usually occurs during an A/D count rather than at the end of one. Because of this, the applied current is removed not when zero crossing occurs, but when the A/D count is completed. Counter U1 keeps on incrementing, after zero crossing, until the five ALE cycles (i.e., one A/D count) is completed.

e. In the example, current S-4 remains on for 2 A/D counts. Then current S+0 is selected and the same takes place as in the previous step. Counter U1 is placed in the wait state until S+0 is completed.

f. After S+0, current S+4 is then applied. At this time, counter U1 starts counting again. Since the QD output of counter U1 was high, U1 is cleared after being clocked by the first ALE cycle. The S+4 current remains on until zero crossing occurs for a maximum time of 12 A/D counts. These A/D counts are also developed using counter U1, as was done in step b.

g. The same takes place for the following applied S-3, S+2, and S-1 currents. Counter U1 counts during each S-3, S+2, and S-1 currents and is in a wait state during the no current (S+0) conditions.

h. When the last S-1 slope crosses zero, counter U1 is disabled by the inguard processor and the rundown operation is completed.

7-195. A/D Logic Circuitry Operation during Rundown. The following paragraphs explain the A/D logic circuitry operation during rundown. Refer to Figure 7-20, and Schematics B1 and B2 for the explanation.

7-196. Counter U1 is enabled by a low on the RESET line which comes from the inguard processor. This low on the RESET line, after going through U7A and U6C, develops a low output at U6B. This enables U3C. The ALE clock is then applied to counter U1 through U3C and clocks U1. When rundown is completed, the RESET line is set high by the inguard processor and the counter is disabled.

7-197. Gate U6B develops a low since the output of U4B is high and the output of U6C is low. The output of U4B is high because both the $\overline{\text{HSA}}$ and $\overline{\text{HSB}}$ lines are high. A high on any of the $\overline{\text{HSA}}$, $\overline{\text{HSB}}$, and $\overline{\text{HSC}}$ lines will develop a high on the output of U4B. The only time the output of U4B goes low is when all of the $\overline{\text{HSA}}$, $\overline{\text{HSB}}$, and $\overline{\text{HSC}}$ lines are low. This only happens during an S+0 condition. The output of U6C is low since its pin 8 is high.

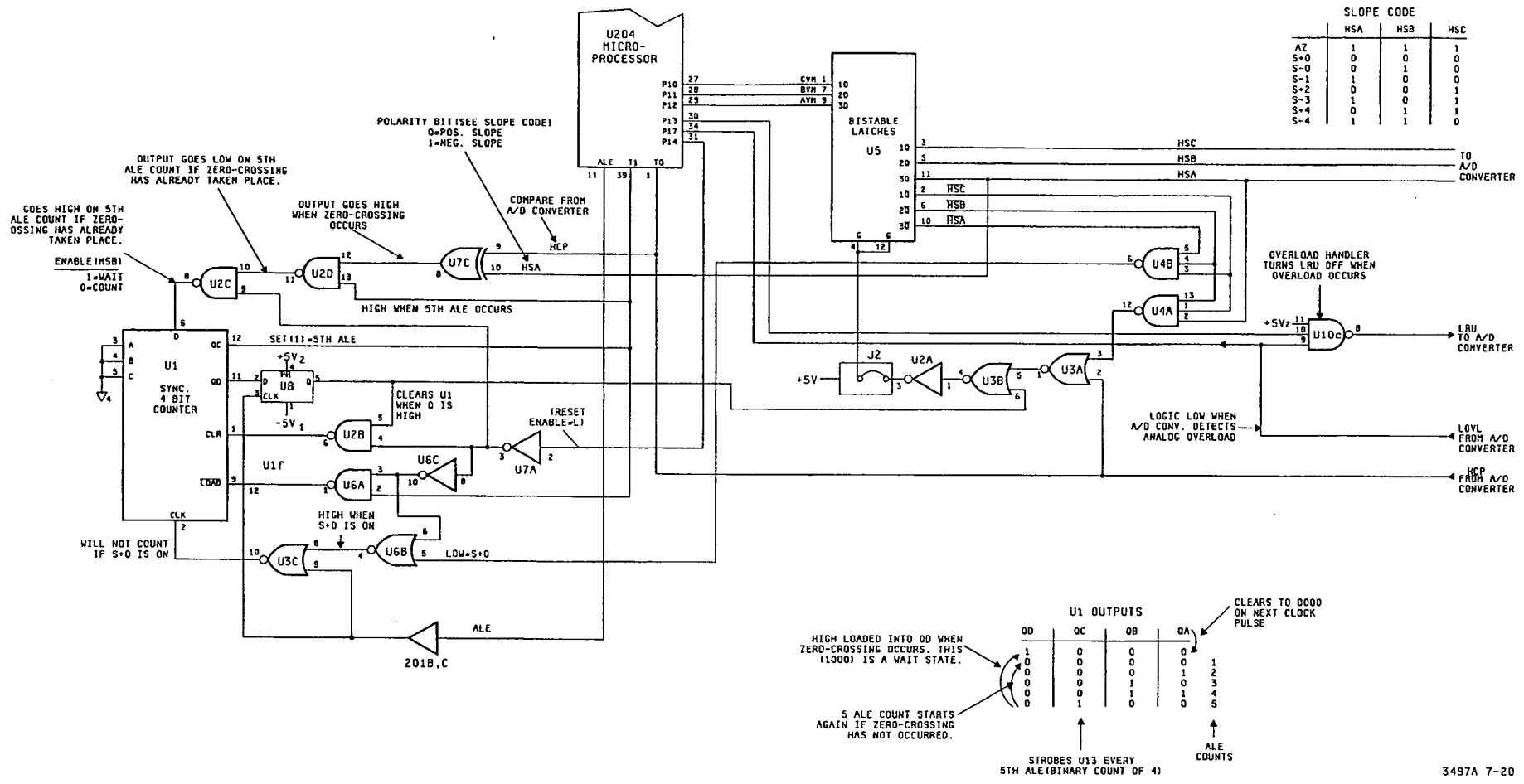


Figure 7-20. A/D Logic and Associated Circuitry

7-198. When counter U1 is enabled, its QC output will go high after the fifth ALE cycle. The inguard processor's internal counter is strobed (T1 input) and lets the processor know that one A/D count is completed. The information at the A, B, C, and D inputs (see next paragraph) of the counter are then loaded into the counter when the counter is clocked (after the fifth ALE cycle). This happens since a high at QC sets the counter's LOAD input low. A high at QC sets the output of NOR gate U6A low since pin 3 of U6A is low. The pin is low because the RESET line is low (see paragraph 7-196).

7-199. If during the five ALE cycles no zero crossing had occurred, the counter's A, B, C. and D inputs are all low. A low on the inputs sets the QA, QB, QC, and QD outputs of U1 low (0000) when the counter is clocked. Inputs A, B, and C are low because they are connected to ground and input D is low because the output of U2C is low.

7-200. If during the five ALE cycles zero crossing had occurred, the counter is placed in a wait state (its QA, QB, QC, and QD outputs are 1000). The counter is set into a wait state when its D input goes high (output of U2C is high). When this is loaded into U1, the counter's QD output goes high and U1 cleared. The counter is cleared when its CLR input is low. This low is developed by U8 when U8 is clocked by the ALE clock. The Q output of U8 is then high and, since both inputs of U2B are now high, the output of U2B goes low.

7-201. At the time when the QC output of counter U1 is high and zero crossing is detected (HCP line changes state), the inguard processor selects an S+0 condition. When this current is selected, all of the $\overline{\text{HSA}}$, $\overline{\text{HSB}}$, and $\overline{\text{HSC}}$ lines go high. This sets the output of U4B low which in turn sets the output of U6B high. A high on U6B turns off U3C and the clock signal for U1 is disabled. This remains until a different current is selected by the processor. Counter U1 is then clocked, and since it was cleared by a high at its QD output, it is set to "0000". The counter then starts incrementing at the next ALE cycle.

7-202. The circuitry which sets the D input of counter U1 high, after zero crossing occurs, includes exclusive OR gate U7C and NAND gates U2C and U2D. The operation is as follows:

a. Before zero crossing occurs, the HCP line (from the A/D converter) and the HSA line (current polarity bit) are at the same high or low state. The high or low state depends on the S+4, S-4, etc. currents applied to the A/D integrator. When the HCP and HSA lines are at the same state, the output of U7C is low. This low develops a high at the output of U2D. The high remains, even if pin 13 of U2D (i.e., the QC output of counter U1) is high or low. As long as counter U1 is enabled by the RESET line, the high at U2D develops a low at the output of U2C. The output of U2C is the D input to counter U1.

b. When zero crossing occurs, the HCP line changes state. This then sets the output of U7C high. This high will not change the output of U2D (i.e., remains high) until the QC output of counter U1 goes high. When QC goes high, the output of U2D goes low. This sets the output of U2C high and the D input to U1 goes high.

7-203. Overload Detection during Runup. When the output of the integrator in the A/D converter exceeds ±12.4V, the LOW OVERLOAD line goes low (see paragraph 7-184). The low on the line does two things: it lets the inguard processor know that an overload condition exists and it disables runup. The processor receives the overload information when the LOL, which is connected to the LOW OVERLOAD line, goes low. This line also sets the output of NAND gate high which disables runup (set line LRU high). When the processor receives the overload, it starts a rundown operation. This discharges the overload voltage at the integrator capacitor. The processor then sets its HRU line high to enable runup.

7-204. Reference Supplies

7-205. The reference supplies provide three stable voltages for the A/D converter: -12VA, -12VB, and +12V. These voltages are used by the A/D converter to develop the S-4, S+4, etc., currents and are also used by some of the input amplifier circuitry. Refer to Schematic D1 for the following explanation on the reference supplies.

7-206. -12VA Supply. This voltage is the most stable of the reference supply voltages and determines the long range stability of the voltmeter option. The voltage is developed by non-inverting amplifier U601 and Q700 using the feedback resistors located in R200 and 7V reference diode (zener diode U600). The reference diode is connected to the positive terminal of U601 and determines the stability of the reference voltage. The diode is very stable since it has its own heater to keep the diode temperature as stable as possible. The output of U601 drives Q700 which outputs the reference voltage. Transistor Q700 is a buffer which prevents the loading down of U601. The feedback resistors in R200 can be coarse and fine adjusted to adjust the amplitude of the reference supply. This is part of the dc voltmeter calibration procedure and is necessary for the voltmeter to measure input voltages accurately.

7-207. -12VB Supply. This supply is a buffered -12V reference voltage and is used by less critical circuitry in the A/D converter. The voltage is developed by X1 gain non-inverting amplifier U700 and the -12VA supply.

7-208. +12V Supply. This supply is developed by U701 using feedback resistors in R200 and the -12VA supply. Amplifier U701 is configured as an X1 gain inverting amplifier. The two 100K ohm resistors in R200 determine

the gain. The stability of the +12V supply depends on the feedback resistors, the -12VA supply, and U701. Because of this, the amplifier has good short term stability.

7-209. DC CURRENT SOURCE CIRCUITRY DESCRIPTION

7-210. The dc current source of the 3497A voltmeter option is able to supply a constant current of 1mA, 100μA, or 10μA. The current source consists of the following circuitry.

Reference
Gate Bias Amplifier
Feedback Resistors
High Voltage Protection
Floating Power Supply

The following paragraphs describe the dc current source circuitry. Unless otherwise noted, refer to Schematic C4 for the explanation.

7-211. Current Generation

7-212. Refer to Figure 7-21 for the following explanation which shows how the current source generates a current of 1mA. Current generation of 100μA and 10μA is similar.

a. The output of the reference circuit, consisting of U401 and associated circuitry, is at approximately -11V which is applied to one side of the 7500 ohm resistor in R128. The negative terminal of U401 is at approximately -3.5V.

b. Since the negative terminal of U401 is at approximately -3.5V, the positive terminal of the gate bias amplifier (U402) is also at -3.5V. This is since the terminal is connected to the negative terminal of U401.

c. Because the non-inverting terminal (positive) of U402 is at -3.5V, its inverting terminal (negative) must also be at -3.5V. This applies -3.5V to the other side of the 7500 ohm resistor in R128. The voltage drop across the resistor is at approximately 7.5V (11V -3.5V) which makes the current going through the resistor 1mA.

d. When a load is connected to the HI and LO Output Terminals, current Is flows from the +17.2V supply through the load resistor, high voltage protection circuitry, FET Q400, the 7500 ohm resistor (in R128), to the output of U401.

e. To satisfy the conditions in steps a through c, the current through the 7500 ohm resistor (i.e., Is) must be 1mA. FET Q400 in conjunction with the gate bias amplifer (U402) makes sure that the current is correct. The FET acts like a variable resistor and regulates the current flow through the load resistor. If too much current flows through the load resistor, the FET is biased (by U401) to a larger resistance. If too little current flows through the load, the FET is biased to a smaller resistance.

7-213. Current Source Circuitry

7-214. The following paragraphs explain the different circuitry of the current source. Refer to Schematic C4.

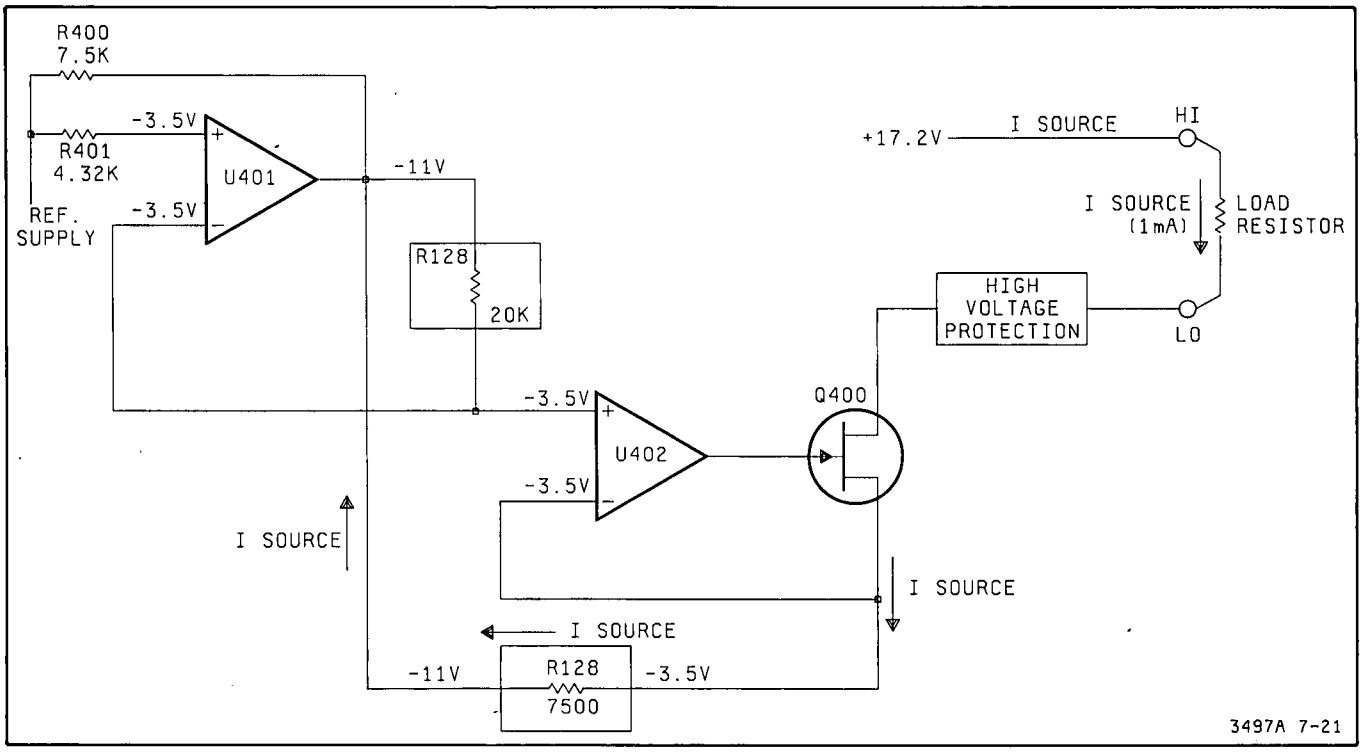


Figure 7-21. Simplified Current Source

7-215. Reference. The reference circuitry consists of Q401 and associated circuitry. The -11V output is developed by the 20K ohm feedback resistor (in R128) and also by the -3.5V applied to the positive terminal of U401. The -3.5V is developed by breakdown diodes CR400 and CR401, resistors R400 and R401, and the +17.2V supply.

7-216. Gate Bias Amplifier. The gate bias amplifier, consisting of U402, is used to bias FET Q400. If current going through the load resistor (current Is, see paragraph 7-211) is too large, the negative terminal of U402 tries to go more positive. This brings the output of U402 lower which turns Q400 on less (i.e., Q400 has more resistance). If the current is too small, the output goes higher and turns Q400 on more (Q400 has less resistance). Another part of the gate bias amplifier circuitry is FET Q401. The FET is configured as a diode and provides a feedback path for U402 when no load resistor is connected to the HI and LO Output Terminals.

7-217. Feedback Resistors. The feedback resistors are located in R128 and are used to configure the current source to output either 1mA, 100μA, or 10μA. The 7501.5 ohm resistor is used to develop a current of 1mA. The 7501.5 ohm resistor in series with the 67499.5 ohm resistor develop 100μA and the 675.203K ohm resistor in series with the 7501.5 ohm and 67499.5 ohm resistors develop 10μA. Each current range can be calibrated using potentiometers R409, R410, and R411 for the 10μA, 100μA, and 1mA Ranges, respectively. The different feedback resistor combinations are selected by relays K401, K402, and K403. The relays are selected by decoder U400 which gets its information from the inguard processor using the BCS and CCS lines. The high and low states of the lines and corresponding current ranges are as follows:

BCS	CCS	Range	Relay On
High	High	None	None
Low	Low	10μA	K401
Low	High	100μA	K402
High	Low	1mA	K403

7-218. High Voltage Protection. The purpose of the high voltage protection circuitry is to protect the current source from voltages inadvertently applied to the HI and LO Output Terminals. If voltages above ±400V are applied to the terminals, gas discharge tube E400 will conduct. This in effect places resistor R414 across the terminals and prevents the voltage from reaching the current source. For voltages below ±400V, transistors Q403 and Q404, and diodes CR402 and CR406 are used to protect the current source. If a negative voltage is applied to the output terminals, diode CR402 becomes back biased and prevents the voltage from reaching the current source. If a negative voltage is applied, CR406 becomes forward biased and applies -.6V across the base-emitter junction of Q403. This turns Q404 off and the applied high voltage is dropped across the emitter-collector junction of Q404.

7-219. Floating Power Supply. The current source uses a floating power supply to isolate the current source circuitry from the rest of the 3497A. The power supply provides two voltages, +17.2V and -17.2V, which are used as a reference supply and the power supplies for the active components in the circuitry. The generation of the two power supply voltages is explained as follows:

a. The ALE clock signal from the inguard logic is applied to counter U300. The counter is used to divide the frequency of the ALE clock down by 10.

b. The output of the counter is applied to the comparators in U301. The comparators are used to develop two signals which are 180 degrees out of phase with each other.

c. One of the output signals from U301 is applied to transistor Q300 and the other is applied to Q301. The transistors are used to drive the primary of transformer T300. Transformer T300 is referenced to the RELAY GROUND (R) (i.e., center tap of T300 is connected to ground R). This ground is connected through the power supply board to LOGIC GROUND (i.e., inguard ground).

d. Transformer T300 is used to drive T301. The output from the secondary of T301 is then used to develop the ±17.2V power supply voltages. Since the secondary of T301 is referenced to ground F instead of the RELAY GROUND and since it is isolated from the primary of T301, the ±17.2V power supplies are isolated from inguard ground.

e. The output of T301 is rectified by full wave rectifier CR302 through CR305 to develop the raw unregulated voltages for the power supplies. The regulated voltages are then developed by transistor Q302 and breakdown diode CR311 for the +17.2V supply and by Q307 and CR310 for the -17.2V supply.

7-220. Another circuit in the current source is varistor RV1. Its purpose is to limit the voltage across the current source ground (ground F) and RELAY GROUND. The varistor is normally open but will be resistive and decrease its resistance value if too much voltage is across the grounds.

7-221. POWER SUPPLIES

7-222. The 3497A's power supplies are separated into two major sections: outguard power supply and inguard power supply. All supplies are located on the power supply board which is located behind the front panel assembly. The outguard power supplies are referenced to chassis ground and the inguard supplies are referenced to inguard ground (LOGIC GND and RELAY GND). This isolates (i.e., floats) the inguard and outguard power supplies from each other. The following paragraphs describe the circuitry.

7-223. Outguard Power Supplies

7-224. The outguard power supply consists of the following circuitry.

+12V Outguard Ref
-12V Outguard
+5V O.G. (Outguard)
Battery Supply

Refer to Schematic D2 for the power supply circuitry explanation in the following paragraphs.

7-225. ±12V Outguard Power Supplies. These supplies are raw unregulated supplies which are developed by full wave bridge rectifier consisting of CR9, CR10, CR13, and CR14. Temperature sensitive resistors RT49 and RT80 are used to protect the supplies from excessive currents. The operation is as follows:

a. If the current of the +12V power supplies is excessive and/or the current of the -12V supply is excessive, RT49 and RT80 heat up, respectively.

b. Since RT49 and RT80 have positive temperature coefficients, their resistance increases to a large value, due to high temperature.

c. The high resistance causes most of the power supply voltage to drop across RT49 or RT80, shutting down the respective supply.

d. The large resistance value remains until RT49 or RT80 cool down (i.e., the supply draws normal current).

7-226. +5V O.G. Power Supply. This supply is used by most of the logic circuitry in the outguard section of the 3497A. It consists of a series regulator (transistor Q1), full-wave rectifier (CR1 and CR2), reference circuitry (U1 and associated circuitry), and protection circuitry (U2A and associated circuitry). The following explains the circuitry operation.

a. Full-wave rectifier CR1 and CR2 in conjunction with filter capacitor C3 develop the raw unregulated voltage for the power supply.

b. The raw voltage is then divided down and regulated to +5V by Q1. The difference between +5V and the raw voltage is dropped across Q1. If more current is needed by the circuitry, Q1 turns on harder. If less current is needed, Q1 turns on less. This is accomplished by controlling the voltage at the base of Q1.

c. Transistor Q1 is regulated by U1 and associated circuitry. In U1 is an operational amplifier and a reference diode (i.e., a breakdown diode). The operation is as follows:

1. The positive terminal of the operational amplifier in U1 is held at approximately +5V and, since the negative terminal is connected to the +5V supply, both terminals are at approximately +5V. The voltage on the negative terminal is developed by the breakdown diode in U1 using R28 and R29. The diode is at approximately +7V which is divided down to approximately +5V by R28 and R29. The diode is supplied by the current source in U1 which receives its voltage from the +12V supply.

2. With both terminals of the amplifier in U1 at +5V, transistor Q1 is biased to output +5V.

3. If the +5V supply changes to a lower value, the negative terminal of the amplifier in U1 goes lower which makes its output go higher. This turns the transistor in U1 on a little less (i.e., collector goes higher) which turns Q7 on a little less. The collector of Q7 then goes higher which then turns Q1 on harder until the power supply is at +5V.

4. If the +5V supply changes to a higher value, the negative terminal of the amplifier in U1 goes higher which makes its output go lower. This turns the transistor in U1 on a little harder (i.e., collector goes lower) which turns Q7 on harder. The collector of Q7 then goes lower which then turns Q1 on less until the power supply is at +5V.

d. The protection circuitry, consisting of U2A and associated circuitry, is used to turn the power supply off if excessive current is drawn. When the power supply draws excessive current, a voltage drop across R23 is developed that makes the positive terminal of U2A lower than the negative terminal. The output of U2A goes low and, since it is connected to the base of the transistor in U1, the collector of the transistor goes low. This turns Q7 on harder which turns off Q1.

7-227. Battery Supply. The battery supply consists of a battery, battery regulator circuitry, and battery charging circuitry. The battery (BT1) is used to back up the 3497A's internal clock (only the date and time, no other clock related functions) when power to the instrument fails. The battery regulator circuitry (U11 and associated circuitry) serves two functions, it regulates the battery voltage going to the internal clock and protects the battery from shorts. The battery charging circuitry (U2B and associated circuitry) charges and keeps the battery charged when the 3497A is turned on and power is connected. The circuitry has two charging states, a fast charge and a trickle charge. The fast charge is selected when the battery needs charging and the trickle charge is selected to keep the battery charged. The following explains battery supply circuitry operation.

a. When power is connected to the 3497A and the instrument is on, the voltage for the internal clock comes from Q6. Transistor Q6 is a series regulator which outputs approximately +6V. This is developed since breakdown diode CR8 is connected to the base of Q6

making the emitter of Q6 approximately +6V. The +6V from Q6 goes through CR7 which then becomes the supply voltage for the clock. The raw power supply voltage for Q6 is the +12V OUTGUARD REF supply.

b. When power is removed from the 3497A, the battery then supplies the voltage to the clock. Dependent on the position of jumper J7, the voltage is supplied under two different conditions: when the power switch is either on or off, or only when the switch is on. With P7 in the ON position, backup voltage is supplied when the power switch is on or off.

c. The battery regulator circuitry is used to regulate the battery voltage when the battery supplies the backup voltage to the clock. The operation is as follows:

1. The positive terminal of U11A is at approximately +2V. This is developed using CR6 and resistors R50 and R51. The negative terminal of U11A is also at approximately at +2V which comes from the battery voltage and R15, R16, and transistor Q5. The transistor voltage depends on the bias voltage from U11B.

2. If the battery supply voltage changes to a lower value, the negative terminal of U11A goes lower which makes its output go higher. This turns transistor Q4 on a little harder. The collector of Q4 goes lower which turns on Q3 a little harder until the battery supply voltage is at the correct value (+6V).

3. If the battery supply voltage changes to a higher value, the negative terminal of U11A goes higher which makes its output go lower. This turns transistor Q4 on a little less. The collector of Q4 goes higher which turns on Q3 a little less until the battery supply voltage is at the correct value (+6V).

d. The battery regulator circuitry protects the battery from shorts that may be applied to the battery supply. This is accomplished by turning Q3 off. If a short occurs, the voltage at the positive pin of U11B goes to zero. This brings the output of U11B low and turns Q5 off. The collector of Q6 then goes high. Since the collector of Q5 is connected through R16 to the negative terminal of U11A, the output of U11A goes low and turns Q3 off.

e. The battery charging circuitry charges and keeps the battery charged when the instrument is on and power is applied. This is accomplished by U2B and associated circuitry. The positive terminal of U2B is at the +5V power supply voltage. When the battery voltage is lower than normal, indicating a discharge condition, the negative terminal of U2B goes low. The voltage at the negative terminal of U2B is determined by the battery voltage using R7, R10, R11 and associated circuitry. With the negative terminal of U2B low, the output of U2B goes high which turns Q2 on. The collector of Q2 goes lower and turns Q1 on which charges the battery. The amount of charge is determined by the voltage at the base of Q1. This voltage is developed by LED CR1 and the +12V OUTGUARD REF supply which prevents Q1 from charging the battery too much. When the battery is charged up, the battery remains charged by a trickle charge developed by R1 and R2.

7-228. Inguard Power Supplies

7-229. Most of the inguard power supplies are similar to each other in that they use voltage regulators to develop the power supply voltages. The only exception is the +30VL supply which is a raw unregulated supply. In addition to the power supplies, the circuitry also includes a -8V power supply (-8 T.C.) which is used by the thermocouple on the 20 Channel Relay Multiplexer with Thermocouple Compensation plug-in option (Option 020). All the power supplies, except the +19VG and -19VG supplies, are referenced to inguard ground. The +19VG and -19VG supplies are referenced to guard. The following explains the power supply circuitry. Refer to Schematic D3 for the explanation.

7-230. +15VL, -15VL Power Supplies. These power supplies use a full-wave bridge rectifier, consisting of CR19, CR20, CR24, and CR25, to develop the raw unregulated voltages. The +15VL is developed by regulator U3 and the -15VL by U4. Capacitors C16, C19, C17, C20, C21, and C22 are used as filter capacitors. Breakdown diodes CR22 and CR29 are used for overvoltage protection.

7-231. -18VL Reg. Supply. This supply uses regulator U8 to develop -18 volts. Although the regulator is a -15V regulator, it develops -18V since its pin 1 is at 3V which is developed by CR31 (-15V plus -3V is equal to -18V). Overvoltage protection of the supply is by CR60. Capacitors C24 and C25 are used as filters. The raw unregulated voltage for the supply comes from rectifiers CR19, CR20, CR24, and CR25 using a voltage doubler (C18, CR27 and CR59, and CR28).

7-232. +30VL Supply. This supply is an unregulated supply which uses rectifiers CR19, CR20, CR24, and CR25, and a voltage doubler (C13, CR18, and CR17) to develop the voltage. Overvoltage protection is by CR23 and C23 is used as a filter capacitor.

7-233. +5 LOGIC Supply. This supply uses regulator U12 and a bridge rectifier, consisting of CR46 to CR49, to develop the supply voltage. Capacitors C29 to C31 are filter capacitors and CR35 is for overvoltage protection.

7-234. +19VG and -19VG Supplies. These supplies use a bridge rectifier, consisting of CR36, CR37, CR41, and CR42, to develop the raw unregulated voltage for the supplies. The +19VG supply uses a regulator U9 and the -19VG supply uses U10. Regulator U10 is a -15V regulator which has its pin 1 at approximately -4V (using CR44) thereby developing -19V. Capacitors CR34 to CR39 are

used as filter capacitors and CR55, CR56, and CR45 are for overvoltage protection.

7-235. T.C. Power Supply. The T.C. power supply, consisting of U7, Q8, and associated circuitry, is used to develop -8V for the Option 020 plug-in card. The positive input of U7, which is configured as an inverting amplifier, is at approximately -2V. The -2V is developed by the -15V INGUARD supply (-15VL) and breakdown diode CR33 which also determines the stability of the amplifier. A -2V on the positive terminal makes the negative terminal also at -2V. Appropriate values of feedback resistors (R33 through R39) are chosen to make the output of the power supply -8V and to make the negative terminal of U7 -2V. Feedback resistors R34 to R37 are selected by jumpers JM7 to JM10. The jumpers select the appropriate resistor values to make the output as close to -8V as possible. Then R46 is adjusted to output exactly -8V. Transistor Q8 is configured as an emitter follower and is used as a buffer.

SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section of the manual shows how to troubleshoot and repair the 3497A mainframes (both HP-IB and Serial I/O), standard front panel, and voltmeter option. The information is given in service groups which include procedures on how to select the appropriate service group. This section of the manual also has the complete schematics (in Service Group E) for the mainframes, the standard front panel, and the voltmeter option. This section also includes the necessary safety considerations. The section is separated as follows:

Safety Considerations - paragraph 8-3
Fuse Replacement - paragraph 8-8
Printed Circuit Board Removal and Installation - paragraph 8-14
Pre-Troubleshooting Information - paragraph 8-26
Troubleshooting - paragraph 8-28
3497A Failures and Service Group Selection - paragraph 8-36

8-3. SAFETY CONSIDERATIONS

8-4. The 3497A has been designed with international safety standards. To maintain these standards, the cautions, warnings, and other safety related information in this manual must be followed when servicing the instrument. Servicing should only be performed by service trained personnel.

8-5. Service and repair of the 3497A while covers and/or printed circuit boards are removed and with any power applied, should be avoided as much as possible. If any work is performed while power and/or voltage is applied, the work should be carried out by a skilled person who is aware of the hazards involved.

8-6. It is possible for capacitors inside the instrument to remain charged when the instrument has been turned off or its power source removed. Make sure the capacitors are discharged before working on the instrument.

8-7. Make sure that only the recommended fuse type (correct current rating, etc.) is used for replacement. The use of repaired fuses and the shorting of fuse holders must be avoided.

WARNING

Only service trained personnel with a knowledge of electronic circuitry should install, reconfigure, or make repairs to this instrument or assembly.

WARNING

Voltages as high as 357V may be present within the protective safety covers and cabinet enclosures of the 3497A. These voltages may be accessible on exposed chassis parts once the safety cover has been removed. LETHAL voltages may be present even though the instrument is disconnected from LINE power. BEFORE any handling or servicing of plug-in options cards takes place, make certain that all sources of external power are either turned off or disconnected.

WARNING

Any interruption of the protective grounding conductor (inside or outside the instrument) or disconnections of the protective earth terminal can make the instrument dangerous. Intentional interruption of the protective grounding conductor is strictly prohibited.

8-8. FUSE REPLACEMENT

8-9. The 3497A mainframe has two fuses, a main ac power fuse and a battery fuse. The power fuse is located at the outguard section's rear panel and the battery fuse is inside the mainframe. The removal procedures for the fuses are in the following paragraphs.

8-10. Power Fuse Replacement

8-11. The fuse is replaced at the fuse holder located on the right rear panel of the instrument (as viewed from the back). To remove the fuse, insert the blade of a small flat blade screwdriver into the slot of the fuse holder cap. Push the cap in and then turn the screwdriver counterclockwise. The cap will then pop out and can then be removed with the fuse. Replace the fuse with a new one and do the procedure in reverse to replace the cap.

8-12. Battery Fuse Replacement

8-13. The battery fuse is inside the mainframe. To replace the fuse, do the following:

a. Turn the 3497A off and remove ac power from the instrument.

b. Turn the 3497A upside down and remove the bottom cover.

c. The fuse is mounted in a fuse clip which is located near the power transformer (right side).

d. Pop the fuse out of the clip and replace it with a new one.

e. Reinstall the bottom cover and turn the instrument rightside up.

8-14. PRINTED CIRCUIT BOARD REMOVAL AND INSTALLATION

8-15. The following paragraphs have procedures to remove printed circuit boards for servicing. The procedures include the removal and installation of the outguard logic board, inguard controller board, and voltmeter option board. These boards may have to be removed for most troubleshooting. Other procedures are for the front panel and power supply boards. These may not have to be removed for troubleshooting purposes, but must be removed to replace any components on the boards. The board removal and installation procedures are in the following paragraphs.

b. Remove the rear panel safety cover by removing the two screws that hold it in place. Then remove the rear cover bracket by removing the screws that hold the bracket in place.

c. Refer to Figure 8-1. Note that the outguard logic board and the inguard controller board are held in by one and two mounting screws, respectively. Determine which board is to be removed and locate the appropriate screws. Loosen the screws, but do not remove them. They are held in place by a rubber grommet.

d. Dependent on which board (inguard or outguard) is to be removed, locate the appropriate built-in finger ring, as shown in Figure 8-1. Pull on the ring to remove the board from the 3497A chassis.

e. Once the board is removed, it can be reconnected to the mainframe for servicing. This is accomplished by using the Board Extender (-hp- Part No. 03497-67913). The following steps explain how to connect the outguard logic board to the extender and then how to plug the extender into the instrument. This is shown in Figure 8-2. In the figure, the outguard board is used as an example on how to connect the board and extender. The same applies for the inguard controller board and plug-in options. Do the following:

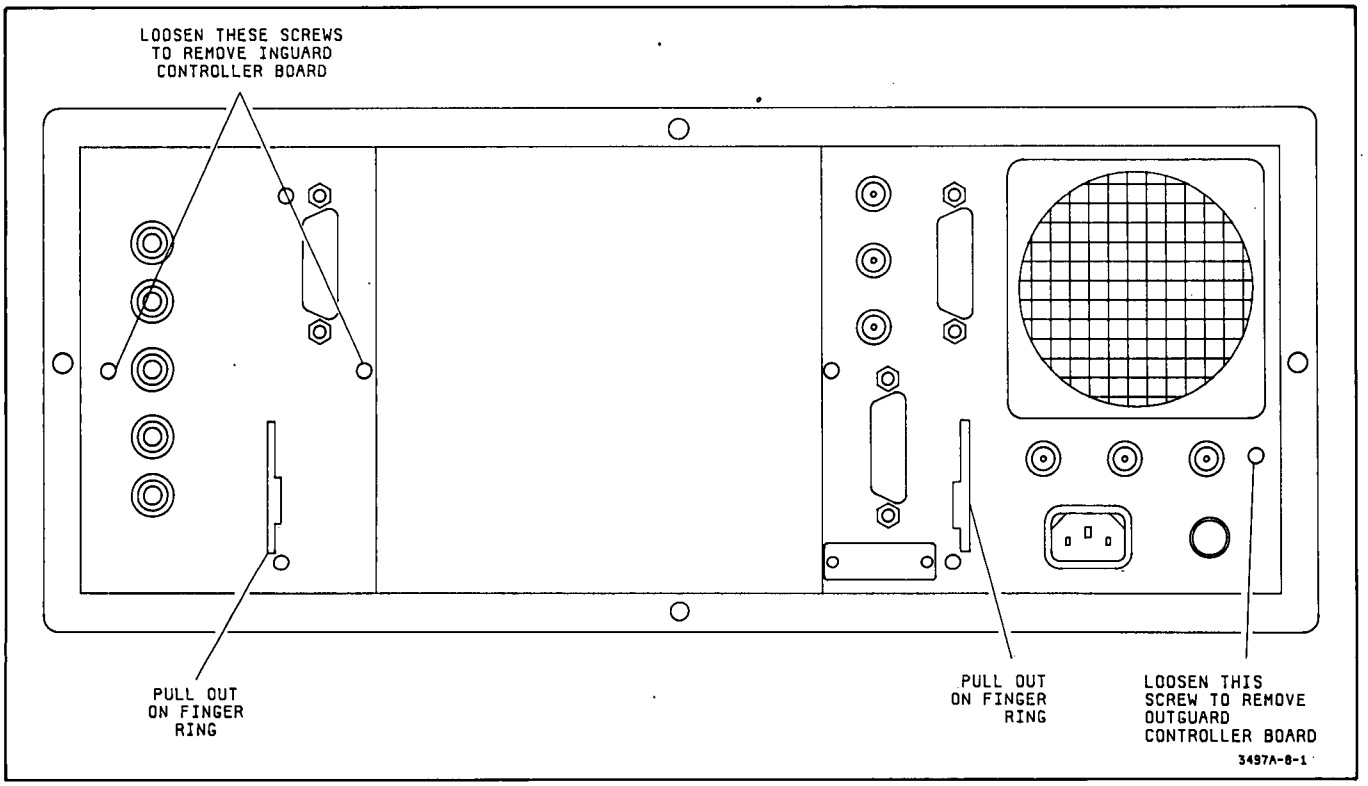


Figure 8-1. Outguard and Inguard Boards Mounting Screws and Finger Rings

8-16. Removing the Outguard Logic And Inguard Controller Boards

8-17. Do the following procedures.

a. Turn the 3497A off and remove the power line cable from the instrument.

1. Refer to Figure 8-2. Locate the arrow marked "CONTROLLER TIMER" on the 3497A mainframe and align the Board Extender into the corresponding slot. Then push the extender into the slot

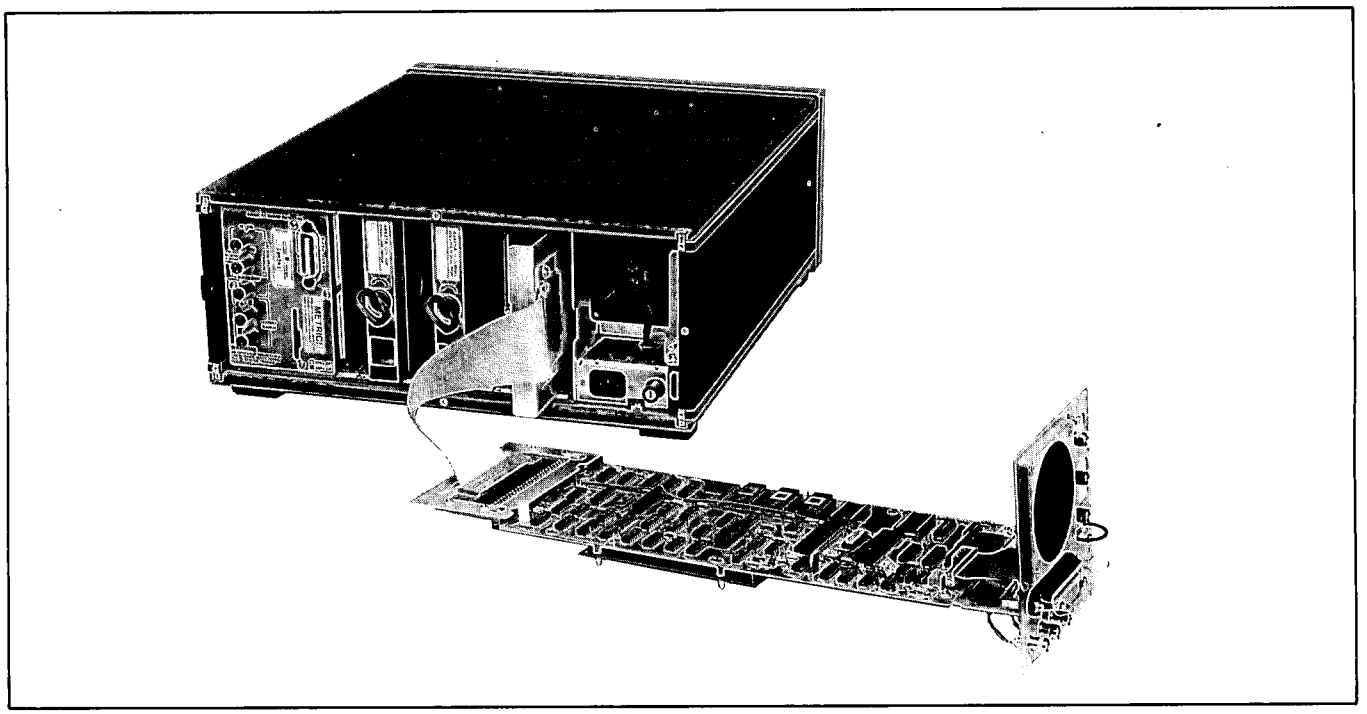


Figure 8-2. Using the Board Extender

until it seats firmly in the motherboard socket. If the inguard controller board is to be installed, align the extender with the "INGUARD CONTROLLER" arrow.

2. Plug the cable from the Board Extender into the outguard logic or inguard controller board edge connector. Troubleshooting can now be performed on the board.

3. To reinstall the boards, after servicing, go to the next paragraph.

8-18. Installing the Outguard Logic and Inguard Controller Boards

8-19. Do the following:

a. Make sure the 3497A is turned off and the power line cable is disconnected from the instrument.

b. Unplug the outguard logic or inguard controller board from the Board Extender. Then remove the Board Extender from the mainframe.

c. If the outguard logic board is to be installed, locate the arrow marked "CONTROLLER TIMER" on the 3497A mainframe. If the inguard controller board is to be installed, locate the arrow marked "INGUARD CONTROLLER" on the 3497A mainframe. Align the board into the corresponding slot. Then push the board into the slot until it seats firmly in the motherboard socket.

d. Locate the appropriate mounting screws on the rear panel, shown in Figure 8-1, and tighten the screws.

e. Reinstall the rear panel safety cover.

8-20. Removing the Voltmeter Option Board

8-21. Since the voltmeter option board is part of the inguard assembly, the inguard controller board must be removed before the voltmeter board can be removed. Do the procedure in paragraph 8-16 to remove the inguard controller. Then do the following:

a. Make sure the inguard controller board is removed from the 3497A.

b. Make sure the 3497A is turned off and the power line cable is disconnected from the instrument.

c. On the inguard assembly, locate the voltmeter board. The board is covered with a metal shield which has to be removed before troubleshooting or service can be performed. Remove the four machine bolts located near the corners of the shield and then remove the shield.

d. With the shield removed, the board is exposed enough to troubleshoot it. If further removal is necessary, continue with the next step.

e. Locate the red and black wires connected to the HI and LO Input terminals. Unplug the wires from the voltmeter board.

f. Locate the red and black wires connected to the inguard controller board and unplug these wires from the board.

g. Locate the voltmeter mounting screw near the center of the board and remove it. The voltmeter board can now be removed.

h. To reinstall the board, do the removal procedure in reverse.

8-22. Removing the Front Panel Board

8-23. The front panel board does not have to be removed to troubleshoot it, but has to be removed to replace components. The following procedure shows how to get to the front panel board and how to remove it. Do the following:

a. Turn the 3497A off and remove the power line cable from the instrument.

b. Open the front panel by unscrewing the captive fastener counterclockwise until it is free. Then swing the front panel out until it is perpendicular with the frame. The front panel board is now exposed enough to troubleshoot it. If the board is to be removed, continue with the next step.

c. To remove the board, make sure the 3497A is turned off and the power line cable is disconnected from the instrument.

d. Locate the four mounting screws on the front panel board and remove them. Two of the screws are located near the lower corners of the board.

e. Locate the ribbon cable which connects the front panel board to the mother board. Unplug the cable at the mother board. Then remove the board by pulling the bottom part of the board away and downward from the front panel assembly.

f. To reinstall the board, do the removal procedure in reverse.

8-24. Removing the Power Supply Board

8-25. The power supply board does not have to be removed to troubleshoot it, but has to be removed to replace components. However, since a metal shield covers the board, the shield must be removed to troubleshoot the board. The following procedure shows how to remove the shield and the board.

a. Turn the 3497A off and remove the power line cable from the instrument.

b. Open the front panel by unscrewing the captive fastener counterclockwise until it is free. Then swing the front panel out until it is perpendicular with the frame.

c. The power supply board is located in front of the mainframe. At this time, the board is covered with a metal shield. Remove the two screws that hold the shield in place and then remove the shield.

d. The power supply board should now be exposed enough to troubleshoot it. If the board is to be removed, continue with the next step.

e. To remove the board, make sure the 3497A is turned off and the power line cable is disconnected from the instrument.

f. Unplug the two cables connected to the power supply board.

g. Locate the four board mounting screws and remove them. Two screws are on the power supply board itself and the other two are near the power transistor located at the top right of the board.

h. The board can now be removed by pulling it outward away from the mainframe.

i. To reinstall the board, do the removal procedure in reverse.

8-26. PRE-TROUBLESHOOTING INFORMATION

8-27. Check the following before troubleshooting the 3497A.

a. Make sure the outguard logic board and inguard controller board are seated firmly into their respective sockets. Also make sure the boards and motherboard connectors are clean.

b. Make sure the failure is not caused by a plug-in option or the 3498A Extender (if connected to the instrument). Remove all of the plug-in options and the extender, and then perform a self-test (see paragraph 8-31). The test is enabled by pressing the SELF-TEST button on the front panel (if the standard front panel is installed) or sending program codes "ST1" over the HP-IB or Serial I/O bus. If the test passes, the 3497A is most likely good and a plug-in option may cause the failure. If the test fails, the 3497A is at fault.

c. Make sure no other external devices connected to the 3497A cause the failure.

8-28. TROUBLESHOOTING

8-29. The following paragraphs have information on the 3497A's self-test feature and some general troubleshooting information for the 3497A mainframes, standard front panel, and voltmeter option. For more complete troubleshooting information, go to the appropriate service group. Go to paragraph 8-37 to select the appropriate group.

8-30. Self-Test

8-31. The 3497A uses an internal self-test to check its operating circuitry. This test can be selected from the front panel (if the standard front panel is installed), or over the HP-IB or Serial I/O bus. Press the SELF-TEST button on the front panel, or send program codes "ST1" over the HP-IB or Serial I/O, to select the test. If the test passes, all the front panel LEDs (and 8E8 is output over the HP-IB or Serial I/O bus) will turn on indicating that the circuitry checked by the test is functional. In addition, 8E8 is also output over the HP-IB or Serial I/O bus, if read over the bus. If the test fails, a number showing which of the 3497A circuitry that has failed will then be displayed. Since a self-test is also performed at turn on, the failure will also be shown on the front panel when the 3497A is turned on. The following paragraphs give the test numbers and circuitry that could cause the failure.

8-32. Test #1. This test fails if "1" is displayed on the front panel or "10" is output over the HP-IB or Serial I/O bus. This shows that communication between the outguard controller and the inguard controller is broken. The cause can be either the inguard or outguard controller circuitry, or the crossguard circuitry. Go to Service Group A1 or A2 to determine the inoperative circuitry. Service Group A1 is for the standard (HP-IB) mainframe and Service Group A2 is for the Serial I/O mainframe (Option RS-232).

8-33. Test #2. This test fails if "2" is displayed on the front panel or "200" is output over the HP-IB or Serial I/O bus. It shows that the voltmeter operation is inoperative. The cause can be either the inguard controller circuitry, A/D logic, or A/D converter. Go to Service Group B for troubleshooting.

8-34. Test #3. This test fails if "3" is displayed on the front panel or "3000" is output over the HP-IB or Serial I/O bus. This shows that the timer/pacer circuitry is inoperative. Since this circuitry is part of the outguard logic circuitry, go to Service Group A1 or A2 for troubleshooting. Service Group A1 is for the standard (HP-IB) mainframe and Service Group A2 is for the Serial I/O mainframe (Option RS-232).

8-35. Board Swapping

8-36. Isolating defective circuits or printed circuit board is best done by exchanging the suspected defective board with a known good board. One thing that needs to be remembered is that the Serial I/O controller board may not operate on older instruments. Make sure the 3497A has operated with the option in the past, before attempting to swap boards.

8-37. 3497A FAILURES AND SERVICE GROUP SELECTION

8-38. 3497A failures are in the following paragraphs. Use the information to determine the 3497A failure. Once the failure is determined, go to the appropriate service group for troubleshooting. The service groups are given in the following paragraphs and also in Table 8-1.

Table 8-1. 3497A Service Groups

Service Group	Title
A1	Outguard Troubleshooting (HP-IB)
A2	Outguard Troubleshooting (Serial I/O)
B	Inguard Logic and A/D Converter Troubleshooting
C	DC Voltmeter and DC Current Source Troubleshooting
D	Miscellaneous Troubleshooting
E	Block Diagrams and Schematics

8-39. Outguard Logic Failures (Service Group A1 or A2)

8-40. These include failures by the outguard controller and timer/pacer circuitry. The failures are as follows:

8-41. Turn-On Failure. This failure is when the 3497A mainframe is completely inoperative. No control using the front panel, and also using the HP-IB or Serial I/O bus is possible. If this failure occurs, the front panel display may be completely blank, or may not show some or only part numbers. If a number is displayed, it would normally be other than a number 1, 2, or 3. A number 1, 2, or 3 indicates a self-test failure. If a turn-on failure is noted, go to Service Group A1 for the standard (HP-IB) mainframe or Service Group A2 for the Serial I/O mainframe.

8-42. Inoperative Keyboard (Standard Front Panel Installed). An inoperative keyboard is when all or part of the keyboard is inoperative. This shows up when pressing a key and no action or an incorrect action takes place. It can be caused by the keyboard circuitry itself or the outguard controller. With a keyboard failure, the HP-IB or Serial I/O bus should still operate. An inoperative keyboard may also, under certain cicumstances, show a display failure. If the keyboard, display, and HP-IB or Serial I/O bus are all inoperative, the failure is most likely a turn-on failure (see paragraph 8-41) instead of a keyboard failure. To troubleshoot the keyboard, go to Service Group A1 for the standard (HP-IB) mainframe or Service Group A2 for the Serial I/O mainframe.

8-43. Inoperative Display and/or Inoperative Beeper (Standard Front Panel Installed). This shows up when all the displays are blank, when they show incorrect information (e.g., segments on the LEDs are missing or wrong), or when the beeper is inoperative. If a 1, 2, or 3 is displayed, it is most likely a self-test failure, not a display failure. The display failure can be caused by the display circuitry itself or the outguard controller. If the display, keyboard, and HP-IB or Serial I/O bus are all inoperative, the failure is most likely a turn-on failure (see paragraph 8-41) instead of a display failure. To troubleshoot the display, go to Service Group A1 for the standard (HP-IB) mainframe or Service Group A2 for the Serial I/O mainframe.

8-44. HP-IB or Serial I/O Failure. This failure is when the 3497A cannot be controlled over the HP-IB or the Serial I/O bus. If the keyboard and the display are also inoperative, the failure is a turn-on failure (see paragraph 8-41) instead of an HP-IB or Serial I/O failure. If there is an HP-IB failure, go to Service Group A1 and if there is an Serial I/O failure, go to Service Group A2.

8-45. Timer/Pacer Failure. A timer/pacer failure is when all or part of the circuitry is inoperative. This includes the time of day functions and the output signals at the rear panel ports. The timer/pacer failures normally show up as Self-Test #3 failure (see 8-34). If a timer/pacer failure is noted, go to Service Group A1 for the standard (HP-IB) mainframe or Service Group A2 for the Serial I/O mainframe.

8-46. Input and Output Ports Failures. Most of the 3497A's input and output ports send and receive information from and to the outguard logic. Other ports are used to send out information from the timer/pacer circuitry. If any of the ports are inoperative, go to Service Group A1 for the standard (HP-IB) mainframe or Service Group A2 for the Serial I/O mainframe.

8-47. Failures with 3498A Extender Connected. If any failures show up only when the 3498A Extender is connected to the 3497A, make sure the 3498A is not causing the failure. If the 3498A is good, the 3497A is most likely at fault. Go to Service Group A1 for the standard (HP-IB) mainframe or Service Group A2 for the Serial I/O mainframe.

8-48. Inguard Logic Failures (Service Group B)

8-49. The inguard logic failures are explained in the following paragraphs.

8-50. Voltmeter Failures. These failures include overload, constant zero, etc., readings. For a description of these failures, see paragraph 8-54. If a voltmeter failure is noted, make sure the failure is not caused by the voltmeter circuitry instead of the inguard logic. A procedure to determine which circuitry is at fault is in Service Group C. Once it is determined that the inguard circuitry and not the voltmeter is at fault, go to Service Group B for troubleshooting.

8-51. Analog Plug-In Options Failure. This failure is present when the analog plug-in options receive the wrong set-up information. The failure can be caused by the inguard controller and associated circuitry, or by the option itself. Make sure the option is good, before troubleshooting the inguard circuitry. If the inguard circuitry is causing the failure, go to Service Group B for troubleshooting.

8-52. Failures with 3498A Extender Connected. This failure is when the analog plug-in options in the 3498A receive the wrong set-up information. If any failures show up with the 3498A Extender connected to the 3497A, make sure the 3498A is not causing the failure. If the 3498A is good, the inguard controller circuitry is most likely at fault. Go to Service Group B for troubleshooting.

8-53. The 3497A Displays Dashes (-------). This is a normal display when the voltmeter option is not installed. If this is displayed when the option is installed, it shows that communication between the option and the inguard logic is broken. The most likely cause is the A/D logic circuitry. Go to Service Group B for troubleshooting.

8-54. DC Voltmeter Failures (Service Group C)

8-55. The following paragraphs explain possible voltmeter failures. If any of these failures are noted, go to Service Group C for troubleshooting.

8-56. Overload. There are two types of overload conditions that can occur. One type is when the input voltage applied to the dc voltmeter is larger than the particular range can handle. This type is normal. For example, if 15V is applied on the 10V Range, the 3497A will display an overload ("OL"). The other type of failure is when an overload is displayed with no voltage applied and/or the input terminals are shorted. This type can be caused by the input switching circuitry, input amplifier, or A/D converter (including the inguard logic). (Note: An overload may be displayed on the lowest voltmeter ranges with the input terminals open. This is a normal condition,)

8-57. Inaccurate Readings. Inaccurate readings are measurements that are not within the voltmeter option's DC Voltage specifications. These can be caused if the option is out of calibration, or by the input switching, input amplifier, or A/D converter circuitry. Before doing any troubleshooting, calibrate the instrument.

8-58. Floating Readings. A floating reading is a reading that does not change irrespective of the input voltage applied. Generally, the displayed reading will appear to be totally random. This can be caused by an open in the voltmeter circuitry.

8-59. Constant Zero Reading. A constant zero reading is normally caused when the input to the input amplifier or the A/D converter is shorted to ground (LO COM). It can also be caused if the A/D converter is inoperative.

8-60. Noisy Readings. This failure can be caused by the input switching, input amplifier, or A/D converter.

8-61. Current Source Failures (Service Group C)

8-62. The following paragraphs explain possible current source failures. If any of these failures are noted, go to Service Group C for troubleshooting.

8-63. Inaccurate Current. Inaccurate currents are currents that are not within the voltmeter option's DC Current Source specifications. These can be caused if the cur-

rent source is out of calibration, or by the circuitry in the current. Before doing any troubleshooting, calibrate the instrument.

8-64. No Current Output. This failure is when the current source outputs no current and is normally caused by the circuitry in the current source.

8-65. Noisy Currents. This failure is when the current source outputs currents that deviate more than the short term specifications of the current source. The failure is normally caused by the circuitry in the current source.

8-66. Miscellaneous Failures (Service Group D)

8-67. These failures include the following:

Outguard Power Supplies Failures
Inguard Power Supplies Failures
Voltmeter Reference Supplies Failures
Battery Charger Failures

If any of these failures are noted, go to Service Group D for troubleshooting.

8-A1-1. INTRODUCTION

8-A1-2. This service group has troubleshooting information for the outguard logic of the 3497A's standard (HP-IB) mainframe (see Service Group A2 for the Serial I/O mainframe troubleshooting). The information is for all of the outguard circuitry which consists of the main controller circuitry, HP-IB circuitry, timer/pacer circuitry, crossguard logic, standard front panel, and associated circuitry.

8-A1-3. PRE-TROUBLESHOOTING INFORMATION

8-A1-4. Read the information in the following paragraphs before doing any troubleshooting.

8-A1-5. Troubleshooting Without Signature Analysis

8-A1-6. Check for stuck nodes on the address bus, data bus, and the outputs of devices used by the outguard. This can be done using a logic probe. A stuck node usually shows the node in a certain steady state when it is supposed to toggle. Try to determine what the 3497A is suppose to be doing and what it is not doing, or vice versa, and then try to logically associate that to a particular circuit. The theory of operation may be helpful to determine the defective circuitry. Then check for the outputs of a device in that circuit to see if they are toggling. If they are not, check the inputs of the device for toggling. If the inputs are toggling, the device is probably defective. This method of troubleshooting does not check for timing errors, but is fast and simple.

8-A1-7. Troubleshooting With Signature Analysis

8-A1-8. A signature analyzer is used to determine the faulty circuitry and component. This is done by placing the circuitry in a certain operating mode and then take signatures using the signature analyzer. When the circuitry is in that mode, the data on the lines develop a unique signal. This data (i.e., signal) is read by the signature analyzer which then develops a unique signature. If the signature is correct, the device developing the signal is correct. If the signature is incorrect, the device may be defective. Before replacing the device, make sure other devices on the line are not causing the incorrect signature.

8-A1-9. When using the procedures in this service group, make sure the charts and procedures are followed in order. If done otherwise, the procedures may appear to be confusing.

8-A1-10. General Troubleshooting Information

8-A1-11. Check and make sure the +5V power supply is good. This supply should be between +4.75V and +5.25V.

8-A1-12. Make sure the outguard processor's clock is operating correctly. Check and make sure that the clock outputs at pins 13 and 15 of U10 are 180 degrees out of phase (see Schematic A1). If the clock signals are missing, replace U10.

8-A1-13. Make sure the processor is properly reset. This can be done by momentarily shorting the $\overline{\text{RST}}$ line (U11 pin 40) to ground. The line should then go high and reset the processor. If, after shorting the line, the 3497A starts operating or if the line remains low, try replacing U10 or U51.

8-A1-14. EQUIPMENT REQUIRED

8-A1-15. The following is the required equipment for the troubleshooting procedures in the following paragraphs.

Oscilloscope -hp- Model 1741A
Signature Analyzer -hp- Model 5004A
Logic Probe

8-A1-16. OUTGUARD FAILURES AND TROUBLESHOOTING

8-A1-17. The following paragraphs have outguard logic failures and some troubleshooting information. For a description of the outguard failures, refer to paragraphs 8-30 and 8-39.

8-A1-18. Turn-On Failure

8-A1-19. This failure usually shows up as an inoperative instrument (i.e., keyboard, display, HP-IB, etc., are all inoperative). The failure can be caused by the main controller and associated circuitry. To determine if the failure is present, check the following.

a. Make sure the display is inoperative. The display may show some information, other than 1, 2, or 3 which is a self-test failure, and will not do any updating.

b. The keyboard will not operate at all.

c. The HP-IB will not operate at all.

If "all" of the conditions are met, the 3497A will most likely have a turn-on failure.

8-A1-20. To troubleshoot the turn-on failure, the outguard logic is placed into a free-run SA (Signature Analysis) mode. Various signatures are then taken to determine if the outguard processor, ROMs, or other areas in the outguard circuitry are causing the failure.

8-A1-21. In the following procedure, various clock signals are checked and then the address bus is checked using SA. If the address bus is good, the outguard controller is most likely operating. The turn-on failure is then most likely caused by the ROMs and RAMs, or by the front panel circuitry (keyboard and displays) or HP-IB circuitry. If the signatures on the address bus are good, more signatures are then taken to check the output of the peripheral decoders. Do the following:

SERVICE GROUP A1

OUTGUARD TROUBLESHOOTING (HP-IB)

Service Group A1 Contents

a. Turn the 3497A off.

b. Remove the outguard logic board from the instrument.

c. Remove the timer/pacer board from the outguard logic board. The board is removed by removing its mounting screw (near the center of the outguard board) and then unplugging the timer/pacer board from the outguard board.

d. Connect the outguard logic board to a Board Extender and plug the extender into the appropriate slot of the instrument (see paragraph 8-16 on how to connect the extender).

e. Turn the 3497A on.

f. If the standard front panel is installed, look at the front panel display and determine if Test #3 fails. If the optional front panel is installed, continue with step h.

g. If the front panel does not display "3", the turn-on failure is still present. Continue with step h. If the front panel display shows a Test #3 failure (i.e., displays "3"), the 3497A does not have a turn-on failure. This is because a displayed "3" is a normal indication with the timer/pacer board removed. This would show that the outguard logic is operating. Since the original failure shows up with the timer/pacer board connected to the outguard board, the timer/pacer circuitry is most likely causing the failure. Do the following (refer to Schematic A3):

1. Remove RP4. Then plug the timer/pacer board back into the outguard logic board.

2. If the 3497A now displays "3", U8, U9, U11, or U12 are most likely at fault.

3. If the turn-on failure is still present, make sure the TIMER PCTL line is not held low. Replace U3 if it is.

h. Turn the 3497A off.

i. Unplug the front panel board from the mainframe motherboard (see paragraph 8-22).

j. Turn the 3497A on.

k. Check for clock signals at TP Bϕ2 and TP DBE. Use an oscilloscope (the 1741A) to check for the signals shown in Figure 8-A1-1. Use the scope set-up information given in the figure to configure the scope.

l. If the clock signals are missing or wrong, check for a defective U10, U13, and U14. If the clock signals are good, check the address bus using SA (continue with next step).

m. Turn the 3497A off.

n. Remove bus break RP3 from its socket (see Figure 8-A1-2).

o. Using short clip leads, connect test points W11 (data line D5) and W12 (data line D7) to ground, as shown in Figure 8-A1-2. This places the 3497A into the free-run SA mode.

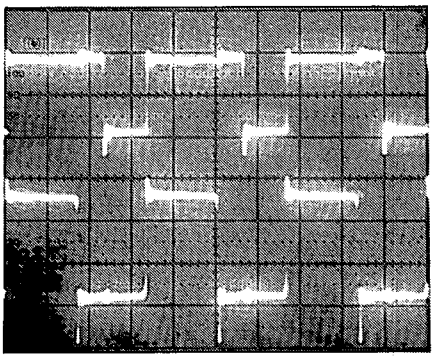


Figure 8-A1-1. Bϕ2 and DBE Clock Signals

p. Obtain a signature analyzer and connect as follows (see Figure 8-A1-2):

Start: TP SS0 (Address A15)
Stop: TP SS0 (Address A15)
Clock: TP Bϕ2
Gnd: TP GND

q. Set the signature analyzer as follows:

Start: In (⎍)
Stop: Out (⎍)
Clock: In (⎍)
Self-Test: Out
Hold: Out

r. Turn the 3497A on. Using the signature analyzer, take the +5V and ground signatures first to make sure the analyzer is setup correctly. The +5V signature is "0001" and the ground signature is "0000". If the signatures are incorrect, make sure the SA setup is correct. If the setup is correct, the outguard processor (U11) or the ROMs (U16, U20, and U24) and RAM (U30) may be at fault. If the signatures are good, check the following signatures.

U11 Pin#	Address Bus	Signature
9	A0	5555
10	A1	CCCC
11	A2	7F7F
12	A3	5H21
13	A4	0AFA
14	A5	UPFH
15	A6	52F8
16	A7	HC89
17	A8	2H70
18	A9	HPP0
19	A10	1293
21	A11	0000
22	A12	3C96
23	A13	3827
24	A14	755U

s. If any signature is incorrect, replace the outguard processor (U11).

t. If the signatures are correct, the other circuitry in the outguard logic is most likely at fault. Refer to Table 8-A1-1 (Outguard Logic Signatures) and take the signatures given in the table. If any signatures are wrong, replace the corresponding component. If all the signatures are good, the data bus is most likely causing the failure. Check for shorts on the lines of the data bus. Then try replacing the components connected to the data bus.

Table 8-A1-1. Outguard Logic Signatures

IC	Pin #	Signature	IC	Pin #	Signature
U31	7	A68C	U32	7	942F
	9	A277		9	F042
	10	9840		10	131H
	11	8P4P		11	85H4
	12	5P18		12	5969
	13	2828		13	0PC5
	14	02H7		14	270P
	15	3APF		15	9CH4
U33	7	1920	U15	9	1181
	9	C34C		10	64HP
	10	597C		11	29A6
	11	UA87		12	5FU8
	12	4154		13	755U
	13	960F		14	3827
	14	84AF		15	0000
	15	3PCF			
U29	3	5555	U45	11	8295
	5	CCCC		12	F82H
	7	7F7F		13	04P6
	9	1293		14	U68U
	11	HAP7		15	F488
	13	3C96			

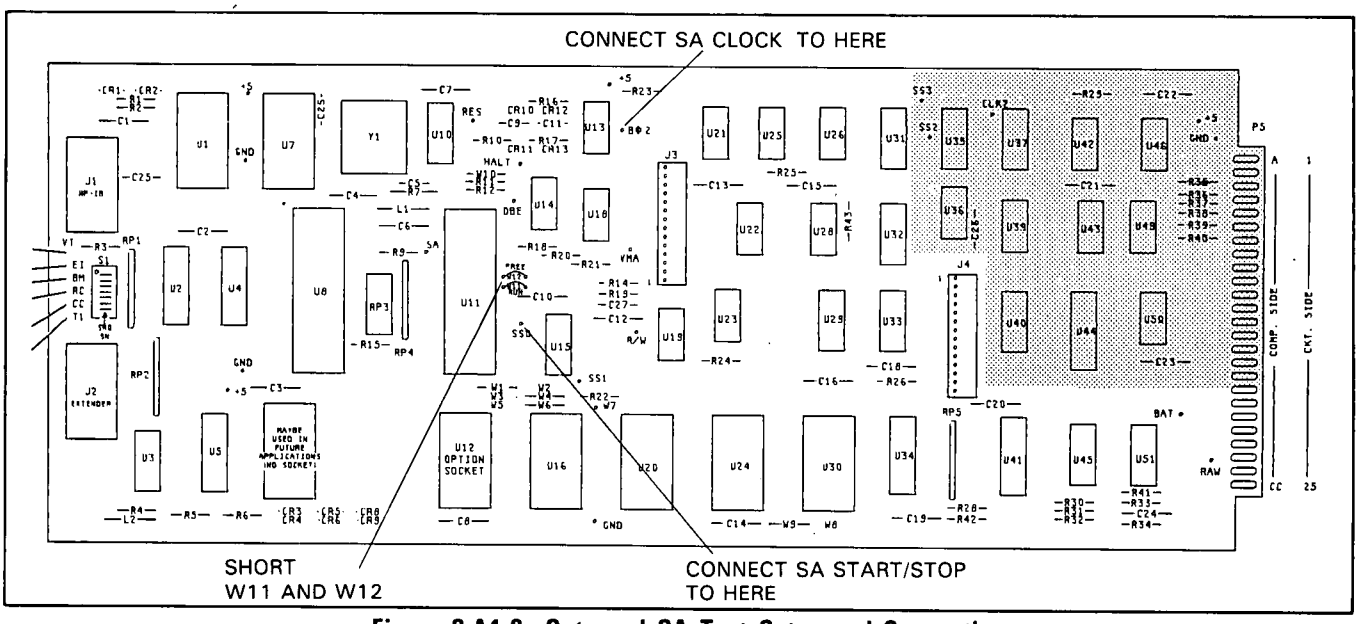


Figure 8-A1-2. Outguard SA Test Setup and Connection

8-A1-22. Self-Test #1 Fails

8-A1-23. This failure usually shows that there is no communication between the outguard and inguard controller. This can be caused by the crossguard logic, outguard logic, or inguard controller circuitry. The outguard controller determines this failure by sending a certain data byte to the inguard controller. This data byte is sent over the crossguard logic to the inguard controller and is used to reset the inguard processor. When the inguard processor is reset, it then sends a data byte with the same information it received, back to the outguard controller. If the data byte going back to the outguard controller is missing or different than the one sent, the controller will then display a Test #1 failure.

8-A1-24. As long as Test #1 fails, the outguard controller will continue sending the same data byte to the inguard controller. This can be used to determine if the outguard crossguard logic, inguard crossguard logic, or inguard controller circuitry is at fault. Do the following procedure to determine the circuitry. Unless otherwise noted, refer to Schematics A1 and AB1 for the procedure).

a. Turn the 3497A off.

b. Connect the inguard controller board to a Board Extender and plug the extender into the appropriate slot of the instrument (see paragraph 8-16 on how to connect the extender).

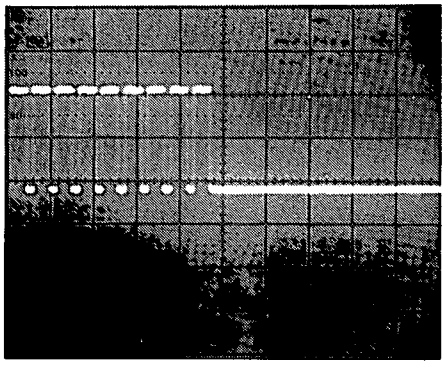
c. Turn the 3497A on.

d. Refer to Schematic B1. Using a logic probe, check and make sure the $\overline{RST}$ line of the inguard processor is toggling (i.e., change back and forth from high-low-high).

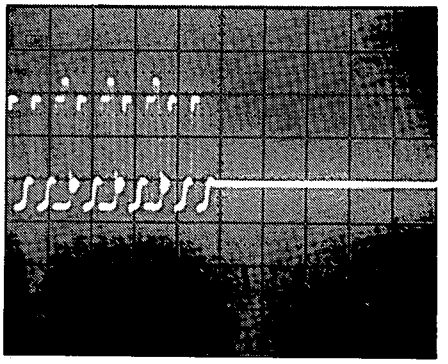
e. If the reset line at TP $\overline{RS}$ is low, check and make sure pin 12 of U110 is toggling. If pin 12 toggles, either U110 is defective or comparator U214 and associated circuitry is holding the reset line low. Check U110, and U124 and associated circuitry. If pin 12 is not toggling, continue with the next step.

f. If the reset line at TP $\overline{RS}$ is high (or low, see previous step), check and make sure pin 8 of U110 is toggling. If pin 8 is toggling, replace U110. If pin 8 is not toggling, the cause is most likely incorrect data developed by U114, U116, or the outguard. Do the following:

1. Check for clock and data signals at TP CLK and TP DATA, respectively. Use an oscilloscope to check for the signals shown in Figure 8-A1-3. Use the scope set-up information given in the figure to configure the scope.



CLOCK SIGNAL (TP CLK)



DATA SIGNAL (TP DATA)

SCOPE SETUP
Vertical: 2V/div
Trigger: Normal, Positive
Sweep: 5μS/Div

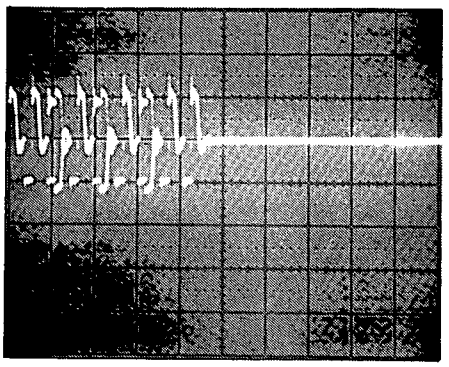
Figure 8-A1-3. Inguard Crossguard Clock and Data Signals

2. If the clock and data signals are good, the data from the outguard is transferred correctly to the inguard. Try replacing U114.

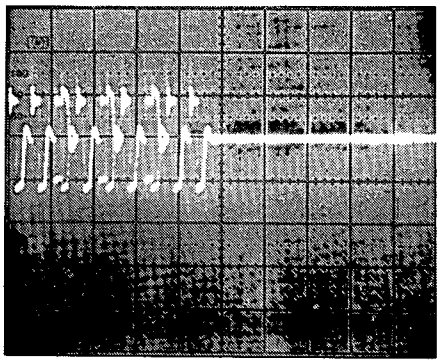
3. If the clock and data signals are incorrect or missing, the wrong data is sent from the outguard to the inguard. To determine the cause, turn the 3497A off and remove the inguard controller board from the extender. Then remove the extender from the instrument.

4. Using the procedure in paragraph 8-16, connect the outguard logic board to the Board Extender and plug the extender into the appropriate slot of the instrument.

5. Turn the 3497A on and check the signals shown in Figure 8-A1-4 at pins 8,11 and 3,6 of U46 (on the outguard crossguard logic circuitry). (Note: The signals will not remain steady on the scope. They will flash on and off at a certain rate.)



U46 PIN 8 AND 11



U46 PIN 3 AND 6

SCOPE SETUP
Vertical: 2V/Div
Trigger: Normal, Positive
Sweep: 5μS/Div

Figure 8-A1-4. Outguard Crossguard Logic Output Signals

6. If the signals are good, the outguard is sending the correct data. Check for defective transformers T1 and T3 (located on the A16 power supply board). If the transformers are good, replace U116 on the inguard controller board.

7. If the signals are incorrect or missing, troubleshoot the outguard crossguard logic circuitry (go to paragraph 8-A1-27).

g. If the reset line at TP $\overline{RS}$ is toggling, the outguard circuitry and the output of the outguard crossguard logic are most likely good. Further isolation is necessary. Do the following:

1. Try replacing U112.

2. If the instrument is still inoperative, turn the 3497A off and remove the inguard controller board from the extender. Then remove the extender from the instrument.

3. Connect the outguard logic board to the Board Extender and plug the extender into the appropriate slot of the instrument.

4. Turn the 3497A on and check the signals shown in Figure 8-A1-5 at pins 4 and 7 of U49 (on the outguard crossguard logic circuitry). (Note: The signals will not remain steady on the scope. They will flash on and off at a certain rate.)

5. If the signals are incorrect or missing, check for defective transformers T2 and T4 (located on the A16 power supply board). If the transformers are good, the inguard controller or inguard crossguard logic circuitry is most likely defective. Go to Service Group B for troubleshooting.

6. If the signals are good, the correct data is sent from the inguard to the outguard crossguard circuitry. Troubleshoot the outguard crossguard logic (go to paragraph 8-A1-27).

8-A1-25. Keyboard, Display, HP-IB, Timer/Pacer (Self-Test #3 Fails), and 3498A Extender Failures

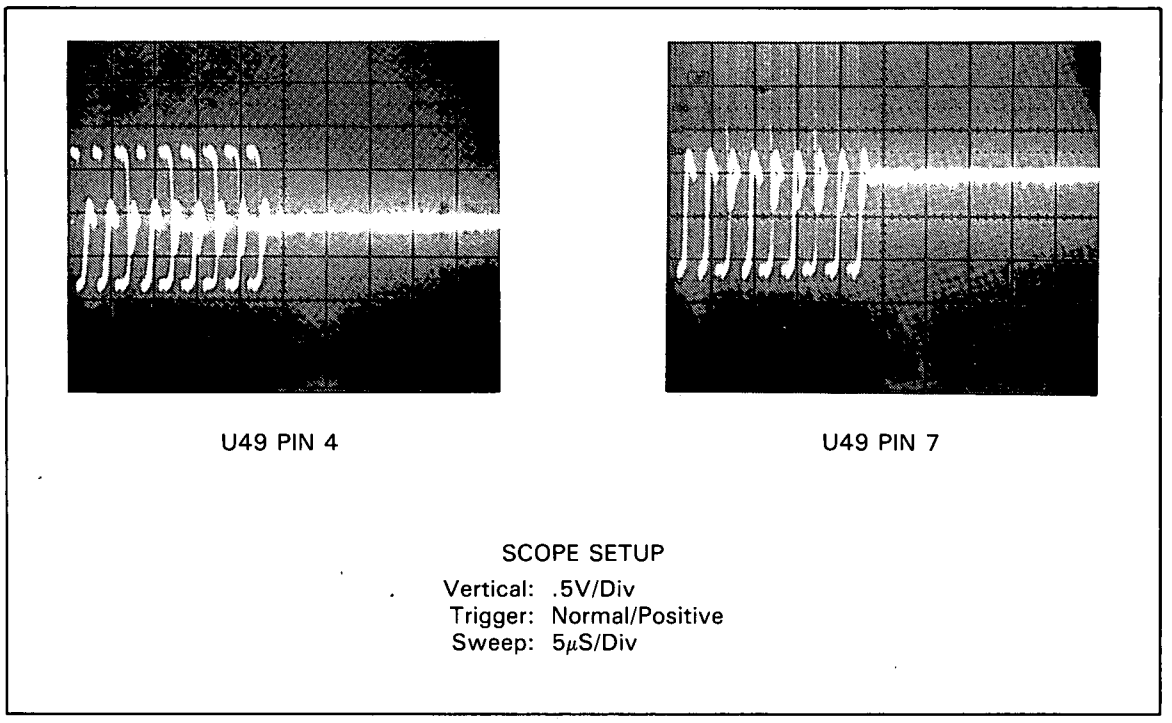


Figure 8-A1-5. Input Signals to the Outguard Crossguard Logic

8-A1-26. Any one of these failures can be caused by the Peripheral Decoders U31, U32, U33, and U45. Except for the HP-IB and 3498A Extender failures, the failures can also be caused by the buffered data bus. If all of the failures are noted, the 3497A has most likely a turn-on failure (go to paragraph 8-A1-18 for troubleshooting). Otherwise, do the following:

a. Turn the 3497A off.

b. Remove the outguard logic board from the instrument.

c. Connect the outguard logic board to a Board Extender and plug the extender into the appropriate slot of the instrument (see paragraph 8-16 on how to connect the extender).

d. Open the 3497A's front panel door. Locate and remove the power supply shield over the power supply board (see paragraph 8-24 for a procedure to remove the shield).

e. Refer to Figure 8-A1-6. Locate transformers T1 through T4 and reconfigure the transformer wiring, as shown in the figure.

f. Obtain a signature analyzer and connect as follows:

Start:	TP SS1 (A15 pin 3)
Stop:	TP SS1 (A15 pin 3)
Clock:	TP Bϕ2
Gnd:	TP GND

g. Set the signature analyzer as follows:

Start:	Out (⎍)
Stop:	Out (⎍)
Clock:	Out (⎍)
Self-Test:	Out
Hold:	Out

h. Turn the 3497A on. Using a clip lead, momentarily short TP SA to ground (TP GND). This places the 3497A into the RAM SA mode.

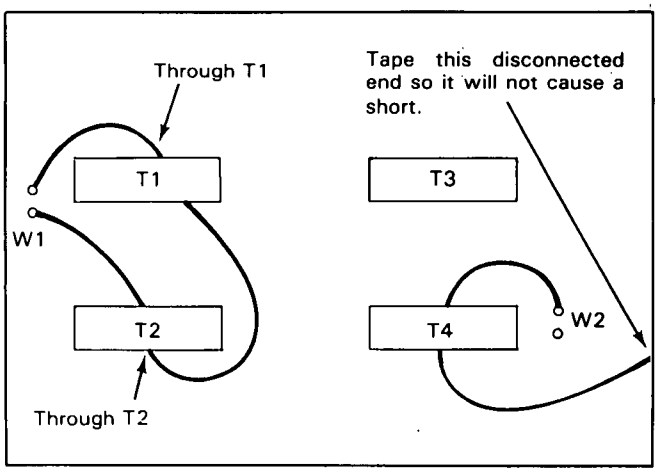


Figure 8-A1-6. Pulse Transformer Test Wiring

i. Using the signature analyzer, take the +5V signature. The signature should be "APHC". If the signature is wrong, make sure the signature analyzer is setup correctly. If the analyzer set-up is correct, the outguard crossguard logic is most likely inoperative. Go to paragraph 8-A1-27 for troubleshooting. If the +5V signature is good, take the following signatures.

U31 Pin #	Signature	U32 Pin #	Signature
7	APHC	7	F737
9	APHC	9	1408
10	APHC	10	APHC
11	APHC	11	APHC
12	APHC	12	APHC
13	4F77	13	APHC
14	U76U	14	APHC
15	APHC	15	APHC

U33 Pin #	Signature	U45 Pin #	Signature
7	APHC	11	0P92
9	35F4	12	F8P6
10	19FP	13	C338
11	APHC	14	48F8
12	8H9H	15	PAP2
13	A6FU		
14	APHC		
15	0P34		

j. If any signatures are wrong, replace the appropriate component.

k. If the signatures are good and the 3497A has an HP-IB or 3498A Extender failure, go to paragraph 8-A1-71 or 8-A1-85, respectively, for troubleshooting. If the signatures are good and the 3497A has a keyboard, display, or timer/pacer failure, continue with the next step.

l. Make sure the signature at pin 19 of U34 is "38C1".

m. If the signature is wrong, do the following:

1. Make sure the signature at pin 4 of U26 is "7514".

2. If the signature is wrong, try replacing U19.

3. If the signature is good, make sure the signature at pin 5 of U26 is "HA52".

4. If the signature is wrong, replace U22, U14, U18, or U28.

5. If the signatures at pins 4 and 5 of U26 are good, replace U26.

n. If the signature at pin 19 of U34 is good, take the following signatures:

U34 Pin #	Signature
11	7U74
12	AP4H
13	F071
14	5HH6
15	52HC
16	H30A
17	994P
18	C26H

o. If any signatures are wrong, try replacing U34. If the signatures are good, troubleshoot the keyboard, display, or timer circuitry. Go to paragraphs 8-A1-40, 8-A1-53, or 8-A1-74 for the keyboard, display, or timer/pacer circuitry, respectively. Once the previous tests have been performed, turn the 3497A off and return the pulse transformer wiring for normal operation, as shown in Figure 8-A1-7.

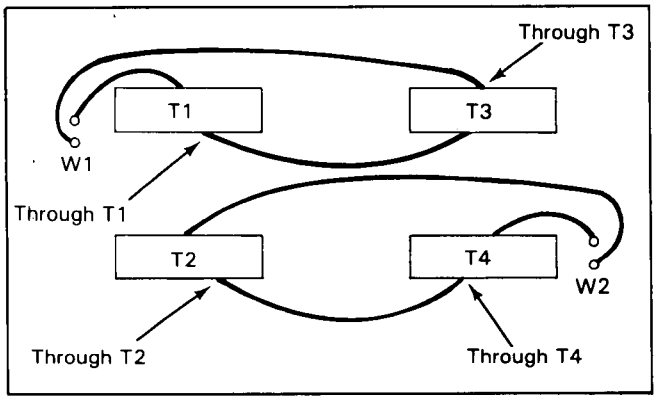


Figure 8-A1-7. Pulse Transformer Wiring for Normal Operation

8-A1-27. OUTGUARD CROSSGUARD LOGIC TROUBLESHOOTING

8-A1-28. General

8-A1-29. Before performing the troubleshooting procedures in the following paragraphs, make sure that the inguard controller or inguard crossguard logic are not causing the failure. Go to paragraph 8-A1-22 to determine the defective circuitry. Do this since a crossguard logic failure normally shows up as a Test #1 failure. If other symptoms are noted, the failure is most likely not a crossguard failure.

8-A1-30. Refer to Schematic AB1 for the following troubleshooting information. The outguard crossguard logic circuitry has two different parts to it: a transmitter and a receiver. The paragraphs have a procedure to isolate the defective circuitry and procedures to troubleshoot the circuitry.

8-A1-31. Transmitter/Receiver Isolation

8-A1-32. Part of this procedure has been performed in paragraph 8-A1-22. If the defective area of the crossguard logic has been determined already, ignore the following procedure. If not known, do the following:

a. Turn the 3497A off.

b. Open the 3497A's front panel door. Locate and remove the power supply shield over the power supply board (see paragraph 8-24 for a procedure to remove the shield).

c. Refer to Figure 8-A1-6. Locate transformers T1 through T4 and reconfigure the transformer wiring, as shown in the figure.

d. Turn the 3497A on.

e. Using an oscilloscope, check the signals shown in Figure 8-A1-4 at pins 8,11, and 3,6 of U46. Use the scope setup information shown in the figure. (Note: The signals may or may not remain steady on the scope. They may or may not flash on and off at a certain rate.)

f. If the signals are incorrect or missing, the transmitter circuitry is at fault. Go to paragraph 8-A1-33 for troubleshooting.

g. If the signals are correct, check the signal shown in Figure 8-A1-5 at pin 4 of U49.

h. If the signal is good, the receiver circuitry is at fault. Go to paragraph 8-A1-38 for troubleshooting.

i. If the signal is missing, make sure transformers T1 and T2 are wired as shown in Figure 8-A1-6. If the wiring is correct, make T1, T2, U49, or R37 may be defective.

8-A1-33. Transmitter Troubleshooting

8-A1-34. Troubleshoot the transmitter circuitry by looking at the signal in Figure 8-A1-6. Refer to the figure and note that the signal should have a total of nine peaks. If the signal has the incorrect number of peaks, or if the signal is completely missing, or if the signal has a different shape, go to paragraphs 8-A1-35, 8-A1-36, or 8-A1-37, respectively, for troubleshooting.

8-A1-35. Incorrect Number of Peaks. This can be caused by counter U35. If the counter is good, try U26 or U36.

8-A1-36. Signal Missing. Do the following:

a. Using a logic probe, make sure pin 5 of U43 is toggling. If the pin is not toggling, make sure pin 3 is toggling. If pin 3 is toggling, replace U43. If pin 3 is not toggling, replace U10.

b. Make sure pin 3 of U36 is toggling. If the pin is not toggling, trace back through U36, U39, U28, and U37 to U43. Replace the defective IC.

c. Make sure pins 2 and 9 of U40 are toggling. If they are not toggling, make sure pin 1 of U40 is toggling. If pin 1 is toggling, replace U40. If pin 1 is not toggling, trace back through U35 and U39 to U46. Replace the defective IC.

d. Make sure pins 5 and 6 of U42 are toggling. Replace U46 if they are not toggling.

8-A1-37. Signal Has Different Shape. If the signal has nine peaks and has a different shape, try replacing U40.

8-A1-38. Receiver Troubleshooting

8-A1-39. Do the following:

a. Using an oscilloscope, check the signal shown in Figure 8-A1-8 at pin 14 of U49. Use the scope setup information shown in the figure. (Note: The signals may or may not remain steady on the scope. They may or may not flash on and off at a certain rate.)

b. If the signal is missing or wrong, replace U49.

c. If the signal is good, check for the same signal at pin 4 of U39.

d. If the signal at pin 4 of U39 is missing, replace U39.

e. If the signal is good, make sure pin 9 of U50 and pin 1 and 19 of U44 are toggling (use a logic probe).

f. If they are not toggling, try replacing U39 or U43.

g. If the pins are toggling, try replacing U44 or U50.

8-A1-40. INOPERATIVE KEYBOARD

8-A1-41. General

8-A1-42. Refer to Schematic A4 for the keyboard troubleshooting information starting in paragraph 8-A1-45. A keyboard failure is when any or all of the keys are inoperative. Since part of the keyboard circuitry is also used by the display circuitry, an inoperative keyboard can also cause an inoperative display.

8-A1-43. Before troubleshooting the keyboard circuitry, make sure the outguard logic is operating correctly. Do this by sending the 3497A set-up information and reading its output using the HP-IB. If this can be accomplished, the outguard logic is most likely good. If unable to remotely configure and read the 3497A, it is most likely a turn-on failure (go to paragraph 8-A1-18 for troubleshooting).

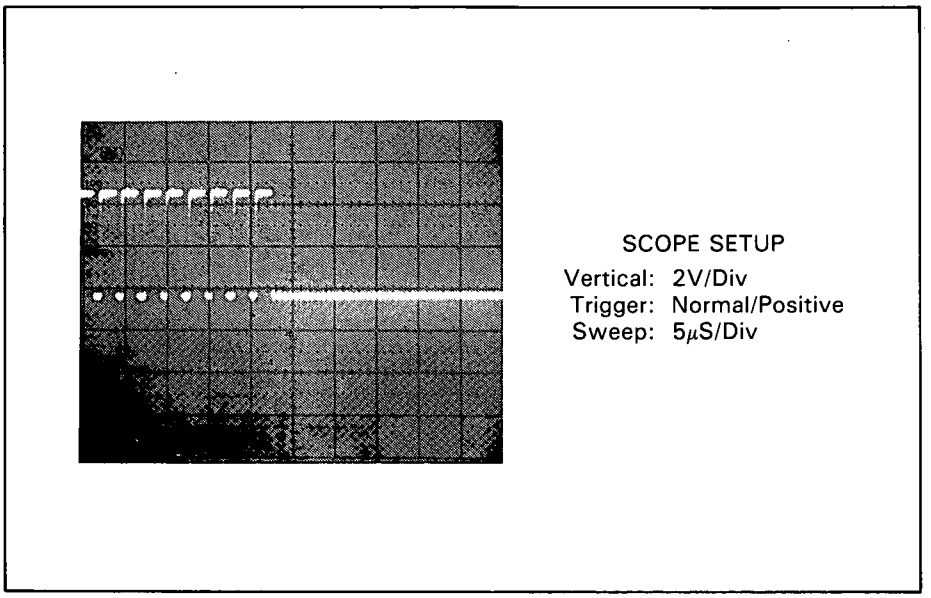


Figure 8-A1-8. Signal at Pin 14 of U49

8-A1-44. Before going to the following paragraphs for troubleshooting, make sure the procedure in paragraph 8-A1-25 has been performed. Since the removal of the front panel board may be required to repair the keyboard, refer to paragraph 8-22 for the removal procedure.

8-A1-45. Keyboard and Display Failure

8-A1-46. If both keyboard and display failure are noted, do the following:

a. Using a logic probe, make sure pins 1 and 19 of U13 are toggling (i.e., continuously changing states).

b. If the pins are not toggling, do the following:

1. Check and make sure pins 4 and 5 of U16 are toggling.

2. If pins 4 and 5 of U16 are not toggling, replace U20. If they are toggling, replace U16.

c. If pins 1 and 19 of U13 are toggling, replace U13.

8-A1-47. All Keys Inoperative

8-A1-48. Do the following:

a. Connect a logic probe to pin 6 of U13 and then press any key on the keyboard.

b. If the logic probe changes from low to high while the key is pressed, U14 and U15 are most likely good. Replace U13.

c. If the logic probe remains either high or low, do the following:

1. Using the logic probe, make sure pin 7 of U15 changes from low to high when a key is pressed.

2. If no change is noted on pin 7, replace U14.

3. If pin 7 changes from low to high, replace U15.

8-A1-49. Some Keys Inoperative

8-A1-50. This failure is most likely caused by a key switch. Use an ohmmeter and make sure the switch closes when the front panel pushbutton is pressed. If the switch is good, try replacing U14.

8-A1-51. Keybounce Failure

8-A1-52. If excessive keybounce is noted, make sure C7 and C8 are good. If they are good, try replacing U14.

8-A1-53. INOPERATIVE DISPLAY (AND/OR BEEPER FAILS)

8-A1-54. General

8-A1-55. Before troubleshooting the display circuitry, make sure the outguard logic is operating correctly. This can be checked by remotely setting the 3497A to a certain configuration (using the HP-IB) and then remotely reading its output. If this can be accomplished, the outguard logic is most likely good. If unable to remotely configure and read the 3497A, it is most likely a turn-on failure (go to paragraph 8-A1-18 for troubleshooting). Also make sure the procedure in paragraph 8-A1-25 has been performed before troubleshooting the display circuitry.

8-A1-56. Refer to Schematic A4 for the display and beeper troubleshooting procedures (starting in paragraph

8-A1-58). A display failure is when any part or all of the displays or annunciators are inoperative, and if the beeper is inoperative. The beeper is included with the display troubleshooting since the beeper circuitry is part of the display circuitry. Since part of the keyboard circuitry is also used by the display circuitry, an inoperative keyboard can also cause an inoperative display. If both keyboard and display are inoperative, do the procedure in paragraph 8-A1-45 first to determine the defective component.

8-A1-57. The display circuitry can be separated into different areas which include the main display (U4 and associated circuitry), channel display (U2, U5, U8, and associated circuitry), and various annunciator circuitry (U1, U9, U6, etc.). Because of this, first determine which circuitry fails and then troubleshoot the circuitry. The following paragraphs have the display failures and troubleshooting information. Since the removal of the front panel board may be required to service the keyboard, refer to paragraph 8-22 for the removal procedure.

8-A1-58. All Displays and Annunciators Inoperative

8-A1-59. Since latch U7 is used to send the display data to the various display circuitry, U7 is the most likely cause. Do the following:

a. Using a logic probe, make sure pin 11 of U7 is toggling (i.e., continuously changing states).

b. If the pin is toggling, replace U7.

c. If the pin is not toggling, make sure pin 4 of U20 and U21 are toggling. If they are not toggling, the 3497A has a turn-on failure (go to paragraph 8-A1-18 for troubleshooting).

d. If both pins 4 are toggling, try replacing U20.

8-A1-60. Main Display Inoperative

8-A1-61. The main display circuitry consists of U4 and associated circuitry. The main display failures and troubleshooting information is in the following paragraphs.

8-A1-62. All the DS6 through DS12 LEDs are On or Off. If "all" of the DS6 through DS12 LEDs are either constantly on or off, it is a good indication that pin 8 of U4 is held either high or low. Use a logic probe and determine if pin 8 is held high or low. If pin 8 continuously toggles, U4 is then the most likely cause. If pin 8 is held high or low, either U17 or U21 are the cause. Do the following:

a. Make sure that pins 10 and 11 of U21 toggle.

b. If they toggle, replace U17. If not replace U21.

8-A1-63. Some of the DS6 through DS12 LEDs are On or Off. If only some of the DS6 through DS12 LEDs are off or some of the segments of the LEDs are missing, the LEDs themselves or U4 are most likely at fault. Before replacing a suspected defective LED, make sure all the a, b, c, etc., and B0, B1, B2, etc. lines of U4 are continuously toggling. If they are toggling, check for a defective LED. If they are not toggling, replace U4.

8-A1-64. DS6 Decimal Point Inoperative. If the decimal point (part of DS6) is inoperative, check and make sure the output at pin 4 of U22 is good. (Note: The LED should only operate if the voltmeter option is installed.) The pin should go low to turn the LED off and high to turn the LED on. Make sure the pin changes state when it is suppose to change (i.e., LED turns off or on). If it does, the LED is defective. If not, make sure U22 receives the correct clock signal from U21. If it does, replace U22. If not, replace U21.

8-A1-65. Channel Display Inoperative

8-A1-66. The channel display is separated into three different circuitry, U2 and DS4, U5 and DS3, and U8 and DS2. The channel display should only be enabled when an analog channel is selected, otherwise the LEDs are off. The channel display failures and troubleshooting information is as follows:

a. If LED DS2 is inoperative, make sure pin 5 of U8 is continuously toggling (use a logic probe). If not, check for toggling at pin 4 of U15 and pin 14 of U20. If any of the pins do not toggle, replace the appropriate IC. If pin 5 of U8 is toggling, check for toggling at pins 12 through 17 of U8. If good, replace DS2. If not toggling, replace U8.

b. If LED DS3 and DS4 are inoperative, make sure pin 5 of U2 is continuously toggling (use a logic probe). If not, check for toggling at pin 12 of U15 and pin 15 of U20. If any of the pins do not toggle, replace the appropriate IC. If pin 5 of U2 is toggling, check for toggling at pins 12 through 17 of U2 and U5. If good, replace DS3 or DS4. If not toggling, replace U5 or U2.

c. If the decimal point for the channel display (part of DS4) is inoperative, check and make sure the output at pin 5 of U22 is good. (Note: The LED should only operate if an analog plug-in option is installed.) The pin should go low to turn the LED off and high to turn the LED on. Make sure the pin changes state when it is suppose to change (i.e., LED turns off or on). If it does, the LED is defective. If not, make sure U22 receives the correct clock signal from U20. If it does, replace U22. If not, replace U20.

8-A1-67. Annunciator(s) Inoperative

8-A1-68. Most annunciators have their own decoder/driver. The only exception is the DCV, SEC, etc., annunciators. To troubleshoot the annunciators, do the following:

a. If a failure is noted by any of the annunciators other than the DCV, SEC, etc., annunciators, make sure pin 11 of U3, U6, and U9 (or pin 9 of U1) are continuously toggling (use a logic probe). If they are not, replace U21. If they are toggling, check and make sure the outputs of the IC are on or off, dependent on whether the annunciators are to be on or off (high = off, low = on). If the outputs are good, replace the defective LED. If not, replace the appropriate IC (U3, U6, U9, or U1).

b. If the DCV, SEC, etc., annunciators are defective, make sure pin 11 of U12 is continuously toggling (use a logic probe). If the pin is not toggling, replace U21. If the pin is toggling, check and make sure the outputs of U12 are on or off, dependent on whether the corresponding annunciators are suppose to be on or off (high = on, low = off). If the outputs are good, make sure the corresponding outputs of U11 are good (U11 inverts the outputs making high = on and low = off). If they are good, replace the defective LED. If not, replace U11.

8-A1-69. Beeper Inoperative

8-A1-70. To check the beeper circuitry, do the following:

a. Press the blue shift button on the front panel. Then press the EXECUTE button. Each time the EXECUTE button is pressed, the beeper should operate.

b. While pressing the button, monitor pin 3 of U16. The pin should go from high-low-high.

c. If the pin does change state, troubleshoot Q1 and the beeper.

d. If the pin does not change state, make sure pin 3 changes from high-low-high.

e. If the pin changes state, replace U16 or associated circuitry.

f. If it does not change, try replacing U22 or U21.

8-A1-71. HP-IB FAILURE

8-A1-72. Refer to Schematic A1 for the HP-IB troubleshooting information in the following paragraphs. An HP-IB failure is when the 3497A cannot be setup or its output read using the HP-IB. If the display and keyboard are also inoperative, the failure is not an HP-IB failure, it is most likely a turn-on failure (go to paragraph 8-A1-18 for troubleshooting).

8-A1-73. Before going to the following procedure, make sure the procedure in paragraph 8-A1-25 has been performed. Because the interfacing between the HP-IB and outguard controller is performed using U1, U7, and U8, these components are the most likely cause of an HP-IB failure. Do the following:

a. Turn the 3497A off.

b. Make sure the outguard logic board is connected to a Board Extender with the extender in the appropriate slot (see paragraph 8-16).

c. Turn the 3497A on.

d. Using a clip lead, momentarily connect TP SA to ground (TP GND).

e. Using a logic probe, make sure pins 17 and 18, 21 to 23, and 25 and 26 of U8 are all high (TTL high). If any are not high, replace U8. If they are high, make sure pins 2 through 9 of U7 are high. If any are not high, replace U7. If they are high, continue with the next step.

f. Turn the 3497A off.

g. Obtain a signature analyzer and connect as follows:

Start:	TP SS1 (U15 pin 3)
Stop:	TP SS1 (U15 pin 3)
Clock:	TP Bϕ2
Gnd:	TP GND

h. Set the signature analyzer as follows:

Start:	Out (⌟)
Stop:	Out (⌟)
Clock:	Out (⌟)
Self-Test:	Out
Hold:	Out

i. Turn the 3497A on.

j. Using a clip lead, momentarily connect TP SA to ground (TP GND). Then take the following signatures:

U8 Pin #	Signature
27	UF23
28	UF23
29	66C0
30	U352
31	8887
32	3451
33	P2A0
34	F6F6
35	1549
36	U319

k. If any signatures are wrong, replace U8.

l. If the signatures are good, take the following signatures:

U7 Pin #	Signature
2	U319
3	1549
4	F6F6
5	P2A0
6	3451
7	8887
8	0252
9	66C0

m. If any signatures are wrong, replace U7. If the signatures are good, try U8.

8-A1-74. TIMER/PACER FAILURE (OR SELF-TEST #3 FAILS)

8-A1-75. General

8-A1-76. Refer to Schematic A3 for the timer/pacer troubleshooting information in the following paragraphs. A timer/pacer failure normally shows up when the internal clock is inoperative, the TIMER output port is inoperative (i.e., Time Interval or Timer Output), or Test #3 fails. Before doing any troubleshooting, make sure crystal Y1 is good.

8-A1-77. Before going to the troubleshooting procedures in the following paragraphs, make sure the procedure in paragraph 8-A1-25 has been performed.

8-A1-78. Test #3 Fails, and Internal Clock, Time Interval, and Timer Output Modes are Inoperative

8-A1-79. This can be caused if the timer microcomputer (U4) is defective or if it receives or outputs the incorrect set-up information. Do the following:

a. Turn the 3497A off.

b. Make sure the outguard logic board is connected to a Board Extender with the extender in the appropriate slot (see paragraph 8-16).

c. Turn the 3497A on. Using a clip lead, momentarily connect TP SA to ground (TP GND).

d. Using a logic probe, make sure pin 6 of U3 is toggling. If the pin is not toggling, replace U3. If the pin is toggling, make sure pin 11 of U3 is toggling. If the pin is not toggling, replace U4, U9, or U12.

e. If pin 11 is toggling, make sure pin 8 of U3 is toggling. If pin 8 is not toggling, replace U3. If the pin is toggling, replace U4, U9, or U12.

8-A1-80. The Time Interval or Timer Output Pulses are Wrong or Missing

8-A1-81. These failures can be caused by the microcomputer, pacer circuitry, or gating logic. The following pargraphs have troubleshooting information for both failures.

8-A1-82. Both Time Interval and Timer Output Fail. The most likely cause is the microcomputer (U4) or U1. Replace U4 or U1.

8-A1-83. Time Interval Fails. Do the following:

a. Set the time interval for a 1 second interval output (program codes TI1).

b. Using a logic probe, make sure the output at pin 14 toggles from high-low-high every 1 second.

c. If it does not toggle, check the following:

1. Make sure pin 13 of U4 is high. If the pin is low, replace U4.

2. Make sure pin 4 of U4 is high. If the pin is low, U4 is in a constant reset state. This can be caused by U1, U6, U8, or U4. Make sure pins 12 and 13 of U1 are both low. If they are low, try U1 and then U4. If either or both pins are high, replace U6 or U8.

d. If pin 13 is high, replace U1.

8-A1-84. Timer Output Fails. This failure can either show up as an incorrect frequency or the output pulse is missing. This can be caused by the pacer circuitry or U4. Do and check the following:

a. Make sure the output at pin 15 of U2 is 10KHz.

b. If the frequency is wrong, replace U2.

c. If the frequency is good and the timer output is at the wrong frequency, do the following:

1. Set the time output for a .7777 second interval output (program code TO7777). This sets the 1, 2, and 4 inputs of the counters to high.

2. Using a logic probe, make sure pins 5, 11, and 14 of U6, U7, U10, and U13 are high and pin 2 of the ICs is low.

3. If the pins on U10 and/or U13 are wrong, replace U11. If the pins on U6 and/or U7 are wrong, replace U8.

4. If all the pins are good, set the time output for a .8888 second interval (program code TO8888). This sets the 8 inputs of the counters to high.

5. Using a logic probe, make sure pins 5, 11, and 14 of U6, U7, U10, and U13 are low and pin 2 of the ICs is high.

6. If the pins on U10 and/or U13 are wrong, replace U11. If the pins on U6 and/or U7 are wrong, replace U8.

7. If all the pins are good, make sure pin 12 of U6, U7, U13, and U10 are toggling. If one of the pins are not toggling, replace the appropriate IC. If they are all toggling, try replacing U6, U7, U10, or U13.

d. If the frequency at pin 15 of U2 is good and the timer output pulse is missing, do the following:

1. Using a logic probe, make sure pin 13 of U4 is low and pin 14 is high.

2. If the levels are wrong, replace U4.

3. If the levels are good, make sure the timer output pulse is good at pin 1 of U1.

4. If the output pulse is good, replace U1.

5. If the pulse is missing, go to step c (paragraph 8-A1-84-c; timer output at the incorrect frequency) for troubleshooting.

8-A1-85. 3498A EXTENDER FAILURES

8-A1-86. Refer to Schematic A1 for the following troubleshooting information. Before doing any troubleshooting, make sure the procedure in paragraph 8-A1-25 has been performed. Also make sure the failure is not caused by the 3498A.

8-A1-87. The 3498A failures are normally caused by the extender buffers (U3 and U5) or by the output extender (U4). If the procedure in paragraph 8-A1-25 has been performed and the failure is still present, try replacing U3, U4, or U5.

8-A1-88. INPUT/OUTPUT PORTS TROUBLESHOOTING

8-A1-89. Refer to Schematic A1 for the following troubleshooting information. Before doing any troubleshooting, make sure the procedure in paragraph 8-A1-25 has been performed.

8-A1-90. Timer Port

8-A1-91. Since this port is the output of the timer/pacer circuitry, go to paragraph 8-A1-74 for troubleshooting.

8-A1-92. Ext Trig and Ext Incr Ports

8-A1-93. Do the following:

a. Cycle power on the 3497A.

b. If the Ext Trig port is inoperative, do the following:

1. Connect a logic probe to pin 9 of U25. The pin should be low.

2. If the pin is high, replace U25.

3. If pin 9 is low, make sure pin 2 of U13 is low.

4. If pin 2 of U13 is high, make sure CR13 is not shorted and R2 is not open (diodes CR11 and CR13 are protection diodes). If CR13 and R2 are good, replace U13.

5. If pin 2 is low, connect the logic probe to pin 9 of U25. Then, momentarily connect the EXT TRIG port to ground. Pin 9 should then change from low-high-low. Replace U25 if it does not change.

c. If the Ext Incr port is inoperative, do the following:

1. Connect a logic probe to pin 5 of U25. The pin should be low.

2. If the pin is high, replace U25.

3. If pin 5 is low, make sure pin 4 of U13 is low.

4. If pin 4 of U13 is high, make sure CR12 is not shorted and R1 is not open (diodes CR10 and CR12 are protection diodes). If CR12 and R1 are good, replace U13.

5. If pin 4 is low, connect the logic probe to pin 5 of U25. Then, momentarily connect the EXT INCR port to ground. Pin 5 should then change from low to high and remain high. Replace U25 if it does not change.

8-A1-94. VM Complete and Channel Closed Ports

8-A1-95. These ports receive their signals from peripheral decoder U32. If the procedure in paragraph 8-A1-25 has been performed and everything passes, make sure CR3 through CR6, and R5 and R6 are good. If they are good, replace U32.

8-A1-96. BBM Sync Port

8-A1-97. Do the following:

a. Connect a logic probe to pin 6 of U21. The pin should be low. If pin 6 is high, replace U21.

b. If pin 6 of U21 is low, make sure pin 3 of U18 is high.

c. If pin 6 of U21 is low, check for a shorted CR1 and open R23. If CR1 and R23 are good, replace U18.

d. If pin 3 of U18 is low, replace U21.

SERVICE GROUP A2

OUTGUARD TROUBLESHOOTING (Serial I/O)

Service Group A2 Contents

8-A2-1. INTRODUCTION

8-A2-2. This service group has troubleshooting information for the outguard logic of the 3497A's Option 232 (Serial I/O) mainframe (see Service Group A1 for the standard HP-IB mainframe troubleshooting). The information is for all of the outguard circuitry which consists of the main controller circuitry, Serial I/O circuitry, timer/pacer circuitry, crossguard logic, standard front panel, and associated circuitry.

8-A2-3. PRE-TROUBLESHOOTING INFORMATION

8-A2-4. Read the information in the following paragraphs before doing any troubleshooting.

8-A2-5. Troubleshooting Without Signature Analysis

8-A2-6. Check for stuck nodes on the address bus, data bus, and the outputs of devices used by the outguard. This can be done using a logic probe. A stuck node usually shows the node in a certain steady state when it is supposed to toggle. Try to determine what the 3497A is suppose to be doing and what it is not doing, or vice versa, and then try to logically associate that to a particular circuit. The theory of operation may be helpful to determine the defective circuitry. Then check for the outputs of a device in that circuit to see if they are toggling. If they are not, check the inputs of the device for toggling. If the inputs are toggling, the device is probably defective. This method of troubleshooting does not check for timing errors, but is fast and simple.

8-A2-7. Troubleshooting With Signature Analysis

8-A2-8. A signature analyzer is used to determine the faulty circuitry and component. This is done by placing the circuitry in a certain operating mode and then take signatures using the signature analyzer. When the circuitry is in that mode, the data on the lines develop a unique signal. This data (i.e., signal) is read by the signature analyzer which then develops a unique signature. If the signature is correct, the device developing the signal is correct. If the signature is incorrect, the device may be defective. Before replacing the device, make sure other devices on the line are not causing the incorrect signature.

8-A2-9. When using the procedures in this service group, make sure the charts and procedures are followed in order. If done otherwise, the procedures may appear to be confusing.

8-A2-10. General Troubleshooting Information

8-A2-11. Check and make sure the +5V power supply is good. This supply should be between +4.75V and +5.25V.

8-A2-12. Make sure the outguard processor's clock is operating correctly. Check and make sure that the clock outputs at pins 13 and 15 of U10 are 180 degrees out of phase (see Schematic A2). If the clock signals are missing, replace U10.

8-A2-13. Make sure the processor is properly reset. This can be done by momentarily shorting the RST line (U11 pin 40) to ground. The line should then go high and reset the processor. If, after shorting the line, the 3497A starts operating or if the line remains low, try replacing U10 or U51.

8-A2-14. OUTGUARD TROUBLESHOOTING

8-A2-15. The outguard troubleshooting procedures are in paragraph 8-A2-18. Use the procedures whenever an outguard failure is noted in the Serial I/O outguard (refer to Service Group A1 for the standard HP-IB outguard). For a description of the outguard failures, refer to paragraphs 8-30 and 8-39.

8-A2-16. Signature Analysis Tests

8-A2-17. Various SA (Signature Analysis) Tests are made in the outguard troubleshooting procedures. Perform the tests in the order they are given. The tests are separated as follows:

Test Number	Test
1	Free Run Test
2	RAM Test
3	Crossguard Test
4	Timer Test
5	Serial I/O Cable Test
6	Front Panel/Display Test
7	Crossguard Test

8-A2-18. OUTGUARD TROUBLESHOOTING PROCEDURES

8-A2-19. General

8-A2-20. To troubleshoot the outguard, check the outguard clock first and then do the outguard SA tests in the order shown in paragraph 8-A2-16 (starting with Test #1).

8-A2-21. Some of the SA tests cause the 3497A beeper to turn on. Since this may be distracting, it is recommended to unplug the front panel board from the mainframe (see paragraph 8-22). Make sure the front panel is plugged back into the mainframe when the test is completed.

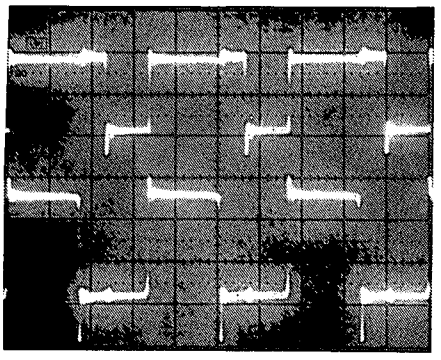
8-A2-22. Equipment Required

8-A2-23. The required test equipment is as follows:

Signature Analyzer -hp- Model 5004A
Oscilloscope -hp- Model 1741A

8-A2-24. Troubleshooting Procedures

8-A2-25. In the procedures in the following paragraphs, various clock signals are checked and then the address bus is checked using SA. If the address bus is good, the outguard controller is most likely operating. The failure is then most likely caused by the ROMs and RAMs, or by the front panel circuitry (keyboard and displays) or Serial I/O circuitry. If the signatures on the address bus are good, more signatures are then taken to check the



CHANNEL A: TP Bϕ2

CHANNEL B: TP DBE

SCOPE SETUP
Vertical: 2V/Div (Channel A & B)
Trigger: Trigger Comp A, Normal, Positive
Sweep: .2μS/Div

Figure 8-A2-1. Bϕ2 and DBE Clock Signals

output of the peripheral decoders, etc. Unless otherwise noted, refer to Schematic A2 when doing the outguard troubleshooting procedures.

8-A2-26. Checking Outguard Clock

8-A1-27. Do the following:

a. Turn the 3497A off.

b. Remove the outguard logic board from the instrument.

c. Connect the outguard logic board to a Board Extender and plug the extender into the appropriate slot of the instrument (see paragraph 8-16 on how to connect the extender).

d. Turn the 3497A on.

e. Check for clock signals at TP Bϕ2 and TP DBE. Use an oscilloscope (the 1741A) to check for the signals shown in Figure 8-A2-1. Use the scope set-up information given in the figure to configure the scope.

f. If the clock signals are missing or wrong, check for a defective U10, U13, and U14. If the clock signals are good, go to the Free Run SA Test #1 in the following paragraph.

8-A2-28. Free Run Test (Test #1)

8-A2-29. The Free Run Test (Test #1) is not segmented (1A, 1B, etc.) as are most other tests because many of the signatures that can be verified are not dependent upon a pass/fail condition of some previous test segment. However, there is a flowchart for the first portion of this test (see Figure 8-A2-2). In the first portion, the microprocessor reads all available ROM memory locations, permitting all bit patterns to be verified as well as the operation of the ROM address decoders and buffers. The remaining signatures are given to check a suspected problem with the Outguard Extender (3498A Interface), Slot Select (U45), Extender Enable (U22, U26), or I/O Address Decoders (U31, U32, and U33).

8-A2-30. Free Run Test #1, Data Bus Signatures. Do the following:

a. Turn the 3497A off.

b. Remove bus break RP3 from its socket.

c. Using short clip leads, connect the three free run test points together.

d. Obtain a signature analyzer and connect as follows:

Start:	U23 pin 8
Stop:	TP SS0
Clock:	TP CLK
Gnd:	TP GND

e. Set the signature analyzer as follows:

Start:	Out (⎍)
Stop:	In (⎍)
Clock:	In (⎍)
Self-Test:	Out
Hold:	Out

f. Turn the 3497A on. Using the signature analyzer, take the data bus signatures in Table 8-A2-1.

8-A2-31. Free Run Test #1, ROM Select Decoder (U15) Signatures. If any of the data bus signatures are incorrect, check the signatures at U15 next. Move the Start input of the signature analyzer to TP SS0. Leave the rest of the inputs connected as in paragraph 8-A2-30. Take the signatures in Table 8-A2-2.

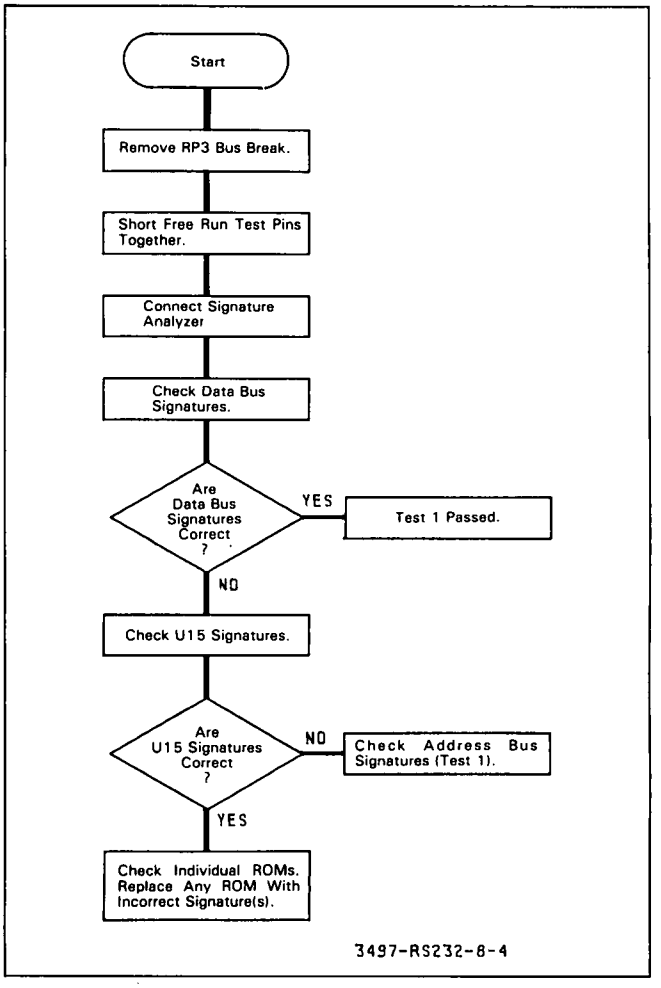


Figure 8-A2-2. Test #1, Free Run Test Flowchart

Table 8-A2-1. Test #1, Data Bus Signatures

+5V Signature: 5FU8			
Bus Break Pin Number	**Bus Bit**	**Signature**	**Notes**
1	0	0488	If all Data Bus Signatures are correct, the ROM portion of Test 1 passes and there is no need to check U15 or the individual ROMs. If any signature is incorrect, follow the flowchart and check U15.
2	1	9A45	
3	2	P37H	
4	3	197U	
5	4	16F6	
6	5	C01A	
7	6	2FU7	
8	7	64PF	

Table 8-A2-2. Test #1, U15 Signatures

+5V Signature: 0001		
Test Point	**Signature**	**Notes**
U15 Pin 1	0000	If these signatures are correct, check the individual ROMs. If any are incorrect, check the Address Bus signatures.
Pin 2	755U	
Pin 3	3827	
Pin 4	5FU8	
Pin 5	64HP	
Pin 6	29A6	
Pin 7	1181	

8-A2-32. Free Run Test #1, Address Bus Signatures. If any of the U15 signatures are incorrect, check the address bus signatures next. Leave the signature analyzer connected as in paragraph 8-A2-31. Take the signatures in Table 8-A2-3.

8-A2-33. Free Run Test #1, Individual ROM Signatures. If all of the U15 signatures are correct and all of the address bus signatures are correct, check the individual ROM signatures. Set-up the signature analyzer and take the ROM signatures as follows:

a. Signature Analyzer Set-up. Set-up as follows:

Start: In (⌝)
Stop: Out (⌟)
Clock: In (⌝)

b. Test A, U16 ROM Signature. Connect the signature analyzer as follows and take the signatures in Table 8-A2-4. If any signatures are wrong, replace U16.

Start: TP ROM 16 (Test Point next to U16)
Stop: TP ROM 16 (Test point next to U16)
Clock: TP CLK
Gnd: TP GND

Table 8-A2-3. Address Bus Signatures

+5V Signature: 0001		
Test Point	**Bus Bit**	**Signature**
U11 Pin 9	A0	5555
Pin 10	A1	CCCC
Pin 11	A2	7F7F
Pin 12	A3	5H21
Pin 13	A4	0AFA
Pin 14	A5	UPFH
Pin 15	A6	52F8
Pin 16	A7	HC89
Pin 17	A8	2H70
Pin 18	A9	HPP0
Pin 19	A10	1293
Pin 20	A11	HAP7
Pin 22	A12	3C96
Pin 23	A13	3827
Pin 24	A14	755U
Pin 25	A15	0001

Table 8-A2-4. U16 Signatures

+5V Signature: 1180	
Test Point	**Signature**
Bus Break Pin 1	U4AU
Pin 2	6UH3
Pin 3	04HH
Pin 4	2983
Pin 5	8P3F
Pin 6	U109
Pin 7	0A65
Pin 8	6520

c. Test B, U20 ROM Signature. Connect the signature analyzer as follows and take the signatures in Table 8-A2-5. If any signatures are wrong, replace U20.

Start: TP ROM 20 (Test Point close to U20)
Stop: TP ROM 20 (Test Point close to U20)
Clock: TP CLK
Gnd: TP GND

Table 8-A2-5. U20 Signatures

+5V Signature: 1180	
Test Point	**Signature**
Bus Break Pin 1	H0U5
Pin 2	4UH1
Pin 3	8963
Pin 4	U165
Pin 5	942C
Pin 6	C282
Pin 7	1602
Pin 8	6P5U

d. Test C, U24 ROM Signature. Connect the signature analyzer as follows and take the signatures in Table 8-A2-6. If any signatures are wrong, replace U24.

Start: TP ROM 24 (Test Point close to U24)
Stop: TP ROM 24 (Test Point close to U24)
Clock: TP CLK
Gnd: TP GND

Table 8-A2-6. U24 Signatures

+5V Signature: 1180	
Test Point	**Signature**
Bus Break Pin 1	HC1C
Pin 2	CF41
Pin 3	C27A
Pin 4	P668
Pin 5	U5A1
Pin 6	A663
Pin 7	UCU0
Pin 8	9CHA

8-A2-34. Test #1, Outguard Extender (3498A Interface) Test. This test checks the outguard extender circuitry. Take the signatures on the 24-pin J2 socket. Do the following:

a. Connect the signature analyzer as follows:

Start: TP SS0
Stop: TP SS0
Clock: TP CLK
Gnd: TP GND

b. Set the signature analyzer as follows:

Start: In (⎍)
Stop: Out (⎎)
Clock: In (⎍)

c. Using the signature analyzer, take the signatures in Table 8-A2-7. Replace the appropriate component if any signatures are wrong.

Table 8-A2-7. Outguard Extender Signatures

+5V Signature: 0001			
Test Point	**Signature**	**Test Point**	**Signature**
J2 Pin 1	0000	J2 Pin 13	2H70
Pin 2	----	Pin 14	HPP0
Pin 3	HC89	Pin 15	8P4P
Pin 4	5P18	Pin 16	0001 (+5V)
Pin 5	52F8	Pin 17	0001 (+5V)
Pin 6	UPFH	Pin 18	0001 (+5V)
Pin 7	0AFA	Pin 19	0001 (+5V)
Pin 8	5H21	Pin 20	0001 (+5V)
Pin 9	1920	Pin 21	0001 (+5V)
Pin 10	7F7F	Pin 22	0001 (+5V)
Pin 11	CCCC	Pin 23	0001 (+5V)
Pin 12	5555	Pin 24	0000 (GND)

8-A2-35. Test #1, Slot Select (U45), Extender Enable (U22, U26) Circuitry. Do the folowing:

a. Connect the signature analyzer as follows:

Start: TP SS0
Stop: TP SS0
Clock: TP CLK
Gnd: TP GND

b. Set the signature analyzer as follows:

Start: In (⎍)
Stop: Out (⎎)
Clock: In (⎍)

c. Using the signature analyzer, take the signatures in Tables 8-A2-8, 8-A2-9, and 8-A2-10. Replace the appropriate component if any signature is wrong.

Table 8-A2-8. U45 Signatures

+5V Signature: 0001			
Test Point	**Signature**	**Test Point**	**Signature**
U45 Pin 1	5H21	U45 Pin 9	1UHC
Pin 2	0AFA	Pin 10	CA59
Pin 3	UPFH	Pin 11	8295
Pin 4	0000 (GND)	Pin 12	F82H
Pin 5	0000 (GND)	Pin 13	04P6
Pin 6	0001 (+5V)	Pin 14	U68U
Pin 7	H9HA	Pin 15	F488
Pin 8	0000 (GND)	Pin 16	0001 (+5V)

Table 8-A2-9. U22 Signatures

+5V Signature: 0001			
Test Point	**Signature**	**Test Point**	**Signature**
U22 Pin 1	0001	U22 Pin 8	1921
Pin 2	5FU8	Pin 9	0001 (+5V)
Pin 3	0001	Pin 10	0001 (+5V)
Pin 4	0000	Pin 11	1920
Pin 5	0001 (+5V)	Pin 12	5FU9
Pin 6	0001	Pin 13	0001
Pin 7	0000 (GND)	Pin 14	0001 (+5V)

Table 8-A2-10. U26 Signatures

+5V Signature: 0001	
Test Point	**Signature**
U26 Pin 1	5P18
Pin 2	8P4P
Pin 3	H057
Pin 4	0001 (+5V)
Pin 5	5FU9
Pin 6	5FU9
Pin 7	0000 (GND)

Table 8-A2-11. I/O Address Decoders Signatures

+5V Signature: 0001					
Test Point	**Signature**	**Test Point**	**Signature**	**Test Point**	**Signature**
U31 Pin 1	1293	U32 Pin 1	1293	U33 Pin 1	1293
Pin 2	HAP7	Pin 2	HAP7	Pin 2	HAP7
Pin 3	3C96	Pin 3	3C96	Pin 3	3C96
Pin 4	5FU8	Pin 4	29A6	Pin 4	64HP
Pin 5	0000	Pin 5	0000	Pin 5	0000
Pin 6	0001 (+5V)	Pin 6	0001 (+5V)	Pin 6	0001 (+5V)
Pin 7	A68C	Pin 7	942F	Pin 7	1920
Pin 8	0000 (GND)	Pin 8	0000 (GND)	Pin 8	0000 (GND)
Pin 9	A277	Pin 9	F042	Pin 9	C34C
Pin 10	9840	Pin 10	131H	Pin 10	597C
Pin 11	8P4P	Pin 11	85H4	Pin 11	UA87
Pin 12	5P18	Pin 12	5969	Pin 12	4154
Pin 13	2828	Pin 13	0PC5	Pin 13	960F
Pin 14	02H7	Pin 14	270P	Pin 14	84AF
Pin 15	3APF	Pin 15	9CH2	Pin 15	3PCF
Pin 16	0001 (+5V)	Pin 16	0001 (+5V)	Pin 16	0001 (+5V)

8-A2-36. Test #1, I/O Address Decoders (U31, U32, and U33) Circuitry. Do the following:

a. Connect the signature analyzer as follows:

Start: TP SS0
Stop: TP SS0
Clock: TP CLK
Gnd: TP GND

b. Set the signature analyzer as follows:

Start: In (⌝)
Stop: Out (⌟)
Clock: In (⌝)

c. Using the signature analyzer, take the signatures in Table 8-A2-11. Replace the appropriate component if any signature is wrong.

8-A2-37. RAM Test (Test #2)

8-A2-38. This test has two parts, 2A and 2B. Test 2B should be run only if Test 2A fails. In these tests, unique bit patterns are written to each RAM location, exercising both the low and high states. These tests, therefore, check the RAM and that the microprocessor is writing to the RAM correctly.

NOTE

To run any portion of Test #2, switch segment 1 of switch S1 must be in the "1" (left) position. This is outlined in step d of Test 2A and is applicable for Tests 2A and 2B.

8-A2-39. Test 2A. Do the following:

a. Turn the 3497A off.

b. Replace bus break RP3 (if it was removed in Test #1).

c. Remove the jumper(s) or clip lead(s) that was used in Test #1.

d. Refer to Figure 8-A2-3 and move switch segment 1 of switch S1 to the "1" (left) position.

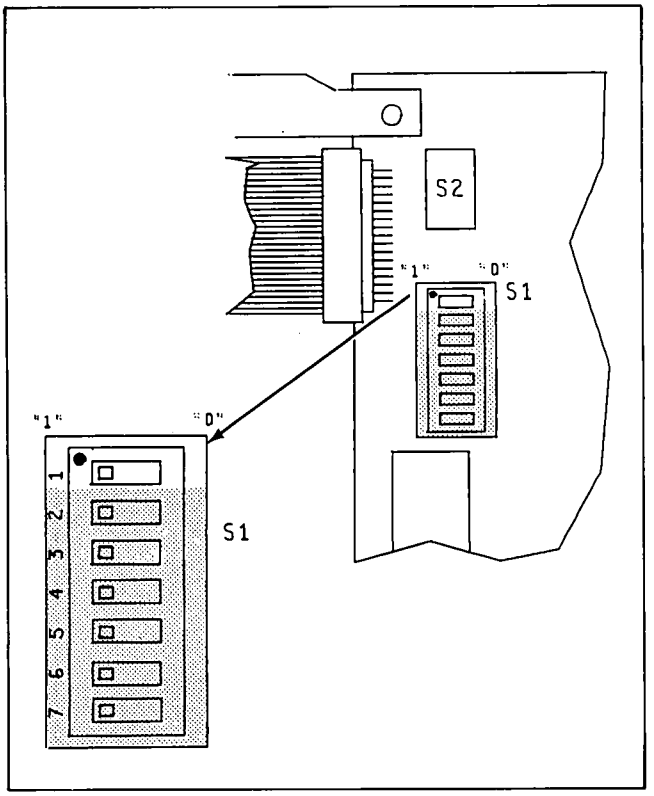


Figure 8-A2-3. Switch Setting for Test #2

e. Connect the signature analyzer as follows:

Start:	TP SS0
Stop:	TP SS0
Clock:	TP CLK
Gnd:	TP GND

f. Set the signature analyzer as follows:

Start:	In (⎍)
Stop:	In (⎍)
Clock:	In (⎍)

g. Turn the 3497A on.

h. Momentarily connect TP SA (next to U11) to ground (TP GND). This places the outguard board into the RAM SA mode.

i. If the +5V signature is "39CC", the test passes. Any other signature (with the signature analyzer gating), the test fails. Proceed to Test 2B. If the signature analyzer is not gating, try to do Test #1 again.

8-A2-40. Test 2B. Perform this test only if Test 2A has been performed and Test 2A failed. Do the following:

a. Make sure steps b, c, and d of Test 2A (paragraph 8-A2-39) have been performed.

b. Connect the signature analyzer as follows.

Start:	TP SS2
Stop:	U31 pin 9
Clock:	TP CLK
Gnd:	TP GND

c. Set the signature analyzer to the same configuration as in Test 2A (see paragraph 8-A2-39, step f).

d. Momentarily connect TP SH to ground. Using the signature analyzer, take the signatures in Table 8-A2-12. Replace the appropriate component if any signature is wrong.

Table 8-A2-12. RAM Signatures

+5V Signature: 2526			
Test Point	**Signature**	**Test Point**	**Signature**
U31 Pin 1	FH1P	U28 Pin 8	5F6C
Pin 2	1C62	Pin 9	794H
Pin 3	F74A		
Pin 4	5210	U30 Pin 9	7U10
Pin 5	06A4	Pin 10	65P6
Pin 6	2526 (+5V)	Pin 11	7127
Pin 15	794H	Pin 13	2H64
		Pin 14	C5F6
U18 Pin 8	794H	Pin 15	A1P8
Pin 9	5F6C	Pin 16	95A1
Pin 10	CP63	Pin 17	72U8

8-A2-41. Crossguard Test (Test #3)

8-A2-42. There are seven tests associated with the crossguard test: 3A, 3B, 3C, 3D, 3E, 3F, and 3G. These tests write nine different bit patterns to the inguard and monitor the bit patterns echoed back via the crossguard logic. A failure can be isolated to the inguard or outguard logic. If there is a failure on the outguard side, it can be further isolated to the outguard transmitter or receiver. To avoid confusion and taking unnecessary signatures, it is important to use Schematic AB1 and follow the Test #3 flowchart shown in Figure 8-A2-4. It is important to be able to identify the transmitter and receiver circuitry in the crossguard logic.

8-A2-43. Test 3A. This test checks the outguard transmitter addressing. Do the following:

a. Connect the signature analyzer as follows:

Start:	TP SS2
Stop:	TP SS2
Clock:	TP CLK
Gnd:	TP GND

b. Set the signature analyzer as follows:

Start:	In (⎍)
Stop:	In (⎍)
Clock:	In (⎍)

c. Refer to Figure 8-A2-5 and move switch segment 2 of switch S1 to the "1" (left) position. Make sure switch segment 1 is in the "0" (right) position.

NOTE

To run any portion of Test #3, switch segment 2 of switch S1 must be in the "1" (left) position. This is outlined in step c of Test 3A and is applicable for Tests 3A through 3G.

d. Momentarily connect TP SA to ground (TP GND).

e. To avoid confusion, refer to the flowchart for the following steps. First, check the signature at pin 9 of U31, which should be "A3PC". If the signature is correct, proceed with step f. If the signature is incorrect, continue with step h.

f. Wire the pulse transformer "exactly" as shown in Figure 8-A2-6. The pulse transformers are located on the power supply board (see paragraph 8-24 for procedure to gain access to the transformers).

g. Check the signature at pin 9 of U37, which should be "5FA7". If both the U31 and U37 signatures are correct, Test 3A passes and there is no need to go to Test 3B, 3C, etc. If Test 3A passes, make sure to rewire the pulse transformers as shown in Figure 8-A2-7. If

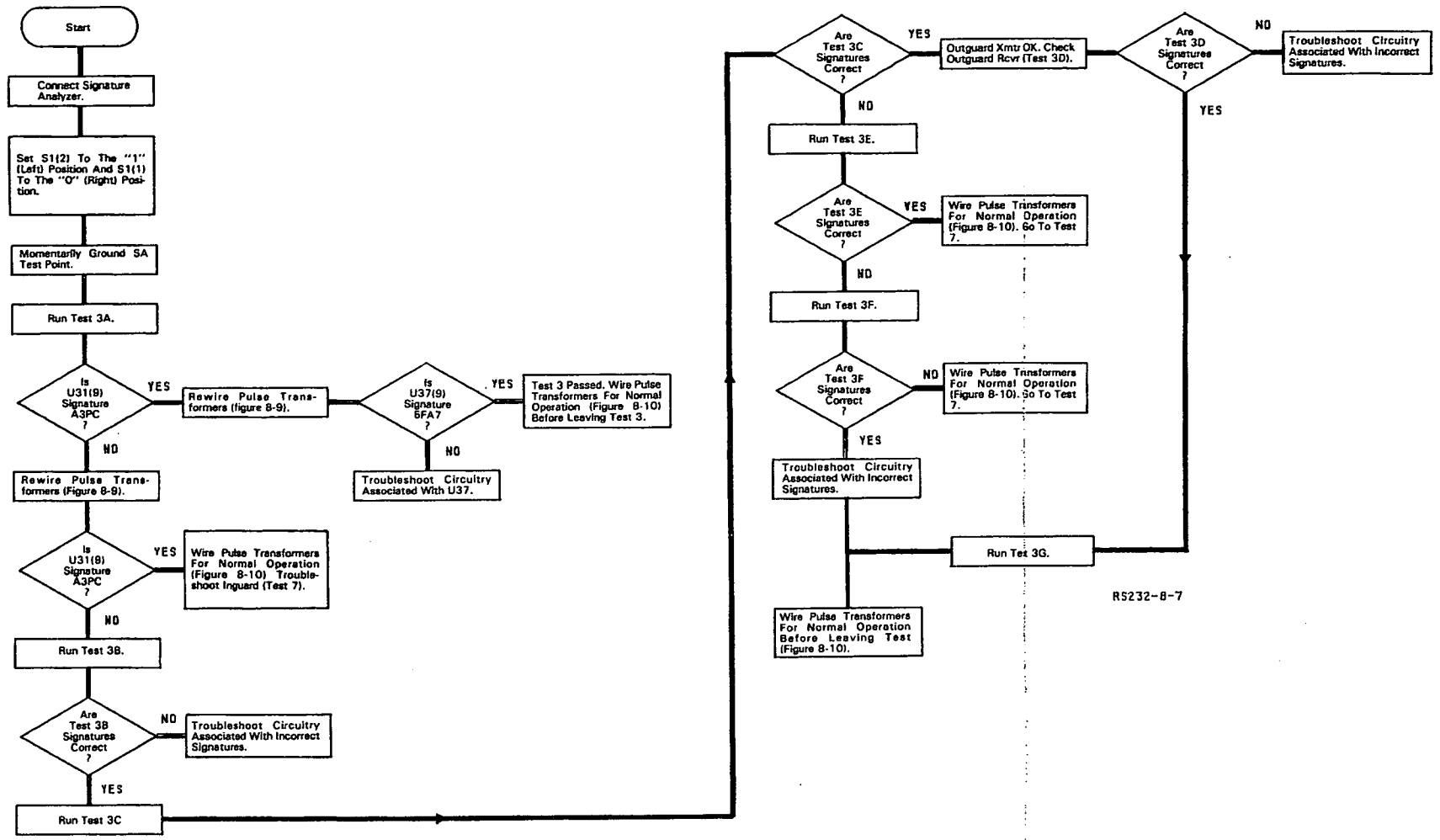


Figure 8A2-4. Test #3, Crossguard Test Flowchart

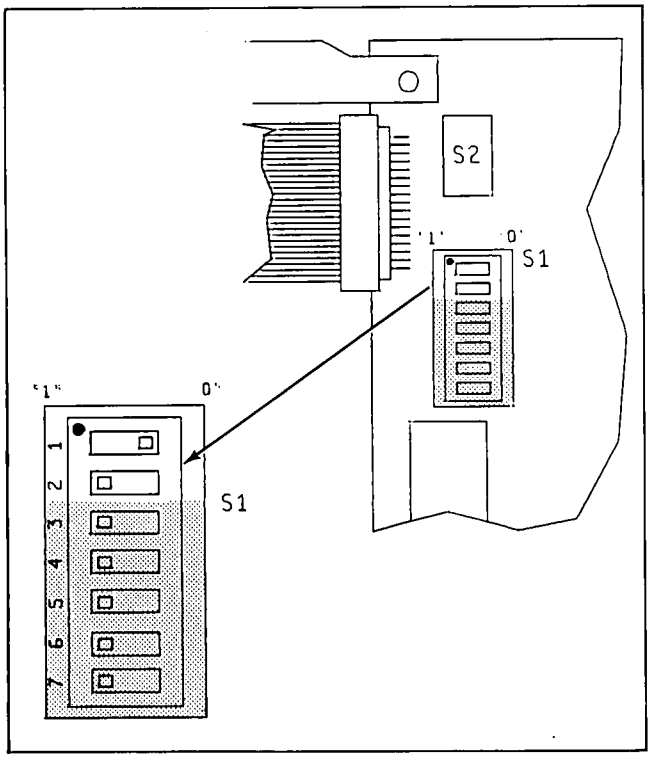


Figure 8-A2-5. Switch Setting for Test #3

the signature at pin 9 of U37 is wrong, check U37 and associated circuitry.

h. Perform this step only if the signature at pin 9 of U31 is wrong. Make sure the pulse transformer is wired as shown in Figure 8-A2-6; then proceed with the next step.

i. Check U31 pin 9 again. If the signature is "A3PC", rewire the pulse transformers as shown in Figure 8-A2-7, and then troubleshoot the inguard section (Test #7). If the signature is other than "A3PC", proceed with Test 3B.

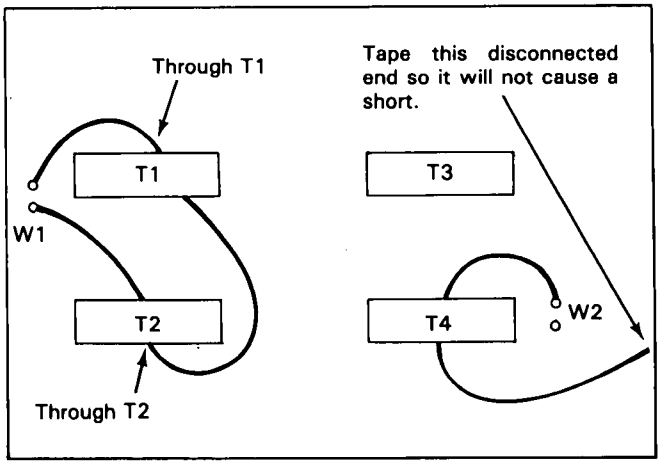


Figure 8-A2-6. Test #3, Pulse Transformer Wiring

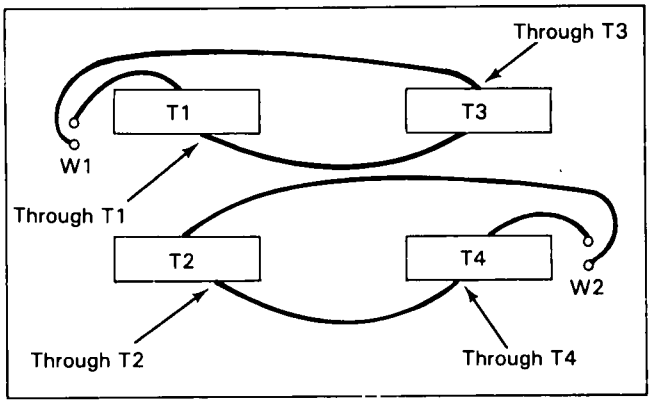


Figure 8-A2-7. Pulse Transformer Wiring for Normal Operation

8-A2-44. Test 3B. Perform this test only if the signature at pin 9 of U31 (see Test 3A) is NOT "A3PC". If the Test 3B signatures are correct, proceed with Test 3C. Do the following:

a. Set up and connect the signature analyzer as given in paragraph 8-A2-42 steps a and b.

b. Momentarily connect TP SA to ground. Using the signature analyzer, take the signatures in Table 8-A2-13. Replace the appropriate component if any signature is wrong.

8-A2-45. Test 3C. Perform this test only if all signatures of Test 3B are correct. Do the following:

a. Connect the signature analyzer as follows:

Start:	U21 pin 6
Stop:	U21 pin 6
Clock:	U36 pin 1

Table 8-A2-13. Test 3B Signatures

NOTE

The signatures in this table take about 1 second to stabilize

+5V Signature: A3PC

Test Point	Signature	Test Point	Signature
U43 Pin 1	F47C	U28 Pin 1	7852
Pin 2	7852	Pin 2	HCC9
Pin 3	A3PC	Pin 12	7852
Pin 4	A3PC (+5V)	Pin 13	HCC9
Pin 5	HCC9		
Pin 6	7852	U39 Pin 5	7852 (probe tip off)
		Pin 6	HCC9
U36 Pin 8	6790	Pin 8	6790
Pin 9	6C45	Pin 9	F47C
Pin 10	AU3P	Pin 12	F8AP
Pin 11	7H89	Pin 13	6C45
Pin 12	80C1		
Pin 13	6C45		

b. Set the signature analyzer as follows:

Start: In (⎍)
Stop: Out (⎍)
Clock: In (⎍)

c. Momentarily connect TP SA to ground. Using the signature analyzer, take the signatures in Table 8-A2-14. Replace the appropriate component if any signature is wrong.

Table 8-A2-14. Test 3C Signatures

NOTE *The signatures in this table take about 1 second to stabilize*		
+5V Signature: 593A		
Test Point	**Signature**	**Notes**
U46 Pin 3 Pin 8	47AF 1P96	If the U46 signatures are correct the Outguard Xmtr is OK, in which case you should proceed with Test 3D. If they are not correct, skip Test 3D and proceed with Test 3E.

8-A2-46. Test 3D. Perform this test only if all signatures of Test 3C are correct. Do the following:

a. Set up and connect the signature analyzer as given in paragraph 8-A2-44 steps a and b.

b. Momentarily connect TP SA to ground. Using the signature analyzer, take the signatures in Table 8-A2-15. Replace the appropriate component if any signature is wrong.

Table 8-A2-15. Test 3D Signatures

NOTE *The signatures in this table take about 1 second to stabilize*		
+5V Signature: 593A		
Test Point	**Signature**	**Notes**
U50 Pin 1 U37 Pin 9	47AF 38U7	If the U50 Pin 1 signature is correct, check U44 in Test 3G.

8-A2-47. Test 3E. This test checks U35, U40, and U42 and should only be performed if the U46 signatures in Test 3C are wrong. Do the following:

a. Set up and connect the signature analyzer as given in paragraph 8-A2-44 steps a and b.

b. Momentarily connect TP SA to ground. Using the signature analyzer, take the signatures in Table 8-A2-16. Replace the appropriate component if any signature is wrong.

Table 8-A2-16. Test 3E Signatures

NOTE *The signatures in this table take about 1 second to stabilize*		
+5V Signature: 593A		
Test Point	**Signature**	**Notes**
U35 Pin 11 Pin 14 U40 Pin 9 U42 Pin 5 Pin 6	64F7 14AC 00H0 47AF 1P96	If these signatures are correct, proceed to Test 7 and troubleshoot the outguard transmitter. If these signatures are incorrect, run Test 3F.

8-A2-48. Test 3F. Perform this test only if the signatures of Test 3E are correct. Do the following:

a. Set the signature analyzer as follows:

Start: U21 pin 6
Stop: U21 pin 6
Clock: TP R/W (Test Point next to U19)
Gnd: TP GND

b. Set the signature analyzer as follows:

Start: In (⎍)
Stop: Out (⎍)
Clock: Out (⎍)

c. Momentarily connect TP SA to ground. Using the signature analyzer, take the signatures in Table 8-A2-17. Replace the appropriate component if any signature is wrong.

Table 8-A2-17. Test 3F Signatures

NOTE *The signatures in this table take about 1 second to stabilize*			
+5V Signature: U399			
Test Point	**Signature**	**Test Point**	**Signature**
U34 Pin 1	U399	U34 Pin 11	5H1F
Pin 2	583P	Pin 12	5H34
Pin 3	HF5P	Pin 13	5H95
Pin 4	7H46	Pin 14	5U11
Pin 5	5500	Pin 15	5500
Pin 6	5U11	Pin 16	7H46
Pin 7	5H95	Pin 17	HF5P
Pin 8	5H34	Pin 18	583P
Pin 9	5H1F	Pin 19	0000
Pin 10	0000 (GND)		

8-A2-49. Test 3G. Perform this test only if the signatures of Test 3F are correct. Do the following:

a. Connect the signature analyzer as follows:

Start:	U21 pin 6
Stop:	U21 pin 6
Clock:	U44 pin 1
Gnd:	TP GND

b. Set the signature analyzer as follows:

Start:	In (⌝)
Stop:	Out (⌟)
Clock:	Out (⌟)

c. Momentarily connect TP SA to ground. Using the signature analyzer, take the signatures in Table 8-A2-18. Replace the appropriate component if any signature is wrong.

Table 8-A2-18. Test 3G Signatures

NOTE

The signatures in this table take about 1 second to stabilize

+5V Signature: 00UP

Test Point	Signature	Test Point	Signature
U44 Pin 1	0000	U44 Pin 10	0000 (GND)
Pin 2	0081	Pin 11	0008
Pin 3	0081	Pin 12	0008
Pin 4	0040	Pin 13	0004
Pin 5	0040	Pin 14	0004
Pin 6	0020	Pin 15	0002
Pin 7	0020	Pin 16	0002
Pin 8	0010	Pin 17	0001
Pin 9	0010	Pin 18	0001

NOTE

Before exiting Test #3, make sure the pulse transformers are wired for normal operation, as shown in Figure 8-A2-7.

8-A2-50. Timer/Pacer Test (Test #4)

8-A2-51. General. This test is in four parts: 4A, 4B, 4C, and 4D. In the tests, 256 bit patterns are written to the timer/pacer assembly and then read back. The SST Test Point on the timer/pacer board must be grounded for these tests so that data paths can be verified in both directions (to and from timer/pacer circuitry). When the test is enabled, the timer microcomputer is held in a reset state and will not interface with the test. The signature on pin 9 of U39 shows the pass/fail condition. A flowchart of Test 4 is in Figure 8-A2-8. Unless otherwise noted, refer to Schematic A3 when doing the tests.

NOTE

To run Test #4, switch segment 3 of switch S1 must be in the "1" (left) position. Also, switch segment 1 and 2 must be in the "0" (right) position. This procedure is outlined in step c of paragraph 8-A2-51 and is applicable for Test 4A, 4B, 4C, and 4D.

8-A2-52. In the following steps, the signature at pin 9 of U31 is verified. If this signature is correct, check the signature on U3 (on the timer/pacer board) to make sure that the addressing is correct. If pin 9 of U31 and the U3 signatures are correct, Test #4 passes. Do the following:

a. Connect the signature analyzer as follows:

Start:	TP SS2
Stop:	TP SS2
Clock:	TP CLK
Gnd:	TP GND

b. Set the signature analyzer as follows:

Start:	In (⌝)
Stop:	In (⌝)
Clock:	In (⌝)

c. Refer to Figure 8-A2-9 and move switch segment 3 of switch S1 to the "1" (left) position. Make sure switch segments "1" and "2" are in the "0" (right) position.

d. Turn the 3497A off.

e. Connect TP SST (on the timer/pacer board) to ground.

f. Turn the 3497A on.

g. Momentarily connect TP SA (on the outguard logic board) to ground (TP GND).

h. Check the signature at pin 9 of U31. If the signature is "5AC8", proceed with step i. If NOT "5ACA", continue with step j.

i. Perform this step only if the signature at pin 9 of U31 is "5AC8". In this step, the U3 signatures (on the timer/pacer board) will be verified to make sure the addressing is correct. Refer to Table 8-A2-19 for the U3 signatures. If the U3 signatures are correct, Test #4 passes and there is no need to continue further. If the test passes, turn the 3497A off and remove the clip lead from TP SST. If any U3 signatures are wrong, try replacing U3.

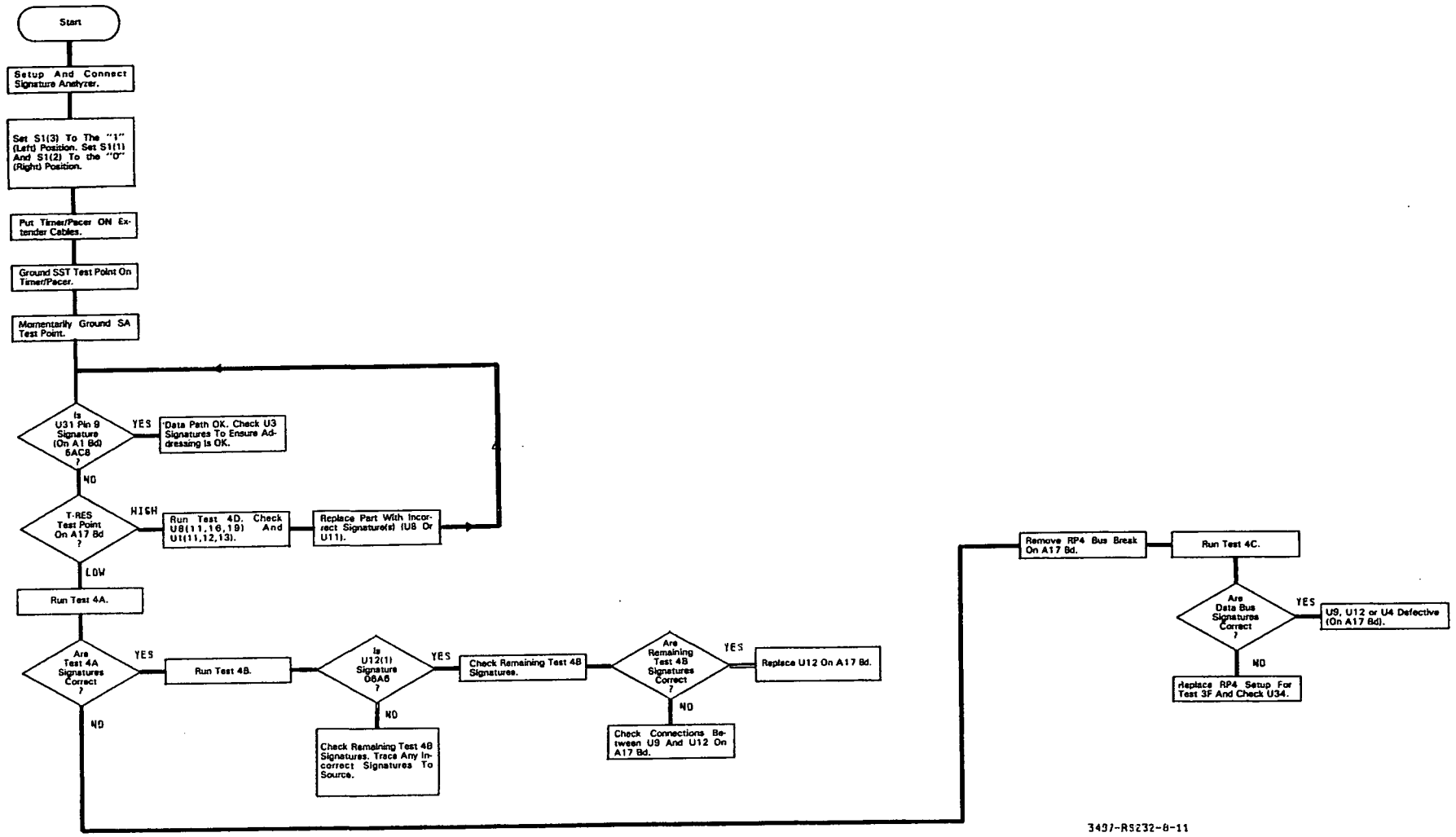


Figure 8-A2-8. Test #4, Timer/Pacer Test Flowchart

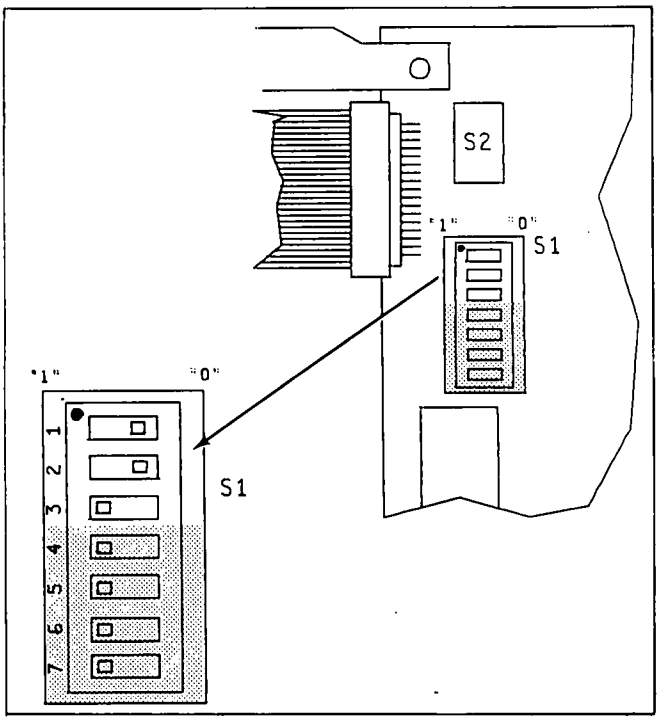


Figure 8-A2-9. Switch Setting for Test #4

j. Perform this step if the signature at pin 9 of U31 is NOT "5AC8". In this step, the signatures at TP T-RES on the timer/pacer board is checked. If the signature is "0000", continue with Test 4A. If the signature is "5AC8", go to Test 4D (paragraph 8-A2-55).

8-A2-53. Test 4A. This test should be performed if the signature at TP T-RES is "0000". In this test, the U9 (on the timer/pacer board) signatures are checked. If the U9 signatures are correct, continue with Test 4B. If any signatures are wrong, continue with Test 4C. To perform Test 4A, leave the signature analyzer setup, and connected as given in Test #4 (see paragraph 8-A2-51). The U9 signatures are listed in Table 8-A2-20.

Table 8-A2-19. U3 Signatures

+ 5V Signature: 5AC8	
Test Point on Timer/Pacer	**Signature**
U3 Pin 3	P5F8
Pin 6	8812
Pin 7	0000 (GND)
Pin 8	H106
Pin 10	6392
Pin 12	5AC8 (+5V)
Pin 13	P5F8
Pin 14	5AC8 (+5V)

Table 8-A2-20. Test 4A Signatures

+ 5V Signature: 5AC8	
Test Point	**Signature**
U9 Pin 1	0000 (GND)
Pin 2	FUP8
Pin 5	83H2
Pin 6	C871
Pin 9	29CF
Pin 11	P5F8
Pin 12	0A16
Pin 15	PU11
Pin 16	0FUU
Pin 19	CC37

8-A2-54. Test 4B. This test should only be performed if the signatures in Test #4 are correct. In Test 4A, U12 on the timer/pacer board is checked. The first signature checked is at pin 1 of U12. If the signature is "06A6", replace U12. If other than "06A6", check the other U12 signatures. If any other U12 signature is wrong, refer to Schematic A3 and trace back to its source. To perform Test 4B, leave the signature analyzer setup, and connected as given in Test #4 (see paragraph 8-A2-51). The U12 signatures are listed in Table 8-A2-21.

Table 8-A2-21. Test 4B Signatures

+ 5V Signature: 5AC8		
Test Point	**Signature**	**Notes**
U12 Pin 1	06A6	If U12 Pin 1 is 06A6, replace U12. If it is NOT 06A6, check the remaining signatures. If any signature is incorrect use the schematics and trace it back to its source.
Pin 2	FUP8	
Pin 4	83H2	
Pin 6	C871	
Pin 8	29CF	
Pin 12	0A16	
Pin 14	PU11	
Pin 16	0FUU	
Pin 18	CC37	

8-A2-55. Test 4C. Do this test only if one or more of the U9 signatures taken in Test 4A are wrong. This can be caused by the following:

a. U9 on the timer/pacer board is defective.

b. U12 on the timer/pacer board is defective.

c. U34 and/or the buffered data bus on the outguard logic board are defective.

d. U4 on the timer/pacer board is defective.

To isolate the failure, remove the RP4 Bus Break (on the timer/pacer board) and take the data bus signatures. (Make sure that RP4 is not confused with the bus break, RP3, on the outguard logic board.) After RP4 is re-

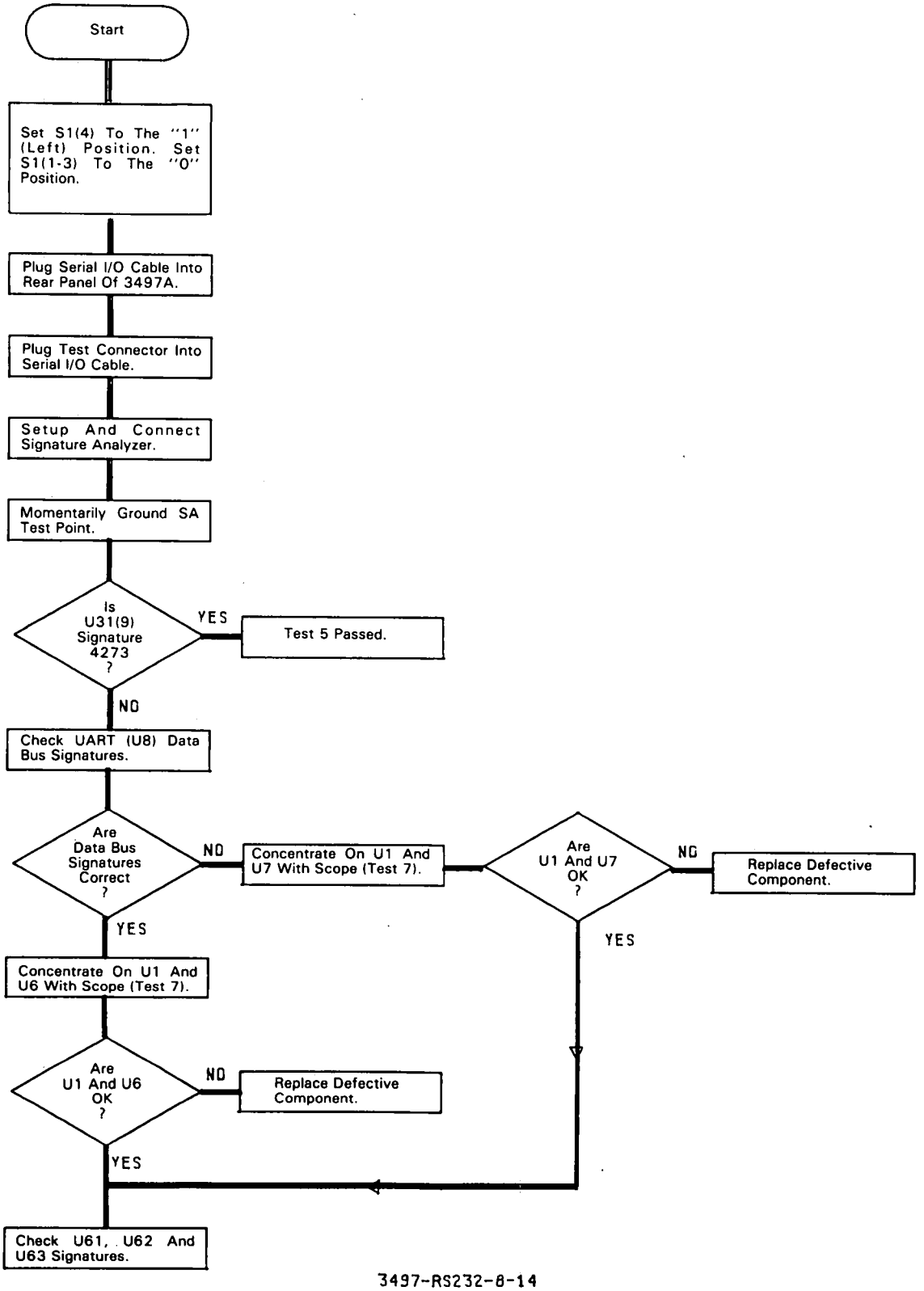


Figure 8-A2-10. Test #5, Serial I/O and Cable Test Flowchart

moved, the signature analyzer setup in this test is the same as in Test #4 (see paragraph 8-A2-51). The only exception is that a 4.7K ohm pull-up resistor needs to be connected between +5V and the signature analyzer probe tip. If the data bus signatures are correct, U9, U12, or U4 may be defective. If any signatures are wrong, check U34 (see Test #3) and associated circuitry. The data bus signatures are listed in Table 8-A2-22.

Table 8-A2-22. Test 4C, Data Bus Signatures

+5V Signature: 5AC8		
Test Point	**Data Bus Bit**	**Signature**
RP4 Pin 1	Bit 0	UA4P
Pin 2	1	4AC4
Pin 3	2	18P5
Pin 4	3	24H1
Pin 5	4	078H
Pin 6	5	C8AP
Pin 7	6	U589
Pin 8	7	49PP
IMPORTANT		
Replace RP4 after running Test 4C		

8-A2-56. Test 4D. Perform this test only if the signature at TP T-RES is "5AC8". This test troublshoots the pacer circuitry. In the test, the U8, U11, and U1D signatures on the timer/pacer board are verified. The first U8 signatures checked are at pins 11, 16, and 19. The signature analyzer is setup and connected the same as in Test #4 (see paragraph 8-A2-51). The U8, U11, and U1D signatures are listed in Table 8-A2-23.

Table 8-A2-23. Test 4D Signatures

+5V Signature: 5AC8			
Test Point	**Signature**	**Test Point**	**Signature**
U8 Pin 1	5AC8 (+5V)	U1 Pin 12	5C27
Pin 2	99A8	Pin 13	5C27
Pin 5	8CA9		
Pin 6	UA01	U11 Pin 1	5AC8 (+5V)
Pin 9	F97U	Pin 2	1612
Pin 11	763C	Pin 5	1473
Pin 12	FH07	Pin 6	45AP
Pin 15	1H80	Pin 9	C920
Pin 16	5C27	Pin 11	8U47
Pin 19	5C27	Pin 12	483H
		Pin 15	4715
U1 Pin 11	0000 (GND)	Pin 16	U00A
		Pin 19	FHC4

8-A2-57. Serial I/O and Cable Test (Test #5)

8-A2-58. Test #5 checks the data to and from the UART (U8) by transferring 1's across the data bus. To run this test, the test connector (-hp- Part Number: 1251-6625) must be used. The connector ties the TX and RX data lines together and the modem output to the modem input lines. The signature at pin 9 of U31 shows a pass/fail condition. The Test #5 flowchart is in Figure 8-A2-10. Unless otherwise noted, refer to Schematic A2 for troubleshooting.

8-A2-59. To perform Test #5, do the following:

a. Refer to Figure 8-A2-11 and move switch segment 4 of switch S1 to the "1" (left) position. Make sure switch segments 1, 2, and 3 are in the "0" (right) position.

b. Make sure the Serial I/O cable (-hp- Part Number: 13222-60005) is plugged into the 3497A's rear panel.

c. Plug the test connector into the RS-232C connector on the end of the Serial I/O cable. This connector ties the lines together, as shown in Figure 8-A2-12.

d. Connect the signature analyzer as follows:

Start:	TP SS2
Stop:	TP SS2
Clock:	TP CLK
Gnd:	TP GND

e. Set the signature analyzer as follows:

Start:	In (⌥)
Stop:	In (⌥)
Clock:	In (⌥)

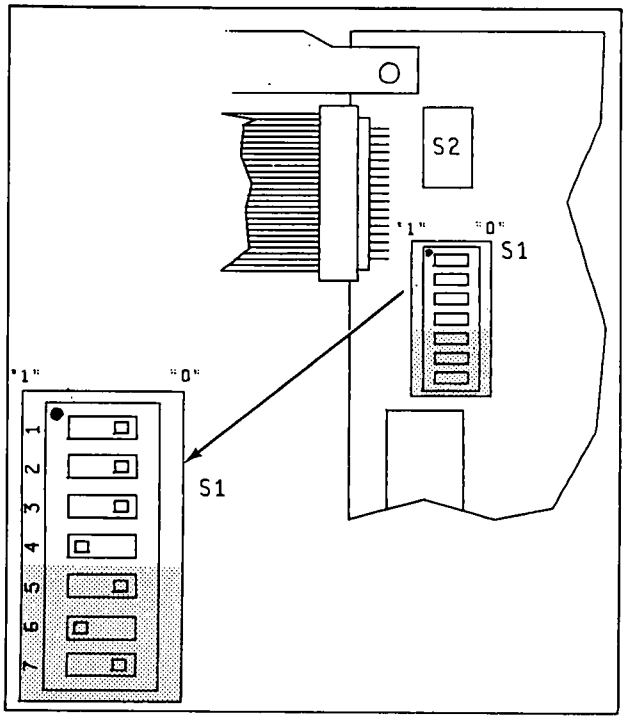


Figure 8-A2-11. Switch Setting for Test #5

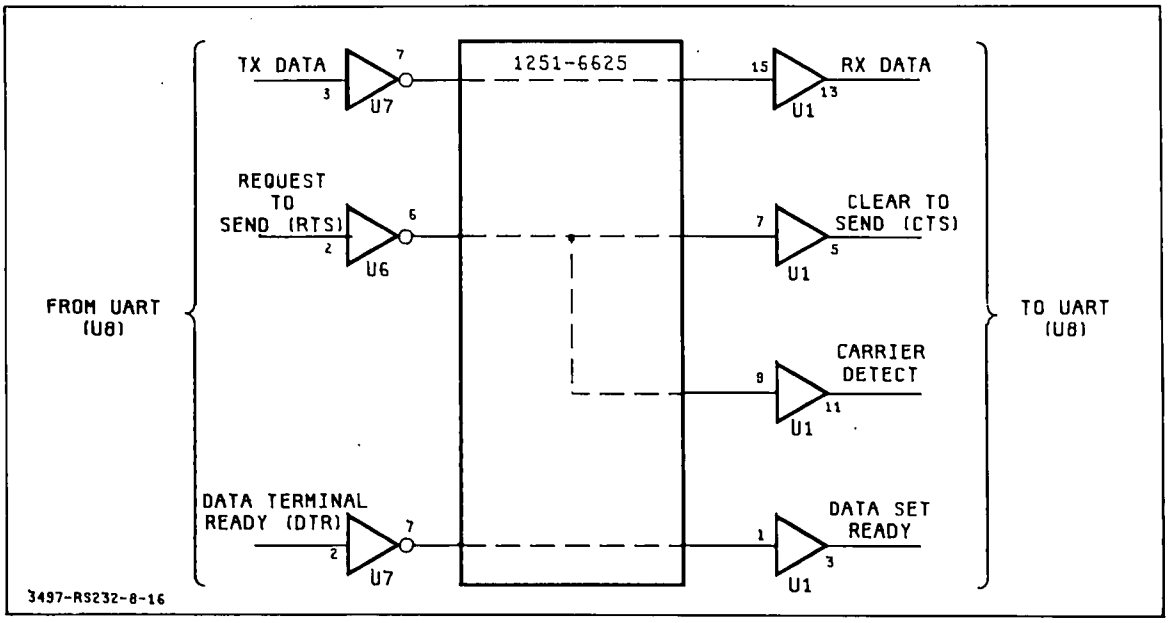


Figure 8-A2-12. Test Connector Schematic

f. Momentarily connect TP SA to ground.

g. Check the signature at pin 9 of U31. If this signature is "4173" (and the signature analyzer gate is flashing), Test #5 passes. If the signature is wrong, refer to the flowchart (see Figure 8-A2-10) and continue with paragraph 8-A2-59. The signatures for Test #5 are listed in Table 8-A2-24.

8-A2-60. Check the data bus signatures at U8 pins 1 through 8 first, as noted on the flowchart. If the data bus signatures are correct, check U1 and U6. If any of the data bus signatures are wrong, check U1 and U7. U1 is the IC containing the serial receivers while U6 ad U7 are the serial drivers. The receivers convert the incoming positive and negative voltage levels (from the serial bus) to TTL levels. The drivers convert the outgoing UART signals from TTL to positive and negative voltage levels required by the serial bus. The nature of this level shifting function coupled with the fact that the UART is performing parallel-to-serial and serial-to-parallel data conversions, cause the TTL side of U1, U6, and U7 to generate unstable signatures. Therefore, there are no signatures listed for these ICs. The best way to troubleshoot U1, U6, or U7 is to use an oscilloscope and trace signals exiting the UART, through the drivers, and back to the receivers. This loop around configuration exists as a result of the test connector. When tracing these signals, look for transitions and proper voltage levels (TTL or RS-232C).

8-A2-61. Front Panel Test (Test #6)

8-A2-62. Test #6 has two parts to it: 6A and 6B. Test 6A is for the display and Test 6B is for the keyboard. Test 6A exercises all display segments for a visual operational verification. If the display appears incorrect, the signatures on the data latches, buffers, and drivers are then checked. Test 6B provides the capability to read back the key code of a depressed key and check the one shots used on the front panel board. Unless otherwise noted, refer to Schematic A4 for the tests.

NOTE

To run any portion of the Test #6, switch segment 5 of switch S1 must be in the "0" (left) position and switch segments 1 through 4 must be in the "1" (right) position. This procedure is outlined in step a of Test 6A and is applicable for Test 6B.

8-A2-63. Test 6A, Display Test. Do the following:

a. Refer to Figure 8-A2-13 and move switch segment 5 of switch S1 to the "1" (left) position. Make sure switch segments 1 through 4 are in the "0" (right) position.

b. Momentarily connect TP SA to ground (TP GND) and observe the 3497A display. The display should appear as follows:

1. The voltmeter display should have a steady display of: "-.2.3.4.5.6.7".

2. All segments of the three 7 segment LEDs and all remaining displays and annunciators should be flashing.

Table 8-A2-24. Test #5 Signatures

NOTE

The signatures in the table that have an asterisk (*) after them should be checked first. These signatures are valid only if the UART is transmitting and receiving data correctly.

+5 V Signature: 4273

Test Point	Signature	Test Point	Signature
U8 Pin 1	49PA*	U61 Pin 3	C206
Pin 2	7128*	Pin 4	C206
Pin 3	HCH2*	Pin 5	0000
Pin 4	06AH*	Pin 6	4273
Pin 5	967A*	Pin 7	0000 (GND)
Pin 6	139F*	Pin 8	4273
Pin 7	P439*	Pin 9	0000
Pin 8	0436*	Pin 10	4F1H
Pin 9	0UU8	Pin 11	0000 (GND)
Pin 10	Unstable	Pin 12	4273 (+5V)
Pin 11	Unstable	Pin 13	4273 (+5V)
Pin 12	4273	Pin 14	4273 (+5V)
Pin 13	4273		
Pin 14	U075	U62 Pin 1	4F1H
Pin 15	0UU8	Pin 2	U23P
Pin 16	0000	Pin 3	U075
Pin 17	4273	Pin 4	Unstable
Pin 18	4273	Pin 5	Unstable
Pin 19	0000 (GND)	Pin 6	Unstable
Pin 20	0000 (GND)	Pin 7	0000 (GND)
Pin 21	4273	Pin 8	4273 (+5V)
Pin 22	U23P	Pin 9	0000 (GND)
Pin 23	CF68	Pin 10	0000 (GND)
Pin 24	C206	Pin 11	4273 (+5V)
Pin 25	0000 (GND)	Pin 12	0000 (GND)
Pin 26	FAH9	Pin 13	0000 (GND)
Pin 27	P828	Pin 14	4273 (+5V)
Pin 28	5U68		
Pin 29	4273 (+5V)	U63 Pin 1	4273
Pin 30	4273 (+5V)	Pin 2	4273 (+5V)
Pin 31	4273 (+5V)	Pin 3	0000
Pin 32	8PP2	Pin 4	4273 (+5V)
Pin 33	8PP2	Pin 5	4273
Pin 34	4273 (+5V)	Pin 6	0000
Pin 35	0000 (GND)	Pin 7	0000 (GND)
Pin 36	Unstable	Pin 8	4273
Pin 37	Unstable	Pin 9	0000
Pin 38	Unstable	Pin 10	4273 (+5V)
Pin 39	4273 (+5V)	Pin 11	0000
Pin 40	4273 (+5V)	Pin 12	4273
		Pin 13	0000
U61 Pin 1	4273	Pin 14	4273 (+5V)
Pin 2	U075		

c. If the display is proper, there is no need to proceed further with Test 6A. If it does not appear proper, proceed with the following steps.

d. Connect the signature analyzer as follows:

Start: TP SS2
Stop: U31 pin 9
Clock: TP CLK
Gnd: TP GND

e. Set the signature analyzer as follows:

Start: In (⎍)
Stop: In (⎍)
Clock: In (⎍)

f. All Test 6A signatures are taken on the front panel board. The signatures are located in Table 8-A2-25. If any signatures are wrong, replace the appropriate component.

8-A2-64. Test 6B, Keyboard Test. Do the following:

8-A2-65. In Test 6B, the twenty 3497A front panel keys (0 through 19) are given numerical assignments as shown in Figure 8-A2-14. Notice that the assignments are not the same as how the keys are actually labeled. To avoid confusion, refer back to Figure 8-A2-14 as step e in paragraph 8-A2-65 is performed.

8-A2-66. The U14 test points (see Table 8-A2-26) need only be checked for a high (+5V) or low (ground) level. This does not require a signature analyzer. If this is the case, skip the following steps a and b and go to step c. To perform the test using a signature analyzer, do all of the following steps.

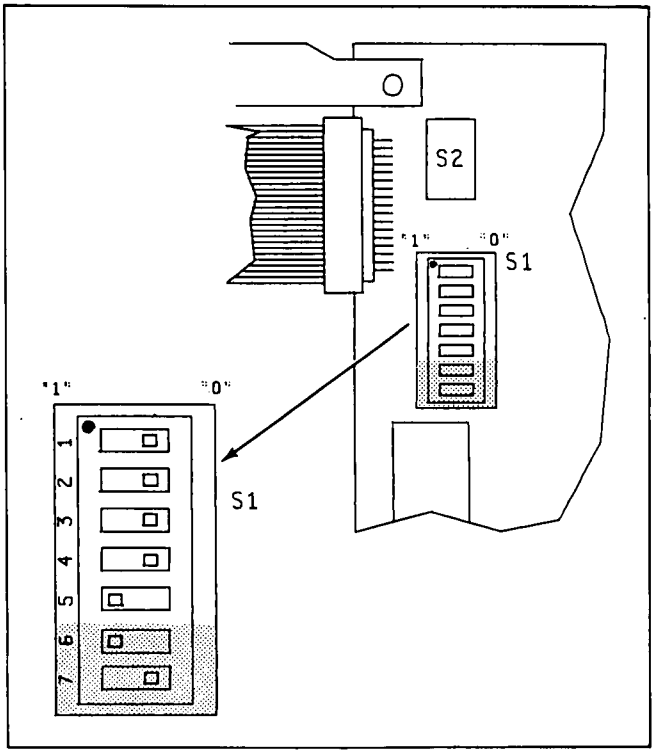


Figure 8-A2-13. Switch Settings for Test 6A

Table 8-A2-25. Test 6A Signatures

Note

Some of the U7 signatures require a 4.7 k Ω pullup resistor between +5V and the signature analyzer probe tip. These signatures are noted with an asterisk (*) in the table.

+5V Signature: U4HP

Test Point	Signature	Test Point	Signature	Test Point	Signature
U7 Pin 1	U4HP	U2 Pin 13	437H	U12 Pin 2	H9AC
Pin 2	H5CA	Pin 14	U4HP (+5V)	Pin 5	A772
Pin 3	62FH*	Pin 15	2378	Pin 6	89F0
Pin 4	20UA*	Pin 16	PP7P	Pin 9	80F1
Pin 5	UHF3	Pin 17	C650	Pin 12	U12C
Pin 6	8U4C			Pin 15	911C
Pin 7	P6F5*	Pin 5	09HH	Pin 16	UF60
Pin 8	6UP1*	Pin 11	7786		
Pin 9	1666	Pin 12	7786	U23 Pin 12	AH3P
Pin 10	0000 (GND)	Pin 13	U7UF		
Pin 11	8FHA	Pin 14	U4HP (+5V)	U18 Pin 1	09HH
Pin 12	9F35	Pin 15	7786	Pin 3	09HH
Pin 13	7H95*	Pin 16	PPCC	Pin 5	09HH
Pin 14	H985*	Pin 17	U6FA	Pin 9	C336
Pin 15	2427			Pin 11	C336
Pin 16	9278	U8 Pin 5	C336	Pin 13	C336
Pin 17	0P0H*	Pin 11	0A63		
Pin 18	109U*	Pin 12	0A63	U20 Pin 1	9105
Pin 19	C815	Pin 13	1163	Pin 2	U3P0
Pin 20	U4HP	Pin 14	U4HP (+5V)	Pin 3	125P
		Pin 15	0A63	Pin 4	3631
U3 Pin 2	3102	Pin 16	5U73	Pin 5	0000 (GND)
Pin 5	1837	Pin 17	86FA	Pin 6	U4HP (+5V)
Pin 6	F684			Pin 7	U4HP
Pin 9	24F6	U6 Pin 2	5H61	Pin 8	0000 (GND)
Pin 11	5PHC	Pin 5	0111	Pin 9	U4HP
Pin 12	59AH	Pin 6	45P0	Pin 10	U4HP (+5V)
Pin 15	9U8A	Pin 9	AU68	Pin 11	Unstable
Pin 16	F828	Pin 11	F311	Pin 12	U4HP (+5V)
Pin 19	31A6	Pin 12	1264	Pin 13	8FHA
		Pin 15	H0PA	Pin 14	C336
U9 Pin 2	1FA8	Pin 16	P7A0	Pin 15	09HH
Pin 5	P824	Pin 19	6708	Pin 16	U4HP (+5V)
Pin 6	P800				
Pin 9	638U	U11 Pin 1	2H75	U21 Pin 1	9105
Pin 11	44P1	Pin 2	H9AC	Pin 2	U3P0
Pin 12	U41P	Pin 3	A772	Pin 3	125P
Pin 15	P356	Pin 4	53AF	Pin 4	29F5
Pin 16	6U5F	Pin 5	7H1P	Pin 5	0000 (GND)
Pin 19	U3F9	Pin 6	89F0	Pin 6	U4HP (+5V)
		Pin 7	741U	Pin 7	5U75
U1 Pin 3	89PC	Pin 8	80F1	Pin 8	0000 (GND)
Pin 6	8697	Pin 10	05U5	Pin 9	5PHC
Pin 11	189P	Pin 11	U12C	Pin 10	50P9
Pin 14	FF0A	Pin 12	65F5	Pin 11	0UF1
		Pin 13	911C	Pin 12	13CP
U2 Pin 5	09HH	Pin 14	08CP	Pin 13	F311
Pin 11	2378	Pin 15	UF60	Pin 14	44P1
Pin 12	2378			Pin 15	17H3
				Pin 16	U4HP (+5V)

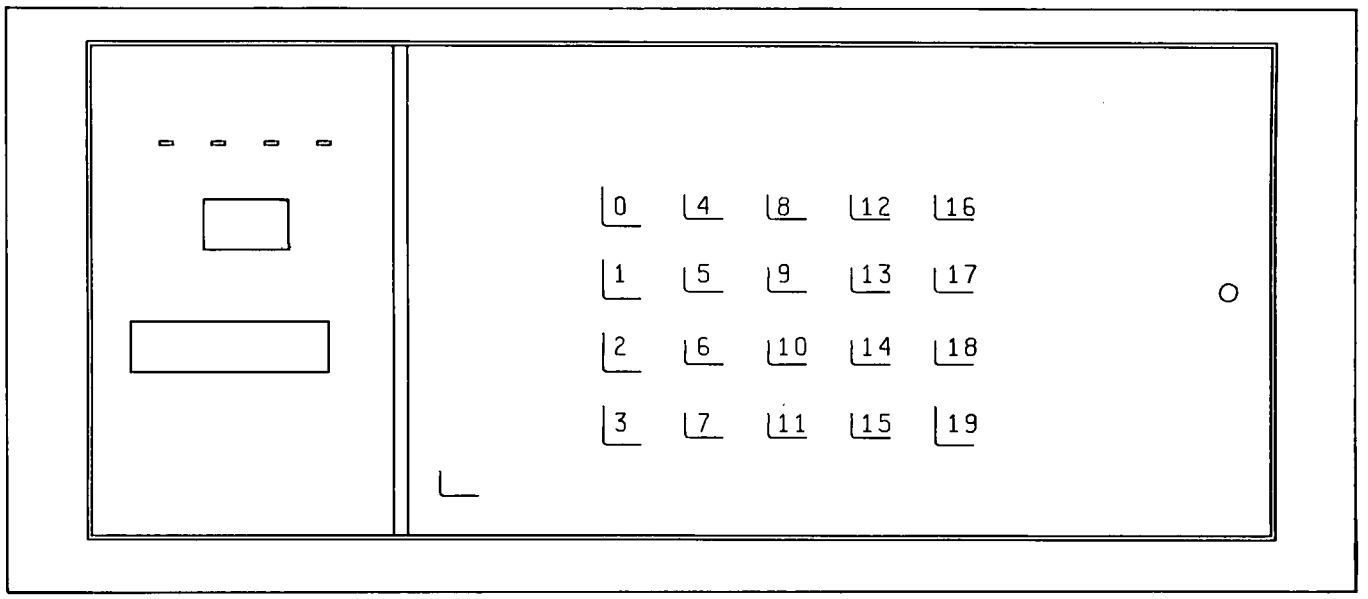


Figure 8-A2-14. Test 6B Front Panel Key Assignments

a. Connect the signature analyzer as follows:

Start:	U31 pin 9
Stop:	TP SS2
Clock:	TP CLK
Gnd:	TP GND

b. Set the signature analyzer as follows:

Start:	In ( )
Stop:	In ( )
Clock:	In ( )

c. Make sure the switch segments are set as outlined in Test 6A.

d. Momentarily connect the TP SA to ground (TP GND).

e. In Table 8-A2-26, the U14 pin assignments (on the front panel) have been given the following test pin assignments.

U14 pin 15 is Test Point E
U14 pin 16 is Test Point D
U14 pin 17 is Test Point C
U14 pin 18 is Test Point B
U14 pin 19 is Test Point A
U14 pin 13 is Test Point DAV

In Table 8-A2-26, Test Points A, B, C, D, E, and DAV are listed vertically on the left side; the keys are listed horizontally across the top. The 0's and 1's in the table have the following meanings.

0 = 0000 (GND) signature
1 = 4969 (+5V) signature

To read Table 8-A2-26, determine from the key being pressed and the test point that is observed, whether that location has a 0 or 1. Then change the 0 or 1 into a signature or level, as previously explained. For example, with the probe at Test Point A, some of the following levels should be noted with the various keys pressed: key 0 = 0, key 1 = 1, key 2 = 0, etc.

f. Once the keys are tested, other signatures, shown in Table 8-A2-27, can then be taken. If a signature is wrong. replace the appropriate component.

8-A2-67. Crossguard Test (Test #7)

8-A2-68. This test requires an oscilloscope instead of a signature analyzer. In this test, the outguard controller writes the same pattern (55 Hex) to the inguard. This pattern is sent over the crossguard and provides a trigger for the oscilloscope. This test is useful for checking the outguard transmitter and receiver, and the inguard receiver. Refer to Schematic AB1 for the test.

8-A2-69. To perform this test, switch segment 7 of switch S1 must be in the "1" (left) position and switch segments 1 through 6 must be in the "0" (right) position, as shown in Figure 8-A2-15.

8-A2-70. After the switches are set (as shown in Figure 8-A2-15), momentarily connect TP SA to ground (TP GND). Then use an oscilloscope to check the signals shown in Figures 8-A2-16 through 8-A2-18. The figures were obtained using an -hp- Model 1741A Oscilloscope using the delayed sweep feature. In Figure 8-A2-18, the pulse transformers are wired so that the crossguard transmitter is tied to the crossguard receiver. This is illustrated in Figure 8-A2-5.

Table 8-A2-26. Test 6B Signatures

+5V Signature: 4969																				
Key Pressed																				
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Test Point	A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
	D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
	E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	DAV	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 8-A2-27. Test 6B Signatures

+5V Signature: 4969

Test Point	Signature
U16 pin 4	34F4
pin 5	49P8
pin 6	7H2F
pin 8	3445
pin 9	7H2F
pin 10	4969 (+5V)
U17 pin 6	4969 (+5V, no key pressed)
pin 3	1969 (+5V, any key pressed)

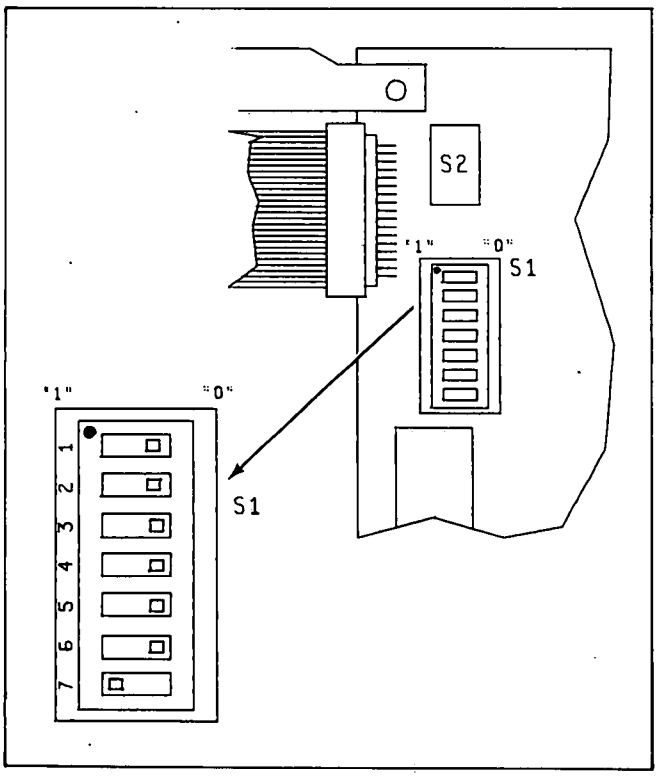


Figure 8-A2-15. Switch Settings for Test #7

Oscilloscope Setup:

Connect External Trigger to SS2 (test point between U31 and U35 on A1 Board)

2V/Div
Channel 1: 10 uS/Div. Connect to U40 Pin 2.
Channel 2: 5 uS/Div. Connect to U40 Pin 9.
Trigger: Positive, External
Chop

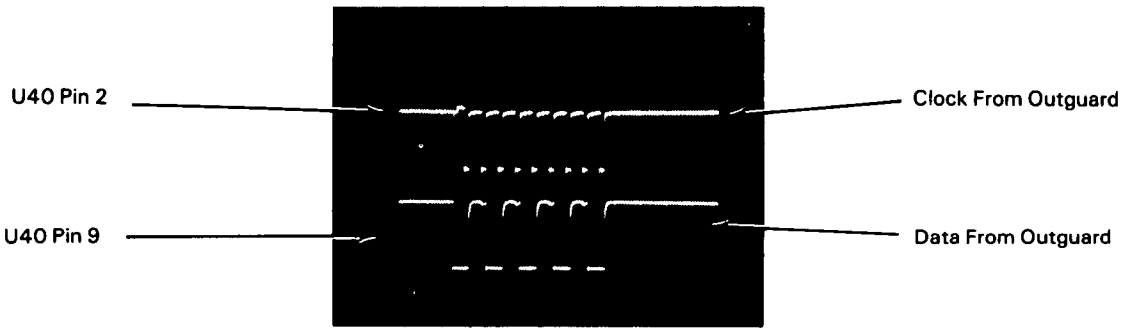


Figure 8-A2-16. Clock and Data from Outguard

Oscilloscope Setup:

Change Channel 2 to 5V/Div and connect to U46 Pin 8.

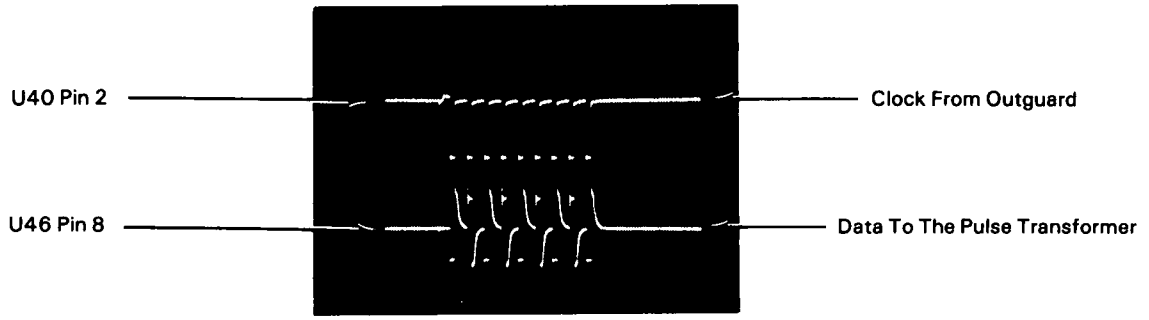


Figure 8-A2-17. Data to the Pulse Transformer

Oscilloscope Setup:

Set 2V/Div on Channels 1 and 2
Connect Channel 1 to U50 Pin 8
Connect Channel 2 to U50 Pin 1

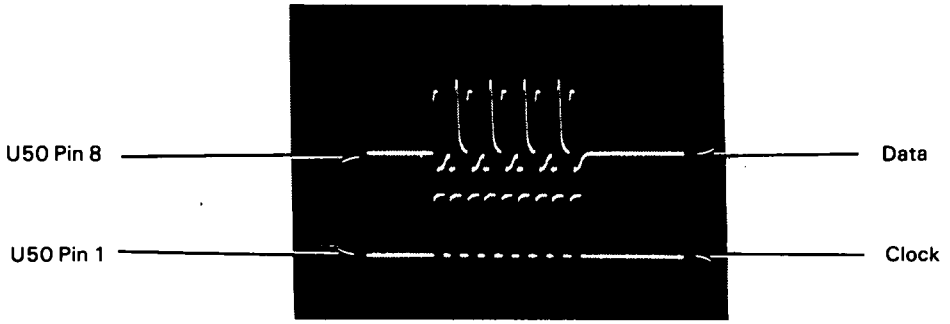


Figure 8-A2-18. Crossguard Transmitter/Receiver Data

SERVICE GROUP B

INGUARD LOGIC AND A/D CONVERTER TROUBLESHOOTING

Service Group B Contents

8-B-1. INTRODUCTION

8-B-2. This service group has troubleshooting information for the 3497A's inguard logic. It includes information on the inguard processor (U204), port extender (U205), BCD to decimal decoders (U206 and U208), inguard crossguard logic, A/D logic, and associated circuitry. Since the A/D converter operation is controlled by the inguard processor using the A/D logic, troubleshooting information for the A/D converter is also included in this service group.

CAUTION

The 3497A mainframe contains CMOS Integrated Circuits which are extremely susceptible to failures due to static discharge. It is especially important that grounded tools and wrist straps be used when handling and troubleshooting these components.

8-B-3. PRE-TROUBLESHOOTING INFORMATION

8-B-4. Read the information in the following paragraphs before doing any troubleshooting.

8-B-5. Troubleshooting Without Signature Analysis

8-B-6. Check for stuck nodes on the data bus. This can be done using a logic probe. A stuck node usually shows the node in a certain steady state when it is supposed to pulse. Try to determine what the circuitry is to be doing and what it is not doing, or vice versa, and then try to logically associate that to a particular component. The theory of operation may be helpful to determine the defective component. Then check for the outputs of the component to see if they are pulsing. If they are not pulsing, check the inputs of the device for pulsing. If the inputs are pulsing, the device is probably defective. This method of troubleshooting does not check for timing errors, but is fast and simple.

8-B-7. Troubleshooting With Signature Analysis

8-B-8. A signature analyzer is used to determine the faulty circuit. This is done by placing the circuitry in a certain operating mode and then taking signatures using the signature analyzer. When the circuitry is in that mode, the data on the lines develop a unique signal. This data is read by the signature analyzer which then develops a unique signature. If the signature is correct, the device developing the signal is correct. If the signature is incorrect, the device may be defective. Before replacing the device, make sure other devices on the line are not causing the incorrect signature.

8-B-9. General Troubleshooting Information

8-B-10. Check and make sure the +5V power supply is good. This supply should be between +4.75V and +5.25V.

8-B-11. Make sure the inguard processor's clock (i.e., the ALE clock) is operating correctly. If the ALE clock is missing or at the incorrect frequency (390KHz for 60Hz operation and 325KHz for 50Hz operation), try replacing Y1. Also, check and make sure U201 is good, if the ALE clock is good at pin 11 of U204. If the clock is still inoperative, replace U204.

8-B-12. Make sure the processor is properly reset. This can be done by temporarily shorting the $\overline{\text{RESET}}$ line (U204 pin 4) to ground. The line should then go high and reset the processor. If, after shorting the line, the inguard logic starts operating or if the line remains low, check for a defective U214 and associated circuitry.

8-B-13. INGUARD LOGIC FAILURES

8-B-14. Since the main purpose of the inguard logic is to control the voltmeter option's A/D operation, most failures caused by the inguard logic show up as voltmeter failures or Self-Test #2 fails. Other failures are incorrect set-up information to the analog plug-in options and Self-Test #1 fails. The inguard logic failures and where to go for troubleshooting are in the following paragraphs. For a description of the failures, refer to paragraph 8-38, 8-48, and 8-54.

8-B-15. Self-Test #1 Fails

8-B-16. This failure usually shows that there is no communication between the outguard and inguard controller. This can be caused by the crossguard logic (inguard or outguard), outguard circuitry, or inguard controller circuitry. A procedure to determine the defective circuitry is in Service Group A1 for the standard (HP-IB) mainframe and in Service Group A2 for the Serial I/O (Option 232) mainframe. The procedure is used to determine if the transmitter part of the inguard crossguard logic is defective. Do the procedure first to determine the faulty circuitry. Once the procedure is performed and it has been determined that the transmitter part of the inguard crossguard circuitry is at fault, go to paragraph 8-B-44 (Crossguard Logic Troubleshooting) for further troubleshooting.

8-B-17. Self-Test #2 Fails

8-C-18. This test usually shows that there is an A/D converter failure. Since the inguard controller, A/D logic, or A/D converter can cause the failure, go to paragraph 8-B-29 (Inguard and A/D Logic Isolation And Troubleshooting) for further isolation.

8-B-19. The 3497A Displays Dashes

8-B-20. When the dashes are displayed with the voltmeter option installed, the cause can be the inguard controller or A/D logic. Go to paragraph 8-B-29 (Inguard and A/D Logic Isolation And Troubleshooting) for further isolation.

8-B-21. Voltmeter Failures

8-B-22. Before troubleshooting the inguard controller, A/D logic, or A/D converter for voltmeter failures, make sure the failures are not caused by the input switching and input amplifier circuitry of the voltmeter. A procedure to determine the defective circuitry is in Service Group C. Do the procedure first to determine the faulty circuitry. If the input amplifier and input switching circuitry is good, go to paragraph 8-B-29 (Inguard and A/D Logic Isolation And Troubleshooting) for further isolation.

8-B-23. Analog Plug-In Option Failures

8-B-24. Dependent on what fails, these failures can be caused by the option itself or the inguard logic circuitry. Before troubleshooting the inguard circuitry, make sure the analog plug-in options are not causing the failure. Then go to paragraph 8-B-29 (Inguard and A/D Logic Isolation And Troubleshooting) for further isolation.

8-B-25. Failures with The 3498A Extender Connected

8-B-26. Dependent on what fails, these failures can be caused by the extender itself or the inguard logic circuitry. Before troubleshooting the inguard circuitry, make sure the extender is not causing the failure. Then go to paragraph 8-B-29 (Inguard and A/D Logic Isolation And Troubleshooting) for further isolation.

8-B-27. Miscellaneous Inguard Failures

8-B-28. These failures include incorrect range set-up of the voltmeter option (dc voltmeter and current source). The failures can be caused by the voltmeter option itself or the inguard logic. Make sure the voltmeter option is not causing the failure before troubleshooting the inguard logic. If the inguard logic is causing the failure, go to paragraph 8-B-29 (Inguard and A/D Logic Isolation And Troubleshooting) for further isolation.

8-B-29. INGUARD AND A/D LOGIC ISOLATION AND TROUBLESHOOTING

8-B-30. General

8-B-31. The inguard logic can cause any of the failures listed in paragraph 8-B-13. Some of the failures can also be caused by the inguard crossguard logic, the A/D logic, the A/D converter, or other associated circuitry.

8-B-32. The procedure in paragraph 8-B-35 is used to determine the defective circuitry in the inguard and A/D logic using signature analysis. Once the faulty circuit is determined, either more signatures are taken or a program is used to determine the faulty component. This depends on the failure. The procedure to isolate the defective circuitry is in the following order.

a. The signatures of some of the ports of the inguard processor are checked.

b. If the signatures are good, most of the A/D logic and inguard processor are most likely good. Direction to another possible faulty area is given.

c. If the signatures are incorrect or missing, the processor itself or the A/D logic is defective. The A/D logic is then checked next.

8-B-33. Equipment Required

8-B-34. The required test equipment to isolate and troubleshoot the inguard and A/D logic is a signature analyzer (-hp- Model 5004A) and a logic probe.

8-B-35. Inguard Logic Isolation Procedure

8-B-36. Refer to Schematic B1 and B2 for the following procedure. The common ground used in the following procedure is inguard ground (TP GND).

a. Turn the 3497A off.

b. Connect the inguard controller board to a Board Extender and plug the extender into the appropriate slot of the instrument (see paragraph 8-14 on how to remove the inguard board and how to connect the extender).

c. Locate the ribbon cable soldered to the voltmeter option board. Disconnect the cable from the inguard controller board (see Figure 8-B-1).

CAUTION

Do not unplug or plug the ribbon cable from the voltmeter into the inguard controller board with the 3497A on or the circuitry on the controller board will be damaged.

d. Locate jumper plug J1 and move the jumper plug to the "P" position, as shown in Figure 8-B-1.

NOTE

Make sure jumper plug J1 is placed back into the "N" (Normal) position, when troubleshooting is completed.

e. Using short clip leads, connect the MAKE test point (TP MAKE) and the clock test point (TP CLK) to the ground test point (TP GND).

f. Connect the signature analyzer as follows (see Figure 8-B-1):

Start:	Pin 3 or 4 of J4 (DSA)
Stop:	Pin 3 or 4 of J4 (DSA)
Clock:	Pin 2 of J4 (ALE)
Gnd:	Pin 1 of J4 (G)

g. Set the signature analyzer as follows:

Start:	Out (⎍)
Stop:	In (⎏)
Clock:	Out (⎍)
Self-Test:	Out
Hold:	Out

h. Turn the 3497A on.

i. Using a short clip lead, temporarily connect the inguard processor's $\overline{\text{RESET}}$ line (TP $\overline{\text{RS}}$) to ground (TP GND). This places the processor into the test mode.

j. Using the signature analyzer, check the +5V signature (0HHH) at TP +5 and the ground signature (0000) at TP GND.

k. If the signatures are wrong, check the following:

1. Make sure the signature analyzer probe is toggling. If the probe is not toggling, check for an ALE clock at the "ALE" pin of J4 (i.e., pin 2; see Schematic B2). If the clock is missing at J4 but is good from the processor (U204), replace U3.

2. If the ALE clock at pin 2 of J4 is good and the +5V and/or ground signatures are still wrong, try replacing the inguard processor (U204).

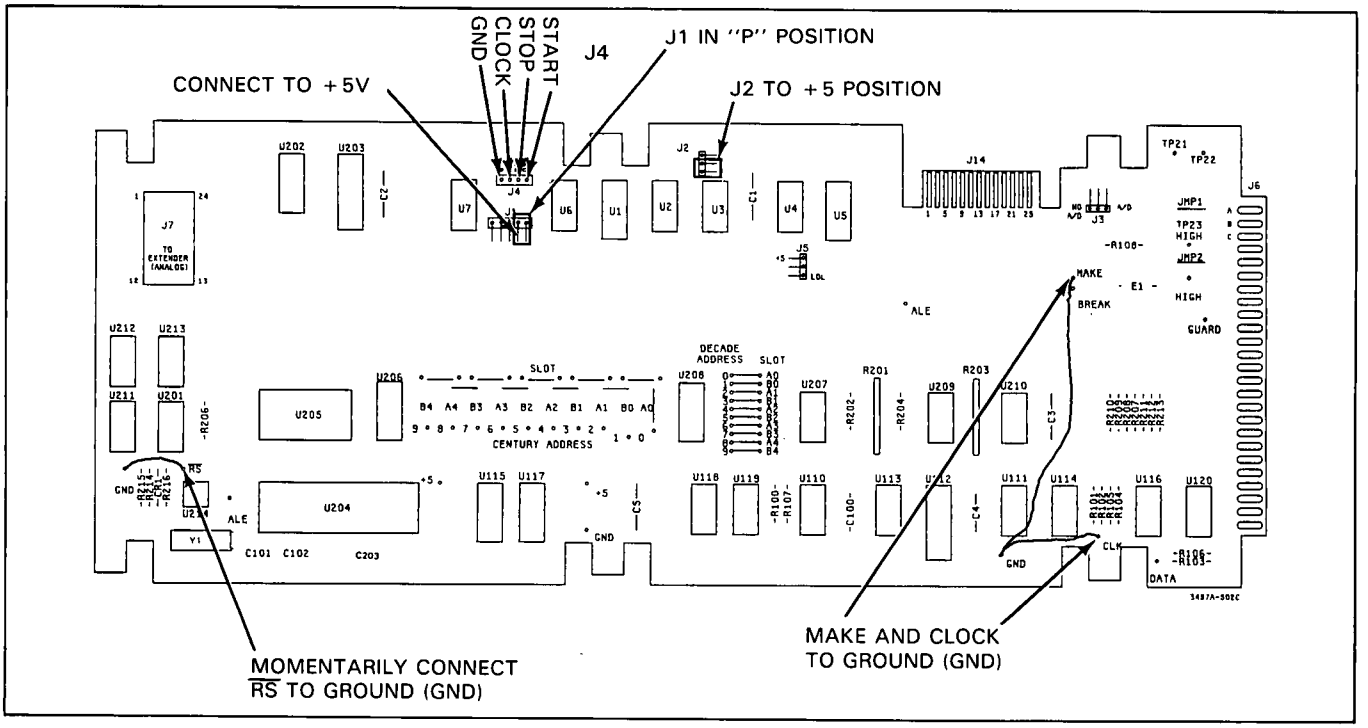


Figure 8-B-1. Setup for Inguard SA Test

l. If the +5V and ground signatures are good, check the following signatures on the inguard processor.

U204 Pin#	Signature
1	810F
27	6H56
28	UHPA
29	78F6
30	A71A
38	0HHH
39	H791

m. If the signatures are good, the inguard processor and most of the A/D logic is probably good; further isolation is necessary. Go to paragraph 8-B-37 for further isolation. Do not change the present test setup.

n. If the signatures are wrong, the inguard processor or A/D logic is most likely at fault. Do the procedure in the flowchart located in Figure 8-B-2 (A/D Logic Troubleshooting). Do not change the present test setup. It will be used in the flowchart.

8-B-37. Inguard Troubleshooting

8-B-38. General. Before doing the procedures in paragraphs 8-B-40 to 8-B-43, make sure the procedure in paragraph 8-B-35 has been performed. Unless otherwise noted, also make sure the test setup is the same as in paragraph 8-B-35.

8-B-39. The troubleshooting information in the following paragraphs is separated into failures. Select the appropriate paragraph by the failure. The common ground used in the procedure is inguard ground (TP GND).

8-B-40. Test #2 Fails. Do the following procedure to determine the defective circuitry or component. This procedure should also be performed if a Voltmeter Failure is present. Refer to Schematic B2 when doing the following procedure.

a. With the same test setup as in paragraph 8-B-35, check the signature at pin 8 of U4C (see Schematic B2). The correct signature is: "AAF7".

b. If the signature is wrong or unstable, replace U4.

c. If the signature is good, remove jumper plug J1 from the "P" position and temporarily set it aside. The inguard processor is now placed into the free-run mode.

NOTE

Make sure jumper plug J1 is placed back into the "N" (Normal) position, when troubleshooting is completed.

d. Check the following signatures of latch U5.

U5 Pin#	Signature
3	0000
5	6U9A
11	88U6

e. If any signatures are wrong or unstable, replace U5.

f. If the signatures are good, the A/D converter is causing the failure. Go to paragraph 8-B-50 for troubleshooting.

8-B-41. Voltmeter Failures. Do the procedure in paragraph 8-B-40 (Test #2 Fails) to determine the faulty circuitry.

8-B-42. The 3497A Displays Dashes. Try replacing the inguard processor (U204).

8-B-43. Analog Plug-In Option Failures. The failures can both be a Make/Break failure or the option receives the incorrect setup information. To troubleshoot these failures, return the 3497A to the normal operating state. Disconnect the signature analyzer and return jumper plug J1 to the "N" (Normal) position. Then do the following procedure.

a. To check the Make/Break circuitry, do the following:

1. Make sure no analog plug-in options are plugged into the mainframe.

2. Connect a logic probe to pin 12 of U212A. The pin should read low.

3. If pin 12 reads high, make sure both $\overline{\text{MAKE}}$ and $\overline{\text{BREAK}}$ lines are high. If they are high, replace U201 or U212, depending on which line is high. If they are low, replace U212.

4. If pin 12 of U212 is low, temporarily connect the $\overline{\text{BREAK}}$ line (TP BREAK) to ground. When connected to ground, pin 12 should go high and when disconnected from ground, the pin should go low again. The same should take place with the $\overline{\text{MAKE}}$ line (TP MAKE). If the BREAK operation only is inoperative, replace U213 or U212. If the $\overline{\text{BREAK}}$ only or both $\overline{\text{MAKE}}$ and $\overline{\text{BREAK}}$ operations are inoperative, replace U212.

5. If the checks in step 4 are good, connect the logic probe to pin 3 of U201. Make sure the pin is low. If high, replace U201. If low, connect the $\overline{\text{MAKE}}$ line (TP MAKE) to ground. If pin 3 of U201 remains low, replace U201. If it goes high, continue with the next step.

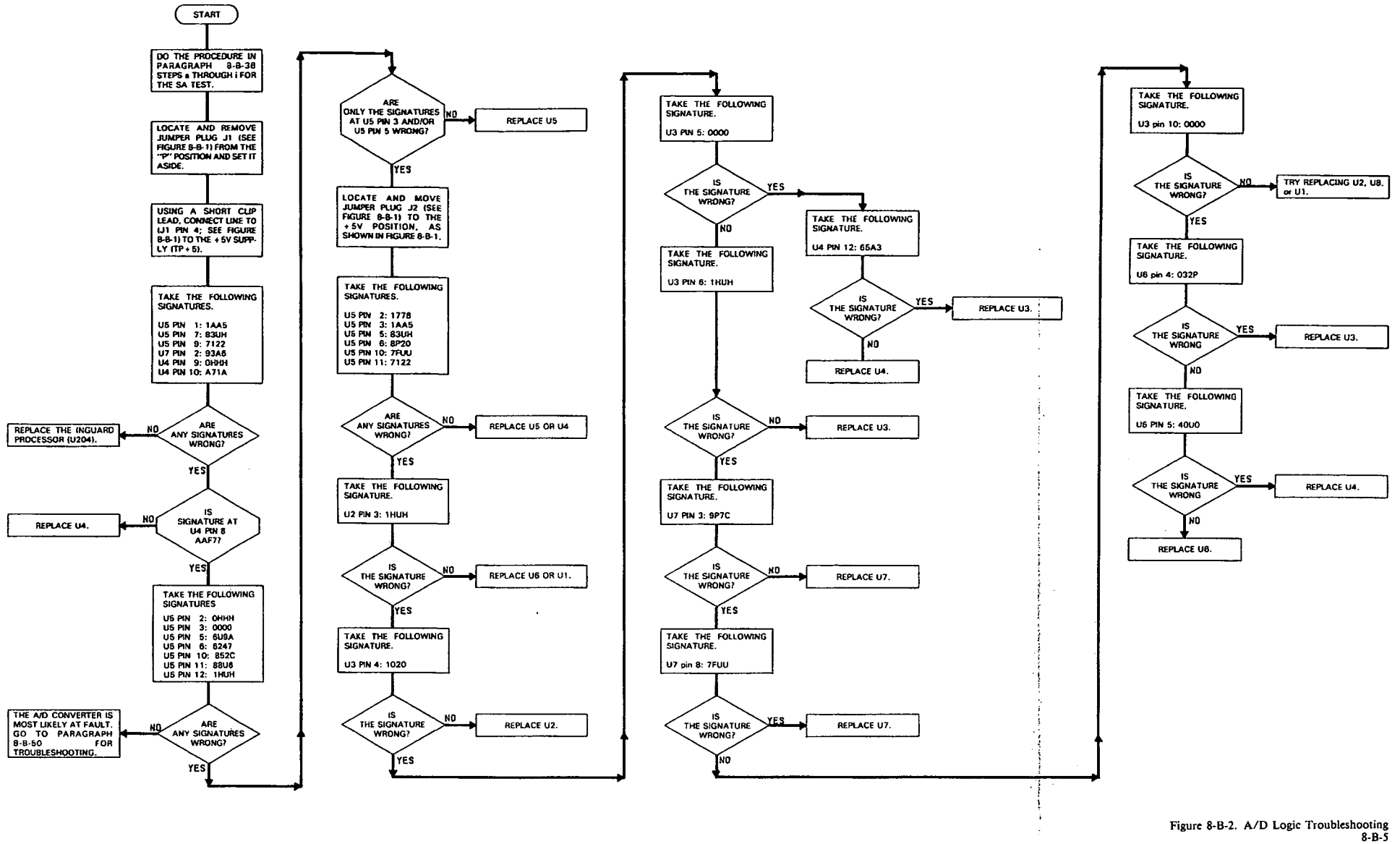


Figure 8-B-2. A/D Logic Troubleshooting

6. Connect the logic probe to pin 6 of U212. Then cycle power on the instrument. Pin 6 of U212 should now be low. If high, check pins 4 and 5 of U212. If either one of the pins are low, replace U205. If good, replace U212.

7. If the checks in steps 5 and 6 are good, replace U211.

b. If the plug-in option receives the wrong set-up information, troubleshoot the analog decoding circuitry (U206, through U210) using a logic probe. Do the following:

1. Locate the EXT INCR Input port and the TIMER output port on the outguard rear panel. Using a BNC cable, connect the ports to each other.

2. Using the front panel or remotely, enter the following program into the 3497A.

```
AF0
AL999
TO10
AE2
```

3. Once the program is entered, use a logic probe and check the state of the output lines of U207, U209, and U210. Make sure they are toggling.

4. If any lines are not toggling, check further back through U206 and U208 to port extender U205. All pins on U205, except pins 13, 14, 15, and 16, should be toggling. If they are, check U206 through U210.

8-B-44. CROSSGUARD LOGIC TROUBLESHOOTING

8-B-45. An inguard crossguard logic failure normally shows up when Test #1 fails. Since this can also be caused by the outguard circuitry, make sure the procedure in Service Group A1 or A2 have been performed before doing the troubleshooting procedure in paragraph 8-B-48.

8-B-46. Equipment Required

8-B-47. The required test equipment to troubleshoot the crossguard logic is a logic probe.

8-B-48. Troubleshooting Procedure

8-B-49. The procedure in this paragraph has information to troubleshoot the transmitter section of the inguard crossguard logic. Information on how to troubleshoot the receiver section is in Service Group A1. Unless otherwise noted, refer to Schematic AB1 for troubleshooting. Do the following:

a. Make sure the inguard controller board is removed from the instrument and connected to a Board Extender. Also make sure the Board Extender is connected into the appropriate slot of the instrument (see paragraph 8-14).

b. Using a logic probe, make sure pins 3 and 8 of U120 are toggling.

c. If they are, check for defective transformers T3 or T4 (located on the power supply board behind front panel). If T3 and T4 are good try replacing U115 or U204 (see Schematic B1).

d. If pins 3 and 8 of U120 are not toggling, do the following:

1. Using a logic probe, make sure the $\overline{\text{WRT}}$ line from the inguard processor is toggling. If not, replace U204 (see Schematic B1).

2. If the line is toggling, make sure pin 9 of U119 is toggling. If not, replace U119.

3. Make sure pin 1 of U120 is toggling.

4. If not, make sure the $\overline{\text{ALE}}$ line is toggling. If the $\overline{\text{ALE}}$ line is not toggling, check for a defective U201 or U204 (see Schematic B1).

5. If the $\overline{\text{ALE}}$ line is toggling, replace U117 or U118.

6. Make sure pins 5 and 6 of U119 are toggling. If not, check for toggling at pin 9 of U115.

7. If pin 9 of U115 is good, replace U119. If not, replace U119.

8. If the 3497A is still inoperative, try replacing U204 (see Schematic B1).

8-B-50. A/D CONVERTER TROUBLESHOOTING

8-B-51. General

8-B-52. Before doing the troubleshooting procedures in the following paragraphs, make sure the failure is not caused by the A/D logic or inguard circuitry. Do the procedure in paragraph 8-B-29 first to determine the faulty circuitry.

8-B-53. A/D converter failures can show up as a Test #2 failure or voltmeter failure. The voltmeter failure consists of Overload, Constant Zero, Floating, Inaccurate, or Noisy Readings on all ranges (see paragraph 8-54 for a description of the failures). The troubleshooting information in paragraphs 8-B-58 to 8-B-63 is separated by failures. Go to the appropriate paragraph by the failure. Unless otherwise noted, refer to Schematic C3 for troubleshooting. The common ground used in the procedures is voltmeter ground 4 (TP GND4).

8-B-54. Equipment Required

8-B-55. The following is the required test equipment to troubleshoot the A/D converter.

Digital Voltmeter -hp- Model 3456A
Oscillocope -hp- Model 1741A
Logic Probe

8-B-56. A/D Converter Failures and Troubleshooting

8-B-57. The A/D converter has two types of circuitry, analog and digital. Most A/D failures can be caused by either one or both of the circuitry. The following paragraphs have the A/D converter failures and troubleshooting information. Before doing any troubleshooting, first isolate the A/D converter from the input amplifier by doing the following:

a. Turn the 3497A off.

b. Make sure the inguard controller board is removed from the instrument and connected to a Board Extender. Also make sure the Board Extender is connected into the appropriate slot of the instrument (see paragraph 8-14).

c. If the voltmeter option board is unplugged from the inguard controller board, locate the ribbon cable from the voltmeter board and plug it back into the inguard controller board.

d. Refer to paragraph 8-20 and remove the shield over the voltmeter board.

e. Lift one end of jumper JMPR200.

f. Turn the 3497A on.

Once jumper JMPR200 is lifted, go to the following paragraphs for troubleshooting. Select the appropriate paragraph by the failure.

8-B-58. Overload Readings. These can be caused by the digital, analog, or overload circuitry of the A/D converter. To determine if the overload circuitry is causing the failure, do the following:

a. Apply 11V dc to to TP A-D IN.

b. Refer to Schematic B1 and place jumper plug J5 to the +5V position.

c. If the overload disappears and the 3497A reads 11V, do the following:

1. With 11V applied to TP A-D IN, make sure the output of the integrator (TP INT) does not go above 12V. Do this by connecting an oscilloscope to TP INT and make sure the peaks on the waveform shown on the scope are below 12V.

2. If the peaks are below 12V, the overload circuitry is defective. Try replacing U203 or associated circuitry.

3. If the peaks go above 12V, the integrator has an offset. This can be caused by an open A/D Autozero FET (Q203) or the integrator itself. Try replacing Q203 and then Q202 and U201.

d. If the overload is still noted, other circuitry in the A/D converter are at fault. Go to paragraph 8-B-63 (Test #2 Fails) for troubleshooting.

8-B-59. Constant Zero Readings. This type of failure normally shows that there is a short at the input of the A/D converter to ground. Check and make sure that there are no shorts. This failure can also be caused by an open R200 (between pins 7 and 8) and an open Q201. If Q201 is good, check the following:

a. Make sure Q201 is turned on by U200. Under normal conditions, pin 3 of U200 should be toggling from 0V to -12V. Make sure it is toggling.

b. If pin 3 of U200 is toggling, replace Q201.

c. If pin 3 is not toggling, check and make sure TP LRU is toggling.

d. If TP LRU is toggling, either U204 or U207 are defective. Make sure pin 2 of U204 is toggling. If it is, replace U207. If not, replace U204.

8-B-60. Floating Readings. Floating readings normally show up if there is an open circuit in the input of the A/D converter. This can be checked by connecting TP A-D IN to ground (TP GND4). If the failure still exists, check for an open between R200 (pin 7) and JMPR200.

8-B-61. Inaccurate Readings. If the readings are only inaccurate a small amount (a couple of counts) the most likely cause is R200. If the readings are very inaccurate, other circuitry in the A/D converter are at fault. Go to paragraph 8-B-63 (Test #2 Fails) for troubleshooting.

8-B-62. Noisy Readings. If only a little noise is noted, the most likely cause is the analog circuitry of the A/D converter. Check for a noisy Q202 and Q203. If the readings are very noisy, other circuitry in the A/D converter are at fault. Go to paragraph 8-B-63 (Test #2 Fails) for troubleshooting.

8-B-63. Test #2 Fails. The troubleshooting information in the following procedure is used to determine which circuitry, analog or digital, is causing the failure. Once this has been determined, the procedure then determines the most likely component causing the failure. Before going to the procedure, do the following checks (if they have not been performed already).

a. Make sure latch U207 is enabled by the ALE clock. Do this by checking for a clock signal at pin 9 of U207. The clock signal level should be from 0V to -12V instead of a TTL level. If the clock is missing or at an incorrect level, check for a defective Q204, Q206, or associated circuitry.

b. Make sure pin 2 of U200 is toggling from 0V to -12V. If pin 2 is toggling, continue with step b. If pin 2 is not toggling, do the following:

1. Make sure pin 3 of U200 is toggling from 0V to -12V.

2. If pin 3 is not toggling, check and make sure TP LRU is toggling.

3. If TP LRU is toggling, either U204 or U207 are defective. Make sure pin 2 of U204 is toggling. If it is, replace U207. If not, replace U204.

c. Make sure Q200, Q201, and Q205 are not shorted.

d. Make sure the base of Q203 toggles from 0V to -12V. If it is not toggling, the digital circuitry of the A/D converter is at fault (go to next paragraph for troubleshooting). Also make sure Q203 is not shorted or open.

8-B-64. Once the previous checks are made and the 3497A still fails, do the following troubleshooting procedure.

a. Turn the 3497A off.

b. Using a clip lead, connect the inguard processor's reset line to ground (TP $\overline{RS}$ to GND; see Schematic B1). This places the inguard processor into the reset state, when the 3497A is turned on.

c. Using another clip lead, turn Q204 off by connecting its base to its emitter.

d. Turn the 3497A on.

e. Since the inguard processor is now in the reset state (i.e., unable to turn on), the outputs of latch U5 (see Schematic B2) are at certain TTL levels (they will most likely be all high). This determines into what static state the A/D converter is placed. Determine the state by reading the high (+5V) and low (0V) levels of pins 6, 8, and 10 of U204 (use a logic probe). Once these levels are determined, refer to Table 8-B-1 and determine the static state of the A/D converter (S-4, Az, etc.).

f. Once the static state of the A/D converter is determined by using Table 8-B-1, the input and output levels of the components in the digital circuitry can then be determined. Do the following:

1. Temporarily connect pin 9 of U207 to ground.

2. Using an oscilloscope, logic probe, or Digital Voltmeter, make sure the components in the digital circuitry of the A/D converter are at the correct input/output levels. Use Table 8-B-2 to determine the correct levels. A high level (which shows low on the logic probe) is 0V and a low level (which shows high on the logic probe) is at -12V.

3. If any levels are wrong, replace the appropriate component. If all the levels are correct, the digital circuitry of the A/D converter is most likely good. Continue with the next step.

Table 8-B-1. Determining the Static Level of The A/D Converter

Static State	U204 Input Levels Pin #10	Pin #8	Pin #6
Az	H	H	H
S-0	L	H	L
S-1	H	L	L
S+2	L	L	H
S-3	H	L	H
S+4	L	H	H
S-4	H	H	L

Note: H = +5V, L = 0V. Levels for the Az state is also for the S+0 state.

Table 8-B-2. States of the A/D Converter Digital Circuitry

IC	Pin #	IC Levels Az	S-0	S-1	S+2	S-3	S+4	S-4
U200	4	H	H	L	H	H	H	H
	5	L	L	H	L	L	L	L
	6	H	L	H	L	H	L	H
	7	L	H	L	H	L	H	L
U204	1	L	H	H	L	L	L	H
	13	L	H	L	H	L	H	L
	14	L	L	H	H	H	L	L
U205	4	H	L	L	L	L	L	L
	5	L	L	L	L	L	L	H
	6	L	L	L	L	H	L	L
	7	L	L	H	L	L	L	L
	10	L	L	L	H	L	L	L
	11	L	H	L	L	L	L	L
	12	L	L	L	L	L	H	L
U206	3	H	H	H	H	H	L	H
	4	H	L	H	H	H	L	H
	10	L	H	L	L	L	L	H
	11	H	H	H	L	H	H	H
U207	2	H	L	H	H	H	L	H
	5	L	H	L	L	L	L	H
	7	L	L	L	L	H	L	L
	10	H	H	H	L	H	H	H
	12	H	L	L	L	L	L	L
U208	2,4	L	H	L	L	L	H	L
	6,10	H	L	H	H	H	H	L
	12	H	H	H	H	L	H	H
	15	L	L	L	H	L	L	L

Note: H = 0V, L = -12V.

g. Troubleshoot the analog circuitry of the A/D converter by doing the following:

1. Keep the same set-up as in steps b and c.

2. Locate the integrator capacitor (C201) and, using a clip lead, short across the capacitor.

3. Using a high impedance Digital Voltmeter (like the 3456A), measure the output of the integrator (TP INT). The output should be 0V ±2mV. (Note: If there is oscillation present on TP INT, connect pin 6 of Q202 to ground.)

4. If the voltage is wrong, check for a defective Q202 or U201 and associated circuitry.

5. If the voltage is good, temporarily connect the junction of C203 and R209 to +5V. Measure the voltage at TP INT and make sure it is negative and above 12V. Then connect C203 and R209 to -12V. Make sure the voltage at TP INT is positive and above 12V.

6. If the voltages at TP INT are wrong, check for a defective Q202 or U201 and associated circuitry.

7. If the voltages at TP INT are good, the integrator is most likely operating correctly. Check for a defective U202, U203, and associated circuitry.

SERVICE GROUP C

DC VOLTMETER AND CURRENT SOURCE TROUBLESHOOTING

Service Group C Contents

8-C-1. INTRODUCTION

8-C-2. This service group has the 3497A voltmeter option's troubleshooting procedures, which includes procedures for the dc voltmeter and dc current source. The service group is symptoms oriented (i.e., what fails) with two levels of troubleshooting. The first level determines the general area of the option that causes the failure and the second level has specific information to troubleshoot the area that fails.

CAUTION

The voltmeter option contains CMOS Integrated Circuits which are extremely susceptible to failures due to static discharge. It is especially important that grounded tools and wrist straps be used when handling and troubleshooting these components.

8-C-3. PRE-TROUBLESHOOTING INFORMATION

8-C-4. The troubleshooting procedures in this service group require that the voltmeter option is to be set to certain ranges and functions. This is accomplished using the standard front panel (if installed), or using the HP-IB or Serial I/O bus (if the RS-232 option is installed). Make sure you know how to select the ranges and functions, before doing the procedures. Section III of this manual and the Operating, Programming, and Configuration Manual explains how to select the ranges and functions.

8-C-5. Before doing any troubleshooting to the voltmeter option, do the following:

a. Make sure the option's power supplies are good. These supplies are called the inguard power supplies and are located on the mainframe power supply board (A16 assembly, see Schematic D3). The supplies can be checked on the voltmeter option board. If the supplies are defective, go to Service Group D for troubleshooting. The supplies are as follows:

Power Supply	Checked at	Voltage Level
+30VL	TP +33	+33V to +44V
+15VL	TP +15	+14.25V to +15.75V
-15VL	TP -15	-14.25V to -15.75V
-18VL	TP -18	-17.1V to -18.9V
+5VL	TP +5L	+4.8V to +5.2V

b. Check the +12V, -12V, and buffered -12V reference supplies. Check the +12V at TP+12, -12V (-12VA) at -12, and buffered -12V (-12VB) at U700 pin 6. If the reference supplies are defective, go to Service Group D for troubleshooting.

c. Check the ALE (Address Latch Enable) clock at TP ALE. Make sure the clock is operating and is at the correct TTL voltage level. The time period of the clock is 2.564μS (390KHz) for 60Hz operation and 3.077μS (325KHz) for 50Hz operation.

8-C-6. Various FETs and relays are used to select the ranges in the voltmeter and current functions. These FETs and relays are turned on and off by comparators and transistors which are controlled by the inguard controller. Make sure the comparators and transistors receive the correct information from the controller before replacing them. If the inguard controller is inoperative, go to Service Group B for further troubleshooting.

8-C-7. Some troubleshooting procedures in this service group require that the Autozero function must be either on or off. Make sure the 3497A is in the correct mode, before doing any troubleshooting.

8-C-8. DC VOLTMETER TROUBLESHOOTING

8-C-9. General

8-C-10. The dc voltmeter consists of the following circuitry: input switching, input amplifier, and A/D converter. Since any of the circuitry can cause voltmeter failures, the defective area must first be isolated. Once this is done, troubleshooting can then be performed on the defective circuitry.

8-C-11. The procedures in paragraph 8-C-15 and the paragraphs following that paragraph isolates and then troubleshoots the defective area. To select the correct procedure, first determine the voltmeter failure and then select the appropriate paragraph. Unless otherwise specified, refer to Schematic C1 to troubleshoot the input switching circuitry and to Schematic C2 for the input amplifier.

8-C-12. Typical dc voltmeter failures are overload, inaccurate, constant zero, floating, or noisy readings on some or all ranges. A description of the different voltmeter failures is given in paragraph 8-54.

8-C-13. Equipment Required

8-C-14. The following is the required equipment for the procedures in the following paragraphs.

Digital Voltmeter -hp- Model 3456A
Stable Voltage Source-System Donner Model M107

8-C-15. Overload, Floating, Constant Zero (with input applied), Inaccurate, or Noisy Readings on All Ranges

8-C-16. Any of these failures can be caused by the input switching circuitry, input amplifier, or A/D converter (includes the A/D Logic). To determine the defective area, do the following procedure.

a. Set the 3497A voltmeter option to the 10V Range and turn Autozero off.

b. Check and make sure if the voltmeter failure is still present. If no failure is detected, the Autozero circuitry causes the failure. Go to paragraph 8-C-43. for troubleshooting. If the failure is still present, continue with step c.

c. Using the stable voltage source, apply + 10V dc to the HI COM and LO COM Input terminals located at the inguard section's rear panel.

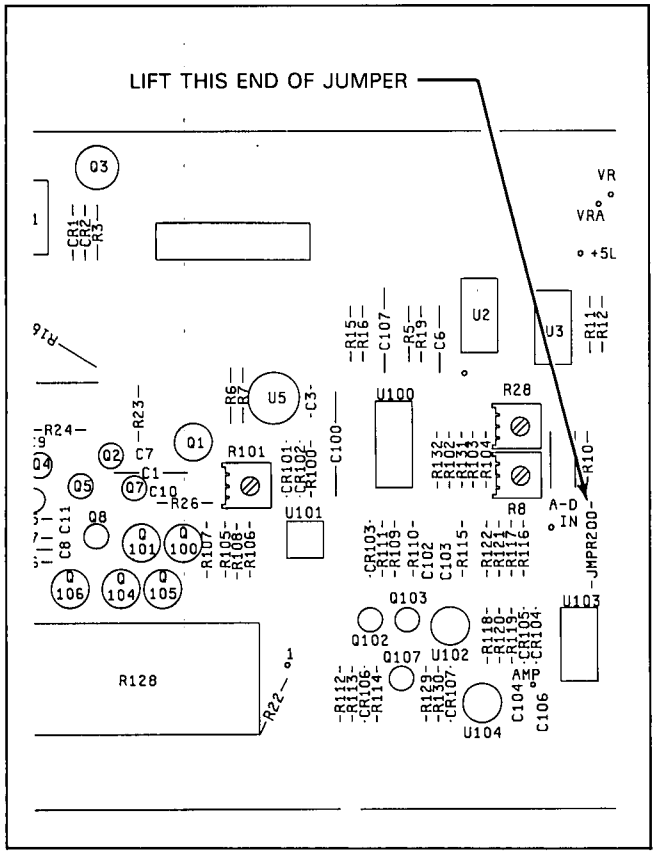


Figure 8-C-1. Jumper JMPR200 Lifted

d. Using the recommended Digital Voltmeter (the 3456A), measure for a stable + 10V at TP A-D IN (i.e., the input to the A/D converter, see Schematic C3)

e. If the + 10V reading on the test voltmeter is good, the A/D converter circuitry is defective. Go to Service Group B for troubleshooting.

f. If the reading on the test voltmeter is an overload, floating, constant zero, or noisy reading, unsolder and lift one end of jumper JMPR200. Lift the end of the jumper that is toward the top of the printed circuit board, as shown in Figure 8-C-1. The A/D Converter should now be disconnected from the input amplifier.

g. Measure for + 10V at jumper JMPR200. If the reading is now good, the A/D converter is causing the failure. Refer to Schematic C3 and check for a defective 108.33K ohm resistor in R200. If the resistor is good, try replacing Q200 and Q201.

h. If the reading is still wrong, measure for + 10V at the gate of dual FET Q101 (pin 3 of Q101 which is the junction of Q101, Q5, Q7, and Q8).

i. If the reading is good, troubleshoot the input amplifier. Go to paragraph 8-C-44 for troubleshooting.

j. If the reading is still wrong, the input switching is most likely defective. Since dual FET Q101 in the input amplifier circuitry can also cause the failure, remove the FET. If the reading is now good, replace FET Q101. If the reading is still wrong, troubleshoot the input switching circuitry. Go to paragraph 8-C-29 for troubleshooting.

NOTE

Make sure jumper JMPR200 is replaced, after troubleshooting the input switching and/or input amplifier circuitry.

8-C-17. Constant Zero Readings (with no input applied) on All Ranges

8-C-18. Refer to Schematic C1. The 100V Range of the voltmeter option will normally show a zero reading, with no input applied, since the 100:1 Divider is used in that range. The 100:1 Divider in effect places a 9.9M ohm resistor across the input terminals. With no external voltage applied, zero volts is measured across the 9.9M ohm resistor showing a zero reading. If the .1V, 1V, and 10V Ranges also show a zero reading, check and make sure relay K1 and Q2 are not shorted. If either component is shorted, a zero reading will show up on the .1V, 1V, and 10V Ranges, with no input applied to the voltmeter option.

8-C-19. Overload, Floating, or Noisy Readings on Some Ranges

8-C-20. Since only some of the ranges fail, these failures can only be caused by the feedback circuitry in the input amplifier, or the low voltage or high voltage paths in the input switching circuitry. This is because only a certain path and a certain feedback is used by a certain range. The following paragraphs list the ranges and possible failures.

8-C-21. Only the .1V Range Fails (Schematic C2). Check for an open or noisy Q105 or Q103, or a defective R128 in the input amplifier circuitry. Make sure Q105 is turned on by U103C.

8-C-22. Only the .1V, 1V, and 10V Ranges Fail (Schematic C1). Make sure the low voltage path in the input switching circuitry is good. Check for a defective Q4, Q9, Q10, and K2. Make sure FET Q4 and relay K2 are turned on by comparators U2A and U1B, respectively. FETs Q9 and Q10 can be checked by measuring the voltage at the junction of Q9, Q10, Q4, and R17 with the input terminals shorted. If the voltage at the junction is positive, Q9 is leaky. If the voltage at the junction is negative, Q10 is leaky.

8-C-23. Only the 1V and 100V Ranges Fail (Schematic C2). Check for an open or noisy Q106 or Q102, or a defective R128 in the input amplifier circuitry. Make sure Q106 is turned on by U103B.

8-C-24. Only the 10V Range Fails (Schematic C2). Check for an open or noisy Q104 or a defective R128 in the input amplifier circuitry. Make sure Q104 is turned on by U103A.

8-C-25. Only the 100V Range Fails (Schematic C1). Make sure the high voltage path in the input switching circuitry is good. Check for a defective Q2 and K1. Make sure the FET and relay is turned on by comparators U2D and U1A, respectively. Also make sure the 100:1 divider in R128 and R4 is good.

8-C-26. Only the .1V Range is Good (Schematic C1). Make sure that Q105 or Q103 in the input amplifier circuitry is not shorted. A shorted Q105 can make the .1V Range good and the other ranges fail. Also make sure Q105 is not turned on by U103C on other than the .1V Range.

8-C-27. Only the 1V and 100V Ranges are Good (Schematic C2). Make sure that Q106 or Q102 in the input amplifier circuitry is not shorted. A shorted Q106 can make the 1V and 100V Ranges good and the other ranges fail. Also make sure Q106 is not turned on by U103B in other than the 1V and 100V Ranges.

8-C-28. Only the 10V Range is Good (Schematic C2). Make sure that Q104 in the input amplifier circuitry is not shorted. A shorted Q104 can make the 10V Range good and the other ranges fail. Also make sure Q104 is not turned on by U103A in other than the 10V Range.

8-C-29. INPUT SWITCHING TROUBLESHOOTING

8-C-30. General

8-C-31. Before troubleshooting the input switching circuitry, make sure the failure is not in the input amplifier. Go to paragraph 8-C-8 to determine the faulty circuitry.

8-C-32. Failures caused by the input switching circuitry can be overload, floating, constant zero, inaccurate, or noisy readings on all ranges. If the failures show up on only some of the ranges, go to paragraph 8-C-19 for troubleshooting. The failures on all ranges can show up with both Autozero enabled or disabled. If the failure only shows up with Autozero enabled, the Autozero circuitry is at fault. Go to paragraph 8-C-43 for troubleshooting. If the failure shows up with both Autozero enabled or disabled, go to paragraph 8-C-35 and the paragraphs following that paragraph for troubleshooting information. Unless otherwise noted, refer to Schematic C1 for troubleshooting.

8-C-33. Equipment Required

8-C-34. The following is the required equipment to test and troubleshoot the input switching circuitry.

Digital Voltmeter - -hp- Model 3456A

8-C-35. Overload, Floating, Constant Zero, Inaccurate, or Noisy Readings on All Ranges

8-C-36. The following paragraphs have troubleshooting information for failures on all ranges. For failures on some ranges, go to paragraph 8-C-19.

8-C-37. Overload Readings. An overload is normally caused when the input to the input amplifier is above ±12V. This can be caused when the gate of a FET that is turned off is shorted to the input of the amplifier. Since a FET is normally turned off by applying -18V to its gate, a shorted FET will apply this voltage to the input of the amplifier. Make sure Q7 and Q8 are good.

8-C-38. Overload readings (and floating readings, see next paragraph) can also be caused if the gate bias amplifier is inoperative. This could prevent the FETs from turning on and open the paths between the input terminals and input amplifier. With the paths open, a floating reading is normally noted. However, the reading could drift high enough to cause an overload. To check the amplifier, do the following:

a. Set the voltmeter option to the 10V Range and turn Autozero off.

b. Apply + 10V to the HI COM and LO COM Input terminals.

c. Connect the input of the gate bias amplifier to the HI COM Input terminal.

d. Using the test Digital Voltmeter, measure for +10V at the output of the gate bias amplifier. Since the gate bias amplifier is a X1 gain non-inverting amplifier, its output is at the same value (within ±5mV) as its input. If the output is different from the input, check for a defective Q1 or U5.

8-C-39. Floating Readings. This can be caused if the path from the input terminals to the input amplifier is open. Since all ranges are inoperative, check for an open Q5 or a defective gate bias amplifier. A procedure to check the gate bias amplifier is in paragraph 8-C-38. FET Q5 can be checked by doing the following:

a. Turn Autozero off and then apply +10V to the HI COM and LO COM Input terminals.

b. Short the source to the drain of Q5.

c. The 3497A should now display +10V.

d. If the reading is incorrect, check for an open path between Q5 and the input amplifier.

e. If the reading is good, check for an open Q5. Make sure Q5 is turned on by U2B. The gate of Q5 should be at approximately +10V (when +10V is applied to the input terminals). If the gate voltage is wrong, check for a defective U2B and associated circuitry and make sure the gate bias amplifier is good (refer to paragraph 8-C-38). (Note: The HDZ line should be low with Autozero off.)

8-C-40. Constant Zero Readings. This failure can only be caused when the input to the input amplifier is shorted to ground (i.e., to the LO COM terminal). Do the following:

a. Turn Autozero off.

b. Make sure Q7 is turned off by measuring approximately -18V at its gate.

c. If the voltage is good, check for a shorted Q7. If incorrect, check for a defective U2C and associated circuitry. (Note: The HDZ line should be low with Autozero off.)

8-C-41. Inaccurate Readings. Inaccurate readings are normally caused by leaky FETs in the input switching circuitry. Since all ranges are inaccurate, the most likely causes are a leaky Q7 and Q8.

8-C-42. Noisy Readings. Make sure the gate bias amplifier is good (refer to paragraph 8-C-38 to check the amplifier). Check for a noisy Q5 and Q7.

8-C-43. Failures with Autozero Enabled. If any dc voltmeter failures only show up with the Autozero function enabled, check for a defective Q5, Q7, or Q8. Do this because these FETs are the only devices being switched on and off with Autozero enabled.

8-C-44. INPUT AMPLIFIER TROUBLESHOOTING

8-C-45. General

8-C-46. Before troubleshooting the input amplifier circuitry, make sure the failure is not in the input switching circuitry. Go to paragraph 8-C-8 to determine the faulty circuitry.

8-C-47. Failures caused by the circuitry in the input amplifier can be overload, floating, constant zero, inaccurate, or noisy readings on all ranges. The circuitry in the input amplifier includes a dc amplifier, integrator amplifier, and feedback circuitry. Paragraph 8-C-50 and the paragraphs following that paragraph have the failures, procedures to isolate the different circuitry, and information on how to troubleshoot the isolated circuitry. Unless otherwise noted, refer to Schematic C2 for troubleshooting.

8-C-48. Equipment Required

8-C-49. The following is the required equipment to test and troubleshoot the input amplifier circuitry.

Digital Voltmeter -hp- Model 3456A
Oscilloscope -hp- Model 1741A

8-C-50. Overload, Floating, Constant Zero, Inaccurate, or Noisy Readings on All Ranges

8-C-51. The following paragraphs have troubleshooting information for failures on all ranges. For failures on some ranges, go to paragraph 8-C-19.

8-C-52. Overload or Noisy Readings. Overloads can be caused by a saturated output (i.e., above ±12V) of the input amplifier. Overload readings and also noisy readings can be caused if the amplifier output is oscillating. Do the following to determine the failure and defective circuitry.

a. Set the voltmeter option to the .1V Range and turn Autozero off.

b. Using a short clip lead, connect the gate of Q101 (pin 3 of Q101 which is the junction of Q101, Q5, Q7, and Q8) to ground.

c. Connect the test oscilloscope to TP AMP and look for oscillation on the scope. Check for oscillation on the other voltmeter option ranges.

d. If no oscillation is present, continue with step e. If oscillation is present, do the following:

1. Check for a defective feedback capacitor (C103) and compensating capacitor (C102) used by the integrator amplifier (U102). The capacitors can be easily checked by connecting another capacitor with the same value in parallel with the suspected defective capacitor.

2. If the capacitors are good, replace U102.

e. Remove the oscilloscope from TP AMP and set the voltmeter option to the 10V Range. Leave the gate of Q101 connected to ground.

f. Connect the test Digital Voltmeter (the 3456A) to TP AMP. Measure for approximately 0V.

g. If the voltage is approximately 0V but noisy (i.e., >10uV change), continue with step h. If the voltage is saturated (i.e., above ±12V), do the following:

1. Make sure diodes CR105 or CR104 are good. If CR104 is shorted, -15V is applied to the amplifier output and if CR105 is shorted, +15V is applied. If the diodes are good, continue with step 2.

2. Leave the gate of Q101 connected to ground and leave the voltmeter option in the 10V Range.

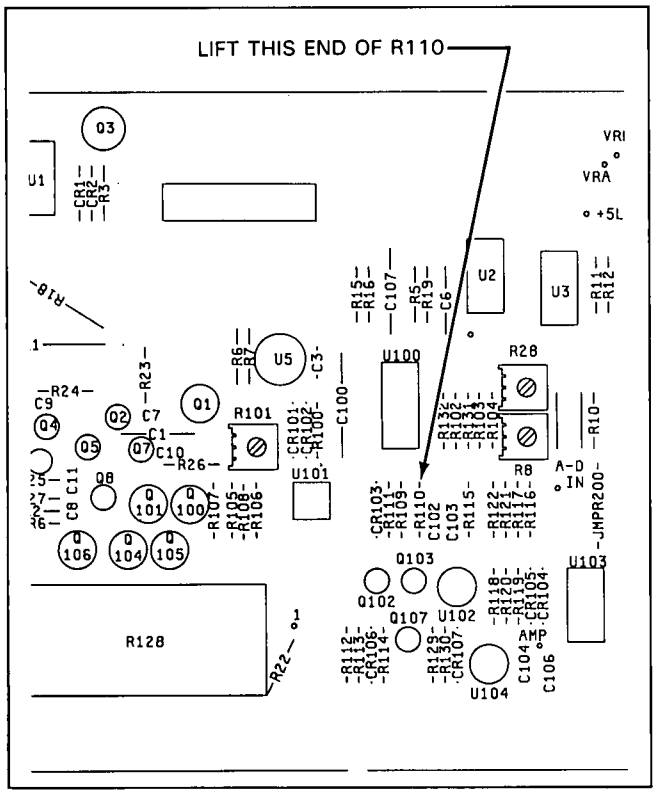


Figure 8-C-2. Removing R110

3. Using another clip lead, carefully connect the output (test point AMP) of the input amplifier to the other gate of Q101 (pin 6 of Q101 which is the junction of Q101, Q104, Q105, and Q106).

4. If the output of the input amplifier is now good (i.e., approximately 0V, ±10mV), feedback FET Q104 may be defective. Since all ranges fail, make sure that Q104 and the other feedback FETs are good and that the appropriate FET is turned on by the appropriate comparator in U103. If the FETs and U103 are good, make sure decoder U105 and is good and that the decoder receives the correct information from the inguard controller.

5. If the output is still saturated, turn the 3497A off.

6. Remove the clip lead from TP AMP and Q101. Leave the other clip lead connected.

7. Unsolder and lift one side of R110 from the printed circuit board, as shown in Figure 8-C-2.

8. Using a clip lead, connect the gate of Q104 to the -18V supply (TP -18).

9. Carefully short the gate of Q101 (pin 6 of Q101 which is the junction of Q101, Q104, Q105, and Q106) to ground.

CAUTION

Make sure the clip leads connected to Q101 do not touch any other components on the printed circuit board, or internal damage to the input amplifier circuitry may occur.

10. Turn the 3497A on and set the voltmeter option to the 10V Range.

11. Using the test Digital Voltmeter, measure for approximately +5V at U101 pin 6. (The OFFSET ADJUST, R101, may have to be adjusted to measure +5V.)

12. If the voltage is good, dual FETs Q100 and Q101, and U101 are good. Try replacing U102 and then resolder R110.

13. If the voltage is incorrect, measure the voltage at pins 2 and 3 of U101. The voltage at the pins should be approximately the same and range from +20V to +25V. If the voltages are good, try replacing U101 and associated circuitry. If the voltages are not equal, check for a defective Q100, Q101, U106, and associated circuitry. Resolder R110 and perform the adjustment procedure for R101 in Section IV of this manual.

h. To troubleshoot for a noisy input amplifier, leave the clip lead connected from the input of the amplifier (pin 3 of Q101) to ground and do the following:

1. Connect the other gate of Q101 (pin 6 of Q101 which is the junction of Q101, Q104, Q105, and Q106) to ground.

2. Using the test Digital Voltmeter, measure the voltage at pins 2 and 3 of U101. The voltage should be quiet and steady with less than 1mV change. (Note: The voltage may have a slow drift, if the 3497A has only been on for a short time.)

3. If the voltages are noisy, replace Q100, Q101, U106, or associated circuitry.

4. If the voltages at pins 2 and 3 are good, measure the voltage at the output (pin 6) of UI101. Make sure the voltage is a steady and quiet +5V (<50μV change). If the voltage is good, replace U102. If the voltage is noisy, try U101.

NOTE

Do the R101 adjustment in Section IV of this manual, if Q100, Q101, or U101 are replaced.

8-C-53. Floating Readings. Floating readings can be caused if the input to the input amplifier is open. To check this, connect the gate of Q101 (pin 3 of Q101 which is the junction of Q101, Q5, Q7, and Q8) to ground. If the output of the input amplifier, measured at TP AMP, is at approximately zero volts, the input circuitry is causing the failure. If a floating reading is still noted, the gate of Q101 may be open. Replace Q101. Do the R101 adjustment in Section IV of this manual, if Q101 is replaced.

8-C-54. Constant Zero Readings. This can only be caused if there is a short to ground at the input or output of the input amplifier. Make sure the gate of Q101 (pin 3 of Q101 which is the junction of Q101, Q5, Q7, and Q8) and TP AMP are not shorted to ground.

8-C-55. Inaccurate Readings. Inaccurate readings can only be caused by an excessive offset and a non-linear input amplifier. The excessive offsets can most of the time be adjusted out by R101 (see Section IV of this manual for the procedure). If an excessive offset is noted or the amplifier is not linear, try replacing Q100, Q101, or U101. Do the R101 adjustment in Section IV of this manual, if Q100, Q101, or U101 are replaced.

8-C-56. DC CURRENT SOURCE TROUBLESHOOTING

8-C-57. The dc current source consists of the following circuitry: reference, gate bias amplifier, selectable feedback resistors, high voltage protection, and floating power supply. Procedures to isolate the defective circuitry is in paragraph 8-C-62 and the paragraphs following that paragraph. To select the correct procedure, first determine the failure and then select the appropriate paragraph. An explanation of the failure is given in paragraph 8-61. Unless otherwise specified, refer to Schematic C4 for troubleshooting.

8-C-58. Equipment Required

8-C-59. The following is the required equipment to test and troubleshoot the dc current source.

Digital Voltmeter -hp- Model 3456A
Oscilloscope -hp- Model 1741A

8-C-60. Other equipment required is a milliamp meter or a resistor/voltmeter combination to check current. For example, to check the 1mA Range using the milliamp meter, measure the current directly. To measure the current using the resistor/voltmeter combination, measure for 1V across the resistor. The voltage can be checked using the test Digital Voltmeter (the 3456A). The value of the voltage depends on the value of the resistor and the current.

8-C-61. High, Low, Noisy, or No Current on Some Ranges

8-C-62. These failures can only be caused if the incorrect feedback resistors are selected, by defective feedback resistors, or by defective resistors in the range adjustment circuitry (i.e., R409 through R411 and associated circuitry). Make sure relay K401, K402, and K403 are selected for the 10μA, 100μA, and 1mA Ranges, respectively. Also make sure that only one relay is enabled for a particular range and that the range resistors are good. Since the relays are selected by decoder U400, make sure the decoder is good before replacing a relay. If U400 is good, the inguard controller may be defective (troubleshooting information for the inguard controller is in Service Group B). The decoder receives the relay select (i.e., range select) information over the BCS and CCS lines. The following lists the state of the lines, and corresponding ranges and selected relays.

BCS	CCS	Range	Relay On
High	High	None	None
Low	Low	10μA	K401
Low	High	100μA	K402
High	Low	1mA	K403

8-C-63. High, Low, Noisy, or No Current on All Ranges

8-C-64. These failures can be caused by any of the circuitry in the current source. To determine the defective circuitry and then troubleshoot the circuitry, do the following procedure. In the procedure, the test Digital Voltmeter is used to check certain voltages. Unless otherwise specified, connect the LOW Input lead of the voltmeter to the F.GND (floating ground) test point. This

is the low reference point of the current source. Do the following:

a. Using the test Digital Voltmeter, measure the ± 17.2V floating power supplies. The power supplies can have a value of 17.2V ± 10% (15.48V to 18.92V). Make sure the supplies are stable.

b. If the power supplies are good, continue with step c. If the power supplies are incorrect or noisy, go to paragraph 8-C-66 for troubleshooting.

c. Set the current source to the 1mA Range and connect either a 1K ohm resistor or a milliampmeter to the HI and LO Output terminals. The resistor and milliampmeter are used to determine the current source failure. They serve no other function.

d. If a high or low current is output by the current source, as shown across the 1K ohm resistor or by the milliampmeter, the range resistors in R128 may be defective. This depends on how high or low the current is. If the current is out of the specified limits a small amount (e.g., < 10%), the resistors are most likely defective. If the current is radically wrong, other circuitry may be defective. Continue with step f for further troubleshooting. (Note: The resistor values in R128 may not be exactly the value shown. The ratio of the resistor values are important, since that, not the actual values, generates the correct currents.)

e. If no current or noisy current is output by the current source, do the following:

1. Make sure R414 is not open. If the resistor is good, using a clip lead, connect the LO Output terminal to the emitter of Q404. This isolates the high voltage protection circuitry from the rest of the circuitry.

2. If no current or noisy current is still output, more isolation is necessary. Go to step f for further isolation.

3. If the correct current is now output, the high voltage protection circuitry is open. Continue with the next step.

4. Disconnect the clip lead from the emitter of Q404 and connect it to the collector (i.e., cathode of CR402).

5. If the current is still correct, CR402 may be open. Replace the diode. If no current or noisy current is now output, check for a defective Q404, Q403, and CR406.

f. Using the test Digital Voltmeter, measure the voltage at pin 22 of R128. The voltage should be approximately -11V (-10.45 to -11.55V) and stable.

g. If the voltage is good, continue with step h. If the voltage is wrong, do the following:

1. Check U401 and the 20.4844K ohm resistor in R128 by measuring for approximately -3.5V (-3.2V to -3.8V) at pins 2 and 3 of U401.

2. If the voltages at pins 2 and 3 of U401 are other than -3.5V and are quiet, and the voltages at the pins are approximately equal to each other, U401 is probably good. Check for a defective CR400, CR401, and R128. Also, make sure R400 and R401 are good.

3. If the voltage at pins 2 and 3 of U401 are not equal and are noisy, try replacing U401.

h. Measure for approximately -3.5V (-3.2V to -3.8V) at pins 2 and 3 of U402. If the voltages are other than -3.5V and are quiet, and the voltages at the pins are approximately equal to each other, try replacing R128.

i. If the voltages are not equal and are noisy, remove Q401. Since Q401 is only used when no load is connected to the the HI and LO Output terminals, the current source should operate with Q401 removed.

j. If the current source is still inoperative, try replacing U402 or Q400.

8-C-65. Floating Power Supply Troubleshooting

8-C-66. The floating power supply is used to supply the reference voltages and supply voltages for the current source circuitry. If the supply is inoperative, do the following checks using the test Digital Voltmeter.

a. If only the + 17.2V supply is inoperative, check for a defective Q302, CR311, and associated circuitry.

b. If only the -17.2V supply is inoperative, check for a defective Q307, CR310, and associated circuitry.

c. If both the ± 17.2V supplies are inoperative, check the voltages at the bridge rectifier consisting of CR302 through CR305. Check for approximately + 22V at the junction of CR304 and CR305, and -22V at the junction of CR302 and CR303.

d. If the voltages are good, check the + 17.2V and -17.2V supplies by doing steps a and b in this procedure.

e. If the voltages are wrong, check for a defective diode in CR302 through CR305. If the diodes are good, using the oscilloscope, check for a 0 to + 5V square wave at pin 3 of U300. The time period of the square wave should be approximately be 25μS for 60Hz operation or 30μS for 50Hz operation. Make sure the square wave is stable.

f. If the square wave is missing or unstable, U300 is most likely defective. Before replacing U300, make sure the ALE clock is present and stable. Do this since a missing or unstable ALE clock could also cause the square wave to be missing or unstable.

g. If the square wave is good, check for a 0 to +5V square wave at pins 1 and 14 of comparator U301. The time period of the square wave should be approximately 50μS for 60Hz operation or 60μS for 50Hz operation. Make sure the waves are stable.

h. If any of the square waves are missing or unstable, check for a defective U301 and associated circuitry.

i. If the square waves are good, check for a defective Q300 and Q301. If the transistors are good, check for a defective T300 and T301.

SERVICE GROUP D
MISCELLANEOUS TROUBLESHOOTING

Service Group D Contents

8-D-1. INTRODUCTION

8-D-2. This service group has information on how to troubleshoot the 3497A's power supplies, battery charger, and the voltmeter option's reference supplies.

8-D-3. POWER SUPPLIES TROUBLESHOOTING

8-D-4. The outguard section of the 3497A has three power supplies, a +5V O.G. (outguard, regulated), +12V OUTGUARD REF, and -12V OUTGUARD supply. The inguard section has eight supplies, a +30VL (unregulated), +15VL, -15VL, -18VL REG., +5V (both LOGIC and RELAY), +19VG, -19VG, and -8V T.C. supply. The following paragraphs have troubleshooting information for the supplies.

8-D-5. Outguard Power Supplies Troubleshooting

8-D-6. The following paragraphs have troubleshooting information for the outguard power supplies. Refer to Schematic D2 for troubleshooting.

8-D-7. ±12V OUTGUARD Supplies. Since these supplies are simple raw and unregulated supplies, make sure the bridge rectifier (consisting of CR9, CR10, CR13, and CR14) is good. Also make sure that the current limiting resistors (RT49 and RT80) are not open.

8-D-8. +5V O.G. Supply. This is a regulated supply that uses U1 to develop the correct output voltage. To check the power supply, do the following:

a. Make sure breakdown diode CR3 is at the correct value (+5V 50 to +6.2V). If the voltage is wrong, replace CR3.

b. Make sure pin 6 of U1 is approximately +7.3V. If the voltage is wrong, replace U1.

c. Make sure the power supply is not in current limit. Check this by doing the following:

1. Remove the outguard logic board and any outguard option boards from the instrument. Also unplug the front panel board.

2. If the power supply is good, the supply is either loaded down by a board or resistors R23 and R24 have changed value.

3. If the resistors are good, make sure that pin 1 of U2 is at approximately +11V.

4. If the voltage is wrong, troubleshoot U1 and associated circuitry.

d. Make sure pin 10 of U1 is approximately +5.7V. If the voltage is wrong, replace U1 or Q7.

e. Try replacing Q1.

8-D-9. Inguard Power Supplies Troubleshooting

8-D-10. The following paragraphs have troubleshooting information for the inguard power supplies. Before troubleshooting the supplies, make sure they are not loaded down by the inguard controller board or any analog plug-in option boards. Refer to Schematic D3 for troubleshooting.

8-D-11. +30VL Supply. Since this supply is a simple raw and unregulated supply, make sure the bridge rectifier (consisting of CR19, CR20, CR24, and CR25) is good.

8-D-12. +15VL, -15VL, -18VL, and +5V LOGIC Power Supplies. These supplies use the same bridge rectifier as the +30VL supply. Make sure the rectifier is good, if all power supplies are defective. If only one supply is defective, the most likely cause is the corresponding voltage regulator. Try replacing the appropriate regulator.

8-D-13. +19VG and -19VG Supplies. If both supplies are defective, check the bridge rectifiers (CR36, CR37, CR41, and CR42). If one supply is defective, replace the corresponding voltage regulator.

8-D-14. BATTERY CHARGER TROUBLESHOOTING

8-D-15. The battery charger circuitry consist of the following circuitry: Battery Regulator and Battery Charger. Refer to Schematic D2 for the troubleshooting information in the following paragraphs.

8-D-16. Battery Regulator. Check the following:

a. Make sure Q6 is good. This transistor is the BATTERY power supply when the 3497A is operating on ac power.

b. Make sure that pin 1 of U11 is 0V when the 3497A is operating on ac power. If the voltage is wrong, troubleshoot U11 and associated circuitry. If the voltage is zero, remove the power cable from the instrument. The voltage should then change to approx-

imately +4.6V. If the voltage is wrong, troubleshoot U11 and associated circuitry.

8-D-17. Battery Charging Circuitry. Check the following:

a. Make sure that pin 7 of U2 is approximately +10V.

b. If the voltage is good, make sure that the base of Q1 is 124 approximately +11.3V. Check Q2 and CR1, if wrong.

c. Try replacing Q1.

8-D-18. VOLTMETER OPTION REFERENCE SUPPLIES TROUBLESHOOTING

8-D-19. Refer to Schematic D1 for the reference supplies troubleshooting. Do the following:

a. If the -12VA supply is wrong, the rest of the supplies should also be wrong. Make sure pin 6 of U601 is approximately -12.6V. If the voltage is wrong, make sure pin 2 of U601 is approximately -6.9V. If pin 1 is wrong, replace U600. If pin 1 is good, try Q700 or U601.

b. If the -12VB supply is wrong and the -12VA is good, replace 140 U700.

c. If the +12V supply is wrong, replace U701.

SERVICE GROUP E
SCHEMATICS AND BLOCK DIAGRAMS

8-E-1. INTRODUCTION

8-E-2. This Service Group has all the Schematics and Block Diagrams for the 3497A's mainframes (both standard HP-IB mainframe and Serial I/O mainframe), standard front panel, and voltmeter option. The Service Group is separated as follows:

GENERAL SCHEMATIC NOTES

1. RESISTANCE IN OHMS, CAPACITANCE IN MICROFARADS, INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
2. ASTERISK DENOTES A FACTORY-SELECTED VALUE. VALUE SHOWN ON SCHEMATIC TYPICAL.
3. ENCLOSES FRONT PANEL MARKING.
4. ENCLOSES REAR PANEL MARKING.
5. CIRCUIT ASSEMBLY BORDERLINE.
6. OTHER ASSEMBLY BORDERLINE. ALSO USED TO INDICATE MECHANICAL INTERCONNECTIONS (GANGING).
7. \918/ DENOTES WIRE COLOR CODE. CODE USED IS SAME AS THE RESISTOR OR COLOR CODE. FIRST NUMBER IDENTIFIES THE BASE COLOR, SECOND NUMBER IDENTIFIES THE NARROWER STRIPE.

   E.G. \918/ DENOTES WHITE BASE, BROWN WIDE STRIPE, GRAY NARROW STRIPE.
8. DENOTES GROUND ON FLOATING COMMON CIRCUITRY.
9. DENOTES GROUND ON CHASSIS COMMON CIRCUITRY. CONNECTED TO INSTRUMENT FRAME GROUND.

Figure 8-E-1. General Schematic Notes

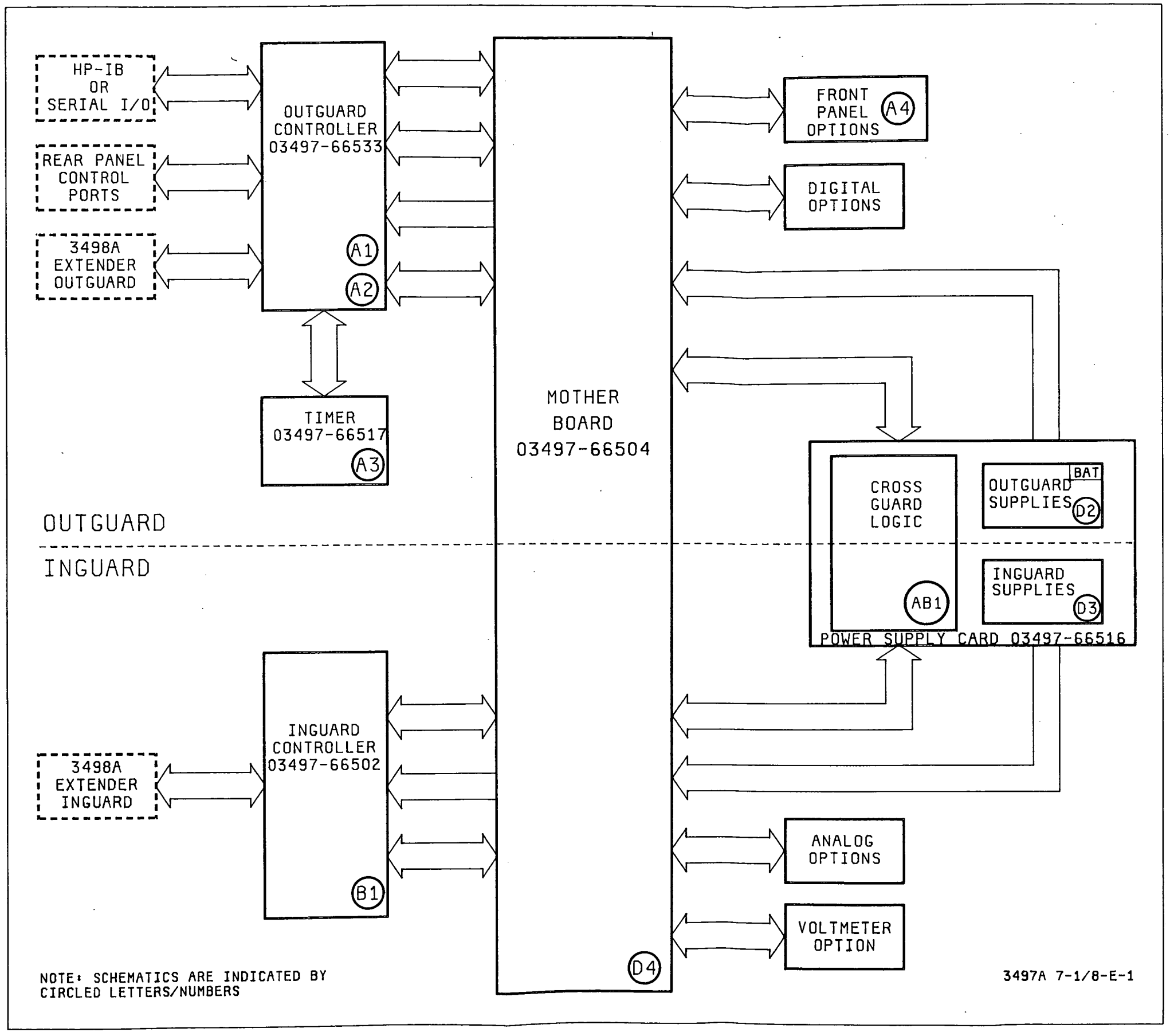


Figure 8-E-2. 3497A Block Diagram

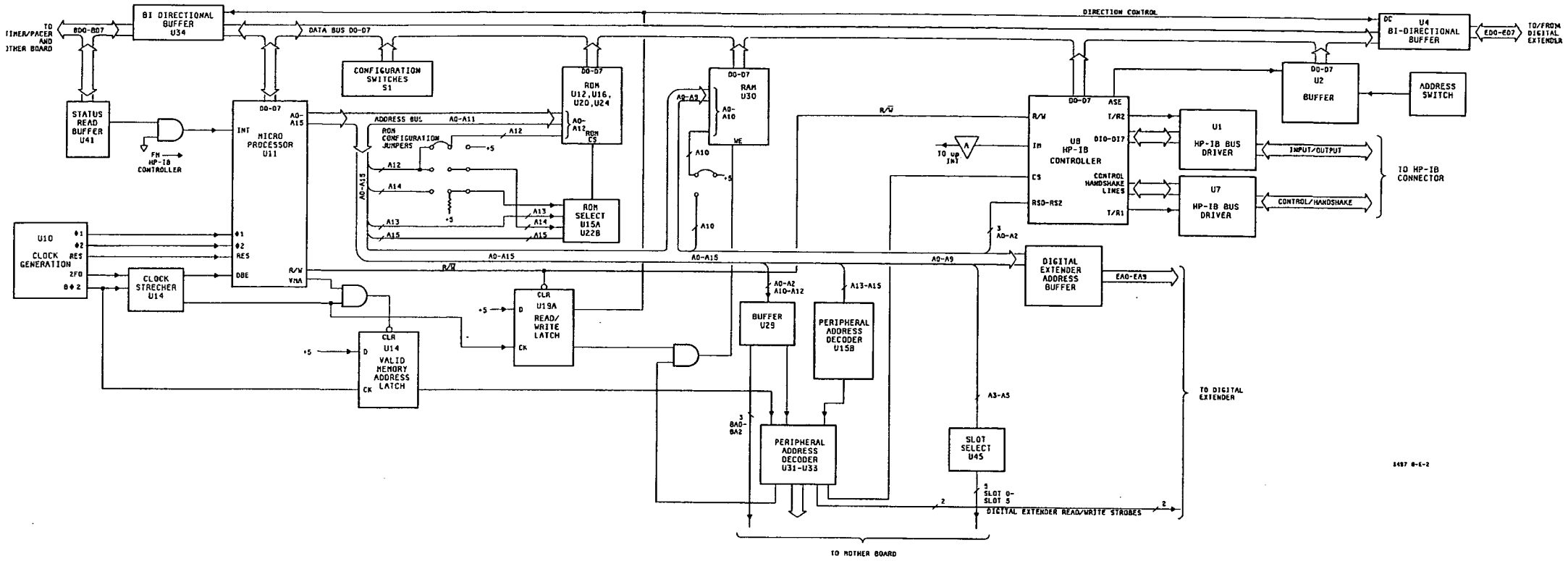


Figure 8-E-3. Outguard and HP-IB Controller Block Diagra

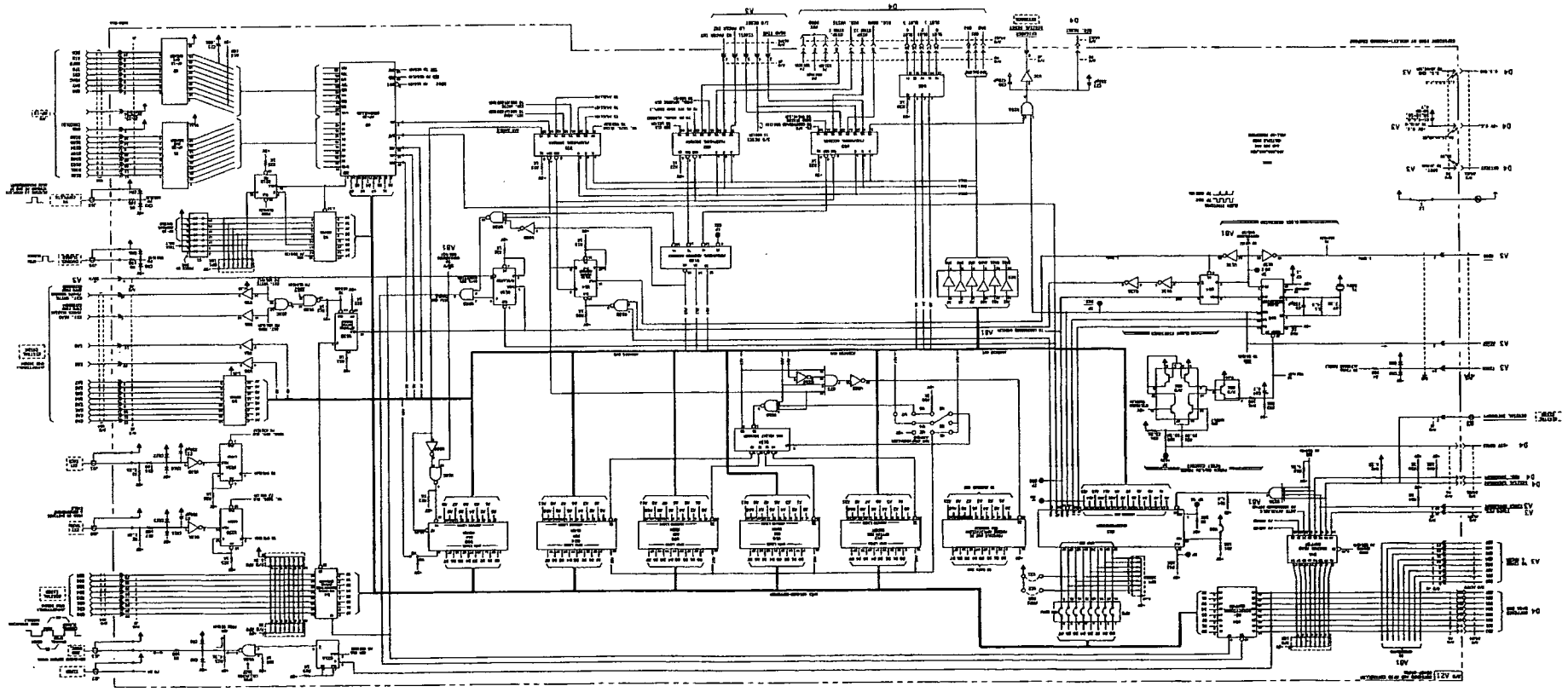


Figure 8-E-4. Outguard and HP-IB Controller (Schematic A1)
8-E-3

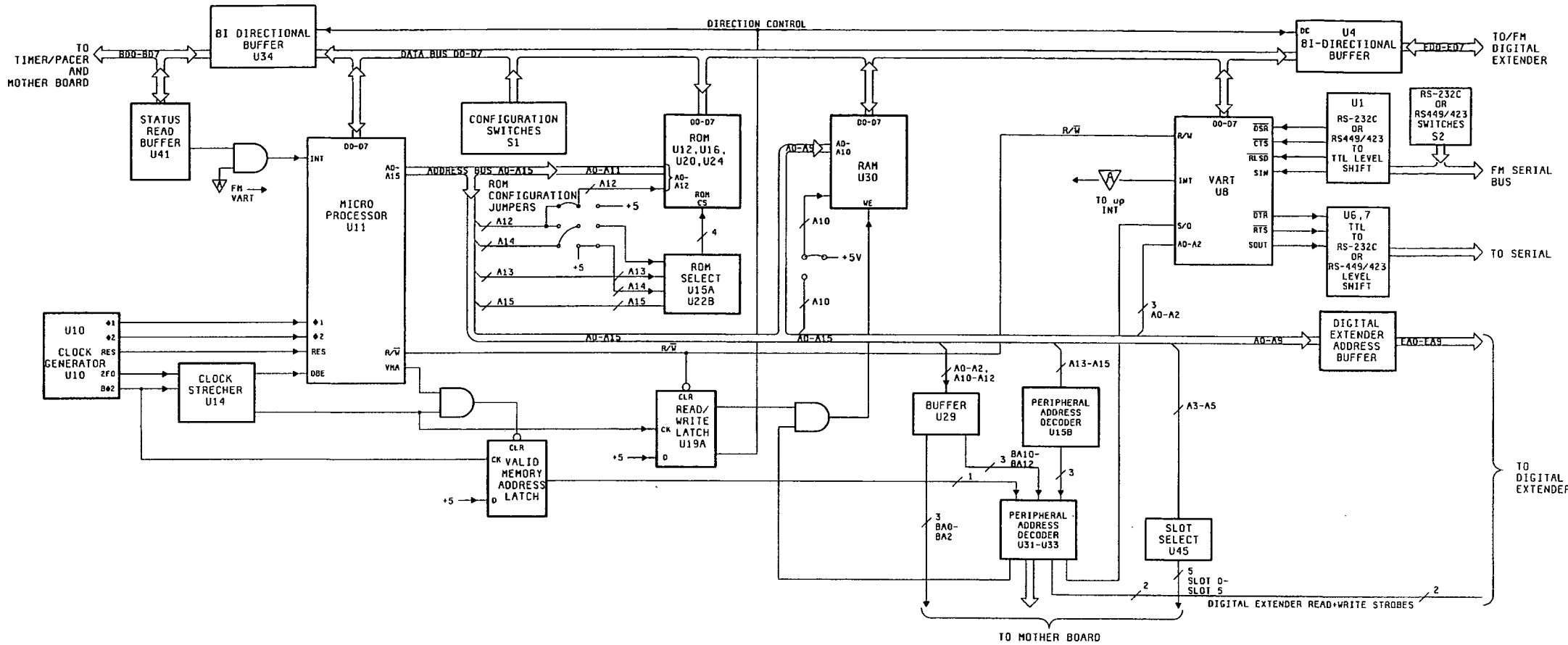
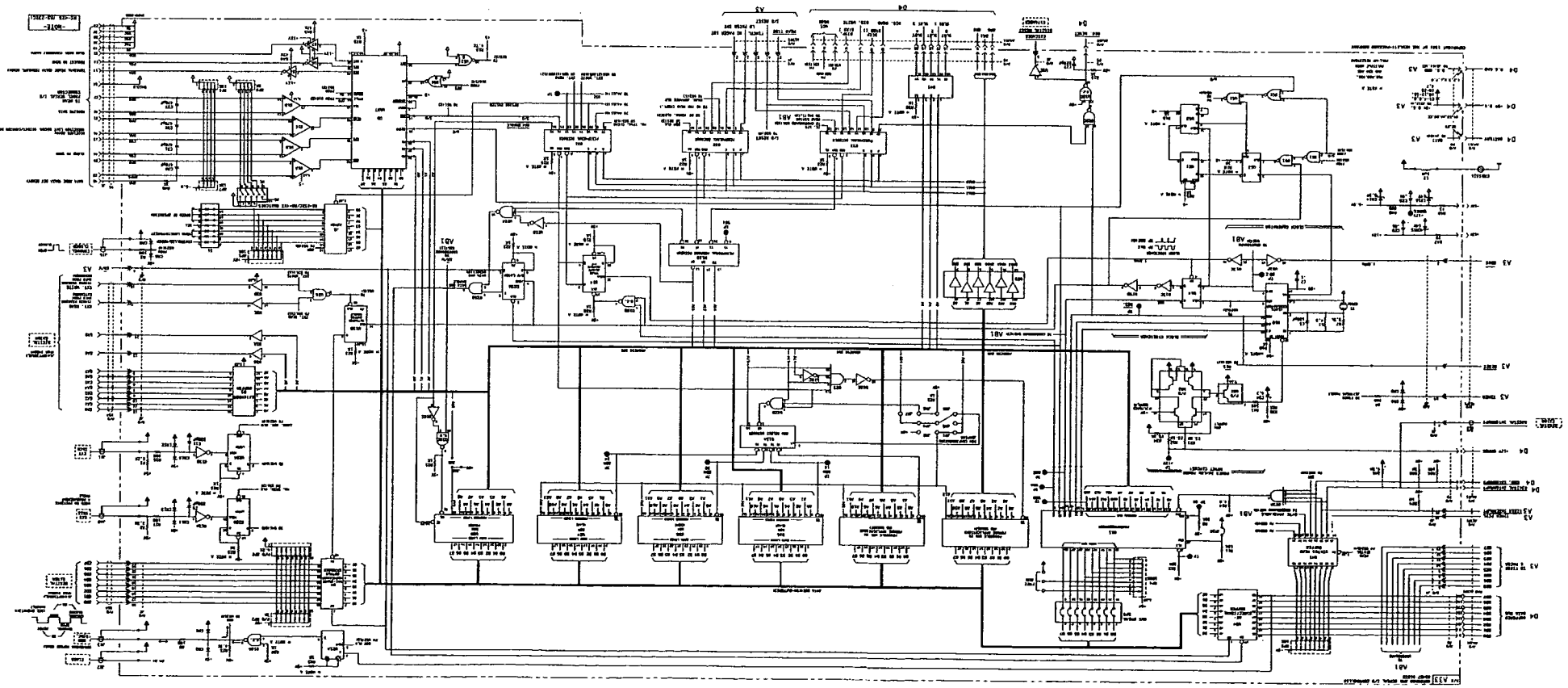


Figure 8-E-5. Outguard and Serial I/O Controller Block I



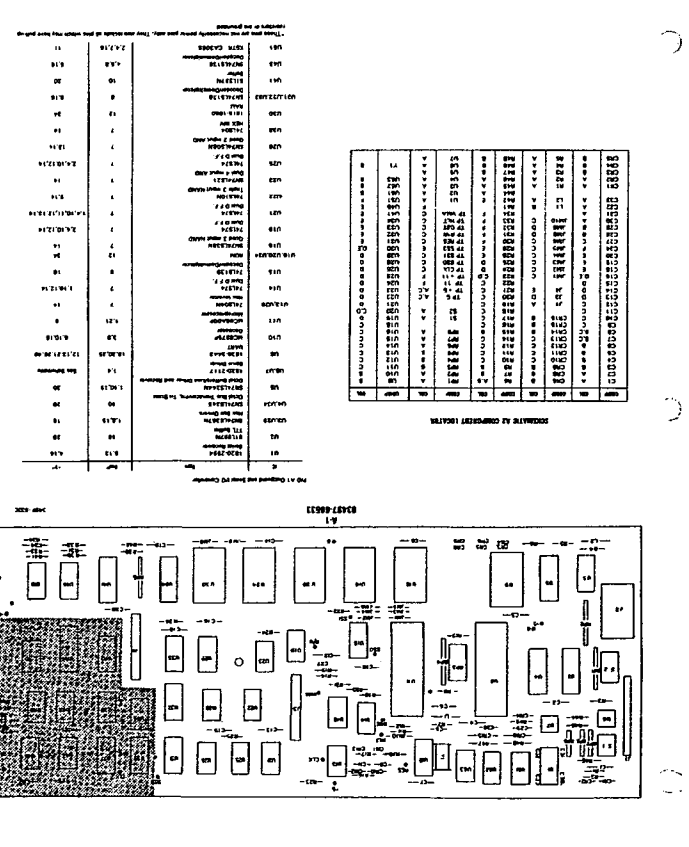


Figure 8-E-6. Outguard and Serial I/O Controller (Schematic A2)

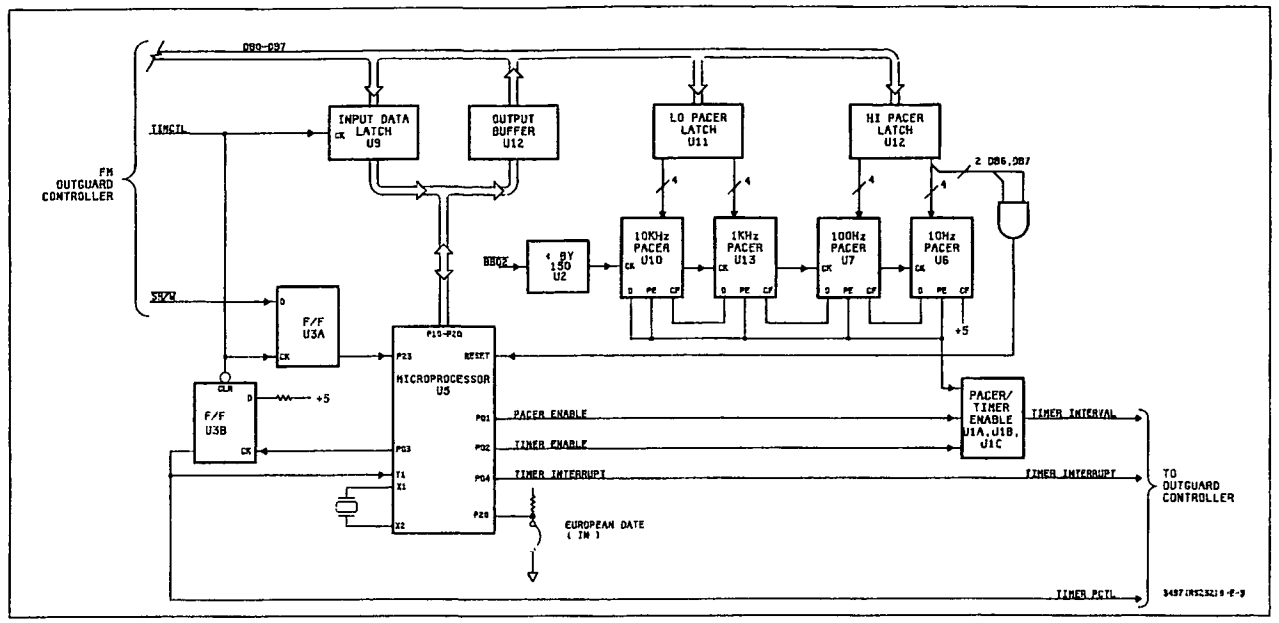
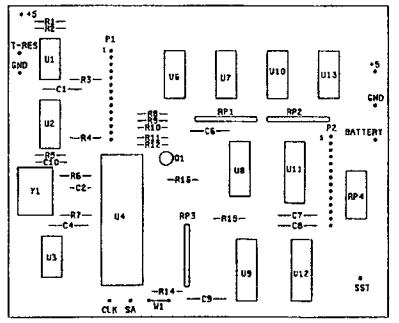


Figure 8-E-7. Timer/Pacer Block Diagram

P1 GOES TO OUTGUARD BD. (A21J3 or A1J3)
P2 GOES TO OUTGUARD BD. (A21J4 or A1J4)



A17
03497-66517

A17 Timer and Pacer

RC	Type	Gnd*	+5*
U1	SN74LS02N Quad 2 Input NAND	7	14
U2	MC14569 Dual BCD Counter	2,3,6,8,10,12,13	4,5,7,11,14,16
U3	74LS74 Dual D F.F.	7	12,14
U4	Microprocessor AM 8048 PC	7,20	40
U5	For possible future up-date		
U6	MC14522CP BCD divide-by-N counter	4,8,10	13,16
U7,U10,U13	MC14522CP BCD divide-by-N counter	4,8,10	16
U8,U11	74LS273 Octal D F F.	10	20
U9	SN74LS374 Octal D F F.	10	20
U12	81LS97N Buffer	10	20

*These pins are not necessarily power pins only. They also include all pins which may have pull-up resistors or are grounded.

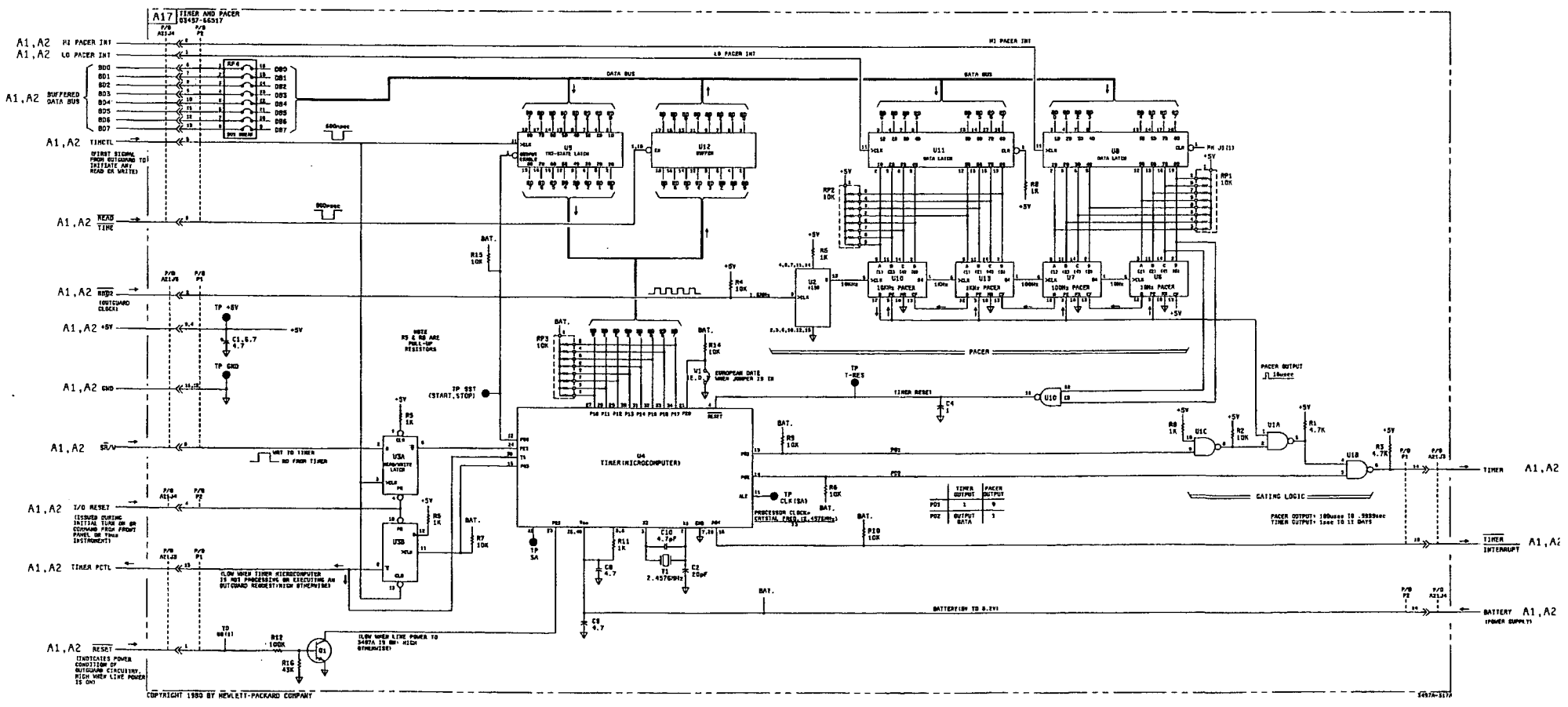


Figure 8-E-8. Timer/Pacer Circuitry (Schematic A3)

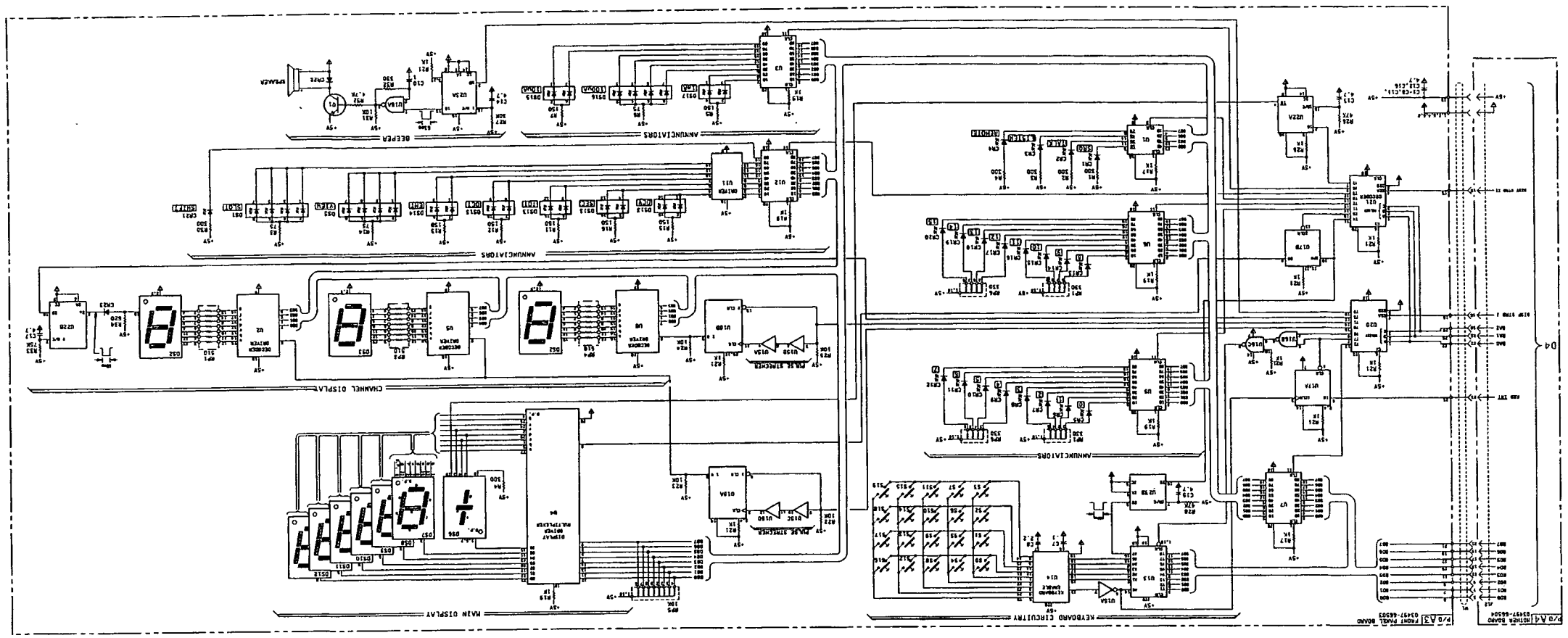
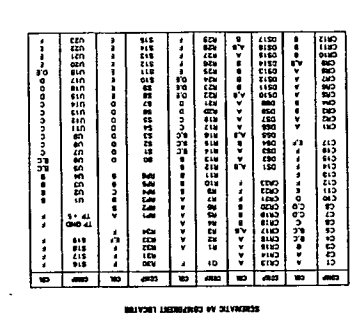


Figure 8-E-9. Front Panel Circuitry (Schematic A4)



SCHEMATIC A4 COMPONENT LOCATOR

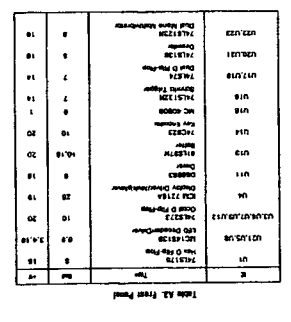
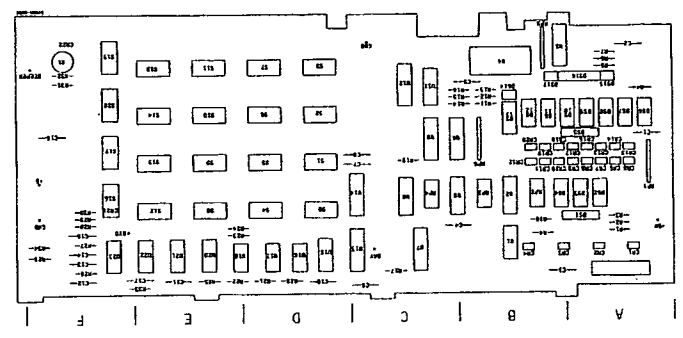
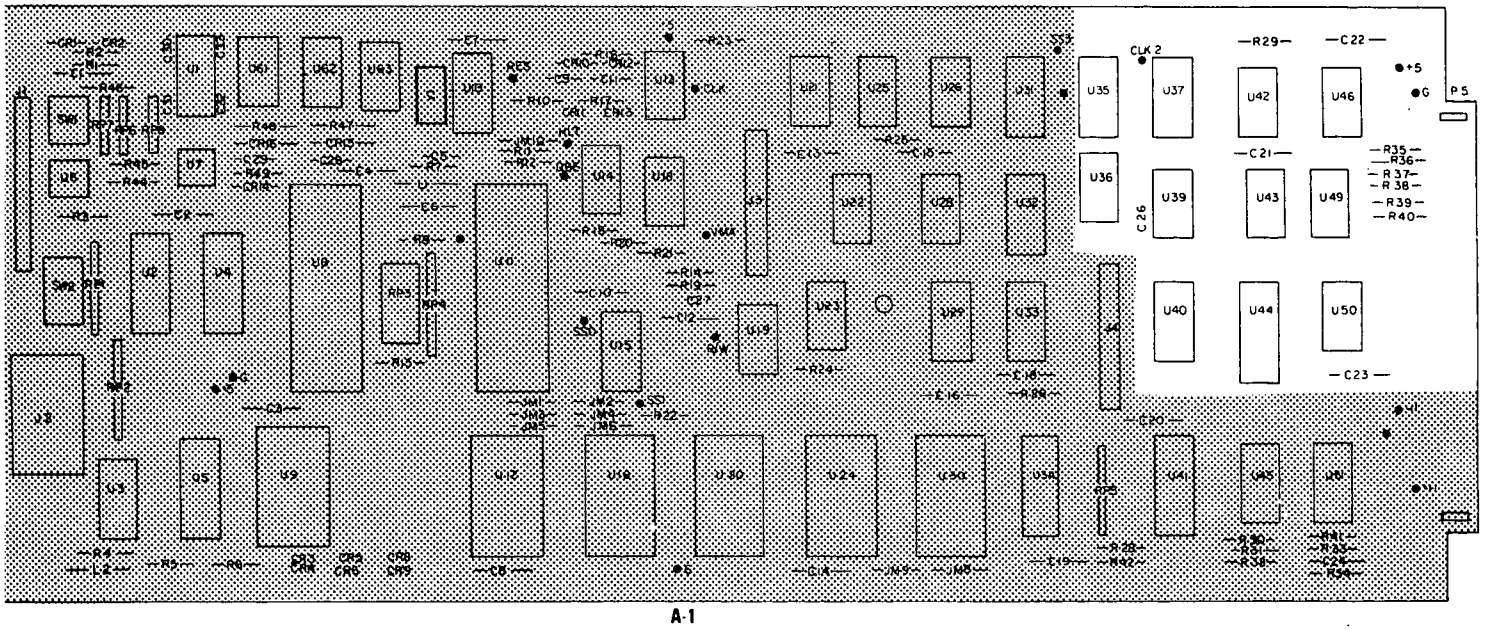


Table A4. Front Panel



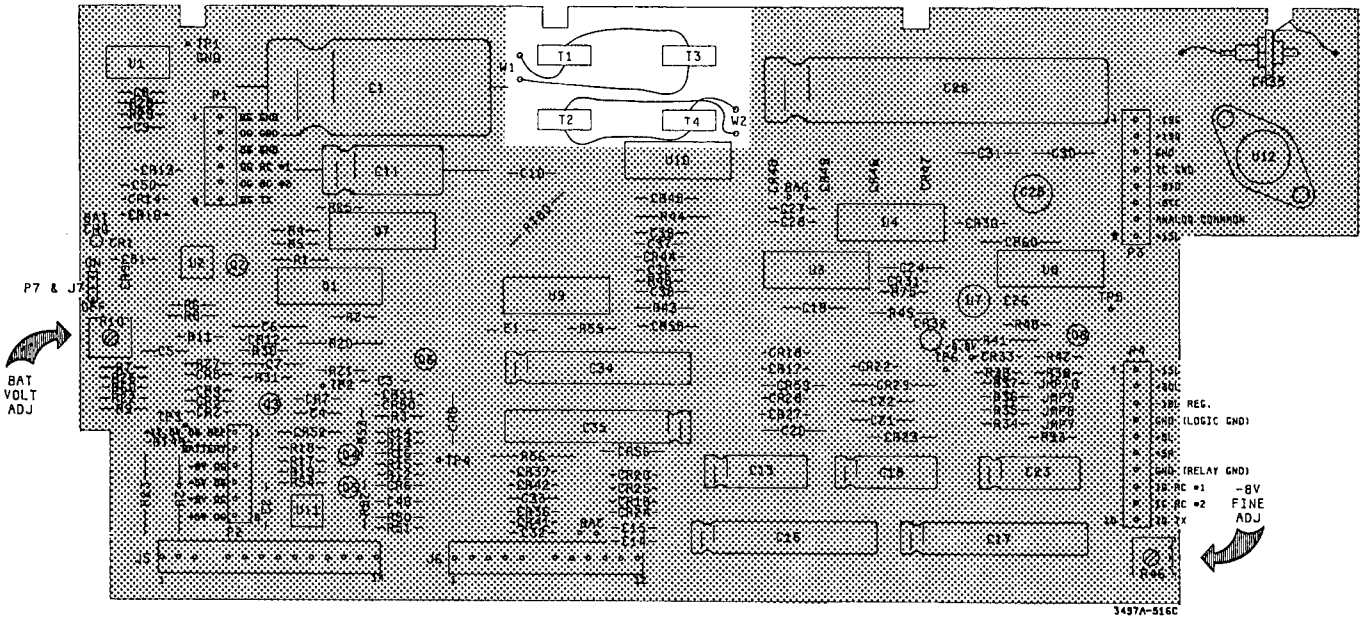
A3
03497-66503



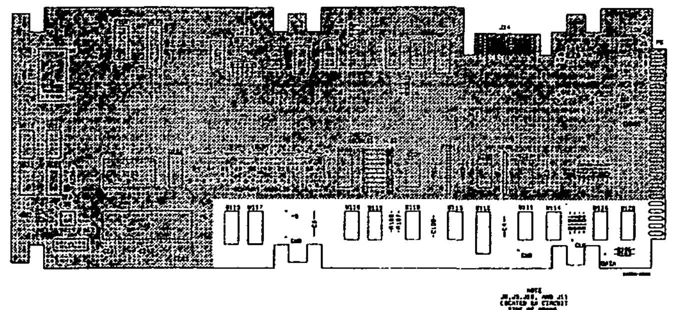
A-1
03497-66533

3497-533C

P1 CONNECTS TO A4J9
P2 CONNECTS TO A4J10
P3 CONNECTS TO A4J1
P4 CONNECTS TO A4J2



A16
03497-66516



A2
03497-66502

P/O A1 Crossguard (Outguard)

IC	Type	Gnd*	+5V*
U28	SN74LS08N Quad 2 input AND	7	13,14
U29,U39	74LS04N Hex Inverter	7	14
U35	SN74LS161N Synchronous 4-bit counter	8	7,9,10,16
U36	SN74LS02N Quad 2 input NOR	7	14
U37	SN74LS112N Dual J-K F.F	8,12	4,10,16
U40	1820-1976 + D Shift Register	8,10,15	16
U42	74LS74 Dual D F.F.	7	14
U43	74LS74 Dual D F.F.	7	1,4,10,12,14
U44	81LS97N Buffer	10	20
U46	7426N Quad 2 input NAND	7	14
U48	XSTR-ARRAY CA3046	3,9,13	8
U50	SN74LS164N 8-bit Parallel-Out Serial Shift Register	7	2,14

*These pins are not necessarily power pins only. They also include all pins which may have pull-up resistors or are grounded.

P/O A2 Crossguard (Inguard)

IC	Type	Gnd*	+5V*
U110	74LS33N Quad 2-input NOR	2,7,11	14
U111	74LS30 8-input NAND	7	14
U112	81LS97N TTL Buffer	10	20
U113	74LS74 Dual D F.F.	7	4,10,12,14
U114	74LS164N 8-Bit Parallel-Out Serial Shift Register	7	2,14
U115	1820-1976 + D Parallel-Load 8-Bit Shift Register	8,15	10,16
U116	CA3046 XSTR-ARRAY	5,9,12	8
U117	74LS161N Synchronous 4-Bit Counter	3,4,6,8,8	7,8,10,16
U118	74LS00 Quad 2-input NAND	7	4,12,14
U119	74LS74 Dual D F.F.	7	1,4,10,12,14
U120	7426N Quad 2-input NAND	7	14

*These pins are not necessarily power pins only. They also include all pins which may be held high or are grounded.

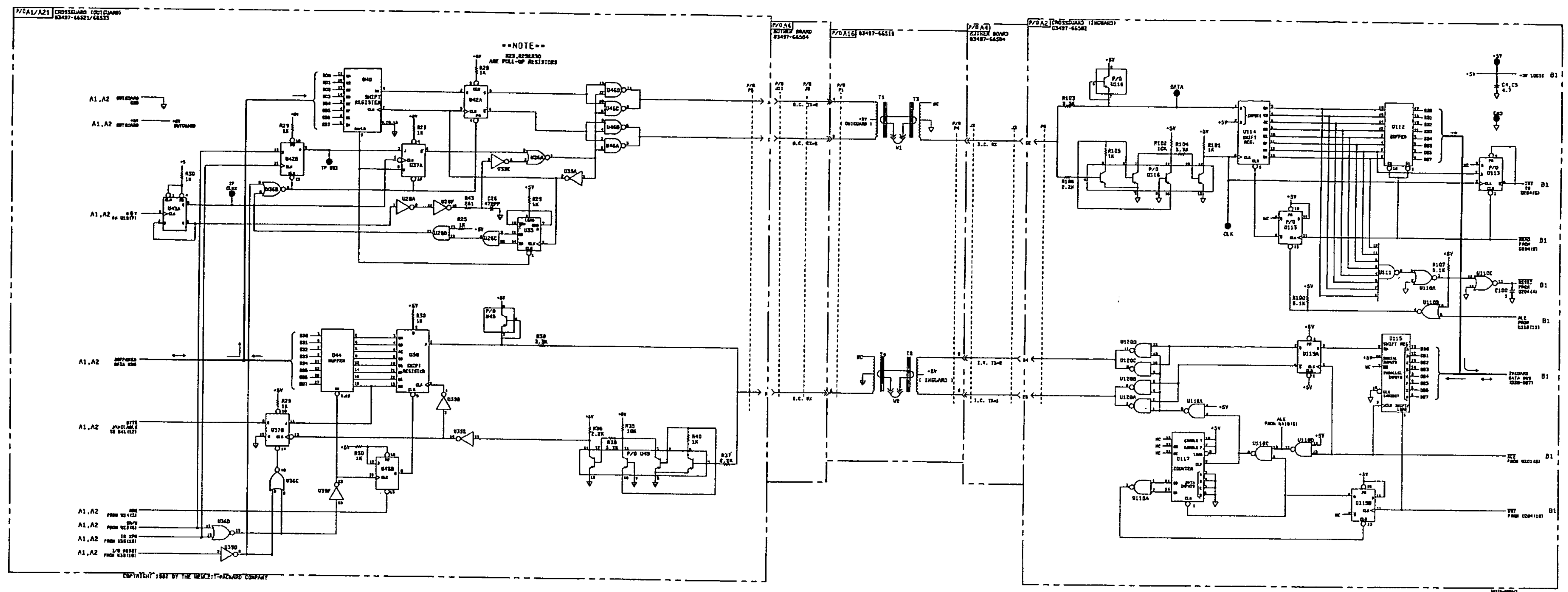


Figure 8-E-10. Crossguard Logic (Schematic A81)

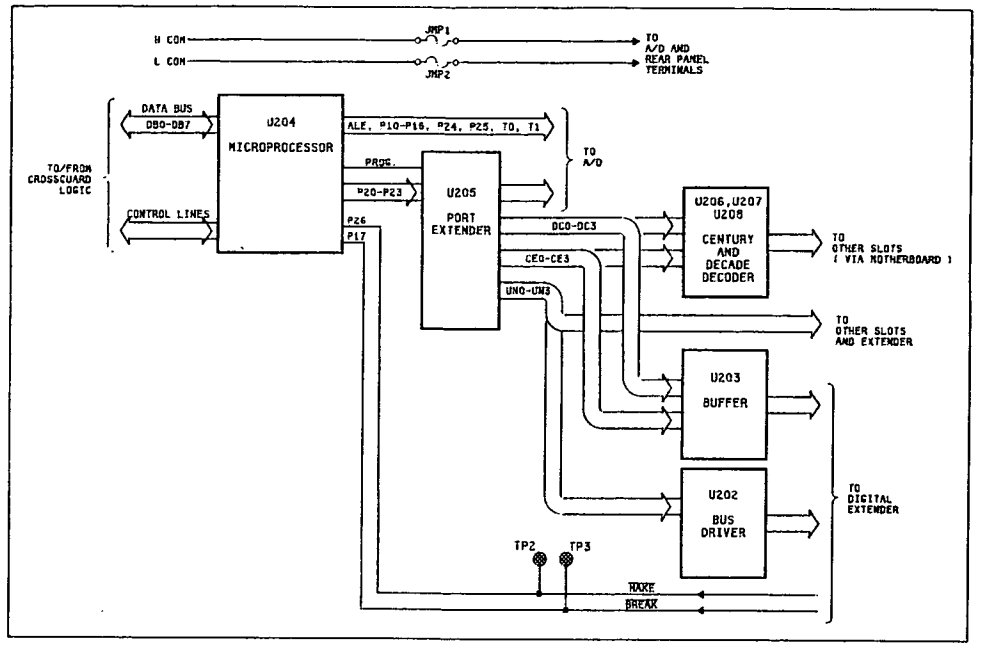
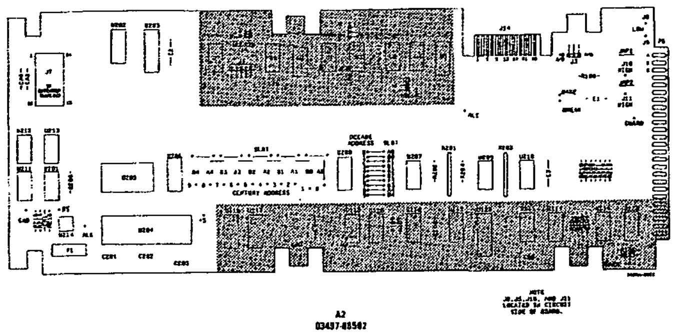


Figure 8-E-11. Inguard Controller Block Diagram



NOTE

Unshaded area shown on this schematic.

P/O A2 Mainframe Inguard Controller

IC	Type	Gnd*	+V*
U201	74LS00 Quad 2 input NAND	7	2,4,9,14
U202	74LS367N Hex Bus Drivers	1,8,15	16
U203	81LS97N TTL Buffer	1,10,19	20
U204	1820-2532 Microprocessor 8748	7,20	5,26,40
U205	P8243 I/O Port Expander (Bi-directional)	6,12	24
U206, U208	74LS145 BCD-to-Decimal Decoder/Drivers	8	16
U207,U209,U210	CD4071BY Quad 2 input OR	7	14
U211	74LS74 Dual D F.F.	7	2,4,14
U212	74LS10N Triple 3 input NAND	7	3,14
U213	74LS74 Dual D F.F.	7	1,4,10,13,14
U214	LM393N Comparator	4	8

* These pins are not necessarily power pins only. They also include all pins which may have pullup resistors or are grounded.

SCHEMATIC B1 COMPONENT LOCATOR

COMP	COL	COMP	COL	COMP	COL	COMP	COL	COMP	COL
C2	B	J3	F	R209	F	TP ALE	A,E	U208	D
C3	E	J7	A	R210	F	TP R9	A	U209	E
C201	A,B			R211	F	TP MAKE	F	U210	E
C202	B	R108	F	R212	F			U211	A
C203	B	R201	E	R213	F	U201	A	U212	A
		R202	D,E	R214	A	U202	B	U213	A
CR1	A	R203	E	R215	A	U203	B	U214	A
CR5	A	R204	E	R216	A	U204	B		
CR6	A	R206	A			U205	B	T1	A
		R207	F	TP +5	B	U206	B		
E1	F	R208	F	TP GND	A	U207	D		

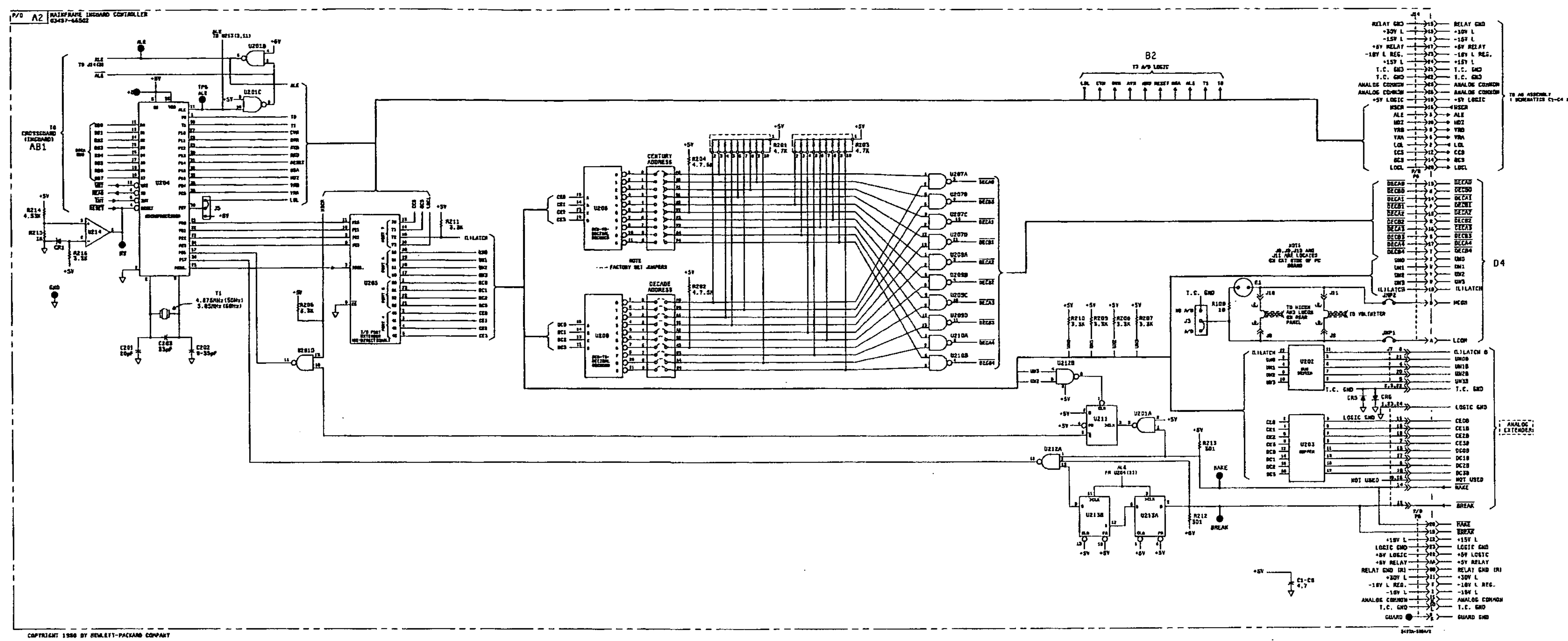
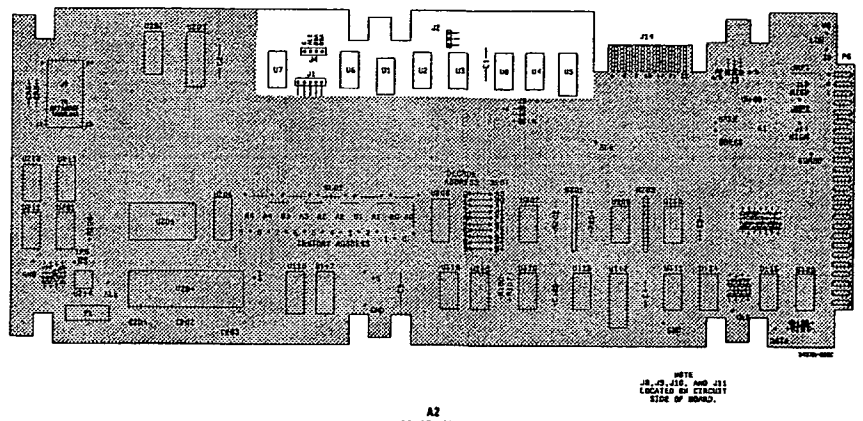


Figure 8-E-12. Inguard Controller (Schematic B1)



A2
03497-66502

NOTE

Unshaded area shown on this schematic.

P/O A2 A/D Logic

RC	Type	Gnd*	+V*
U1	74LS163 Synchronous 4-Bit Counter	3,4,8,8	7,10,16
U2	74LS00 Quad 2-Input NAND	7	2,14
U3	74LS02N Quad 2-Input NOR	7,12	14
U4	74LS10N Triple 3-Input NAND	7	11,14
U5	74LS375 4-Bit Bistable Latches	8	16,16
U6	74LS02N Quad 2-Input NOR	7,8	14
U7	74LS86N Quad 2-Input EOR	7	1,4,14
U8	74LS74AN Dual D F.F.	7,13	1,4,14

*These pins are not necessarily power pins only. They also indicate all pins which may be hard high or are grounded.

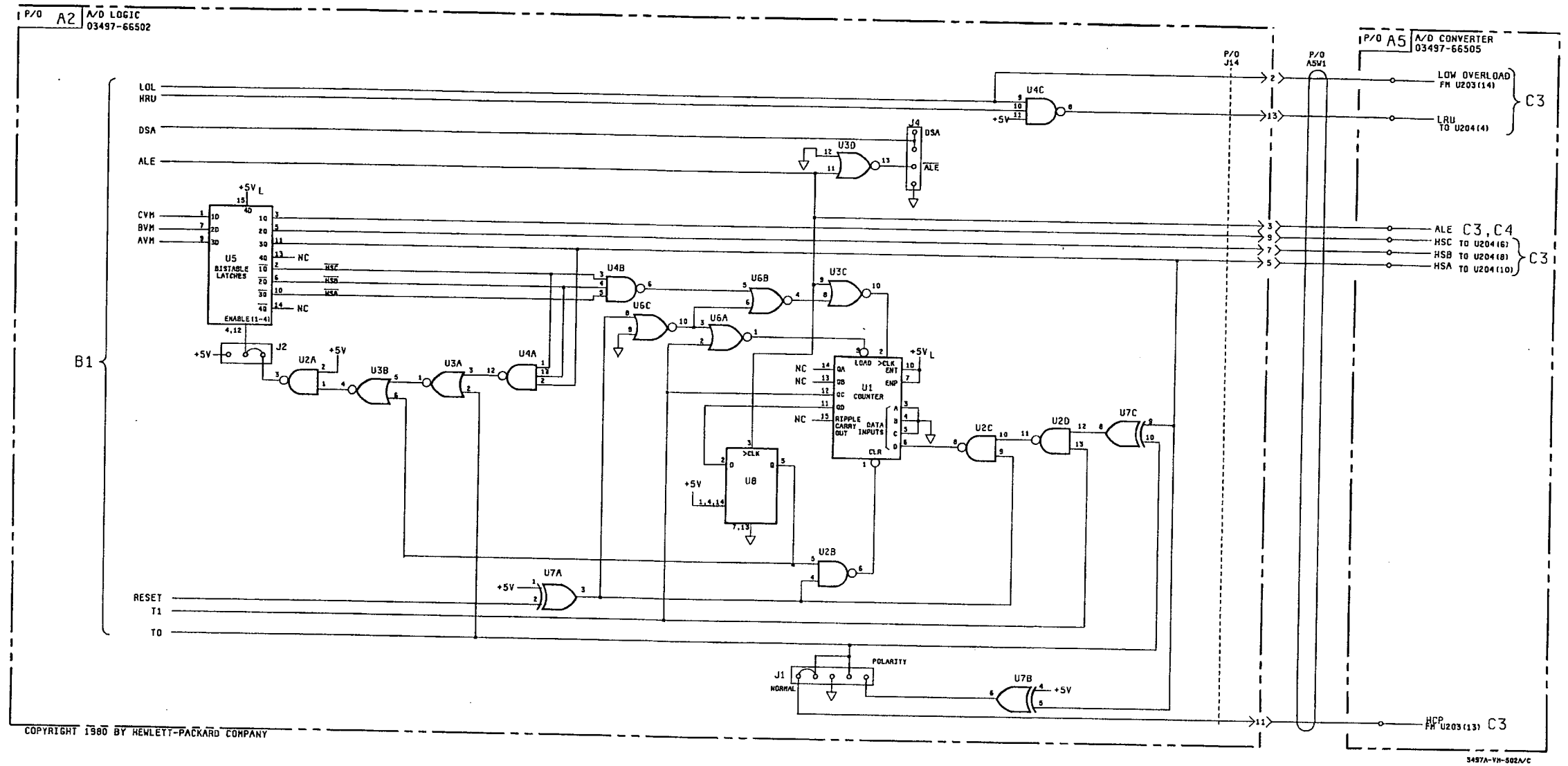


Figure 8-E-13. A/D Logic (Schematic B2)

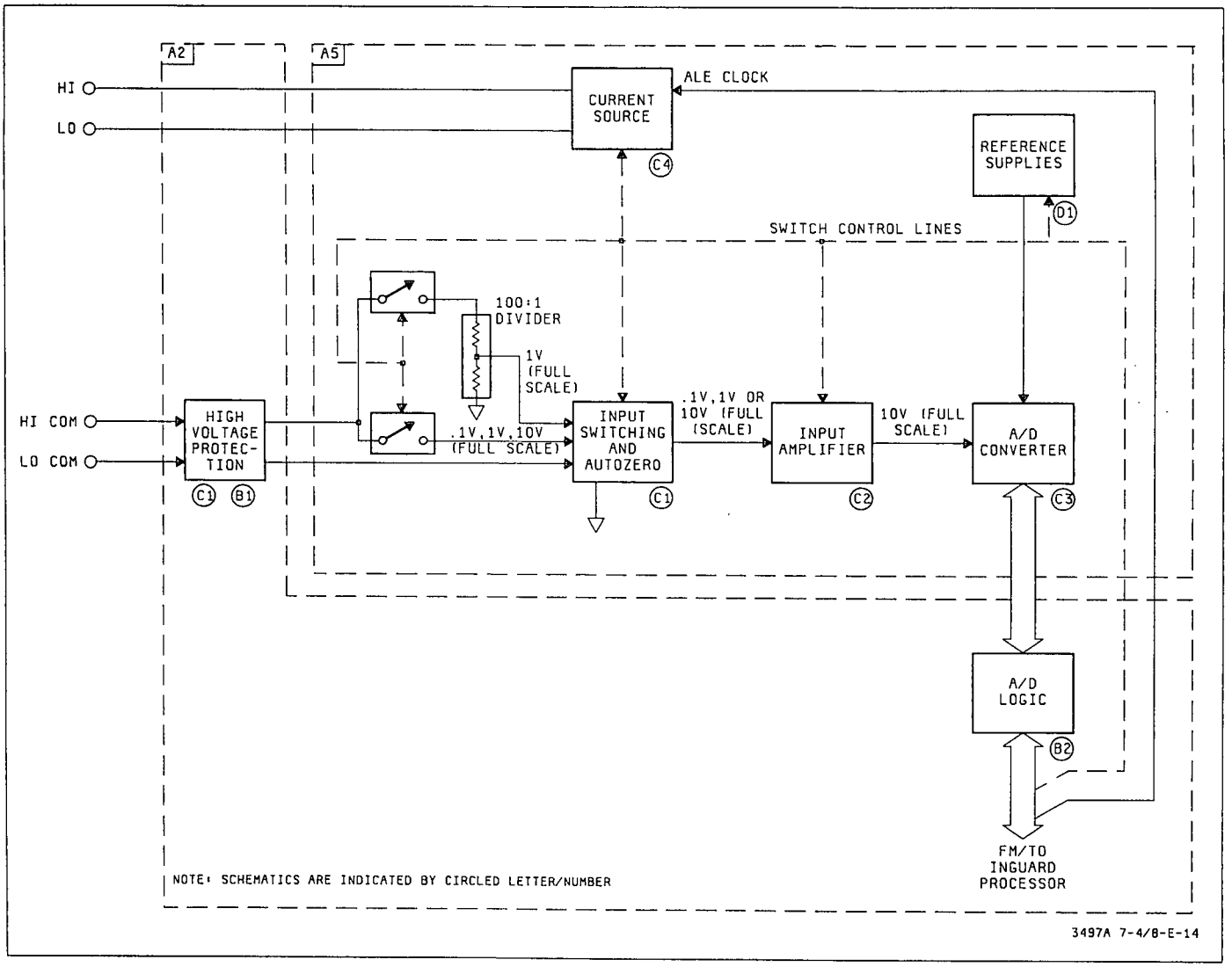
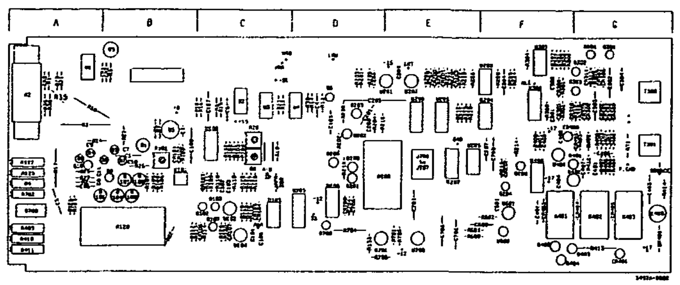
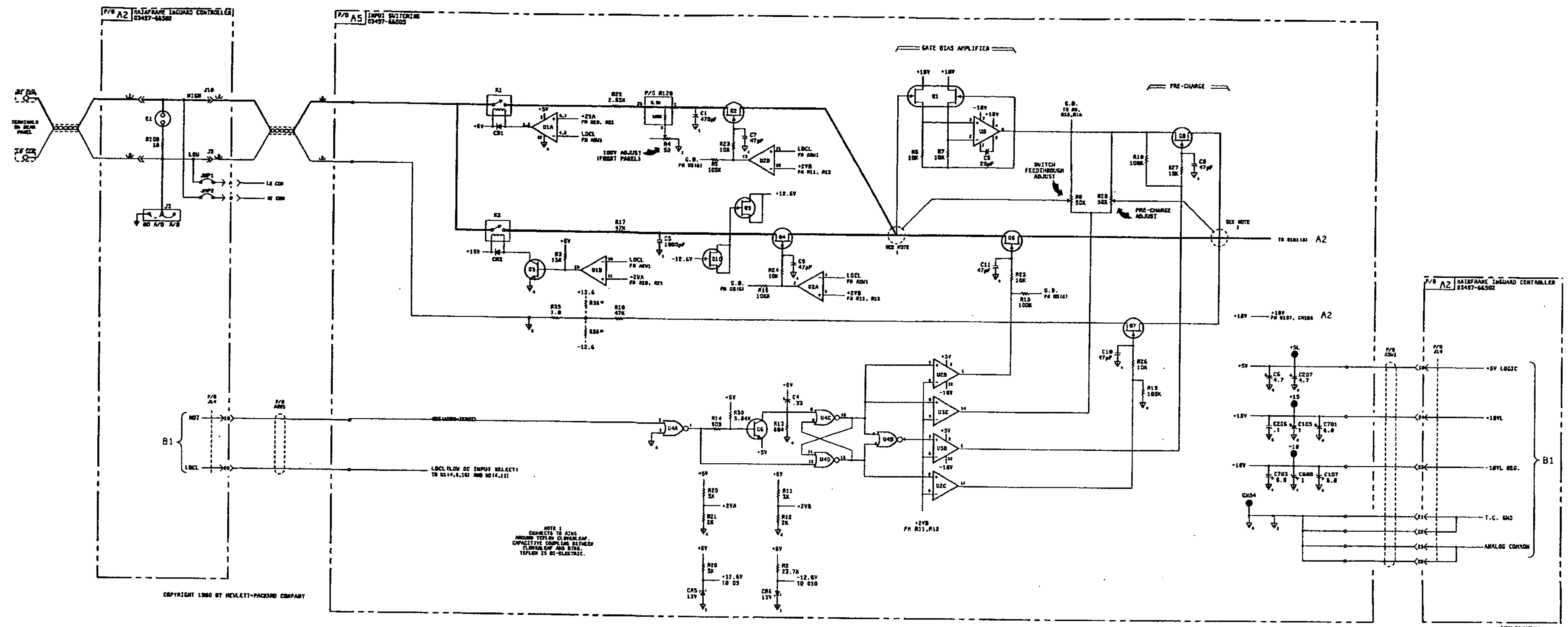


Figure 8-14. Voltmeter Block Diagram



A5
03457-60585

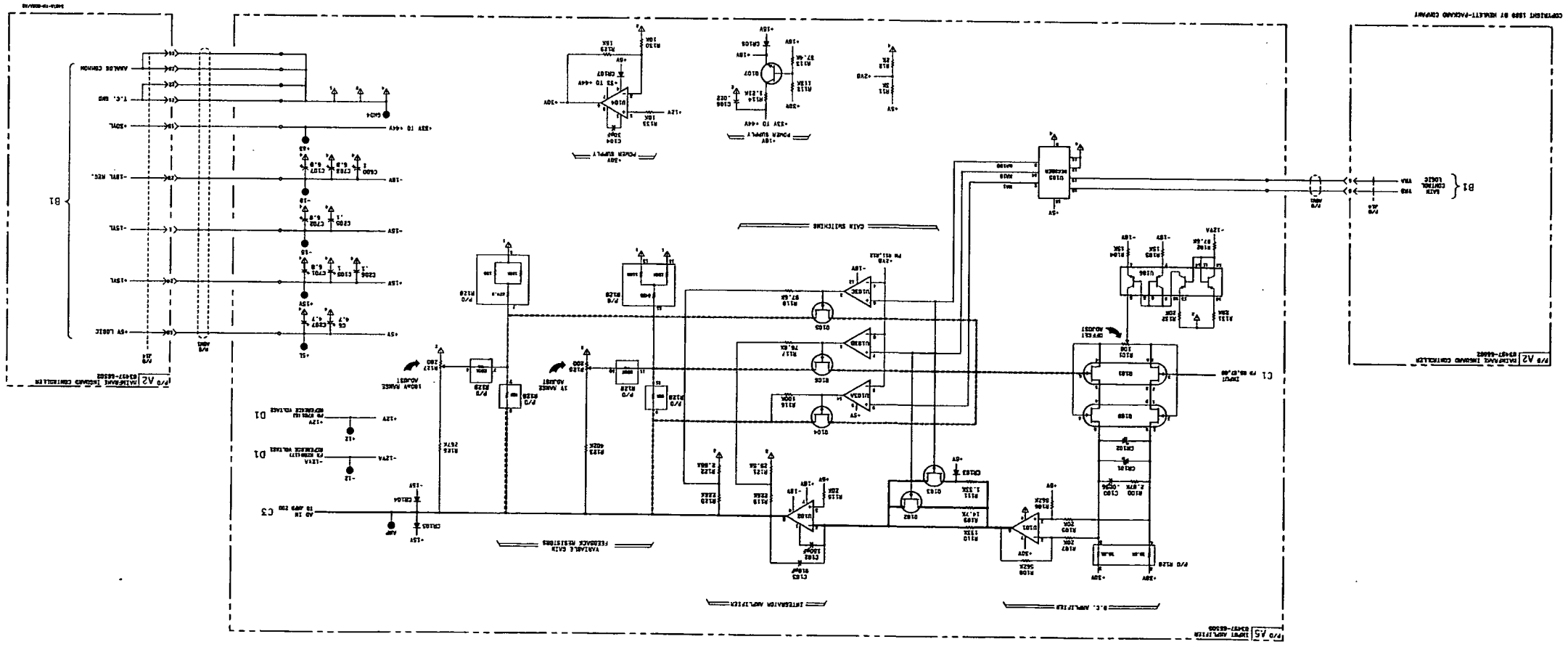


SCHEMATIC C1 COMPONENT LOCATOR

COMP	COL	COMP	COL	COMP	COL	COMP	COL	COMP	COL
C1	B	K1	A	R2	A	R18	A	TP 1	B
C3	B	K2	A	R3	B	R19	C	TP 33	D
C4	D			R4	A	R20	A	TP +15	C
C5	A	Q1	B	R5	C	R21	A	TP +5L	C
C6	C	Q2	B	R6	B	R22	B	TP -15	E
C7	B	Q3	B	R7	B	R23	B	TP -18	B
C8	A	Q4	A	R8	C	R24	A	TP GND4	E
C9	A	Q5	B	R10	C	R25	A		
C10	B	Q6	D	R11	C	R26	B	U1	A
C11	A	Q7	B	R12	C	R27	A	U2	C
		Q8	B	R13	D	R28	C	U3	C
CR1	A,B	Q9	A	R14	D	R30	D	U4	D
CR2	B	Q10	A	R15	C	R35	A	U5	B
CR5	A			R16	C	R36	A		
CR6	A	R1	A	R17	A				

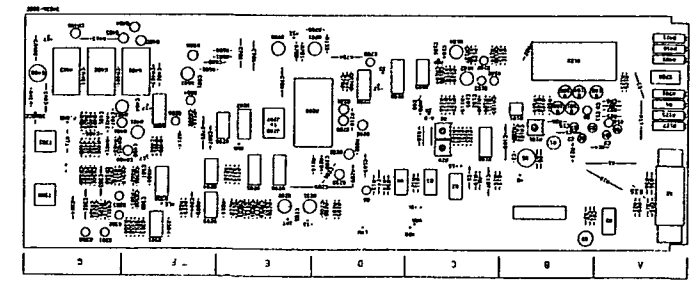
Figure 8-E-15. Voltmeter Input Switching (Schematic C1)

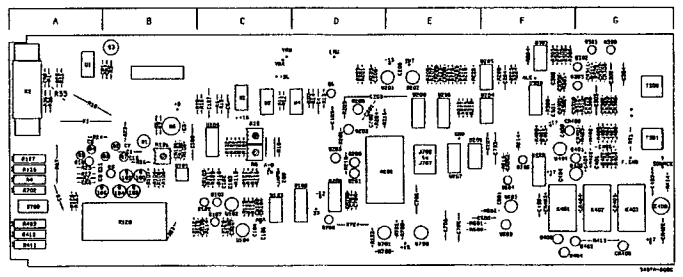
Figure 8-E-16. Voltmeter Input Amplifier (Schematic C2)



SCHEMATIC C2 COMPONENT LOCATOR

COMP	COL	COMP	COL	COMP	COL	COMP	COL	COMP	COL
C100	B	D100	B	R106	B	R121	C	TP -15	E
C102	B	D101	B	R107	B	R123	C	TP GND4	E
C103	C	D102	C	R108	B	R125	A	TP AMP	C
C104	C	D103	B	R109	C	R126	A	TP 33	C
C105	C	D104	B	R110	C	R126	A	TP VBIA	C
C106	C	D105	B	R111	C	R127	A	TP VBG	C
C107	C	D106	A,B	R112	C	R128	B		
C108	B	D107	C	R113	B,C	R129	C	U100	C
CR101	B	R100	B	R114	C	R130	C	U101	B
CR102	B	R101	B	R116	C	R131	C	U102	B
CR103	C	R102	C	R117	C	R132	C	U103	C
CR105	C	R103	C	R118	C	R133	D	U104	C
CR106	C	R104	C	R119	C	R134	C	U105	D
CR107	C	R105	B	R120	C	TP -15	E	TP +5L	C





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SCHEMATIC C3 COMPONENT LOCATOR

COMP	COL	COMP	COL	COMP	COL	COMP	COL	COMP	COL
C200	D	Q200	D	R206	E	R221	E	TP -12	D
C201	D	Q201	D,E	R207	E	R222	E	TP +12	E
C203	D,E	Q202	D	R208	F	R223	E	TP ALE	F
C204	F	Q203	D	R209	D	R224	E		
C205	E	Q204	F	R210	E	R225	F	U200	E
C207	F	Q206	F	R212	E			U202	E
				R213	E	TP +5L	C	U203	F
CR200	E	R200	D,E	R214	F	TP GND4	E	U204	F
CR201	E	R201	D	R215	F	TP +15	C	U205	E
CR202	F	R202	D	R216	D	TP -15	E	U206	E
CR203	E	R203	D	R218	D	TP A-D	C	U207	E
		R204	D	R219	E	TP LRU	D	U208	D
JMPR200	C	R205	D	R220	E	TP INT	E		

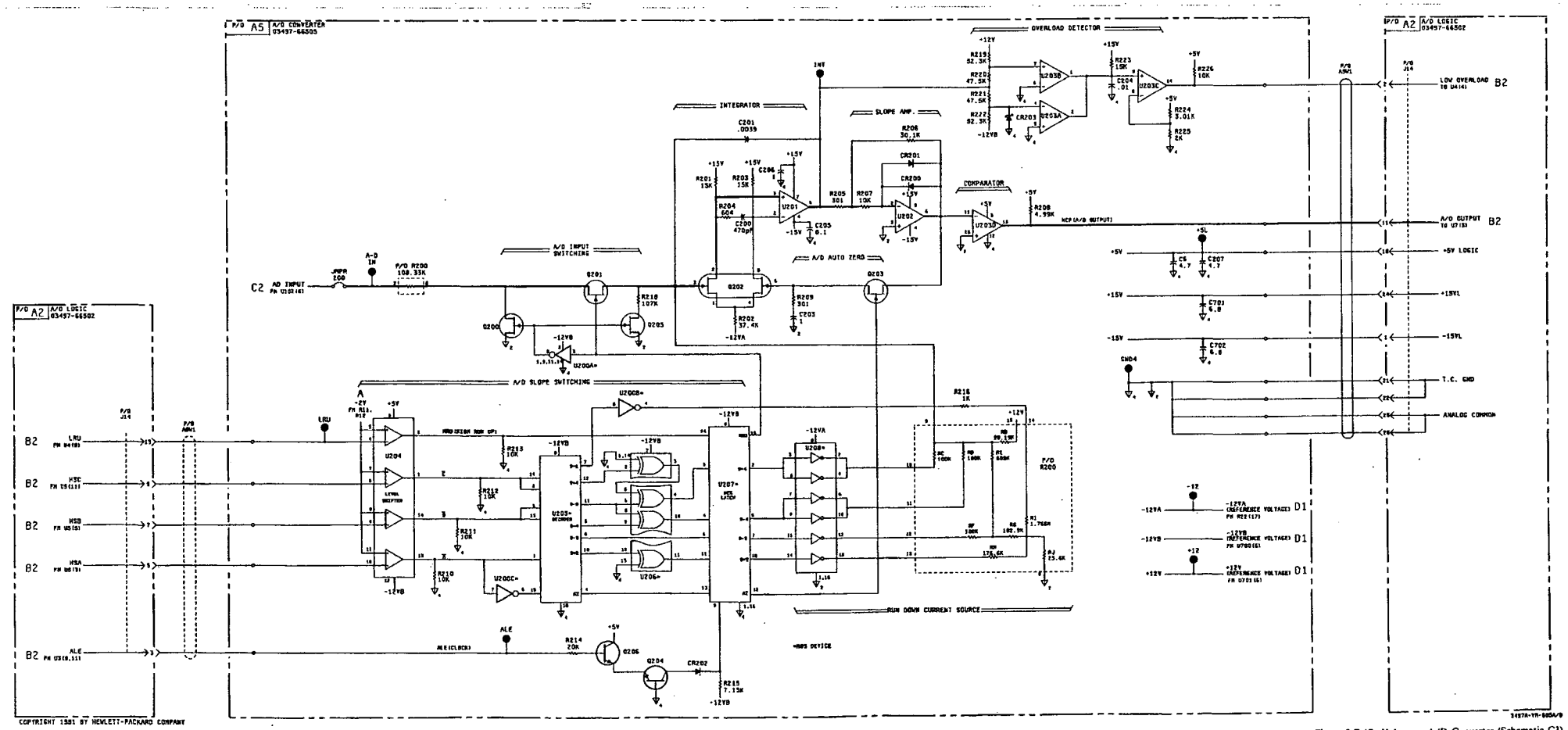
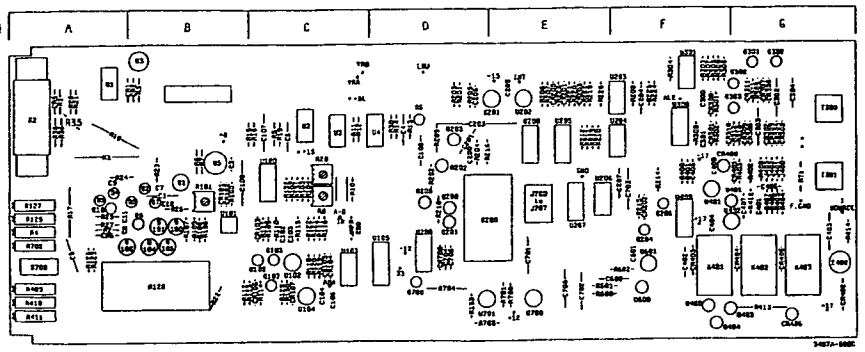


Figure 8-E-17. Voltmeter A/D Converter (Schematic C3)



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SCHEMATIC C4 COMPONENT LOCATOR

COMP	COL	COMP	COL	COMP	COL	COMP	COL	COMP	COL
C300	F	CR306	G	K401	F	R306	F	R413	G
C301	F	CR307	G	K402	G	R307	F	R414	G
C302	G	CR308	G	K403	G	R308	F		
C303	G	CR309	G			R309	G	RT1	G
C304	G	CR310	F	Q300	G	R310	G		
C400	F	CR311	G	Q301	G	R311	G	T300	G
C401	G	CR400	F	Q302	F,G	R312	F	T301	G
C402	F	CR401	F	Q303	F,G	R400	F		
C403	G	CR402	G	Q400	F	R401	F,G	TP +17	F,G
C404	F	CR403	F	Q401	F	R402	F,G	TP −17	F
C405	F	CR404	G	Q403	G	R403	G	TP FGND	G
C406	G	CR405	G	Q404	F,G	R404	G	TP ALE	F
C407	G	CR408	G			R405	G	TP +5L	C
				R128	A,B	R406	G	TP GND4	E
CR300	F	E400	G	R300	F	R407	G		
CR301	F			R301	F	R408	G	U300	F
CR302	G	J400	G	R302	F	R409	A	U301	F
CR303	G	J401	G	R303	F	R410	A	U400	F
CR304	G	J402	G	R304	F	R411	A	U401	F
CR305	G	J403	G	R306	F	R412	G	U402	F

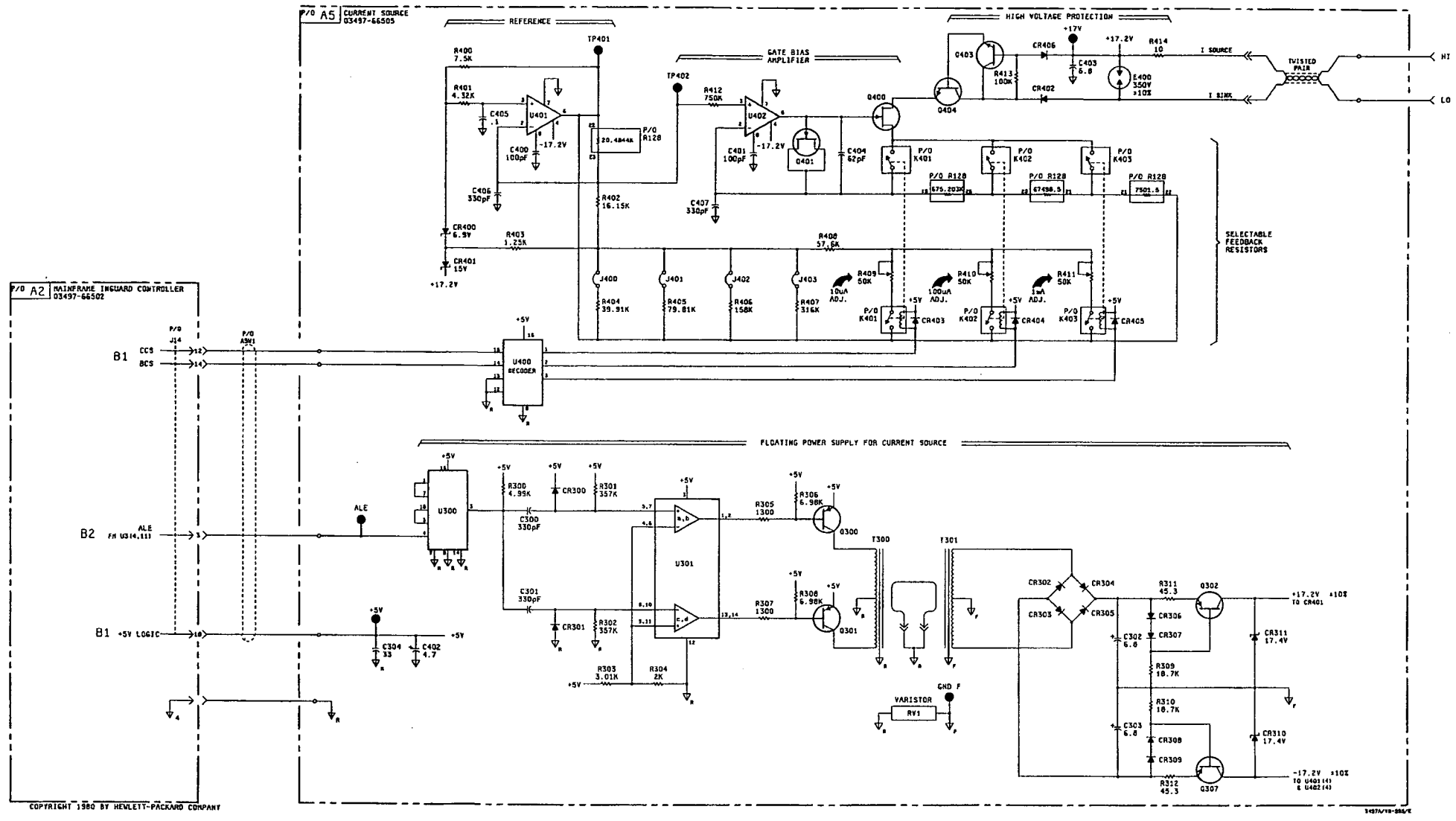
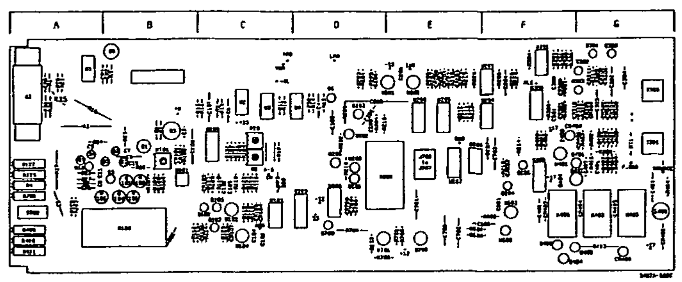


Figure 8-E-18. Current Source (Schematic C4)



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SCHEMATIC D1 COMPONENT LOCATOR

COMP	COL	COMP	COL	COMP	COL	COMP	COL
C600	E,F	CR700	D	R701	E	TP +12	E
C601	F			R702	A	TP GND4	E
C701	E	J700	E	R704	D		
C702	E			R705	E	U600	F
C703	F	R200	D,E	R706	D	U601	F
C704	D	R600	E	S700	A	U700	E
C705	D	R601	F			U701	D
C706	E	R602	F	TP -12	D		

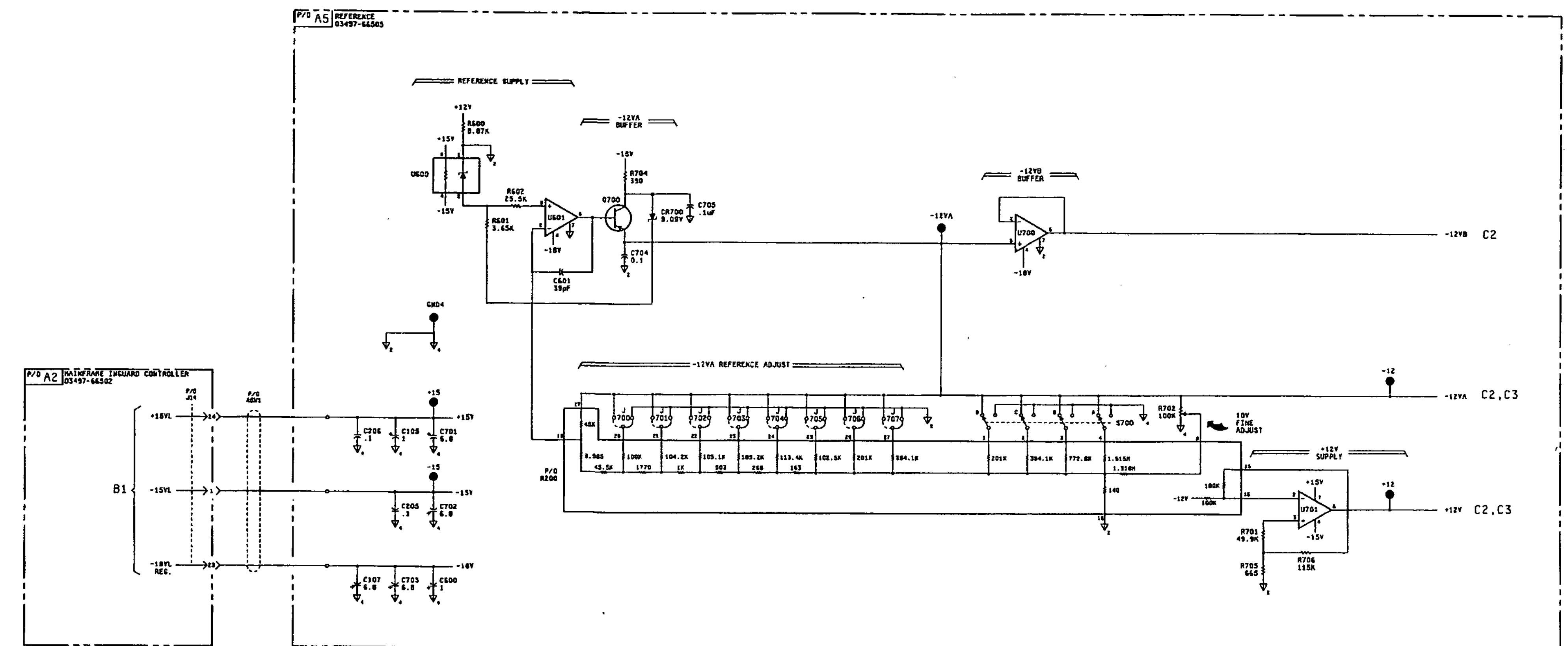

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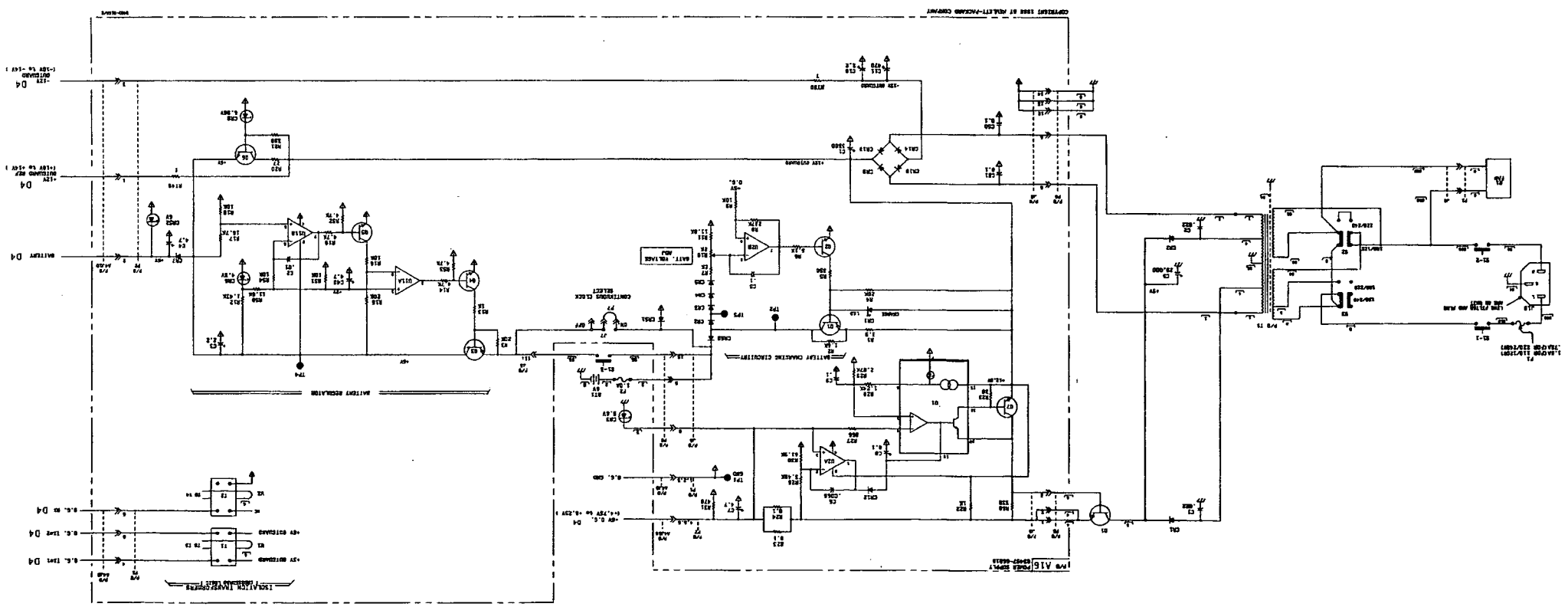
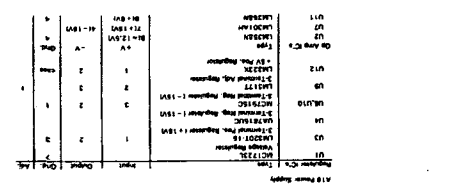
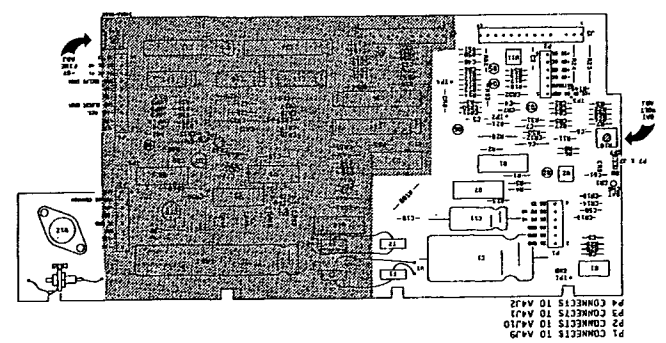
Figure 8-E-19. Reference (Schematic D1)

Figure 8-E-20. Outguard Power Supplies (Schematic D2)



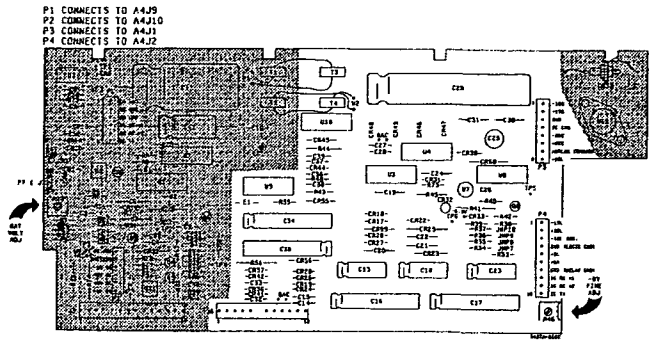




NOTE

Unshaded area shown on this schematic.

P1 CONNECTS TO A4J9
P2 CONNECTS TO A4J10
P3 CONNECTS TO A4J1
P4 CONNECTS TO A4J2



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NOTE

Unshaded area shown on this schematic.

A16 Power Supply

Regulator IC's	Type	Input	Output	Gnd	Adj.
U1	MC7723L Voltage Regulator		7		
U3	LM320T-15 3-Terminal Pos. Regulator (+15V)	1	2	3	
U4	UA7815UC 3-Terminal Neg. Regulator (-15V)				
U5,U10	MC7915C 3-Terminal Neg. Regulator (-15V)	3	2	1	
U8	LM317T 3-Terminal Adj. Regulator	2	3		1
U12	LM323K +5V Pos. Regulator	1	3	case	

Op Amp IC's	Type	+V	-V	Gnd
U2	LM358N	8(+12.6V)		4
U7	LM201AH	7(+15V)	4(-15V)	
U11	LM358N	8(+8V)		4

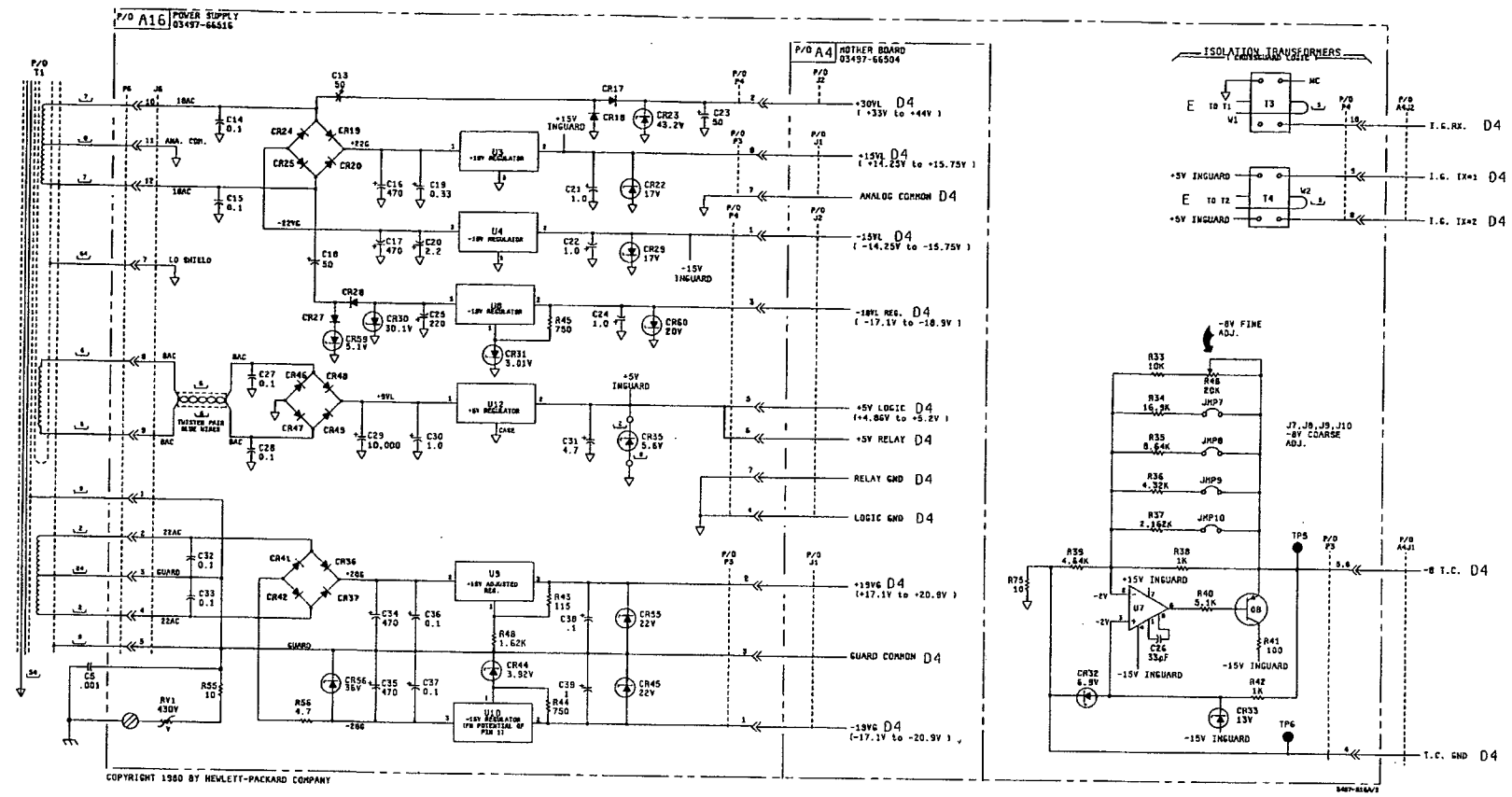
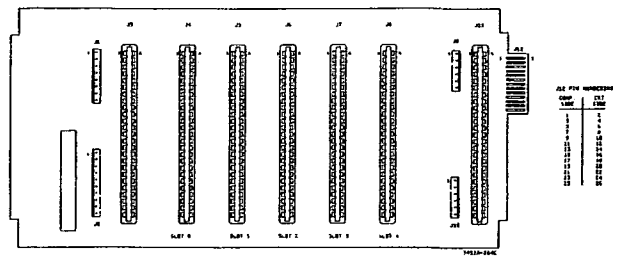


Figure 8-E-21. Inguard Power Supplies (Schematic D)



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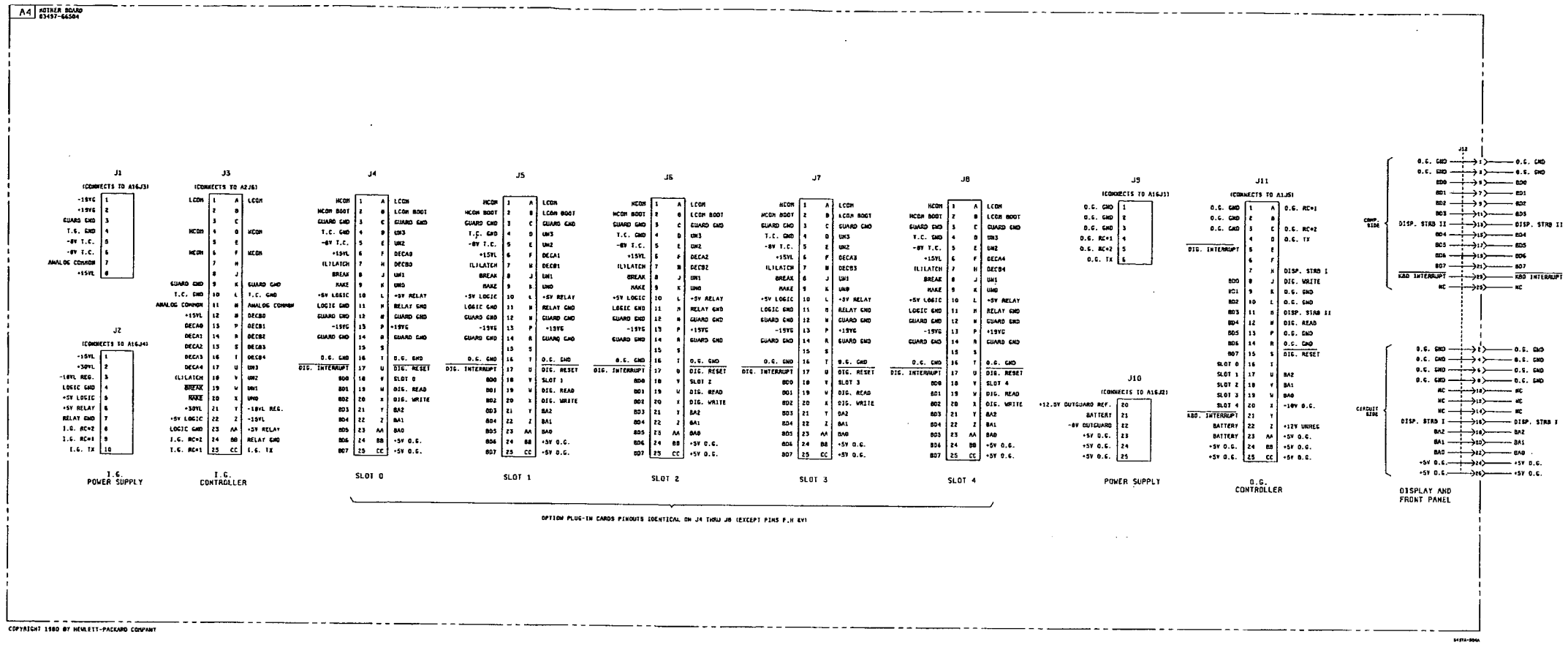


Figure 8-E-22. Mother Board (Schematic D4)

APPENDIX A
CONDENSED DESCRIPTION OF THE HEWLETT-PACKARD INTERFACE BUS

A-1. GENERAL BUS DESCRIPTION

A-2. The Hewlett-Packard Interface Bus (HP-IB) is a carefully defined instrumentation interface which simplified the integration of instruments, calculators, and computers into systems. It minimizes compatibility problems between devices and has sufficient flexibility to accommodate future products. The Hewlett-Packard Interface Bus has been formally proposed to the International Electrotechnical Commission (I.E.C.), as an international standard, and to the Institute of Electrical and Electronic Engineers (I.E.E.E.) as an American standard.

A-3. The HP-IB employs a 16 line Bus to interconnect up to 15 instruments. This Bus is normally the sole communication link between the interconnected units. Each instrument on the Bus is connected in parallel to the 16 lines of the Bus. Eight of the lines are used to transmit data and the remaining eight are used for communication timing (Handshake), and control.

A-4. Data is transmitted on the eight HP-IB data lines as a series of eight-bit characters referred to as "bytes". Normally, a seven-bit ASCII (American Standard Code for Information Interchange) code is used with the eighth bit available for a parity check, if desired. Data is transferred by means of an interlocked "handshake" technique. This sequence permits asynchronous communication over a wide range of data rates.

A-5. Communication between devices on the HP-IB employs the three basic functional elements listed below. Every device on the Bus must be able to perform at least one of these functions:

a. LISTENER—A device capable of receiving data from other instruments. Examples of this type of device are: printers, display devices, programmable power supplies, programmable signal sources and the like.

b. TALKER—A device capable of transmitting data to other instruments. Examples of this type of device are: tape readers, voltmeters that are outputting data, counters that are outputting data, and so on.

c. CONTROLLER—A device capable of managing communications over the HP-IB such as addressing and sending commands. A calculator or computer with an appropriate I/O interface is an example of this type of device.

A-6. An HP-IB system allows only one device at a time to be an active talker. Up to 14 devices may simultaneously be listeners. Only one device at a time may be an active controller.

A-7. BUS STRUCTURE

A-8. The HP-IB interface connections and Bus structure are shown in Figure A-1.

A-9. Management (CONTROL) Lines

A-10. The active controller manages all Bus communications. The state of the ATN (attention) line, determined by the controller, defines how data on the eight data (DIO) lines will be interpreted by the other devices on the Bus. When ATN is low (true), the HP-IB is in Command Mode. In Command Mode the controller is active and all other devices are waiting for instructions. Command Mode instructions which can be issued by the Controller in "Command Mode" include:

a. TALKER ADDRESS—A seven bit code transmitted on the HP-IB which enables a specific device to talk. Only one Bus device at a time may act as the talker. When the controller addresses a unit to talk the previous talker is automatically unaddressed and ceases to be a talker. Confusion would result if more than one device were allowed to talk at a time.

b. LISTENER ADDRESS—A seven-bit code transmitted on the HP-IB which enables a specific device to listen. Several Bus devices at a time (up to 14) may be listeners.

c. UNIVERSAL COMMANDS—Bus devices capable of responding to these commands from the controller will do so at any time regardless of whether they are addressed. These commands will be covered in more detail later.

d. ADDRESSED COMMANDS— These commands are similar to universal commands except that they are recognized only by devices that are addressed as listeners.

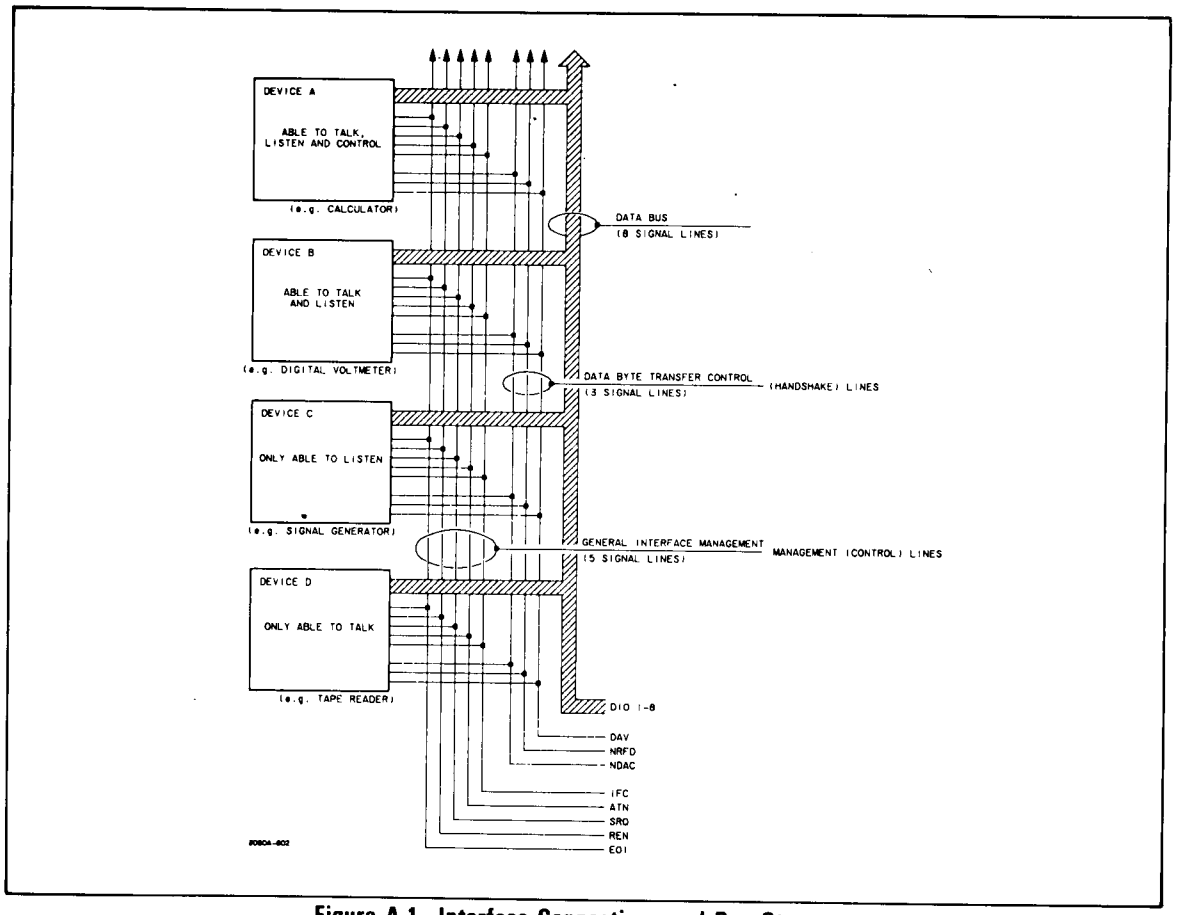


Figure A-1. Interface Connections and Bus Structure.

e. UNADDRESS COMMANDS—

1. "Unlisten" Address Command—

This command unaddresses all listeners that have been previously addressed to listen.

2. "Untalk" Address Command—

This command unaddresses any talker that had been previously addressed to talk.

A-11. Bus Commands

A-12. In "Command Mode" one or more special codes known as "bus commands" may be placed on the HP-IB. These commands have the same meaning in all Bus systems. Each device is designed to respond to those commands that have a useful meaning to the device and will ignore all others. The operating manual for each device will state which Bus commands it will obey.

A-13. Bus commands fall into three categories.

a. Universal commands affect all responding devices on the Bus, whether addressed or not.

b. Addressed commands affect only responding devices which are addressed to listen. Addressed commands allow the controller to initiate a simultaneous action from a selected group of devices on the Bus.

c. Unaddress commands are obeyed by all addressable devices. These commands unaddress devices that are currently addressed.

The Bus commands are summarized in Table A-1.

A-14. Service Request and Serial Polling

A-15. Some devices that operate on the interface bus have the ability to request service from the system controller. A device may request service when it has completed a measurement, when it has detected a critical condition, or for any other reason. Service request is initiated when a device sets the HP-IB line labeled SRQ low. The controller has the option of determining when or if a service request will be serviced. The following sequence is used to respond to a service request:

a. The controller checks for the presence of a service request.

b. If a service request is present, the controller sets the serial poll mode. The serial poll mode is initiated by the controller transmitting the Universal Command "SPE" (ASCII character "CAN" [Octal 030]) in the "Command Mode".

Table A-1. Summary of Bus Commands.

	Command	ASCII Character	Octal Code	Purpose
Unaddress Commands	UNL UNLISTEN	?	077	Clears Bus of all listeners.
	UNT UNTALK	—	137	Unaddresses the current talker so that no talker remains on the Bus.*
Universal Commands	LLO Local Lockout	DC1	021	Disables front panel local-reset button on responding devices.
	DCL Device Clear	DC4	024	Returns all devices capable of responding to pre-determined states, regardless of whether they are addressed or not.
	PPU Parallel Poll Unconfigure	NAK	025	Sets all devices on the HP-IB with Parallel Poll capability to a predefined condition.
	SPE Serial Poll Enable	CAN	030	Enables Serial Poll Mode on the Bus.
	SPD Serial Poll Disable	EM	031	Disables Serial Poll Mode on the Bus.
Addressed Commands	SDC Selective	EOT	004	Returns addressed devices, capable of responding to pre-determined states.
	GTL Go to Local	SOH	001	Returns responding devices to local control.
	GET Group Execute Trigger	BS	010	Initiates a simultaneous pre-programmed action by responding devices.
	PPC Parallel Poll Configure	ENQ	005	This command permits the DIO lines to be assigned to instruments on the Bus for the purpose of responding to a parallel poll.
	TCT Take Control	HT	011	This command is given when the active controller on the Bus transfers control to another instrument.

***NOTE**

Talkers can also be unaddressed by transmitting an unused talk address on the Bus.

c. The controller polls one of the devices that may have requested service. It then polls the next device, and so on. Once the serial poll mode has been enabled, responding devices on the Bus are prepared to accept a serial poll. This is done by setting ATN, addressing the device as a talker, and then removing ATN. If the device has requested service, it will respond by setting DIO line 7 low. Other DIO lines may also be set low indicating the nature of the service request.

d. For each device that has requested service, the controller takes appropriate action.

e. When all devices have been polled, the controller terminates the serial poll mode by issuing the Universal Command SPD (ASCII Character "EM", [Octal 031]).

A-16. The full sequence of operations is not necessary in all cases. For example, a system may have only one device that requests service and then only for a single purpose. When the controller detects a service request, the source of the request and the appropriate action is known immediately. Thus the use of the service request and the serial poll depends entirely on the make-up of each system and the devices involved.

A-17. Parallel Poll

A-18. Parallel polling permits the status of up to eight devices on the HP-IB to be checked simultaneously. The operator assigns each device a data line (DIO1 thru DIO8) which the device sets low during the parallel poll routine if it requires service. More devices can be handled, if desired, by sharing the use of each DIO line.

Table A-2. Code Assignments for "Command Mode" of Operation.

(SENT AND RECEIVED WITH ATN TRUE)

b_7 b_6 b_5 / Bits (2)					0 0 0	(1) MSG	0 0 1	MSG	0 1 0	MSG	0 1 1	MSG	1 0 0	MSG	1 0 1	MSG	1 1 0	MSG	1 1 1	MSG
b_4 ↓	b_3 ↓	b_2 ↓	b_1 ↓	COLUMN → ROW ↓	0		1		2		3		4		5		6		7	
0	0	0	0	0	NUL		DLE		SP		0		@		P		`		p	
0	0	0	1	1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0	0	1	0	2	STX		DC2		"		2		B		R		b		r	
0	0	1	1	3	ETX		DC3		#		3		C		S		c		s	
0	1	0	0	4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0	1	0	1	5	ENQ	PPC (3)	NAK	PPU	%		5		E		U		e		u	
0	1	1	0	6	ACK		SYN		&		6		F		V		f		v	
0	1	1	1	7	BEL		ETB		'		7		G		W		g		w	
1	0	0	0	8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1	0	0	1	9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1	0	1	0	10	LF		SUB		*		:		J		Z		j		z	
1	0	1	1	11	VT		ESC		+		;		K		[		k		{	
1	1	0	0	12	FF		FS		,		<		L		\		l		|	
1	1	0	1	13	CR		GS		–		=		M		]		m		}	
1	1	1	0	14	SO		RS		.		>		N		^		n		~	
1	1	1	1	15	SI		US		/		?	UNL	O		_	UNT	oo		DEL	

MLA ASSIGNED TO DEVICE

MLA ASSIGNED TO DEVICE

MTA ASSIGNED TO DEVICE

MTA ASSIGNED TO DEVICE

MEANING DEFINED BY PCG CODE

MEANING DEFINED BY PCG CODE

(4)

ADDRESSED COMMAND GROUP (ACG)

UNIVERSAL COMMAND GROUP (UCG)

LISTEN ADDRESS GROUP (LAG)

TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

NOTES:
(1) MSG = INTERFACE MESSAGE
(2) b_1 = DIO1 . . . b_7 = DIO7
(3) REQUIRES SECONDARY COMMAND
(4) DENSE SUBSET (COLUMN 2 THROUGH 5). ALL CHARACTERS USED IN BOTH COMMAND & DATA MODES.

A-19. The parallel polling function requires the controller to periodically poll the instruments connected to the Bus. The controller interrogates (polls) the instruments by sending an EOI with ATN activated. When either EOI or ATN is removed, the controller stops polling.

A-20. Code Summary

A-21. A code assignment summary is shown in Table A-2. These assignments apply only when operating in "Command Mode".

A-22. In "Data Mode" there are no specific code assignments. However, the devices communicating in this mode must agree on the meaning of the codes they use.

A-23. The set of codes labeled "Primary Command Group" are the codes commonly used to communicate on the HP-IB. The "Secondary Command Group" is used when addressing extended listeners and talkers, or enabling the Parallel Poll Mode.

A-24. Other Bus Lines

A-25. The three remaining HP-IB lines and their functions are:

a. REN—(Remote Enable)—The system controller sets REN low and then addresses the devices to Listen before they will operate under remote control.

b. IFC—(Interface Clear)—Only the system controller can activate this line. When IFC is set (true) all talkers, listeners and active controllers go to their inactive states.

c. EOI—(End of Identify)—This line is used to indicate the end of a multiple byte transfer sequence or, in conjunction with ATN, to execute a parallel polling sequence.

NOTE

Individual instruments, at power-on, can momentarily set the IFC line to a true state.

A-26. Address Codes

A-27. Devices with the functional capability of Talker normally recognize a single byte address. A certain group of ASCII seven-bit bytes is reserved for talk addresses (refer to Table A-3). The state of the eighth bit is ignored in the "Command Mode" when addresses are being transmitted. Each device has a unique talk address which can normally be modified. The talk address, bits one through five, are individually selected in each device to be either high or low. The selection of these bits allows changing the device talk and/or listen address.

NOTE

An "extended talker" is capable of recognizing a two byte talk address.

A-28. Devices with the functional capability of Listener normally recognize a single character address. The seven-bit codes reserved for Listen addresses are listed in Table A-3. Each device has a unique listen address which can normally be modified.

NOTE

An "extended listener" is capable of recognizing a two byte listen address.

NOTE

Bits 6 and 7 determine whether the "address" is a "listen" or "talk" address (see Table A-3).

A-29. Devices with both talk and listen addresses have these addresses assigned in pairs, eg., if the fourth address in the column of listen addresses " ≠ " is selected, the talk address is "C", the fourth address in the talker address column. The talk address is automatically changed whenever the listen address is changed and vice versa. Addresses are normally alterable by the use of switches or jumpers within the instrument.

A-35. Data Lines

A-36. A set of eight interface lines is available to carry all seven bit interface messages and device dependent messages. These are DATA INPUT OUTPUT lines, DIO1 through DIO8. Only seven lines are required for transfer of data. The eighth line is usually used for a parity check. The data on the DIO lines is transferred in a bit parallel, byte serial form, asynchronously and bidirectionally.

a. DATA MODE—When ATN (attention) goes high (false), the HP-IB is in the "Data Mode". In this mode data may be transferred between devices that were addressed when the HP-IB was in "Command Mode". Messages that can be transferred in "Data Mode" include:

b. PROGRAMMING INSTRUCTIONS—Codes are seven bit bytes placed on the HP-IB data (DIO) lines. The meaning of each byte is device dependent and is selected by the equipment designer. These types of messages are usually between the controller acting as the talker and a single device that has been addressed as a listener.

c. DATA CODES—Data codes are seven-bit bytes placed on the data lines. The meaning of each byte is device dependent. For meaningful communication to occur, both the talker and listener must agree on the meaning of the codes they use.

Table A-3. Address Codes.

Listen Addresses									Talk Addresses								
Bits								ASCII	Bits								ASCII
b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	Character	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	Character
X	0	1	0	0	0	0	0	SP	X	1	0	0	0	0	0	0	@
X	0	1	0	0	0	0	1	!	X	1	0	0	0	0	0	1	A
X	0	1	0	0	0	1	0	"	X	1	0	0	0	0	1	0	B
X	0	1	0	0	0	1	1	≠	X	1	0	0	0	0	1	1	C
X	0	1	0	0	1	0	0	S	X	1	0	0	0	1	0	0	D
X	0	1	0	0	1	0	1	%	X	1	0	0	0	1	0	1	E
X	0	1	0	0	1	1	0	&	X	1	0	0	0	1	1	0	F
X	0	1	0	0	1	1	1	'	X	1	0	0	0	1	1	1	G
X	0	1	0	1	0	0	0	(	X	1	0	0	1	0	0	0	H
X	0	1	0	1	0	0	1	)	X	1	0	0	1	0	0	1	I
X	0	1	0	1	0	1	0	*	X	1	0	0	1	0	1	0	J
X	0	1	0	1	0	1	1	+	X	1	0	0	1	0	1	1	K
X	0	1	0	1	1	0	0	'	X	1	0	0	1	1	0	0	L
X	0	1	0	1	1	0	1	–	X	1	0	0	1	1	0	1	M
X	0	1	0	1	1	1	0	.	X	1	0	0	1	1	1	0	N
X	0	1	0	1	1	1	1	/	X	1	0	0	1	1	1	1	O
X	0	1	1	0	0	0	0	0	X	1	0	1	0	0	0	0	P
X	0	1	1	0	0	0	1	1	X	1	0	1	0	0	0	1	Q
X	0	1	1	0	0	1	0	2	X	1	0	1	0	0	1	0	R
X	0	1	1	0	0	1	1	3	X	1	0	1	0	0	1	1	S
X	0	1	1	0	1	0	0	4	X	1	0	1	0	1	0	0	T
X	0	1	1	0	1	0	1	5	X	1	0	1	0	1	0	1	U
X	0	1	1	0	1	1	0	6	X	1	0	1	0	1	1	0	V
X	0	1	1	0	1	1	1	7	X	1	0	1	0	1	1	1	W
X	0	1	1	1	0	0	0	8	X	1	0	1	1	0	0	0	X
X	0	1	1	1	0	0	1	9	X	1	0	1	1	0	0	1	Y
X	0	1	1	1	0	1	0	:	X	1	0	1	1	0	1	0	Z
X	0	1	1	1	0	1	1	;	X	1	0	1	1	0	1	1	[
X	0	1	1	1	1	0	0	<	X	1	0	1	1	1	0	0	\
X	0	1	1	1	1	0	1	=	X	1	0	1	1	1	0	1	]
X	0	1	1	1	1	1	0	>	X	1	0	1	1	1	1	0	^
X = don't care																	

A-37. Data Byte

A-38. Individual data bytes transmitted on the HP-IB can be described in an octal code. The binary bits are separated into groups of three starting from the right-hand side (see Table A-4). Within the groups each binary bit is assigned a weight — "1", "2", and "4" respectively. The octal numbers corresponding to each group of bits is the summation of the weights of the binary ones in each group.

NOTE

In Table A-4 the hundreds group has two bits rather than three since there are eight data lines. When seven-bit character ASCII code is used the hundreds groups contains only one bit which can take on the octal value of "0" or "1".

A-30. Handshake Lines

A-31. Each character byte transferred on the HP-IB data lines employs the three-wire handshake sequence. This sequence has the following characteristics:

a. Data transfer is asynchronous — Data can be transferred at any rate suitable for the devices operating on the Bus. (Data rates up to 500 kilobytes per second are typical; with a maximum of 1 megabyte per second).

b. Devices with different input/output speeds can be interconnected. Data transfer rate automatically adjusts to slowest active device.

c. More than one device can accept data at the same time.

A-32. The following definitions are used throughout the remaining text.

Source—A device transmitting information on the Bus in either the Command or Data Mode.

Talker—An "addressed" source in the Data Mode only.

Acceptor—A device receiving information on the Bus in either the Command or Data Mode.

Listener—An "addressed" acceptor in the Data Mode only.

Table A-4. Octal Code Conversion.

Bits	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	Octal Code
Weights	"2" (Hundreds)	"1" (Hundreds)	"4" (Tens)	"2" (Tens)	"1" (Tens)	"4" (Ones)	"2" (Ones)	"1" (Ones)	
	1	0	0	1	1	0	1	0	2 3 2
	1	1	1	1	1	0	0	0	3 7 0
	0	1	0	0	1	0	1	1	1 1 3
	0	0	0	1	0	1	1	1	0 2 7

A-33. The Data Transfer or "HANDSHAKE" lines are shown in Figure A-1. The mnemonics of each line have the following meanings:

DAV — Data Valid
NRFD — Not Ready for Data
NDAC — Not Data Accepted

The handshake timing sequence is illustrated in Figure A-2.

A-34. Each data byte transferred by the interface system uses the handshake process when exchanging data between source and acceptor. The handshake timing sequence is illustrated in Figure A-2. In Data Mode, the source is a Talker and the acceptor is a Listener.

A-39. INTERFACE

A-40. A list of the available functions is given in Table A-5. Every HP-IB compatible device is able to perform at least one function on the HP-IB. Devices ignore all commands relating to functions they do not have.

Example:

An HP-IB compatible programmable voltage source includes the "listen function" so that it can be programmed to accept data. However, it does not output information so it does not include a "talk function". Therefore, the programmable voltage source would ignore all information on the HP-IB pertaining to the "talk function".

A-41. Bus Operating Considerations

a. When a device capable of activating IFC is powered on during system operation, it may cause the active controller on the Bus to relinquish control, resulting in errors. The Controller must transmit IFC to regain active Control.

b. Prior to addressing new listeners it is recommended that all previous listeners be unaddress using the Unlisten Command (?).

c. Only one talker can be addressed at a time. When a new talker is addressed the former talker is automatically unaddressed.

d. The maximum accumulative length of the HP-IB cable in any system must not exceed more than 2 meters of cable per device or 20 meters, whichever is less.

e. For additional programming information consult the HP-IB User Guide for the appropriate calculator.

A-42. HP-IB CONNECTOR

A-43. Figure A-3 shows the pin configuration of the HP-IB Connector.

A-44. SYSTEM CONFIGURATIONS

A-45. HP-IB Systems can be categorized into three types:

a. SYSTEMS WITH NO CONTROLLER—The mode of data transfer is limited to a direct transfer between one device manually set to "talk only" and one or more devices manually set to "listen only" to form a very basic fixed network system.

b. SYSTEMS WITH A SINGLE CONTROLLER—The modes of data transfer for these systems are:

1. Direct transfer between talkers and listeners (Data Mode).

2. Transfer from a device to a controller (Data Mode).

3. Transfer from a controller to a device (Command Mode).

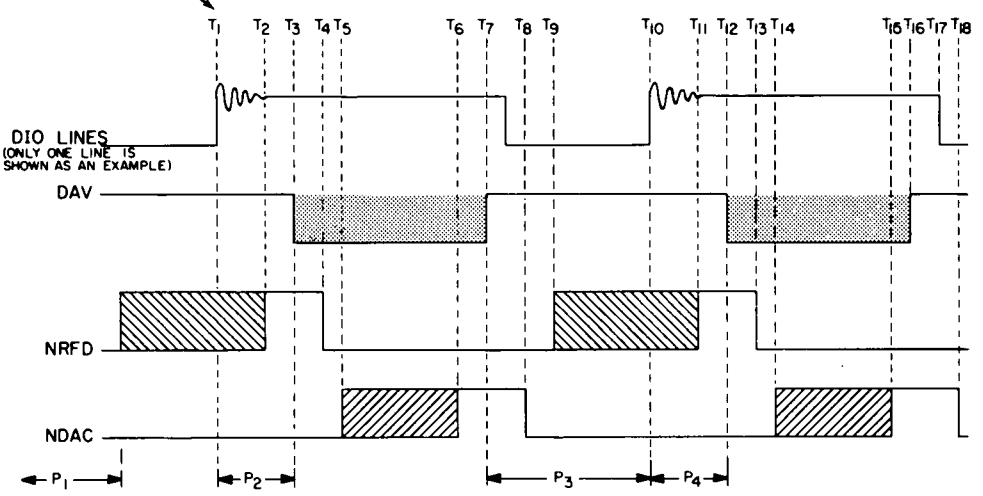
c. SYSTEMS WITH MULTIPLE CONTROLLERS—The modes of data transfer for these systems are the same as those listed in 2. In addition a method of passing control from one controller to another is required. One controller must be designated as the system controller. The system controller is the only device that can control the HP-IB lines designated IFC (Interface Clear) and REN (Remote Enable). When the system controller sets IFC low, all I/O operations cease and all talkers, listeners and controllers are unaddressed. Control is passed to a different controller by addressing it as a talker and commanding it to "take control" (Octal code 011).

The timing diagram illustrates the handshake process by indicating the actual waveforms on the DAV, NRFD, and NDAC lines. The NRFD and NDAC signals each represent composite waveforms resulting from two or more Listeners accepting the same data byte at slightly different times. This is usually due to variations in the transmission path length and individual instrument response rates (delays).

The flow chart represents the same sequence of events in a different form.

The subscripted letters on the timing diagram refer to the same event on the list of events.

HANDSHAKE line timing diagram for one talker and multiple listeners using the handshake process. Two cycles of the handshake sequence are shown. Also refer to the flow diagram and list of events on this figure.



Period in which data is guaranteed to be valid.

Period in which all listeners become ready for data.

Period in which all listeners accept data.

List of Events for Handshake Process

— Source initializes DAV to high (False—data not valid).

P_1 — Acceptors initialize NRFD to low (True—none are ready for data), and set NDAC to low (True—none have accepted the data).

T_1 Source checks for error condition (both NRFD and NDAC high), then places data byte on DIO lines.

P_2 Source delays to allow data to settle on DIO lines

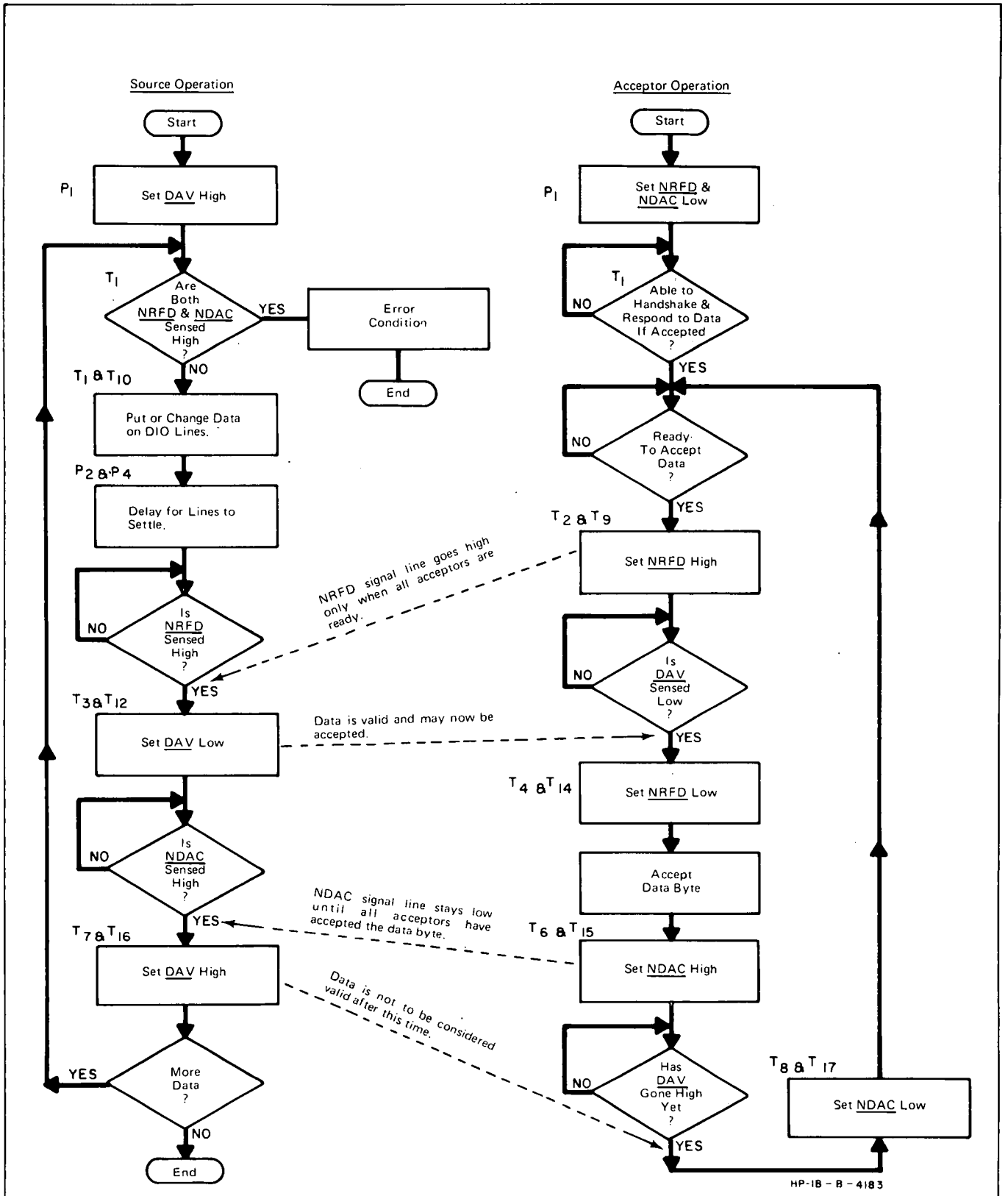
T_2 Acceptors have all indicated readiness to accept first data byte; NRFD goes high.

Figure A-2. Handshake Timing Sequence.

T_3	When the data is settled and valid, and the source has sensed NRFD high, DAV is set low.
T_4	First acceptor sets NRFD low to indicate that it is no longer ready, then accepts the data. Other acceptors follow at their own rates.
T_5	First acceptor sets NDAC high to indicate that it has accepted the data (NDAC remains low due to other acceptors driving NDAC low).
T_6	Last acceptor sets NDAC high to indicate that it has accepted the data; all have now accepted and NDAC goes high.
T_7	Source, having sensed that NDAC is high, sets DAV high. This indicates to the acceptors that data on the DIO lines must now be considered not valid. Upon completion of this step, one byte has been transferred.
P_3 (T_7-T_{10})	Source changes data on the DIO lines.
T_8*	Acceptors, upon sensing DAV high set NDAC low in preparation for next cycle. NDAC goes low as the first acceptor sets it low.
T_9	First acceptor indicates that it is ready for the next data byte by setting NRFD high. (NRFD remains low due to other acceptors driving NRFD low).
T_{10}	Source checks for error condition (both NRFD and NDAC high), then places data byte on DIO lines (as at T_1).
P_4 $(T_{10}-T_{12})$	Source delays to allow data to settle on DIO lines.
T_{11}	Last acceptor indicates that it is ready for the next data byte by setting NRFD high; NRFD signal line goes high.
T_{12}	Source, upon sensing NRFD high, sets DAV low to indicate that data on DIO lines is settled and valid.
T_{13}	First acceptor sets NRFD low to indicate that it is no longer ready, then accepts the data.
T_{14}	First acceptor sets NDAC high to indicate that it has accepted the data.
T_{15}	Last acceptor sets NDAC high to indicate that it has accepted the data (as at T_6).
T_{16}	Source, having sensed that NDAC is high, sets DAV high (as at T_7).
T_{17}	Source removes data byte from DIO signal lines after setting DAV high.
T_{18}*	Acceptors, upon sensing DAV high, set NDAC low in preparation for next cycle.

*Note that all three handshake lines return to their initialized states, as at T_1 and T_2.

Figure A-2. Handshake Timing Sequence (Cont'd).



Logical flow of events for Source and Acceptor when transferring data using the handshake process. See preceding list of events.

Figure A-2. Handshake Timing Sequence (Cont'd).

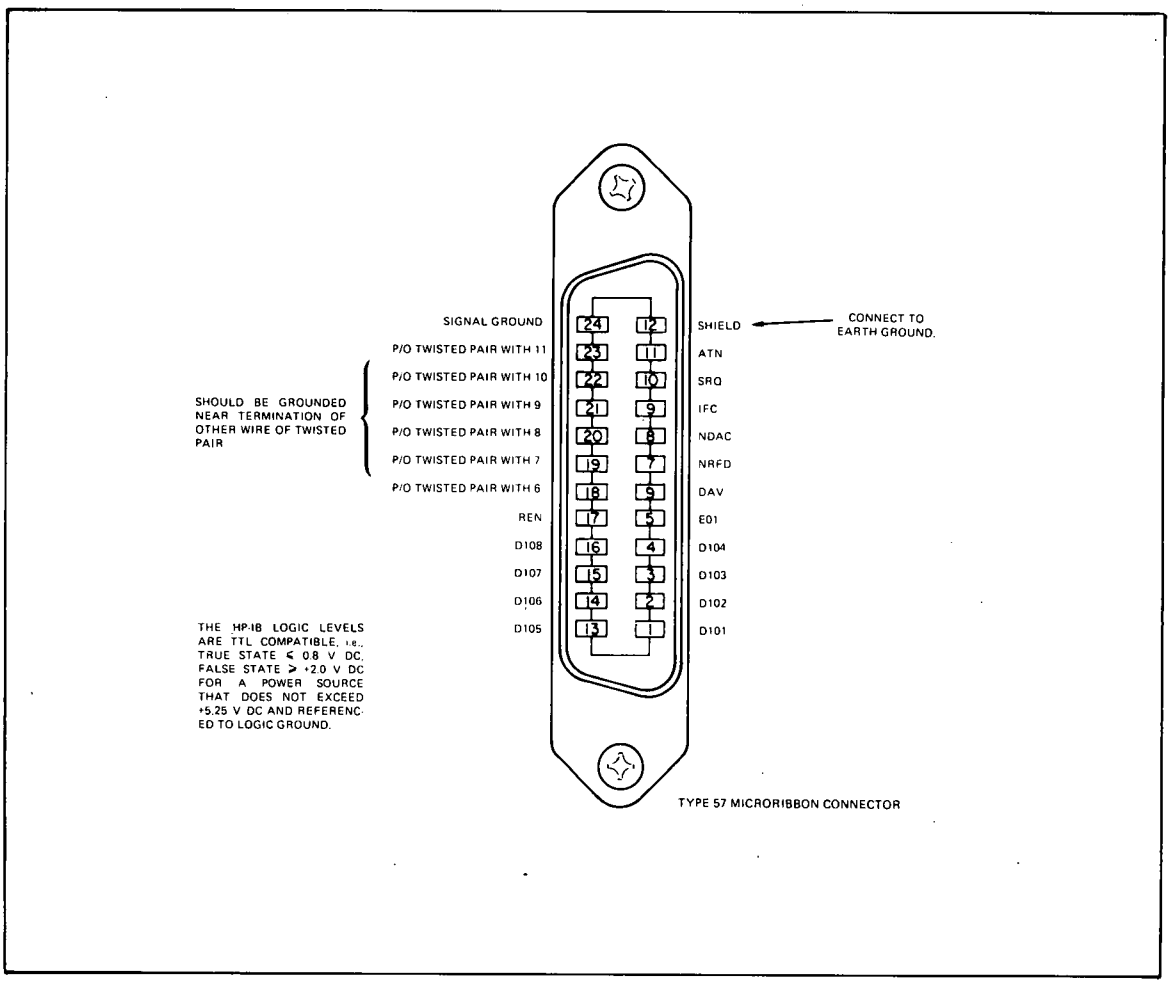


Figure A-3. HP-IB Connector.

TABLE A-6. GLOSSARY OF TERMS

ACCEPTOR — A device receiving information on the Bus in either the Command or Data Mode (Also, see Source).

ADDRESS — A 7-bit code applied to the HP-IB in "Command Mode" which enables instruments capable of responding to listen and/or talk on the Bus.

ADDRESSED COMMANDS — These commands allow the Bus controller to initiate simultaneous actions from addressed instruments which are capable of responding.

ATN — Mnemonic (Attention) referring to the "Command Mode" of operation on the HP-IB, or the control line which places the HP-IB in this mode.

BIT — The smallest part of an HP-IB character (Byte) which contains intelligible information.

BUS COMMANDS — A group of Special Codes which initiates certain types of operation in instruments capable of responding to these codes. Each instrument on the HP-IB is designed to respond to those codes that have useful meaning to the device and ignore all others.

BYTE — An HP-IB character sent over the DIO lines, normally consisting of seven-bits.

COMMAND MODE — In this mode devices on the HP-IB can be addressed or unaddressed as talkers or listeners. Bus commands are also issued in this mode.

CONTROLLER — Any device on the HP-IB which is capable of setting the ATN line and addressing instruments on the Bus as talkers and listeners. (Also see System Controller.)

DEVICE CLEAR (DCL) — ASCII character "DC4" (Octal 024) which, when sent on the HP-IB will return all devices capable of responding to pre-defined states.

DATA MODE — The HP-IB is in this mode when the control line "ATN" is high (false.) In this mode data or instructions are transferred between instruments on the HP-IB.

DAV — Mnemonic referring to the control line "Data Valid" on the HP-IB. This line is used in the HP-IB "Handshake" sequence.

DIO — Mnemonic referring to the eight "Data Input/Output" lines of the HP-IB.

EOI — Mnemonic referring to the control line "End or Identify" on the HP-IB. This line is used to indicate the end of a multiple byte message on the Bus. It is also used in parallel polling.

EXTENDED LISTENER — An instrument which requires two HP-IB bytes to address it as a listener. (Also see Listener.)

EXTENDED TALKER — An instrument which requires two HP-IB bytes to address it as a talker. (Also see Talker.)

GO TO LOCAL (GTL) — ASCII character "SOH" (Octal 001) which, when sent on the HP-IB, will return devices addressed to listen and capable of responding back to local control.

GROUP EXECUTE TRIGGER (GET) — ASCII character "BS" (Octal 010) which, when sent on the HP-IB, initiates simultaneous actions by devices addressed to listen and capable of responding to this command.

GLOSSARY OF TERMS (Cont'd)

HANDSHAKE — Refers to the sequence of events on the HP-IB during which each data byte is transferred between addressed devices. The conditions of the HP-IB handshake sequence are as follows:

a. NRFD, when false, indicates that a device is ready to receive data.

b. DAV, when true, indicates that data on the DIO lines is stable and available to be accepted by the receiving device.

c. NDAC, when false, indicates to the transmitting device that data has been accepted by the receiver.

HP-IB — An abbreviation that refers to the "Hewlett-Packard Interface Bus".

IFC — Mnemonic referring to the Control line "Interface Clear" on the HP-IB. Only the system controller can activate this line. When IFC is set (true) all talkers and listeners on the HP-IB are unaddressed, and controllers go to the inactive state.

LISTENER — A device which has been addressed to receive data or instructions from other instruments on the HP-IB. (Also see Extended Listener.)

LOCAL LOCKOUT — ASCII character "DC1" (Octal 021) which, when sent on the HP-IB, disables the front panel controls of responding devices.

NDAC — Mnemonic referring to the control line "Data Not Accepted" on the HP-IB. This line is used in the "Handshake" sequence.

NRFD — Mnemonic referring to the control line "Not Ready For Data" on the HP-IB. This line is used in the "Handshake" sequence.

PARALLEL POLLING — A method of simultaneously checking status on up to eight instruments on the HP-IB. Each instrument is assigned a DIO line on which to indicate whether it requested service or not.

PRIMARY COMMANDS — The group of ASCII characters which are typically used on the HP-IB.

REN — Mnemonic referring to the control line "Remote Enable" on the HP-IB. This line is used to enable Bus compatible instruments to respond to commands from the controller or another talker. It can be issued only by the system controller.

SECONDARY COMMANDS — The group of ASCII characters which are used to increase the address length of extended talkers and listeners to two bytes.

SELECTIVE DEVICE CLEAR — ASCII character "EOT" (Octal 004) which, when sent on the HP-IB, returns addressed devices capable of responding to a predetermined state.

SERIAL POLLING — The method of sequentially determining which device connected to the HP-IB has requested service. Only one instrument is checked at a time.

SERIAL POLL DISABLE (SPD) — ASCII character "EM" (Octal 031) which, when sent on the HP-IB, will cause the Bus to go out of serial poll mode.

SOURCE — A device transmitting information on the Bus in either the Command or Data Mode (also see Acceptor).

SRQ — Mnemonic referring to the control line "Service Request" on the HP-IB. This line is set low (true) by any instrument requesting service.

SYSTEM CONTROLLER — This is an instrument on the HP-IB which has all the features of a standard controller with the added ability to control the IFC and REN lines. (Also see Controller.)

TALKER — A device that has been addressed to transmit data on the HP-IB. (Also see Extended Talker.)

GLOSSARY OF TERMS (Cont'd)

UNADDRESS COMMANDS — These commands are obeyed by all addressable devices. This category consists of the Unlisten Command (?) and the Untalk Command (—). When the Unlisten Command (?) is transmitted on the HP-IB, all devices on the Bus will be unaddressed as listeners. When the Untalk Command (—) is transmitted, all devices will be unaddressed as talkers.

UNIVERSAL COMMANDS — These commands affect every device capable of responding on the HP-IB, regardless of whether they have been addressed or not; e.g., Serial Poll Enable (SPE) and Serial Poll Disable (SPD).

UNLISTEN COMMAND — See "UNADDRESS COMMANDS".

UNTALK COMMAND — See "UNADDRESS COMMANDS".

APPENDIX B
SERIAL I/O CONCEPTS AND THE 3497A

B-1. COMPARING SERIAL I/O TO PARALLEL I/O

B-2. What do these two terms mean? Simply stated, serial I/O is the transfer of data, one bit after another in succession, over a line. Parallel I/O, on the other hand, transfers a whole word simultaneously (usually eight or more bits) but requires a separate wire (or line) for each bit. Parallel I/O is usually faster, but not in all cases. Data transfer speeds primarily depend upon the functional capability of the devices.

B-3. Parallel I/O has dedicated lines to handshake each word transferred whereas Serial I/O doesn't. In fact, serial I/O doesn't necessarily require a handshake at all. If the 3497A handshakes a transfer, it does so with either the ENQ/ACK or DC1 messages. These should not be confused with a hardware handshake. Strictly speaking, these are protocols where message bytes are sent to implement the handshake function.

B-4. Perhaps the most important distinction that can be made between serial and parallel I/O transfers, are the respective distances allowed between devices. Since parallel I/O has a separate wire for each bit, there are prohibitive cost and logistic considerations when long distances exist between devices. Serial I/O, however, permits data transfers via telephone lines when the appropriate modems are used. Even in a point to point hookup, serial I/O usually permits greater distances.

B-5. STANDARDS AND LINE PROTOCOLS

B-6. Confusion often accompanies the distinction between line protocols and standards. Line protocols are disciplines used for orderly information transfers over a communication channel. In other words, they establish the grammar by which devices communicate. Furthermore, some of the synchronous protocols are quite complex in structure.

B-7. A standard will usually define a protocol, but not always. RS-232C and RS-449/423 are examples of standards where protocols aren't defined, but they are the exception rather than the rule. A standard, however, will always define the electrical and mechanical requirements devices must adhere to for them to interoperate with other devices.

B-8. SYNCHRONOUS VS ASYNCHRONOUS

B-9. This manual makes several references to both synchronous and asynchronous operation. Since the 3497A is asynchronous, it will be discussed thoroughly. However, to compare the two, a brief description of synchronous is given first.

B-10. Synchronous

B-11. Synchronous transmission involves a continuous bit-by-bit serial stream of characters to make up a message block, with no time interval between the characters. The transmitting and receiving station clocks must be precisely synchronized with each other so that each bit time is properly marked. Synchronous operation eliminates the need for start and stop bits to frame characters. Instead, start and stop indicators frame entire message blocks. This type of transmission requires that the transmitting station have the next character ready to transmit in the first bit time following the end of the preceding character. If it isn't ready, it must fill in with some pre-defined sync character to ensure that the transmitting and receiving stations do not get out of step with each other.

B-12. There are a number of synchronous line protocols in use today, such as Binary Synchronous Communications (BSC) and High Level Data Link Control (HDLC) to name only a couple. Some of the synchronous protocols are quite complex.

B-13. Asynchronous

B-14. Perhaps the first thing that should be noted about this type of operation is that you don't have to be concerned about a complex line protocol. With asynchronous, the character generation is random, thereby making the arrival of an asynchronous character unpredictable. For example, the interval between characters that are typed in from a keyboard will be determined by the operators skill. This makes it necessary to provide built in character synchronization, which is done with start and stop bits. The asynchronous character structure is shown in Figure B-1.

B-15. Characters are transmitted using two voltage levels to represent the two possible states of a binary digit as shown in Table B-1.

Table B-1. Binary States

Voltage Level	Logic State	Line State	Level Name
+3V to +25V	0	High	Space
−3V to −25V	1	Low	Mark

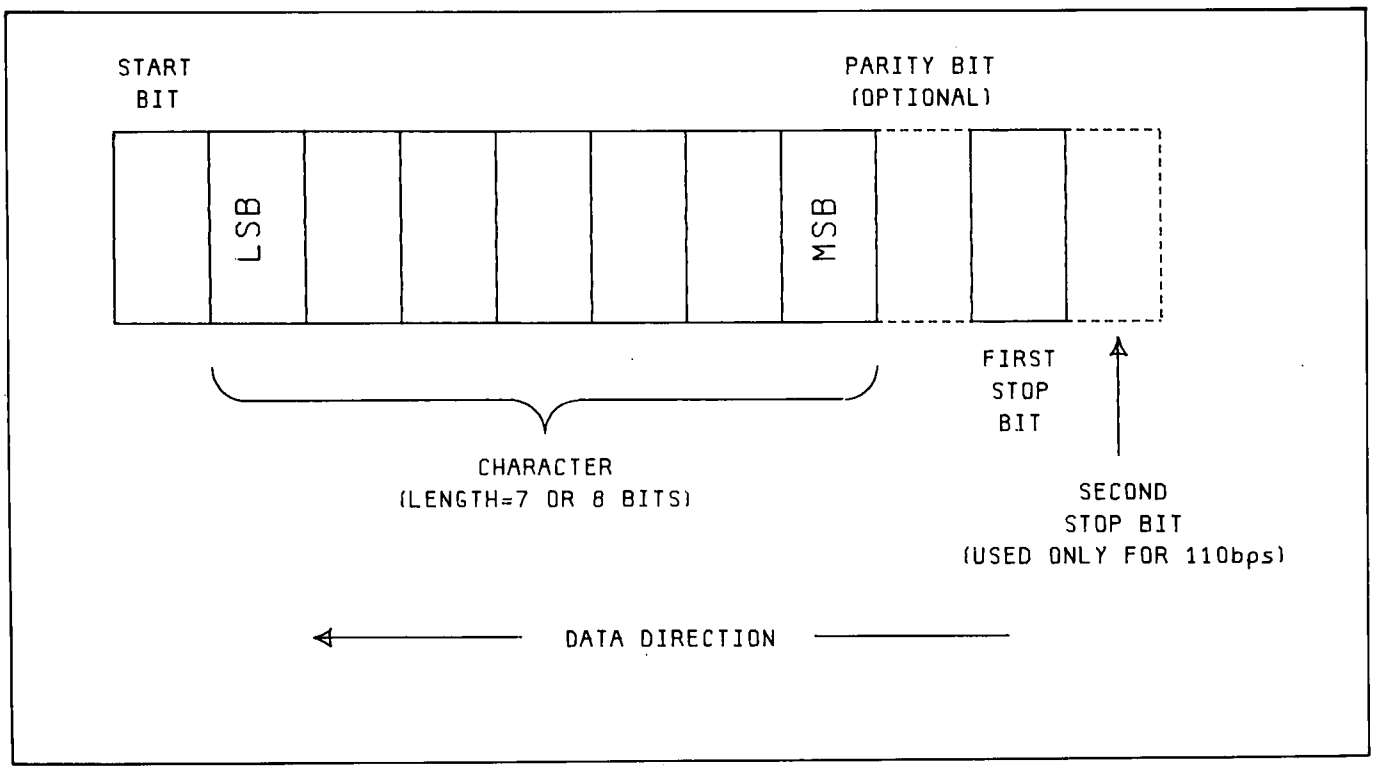


Figure B-1. Asynchronous Character Structure

B-16. When data is not being transmitted, the line is idle (low or mark). The transmitting device drives the line high (space) for one bit time when it has a character to send, hence the name start bit. The actual character is then transmitted, followed by a parity bit (optional when the 3497A is configured for 8-bit ASCII). The stop bit(s) is then sent which involves the transmitting device holding the line low (mark) for one or two bit times. The actual character transmission is shown in Figure B-2, which, in this instance, is the 7-bit ASCII representation of the letter "E". A more detailed explanation for each part of the character transmission follows Figure B-2.

B-17. Idle State. The line is held at this low voltage level (mark) when no character is being transmitted.

B-18. Start Bit. The start bit is inserted at the beginning of the character by the transmitting device. This is done by driving the line high (space) for one bit time. The start bit signals the receiving device that a character is starting so it can turn on its internal clock and input the character.

B-19. Character Bits. The 7-bit ASCII representation of the character "E" is 1000101. Notice that the character

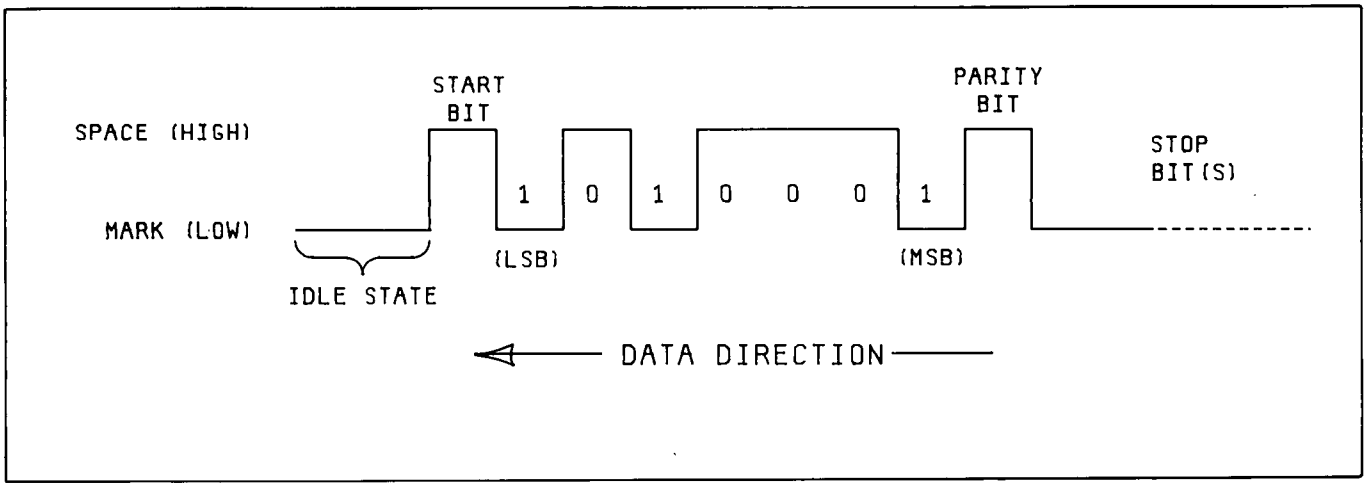


Figure B-2. Asynchronous Character Transmission

itself is seven bits in length without the start, stop or parity bits. These are the bits you have to consider when you are setting up a character length specification. The 3497A can be configured for 7 or 8 bit ASCII. Also, it is important that the computer has the same character length specification as the 3497A.

B-20. Parity Bit. The parity bit provides a means of checking a received character for errors. When used, it is computed and inserted after the character bits by the transmitting device. The receiving device then does a computation on the received character bits to determine what the parity bit should be and compares that with what it received.

B-21. Parity can be specified as odd or even. Odd parity simply means that the total number of 1's contained the character bit pattern, including the parity bit, is an odd number. For even parity, there is an even number of 1's. For example, note that the 7-bit ASCII "E" has three 1's, an odd number. In this instance, if odd parity is specified, the parity bit would be a 0 making the total number of 1's an odd number. For even parity, it would be a 1 making the total number of 1's an even number. Table B-2 shows how parity bits are determined.

Table B-2. Parity Specification

Parity Specified	Number of "1" Bits In Character	Parity Bit Sent
Odd	Odd	0
Odd	Even	1
Even	Odd	1
Even	Even	0
None	Odd or Even	None

B-22. The parity bit is optional when the 3497A is configured for 8-bit ASCII. If parity isn't specified, a parity bit isn't sent and no error checking is performed. Also, the length of time it takes to send an 8-bit ASCII character with a parity bit is reduced by one bit time.

B-23. Stop Bit(s). One stop bit is added following the parity bit for all operating speeds except 110 bps, which uses two stop bits. This involves the transmitting device allowing the line to stay idle (low) for one or two bit times. This gives the receiving device enough time to process the character before the next one is sent.

B-24. Bits and Bauds

B-25. The term "bit" is a contraction of binary digit. Bits are perhaps best represented by the square waves that were previously shown to transmit the ASCII "E". "Baud" refers to the speed of signal units and is the yardstick for measuring modems in bits per second (bps). If one bit is used as the signal unit, which is quite common, then baud speed and bps are the same. When two bits form the signal unit (double bit or dibit) then the baud rate is half the bps. When three bits form the signal unit (triple bit or tribit) then the baud rate is one third the bps. Most modems handle two state bits making baud and bps the same.

B-26. Modems (Data Sets)

B-27. The modem name is derived from the modulation and demodulation functions the device performs. Modems, also called data sets, are required when communication is performed over telephone lines. The 3497A can operate with asynchronous full duplex modems.

B-28. Modulation is the process of converting the RS-232C or RS-449/423 level digital signals to analog waveforms for transmission over telephone lines. It follows then that demodulation is the process of reconverting the analog signals back to RS-232C or RS-449/423 digital signals. This is illustrated in Figure B-3.

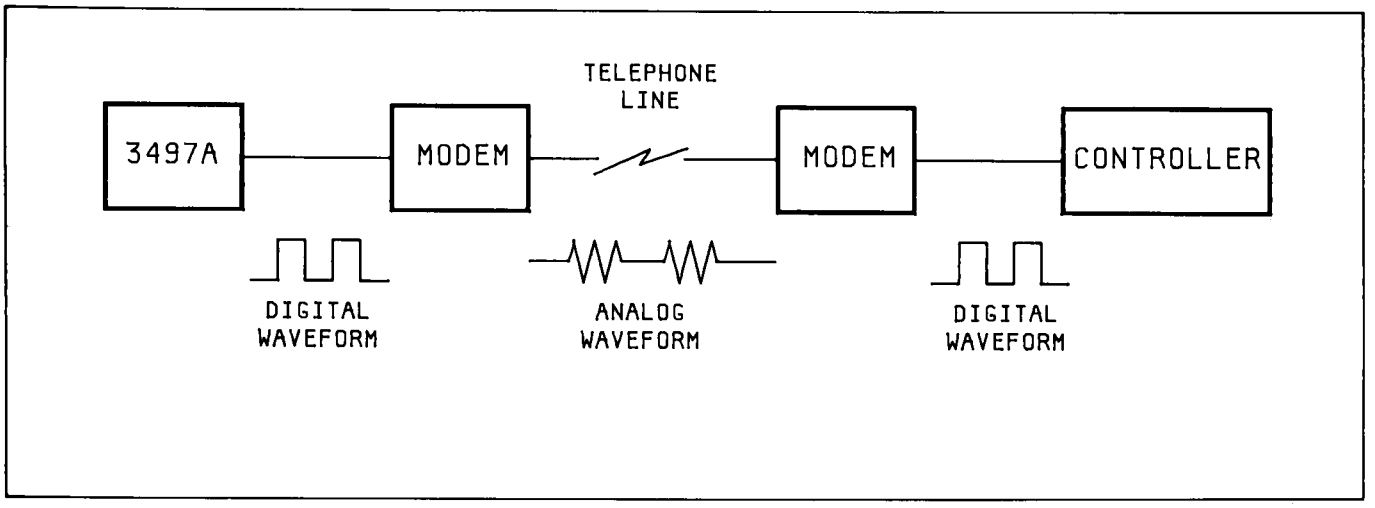


Figure B-3. MODEM Functions in a System

B-29. An asynchronous modem simply means that it operates at random speeds. That is, the character generation is random and the arrival of a character is unpredictable. This is illustrated in the Figure B-4.

B-30. A full duplex modem is capable of transmitting and receiving data simultaneously. A half duplex modem can transmit and receive data, but it can't do both at the same time. You may wonder why full duplex operation is required in a data acquisition system since, typically, the 3497A will be instructed to perform some specified task and then transmit the results back to the computer. However, two-way simultaneous transmission is required when the 3497A sends a break. That is, when the 3497A sends a break, it may do so while the computer is still sending commands.

B-31. Echo

B-32. The 3497A does not support echo, and any computer used in the system should have this feature turned off. Where echo is supported, the receiving device transmits each character it receives back to the transmitting device. The returned character is usually then displayed on a CRT or printed on a printer, permitting a visual check to be made of the character transmission. However, characters echoed back to the 3497A will be interpreted as commands. Since they will not be understood, the 3497A will set the "Message Not Executed" Bit in its status register and, if enabled to do so, send a break. Another likely occurrence will be an input buffer overflow.

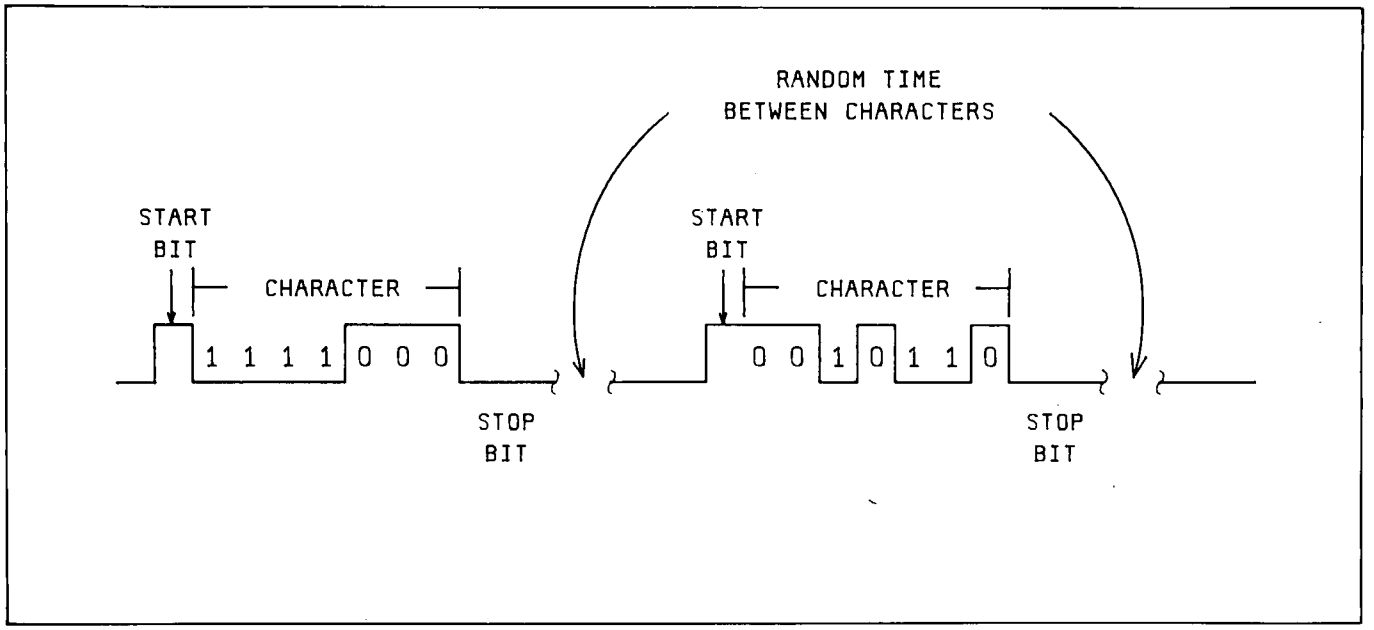


Figure B-4. Asynchronous Bit Flow

APPENDIX C
ASCII TABLE

ASCII Char.	EQUIVALENT FORMS				HP-IB
	Binary	Oct	Hex	Dec	
NULL	00000000	000	00	0	
SOH	00000001	001	01	1	GTL
STX	00000010	002	02	2	
ETX	00000011	003	03	3	
EOT	00000100	004	04	4	SDC
ENQ	00000101	005	05	5	PPC
ACK	00000110	006	06	6	
BELL	00000111	007	07	7	
BS	00001000	010	08	8	GET
HT	00001001	011	09	9	TCT
LF	00001010	012	0A	10	
VT	00001011	013	0B	11	
FF	00001100	014	0C	12	
CR	00001101	015	0D	13	
SO	00001110	016	0E	14	
SI	00001111	017	0F	15	
DLE	00010000	020	10	16	
DC1	00010001	021	11	17	LLO
DC2	00010010	022	12	18	
DC3	00010011	023	13	19	
DC4	00010100	024	14	20	DCL
NAK	00010101	025	15	21	PPU
SYNC	00010110	026	16	22	
ETB	00010111	027	17	23	
CAN	00011000	030	18	24	SPE
EM	00011001	031	19	25	SPD
SUB	00011010	032	1A	26	
ESC	00011011	033	1B	27	
FS	00011100	034	1C	28	
GS	00011101	035	1D	29	
RS	00011110	036	1E	30	
US	00011111	037	1F	31	

ASCII Char.	EQUIVALENT FORMS				HP-IB
	Binary	Oct	Hex	Dec	
space	00100000	040	20	32	LA0
!	00100001	041	21	33	LA1
"	00100010	042	22	34	LA2
#	00100011	043	23	35	LA3
$	00100100	044	24	36	LA4
%	00100101	045	25	37	LA5
&	00100110	046	26	38	LA6
'	00100111	047	27	39	LA7
(	00101000	050	28	40	LA8
)	00101001	051	29	41	LA9
*	00101010	052	2A	42	LA10
+	00101011	053	2B	43	LA11
,	00101100	054	2C	44	LA12
-	00101101	055	2D	45	LA13
.	00101110	056	2E	46	LA14
/	00101111	057	2F	47	LA15
0	00110000	060	30	48	LA16
1	00110001	061	31	49	LA17
2	00110010	062	32	50	LA18
3	00110011	063	33	51	LA19
4	00110100	064	34	52	LA20
5	00110101	065	35	53	LA21
6	00110110	066	36	54	LA22
7	00110111	067	37	55	LA23
8	00111000	070	38	56	LA24
9	00111001	071	39	57	LA25
:	00111010	072	3A	58	LA26
;	00111011	073	3B	59	LA27
<	00111100	074	3C	60	LA28
=	00111101	075	3D	61	LA29
>	00111110	076	3E	62	LA30
?	00111111	077	3F	63	UNL

ASCII Char.	EQUIVALENT FORMS				HP-IB
	Binary	Oct	Hex	Dec	
@	01000000	100	40	64	TA0
A	01000001	101	41	65	TA1
B	01000010	102	42	66	TA2
C	01000011	103	43	67	TA3
D	01000100	104	44	68	TA4
E	01000101	105	45	69	TA5
F	01000110	106	46	70	TA6
G	01000111	107	47	71	TA7
H	01001000	110	48	72	TA8
I	01001001	111	49	73	TA9
J	01001010	112	4A	74	TA10
K	01001011	113	4B	75	TA11
L	01001100	114	4C	76	TA12
M	01001101	115	4D	77	TA13
N	01001110	116	4E	78	TA14
O	01001111	117	4F	79	TA15
P	01010000	120	50	80	TA16
Q	01010001	121	51	81	TA17
R	01010010	122	52	82	TA18
S	01010011	123	53	83	TA19
T	01010100	124	54	84	TA20
U	01010101	125	55	85	TA21
V	01010110	126	56	86	TA22
W	01010111	127	57	87	TA23
X	01011000	130	58	88	TA24
Y	01011001	131	59	89	TA25
Z	01011010	132	5A	90	TA26
[	01011011	133	5B	91	TA27
\	01011100	134	5C	92	TA28
]	01011101	135	5D	93	TA29
^	01011110	136	5E	94	TA30
_	01011111	137	5F	95	UNT

ASCII Char.	EQUIVALENT FORMS				HP-IB
	Binary	Oct	Hex	Dec	
`	01100000	140	60	96	SC0
a	01100001	141	61	97	SC1
b	01100010	142	62	98	SC2
c	01100011	143	63	99	SC3
d	01100100	144	64	100	SC4
e	01100101	145	65	101	SC5
f	01100110	146	66	102	SC6
g	01100111	147	67	103	SC7
h	01101000	150	68	104	SC8
i	01101001	151	69	105	SC9
j	01101010	152	6A	106	SC10
k	01101011	153	6B	107	SC11
l	01101100	154	6C	108	SC12
m	01101101	155	6D	109	SC13
n	01101110	156	6E	110	SC14
o	01101111	157	6F	111	SC15
p	01110000	160	70	112	SC16
q	01110001	161	71	113	SC17
r	01110010	162	72	114	SC18
s	01110011	163	73	115	SC19
t	01110100	164	74	116	SC20
u	01110101	165	75	117	SC21
v	01110110	166	76	118	SC22
w	01110111	167	77	119	SC23
x	01111000	170	78	120	SC24
y	01111001	171	79	121	SC25
z	01111010	172	7A	122	SC26
{	01111011	173	7B	123	SC27
|	01111100	174	7C	124	SC28
}	01111101	175	7D	125	SC29
~	01111110	176	7E	126	SC30
DEL	01111111	177	7F	127	SC31